SOS Radiation Hard

Hi-Rel IC and ASIC Handbook

June 1995

GEC PLESSEY
SEMICONDUCTORS

DATASHEET ANNOTATION

GPS annotate datasheets in the top right hand corner of the first page, to indicate product status. These annotations are as follows:

TARGET SPECIFICATION

This is the most tentative form of information and represents a very preliminary product specification. No actual design work on the product has started.

PRELIMINARY INFORMATION

The product is in design and development. The datasheet represents the product as it is understood but details may change.

ADVANCE INFORMATION

The product design is complete and final characterisation for volume production is well in hand.

No annotation

The product parameters are fixed and the product is available to datasheet specification in volume.

If you have any queries about the status of any GPS product, please contact your nearest GPS Customer Service Centre.

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Product List

GPS Space & Radiation Hard Products Technical Helpline

Technical and applications assistance with any GPS space product can be obtained from our technical desk direct from the factory on:

Telephone: Int. +44 1522 502274
or +44 1522 502371 (Laboratory)
or +44 1522 500500 (Exchange)

Facsimile: Int. +44 1522 502393
or +44 1522 500550

Internet: apps@lincoln.gpsemi.com

Alternatively call your local sales office.

Hardware & Software Support for MIL-STD-1750 Products

Hardware:

Hewlett Packard	Offer an HP64000-UX Logic Development System. Essential parts are the HP64120A, (card cage), the HP64155B (128K memory controller), the HP64302A (trace analyser) and some associated software. Extra features are available.
Tasco Electronic Services Inc.	Offer an MDC281, an HMA31750 and an NMA31750 emulator for use in conjunction with the HP development system. They allow the user to take full advantage of the emulator capabilities of the HP system and all related design and development aids. Also offered is an HMA31750 Inverse Assembler for use with HP Logic Analyzers.
Tektronix	Offer an MAS281 emulator (cannot support 1750B for the MA31750). Is attached to device in system to offer register access and step by step debugging facilities.
Tharsys	Offer a low cost single-board computer for the NMA31750 with the BMA31751 (options are available to run the HMA31750 with the AMA31751).

Software:

TLD Systems	ADA cross compiler available for several host machines eg. Digital's Vax (VMS), Data General Eclipse MV/Family (AOS/VS), HP 9000 series 300 (HP-UX), HP Apollo 9000 series 400 (HP-UX), IBM RISC System/6000 series (AIX) and SUN Microsystem's SPARC and SUN-3.
Tartan	Offer an ADA compiler system to run on a DEC VAX system (operating system V5.2 or later). Support and debugging tools to be used in conjunction with the HP or Tektronix emulators are available.
IPT	C cross compiler operating on the VAX (VMS operating system).
GPS	Supply on request a 1750 assembler, program downloading software and a monitor ROM program.

Contact Addresses:

Hewlett Packard	USA:	5161 Lankershim Blvd No. Hollywood, CA 91601 Tel: (818) 505 5600
	Europe:	150, Route du Nant d'Avril 1217 Meyrin 2 Geneva, Switzerland. Tel: (41 22) 780 8111
IPT	USA:	1096 East Meadow Circle, Palto Alto CA 94303 Tel: (415) 494 7500
Tartan	USA:	Pittsburgh Corporate Office 300 Oxford Drive, Monroeville PA 15146 Tel: (412) 856 3600
Tasco Electronic Services Inc.	USA:	80 Express Street, Plainview, NY 11803 Tel: (516) 938 6464
	Europe:	ADAR Active Technologies B.V., Willemsparkweg 100, 1071 HM Amsterdam, Netherlands Tel: (20) 679 9921
Tharsys	Europe:	Alain Dherbecourt Napa Centre, 3, Rue Ariane, Parc Technologie du Canal, Ramonville 31520 France. Tel: 61751587
TLD Systems	USA:	3625 Del Amo Blvd Suite 100, Torrance CA 90503 Tel: (213) 542 5433

Introduction

The General Electric Company plc

GEC Plessey Semiconductors (GPS) is part of the General Electric Company plc (GEC), which is a wholly British Company. GEC is one of the largest electronics and electrical engineering organisations in the world and, with 160,000 employees is one of the largest UK employers.

GPS offers one of the most extensive ranges of state of the art technologies available in the world. This range includes a variety of CMOS and Bipolar technologies, as well as Power Semiconductor products.

The company has six manufacturing sites worldwide, sales offices in 27 countries and a total of around 3500 employees. There are also 10 design centres strategically placed in different countries to support ASIC design activity and offer technical advice on standard products.

GPS Strategy For Space

GEC Plessey has a marketing strategy to exploit high growth market areas including communications electronics, ASICs, automotive, computer peripherals and space.

GPS is also one of the few space semiconductor companies operating as a completely independent entity without ties to the OEM equipment market. This means that customers can confidently design with GPS products without concern over security of supply that often accompanies the use of components originating from subsidiaries of competing spacecraft vendors.

GPS now possesses one of the most extensive product ranges in the world specifically targeted at the space market. This product range spans CMOS Silicon On Sapphire (SOS) technology at 0.6 micron, high speed (24GHz) trench isolated bipolar at 0.6 micron gate lengths and a variety of hybrid and microwave circuit capabilities.

GPS will continue the development of new technologies and products with the goal of becoming a first choice supplier for space grade radiation hard components.

GPS Quality - European Space Agency Capability Approval

The company has a long history of quality approvals. The latest and most notable is the ESA Capability Approval for 2.5 micron SOS products. This Capability Approval was awarded in March 1993. Since that time GPS have been offering both ASICs and standard components with full SCC9000 level B qualification. The ESA Capability Approval for 1.5 micron SOS is ongoing.

To add to the ESA Capability Approval are Self Certifications to MIL-STD-883 for both SOS and bipolar processes. The company now has a number of SMD's lodged with DESC.

CMOS-SOS Integrated Circuits

The Lincoln based Integrated Circuit operation produces specialist circuits for the space market. The operation employs over 600 people with a very high percentage of graduate level engineering staff.

This IC facility manufactures product for direct sale to end customers and also to other parts of the organisation, where further integration results in more complex products.

The IC facility carries out all manufacturing from design to product shipment in Lincoln, England.

GPS Radiation Hard Silicon on Sapphire

There is an increasing demand for space and defence systems which can survive radiation effects and ensure continued operation. As satellites and space probes mature, microprocessors, static RAMS, gate arrays and other VLSI ICs with the ability to carry out complex data processing tasks in the extremely stringent environment of space

become essential. Space imposes its own set of requirements, demanding a hardness to radiation which is normally screened out by the atmosphere. This radiation, in the form of cosmic rays, electrons, protons and x-rays, alters the electrical characteristics of circuits and causes a degradation in integrated circuit performance, which can lead to catastrophic device and system failures.

Of all the current silicon-based semiconductor technologies, only CMOS SOS (silicon-on-sapphire) offers the necessary resistance to the hazards of single event upset, transient and total dose radiation. It also provides the advantages of low power consumption and fast internal switching speeds, making CMOS SOS the key technology for defence and space applications. Independent investigators consider that its SEU immunity makes it the only choice for many key space applications

History in CMOS SOS

The company has been involved in SOS research and development for more than 15 years and is committed to the long term support of SOS processes and products for space and defence applications. Process and design techniques are in unison to maximise the benefits of the technology.

Initial research and development on SOS began at the GEC Hirst Research Centre in 1973. This work continued through to pilot designs which were released in 1979/1980. With the formation of Marconi Electronic Devices in 1981, manufacturing was transferred to the Lincoln facility and a 5 micron process attained full production status in 1982. Development work progressed to achieve smaller geometries and increased radiation hardness. A 3 micron process was established in 1984 and a double level metal variant of this process went into production in 1986. A 2.5 micron variant was introduced in 1989. Both 1.5 and 1.1 micron process is now being used to manufacture memories and semicustom products.

Production processes are based on in-house developed silicon on sapphire technology with drawn gate lengths of 3, 2.5, 1.5 and 1.1 micron. Both single and double level metal technologies are now available. At the time of publication GPS are in the process of introducing a 0.6 micron Low Power Process in Silicon on Sapphire.

A range of standard products and semicustom capabilities have been developed to provide all the key elements required in space and defence systems.

SOS Radiation Hardness Summary (1.5 micron)

Total Dose 1 Digital	$>10^6$ Rad(Si)
Dose Rate Survive	$>10^{11}$ Rad(Si)/S
Dose Rate Upset	$>10^{12}$ Rad(Si)/Si
Single Event Upset (Errors/Bit day)	$<4 \times 10^{-11}$ Neutrons
Latch Up	Not Possible

SOS Performance Summary (1.5 micron)

Transistor Count	>400K
Toggle Frequency	>100MHz
Gate Delay	<1.0ns
Pin Count	172
Power	<1.0µW/MHz/Gate

Wafer Fabrication

The Lincoln wafer fabrication facility was established in 1981 and has been substantially extended and enhanced to its current capacity of 2500 wafer starts per week. A range of CMOS-SOS processes are run in the facility covering feature sizes from 5 to 0.6µm. Wafer size is 4 in.

All manufacturing groups operate on a 24 hour per day, 3 shift basis producing ASICs, memory circuits and microprocessors up to space standards. All manufacturing processes are controlled by means of a computer-aided manufacturing system (PROMIS) which extends through wafer fab, assembly, and test. Extensive use is made of this system to collect wafer related engineering data which is then processed using statistical software packages.

Facilities

Integrated manufacturing facilities consist of 17,000 sq. ft of wafer fabrication clean room (with separate areas for manufacturing and development), 9000 sq. ft of assembly floor (part Class 100 clean room), a 6000 sq. ft test floor and 2000 sq. ft of characterisation area. Additional laboratory space is provided for functions such as product engineering.

The wafer fabrication area is primarily built to Class 100 standards with 200 sq. ft of Class 10 area which is utilised for, the critical steps in the 1.5μm SOS process and development programs on 0.6μm technology. These areas are environmentally controlled to temperature control limits of +0.5°C and humidity control of +2.5%. Particulate counts indicate an environment which is close to Class 1. Utilities installations are to an appropriate standard with all process gases run in continuously welded stainless steel lines using purifiers and point of use filtration as appropriate. A high purity de-ionising water ring main is provided for sub 1.0μm geometry processes.

Continuous monitoring of many facility parameters is carried out by a computer based building management system and this provides the ability to datalog and generate trend data for these parameters Where appropriate these measurements are backed up by manual measurement such as bacteria counts, carried out on a regular basis in the DI water system.

Computer Aided Manufacture

The PROMIS computer aided manufacturing system is used to define all process flows and to track material through development and mainstream manufacturing.

By this method it is possible to cope with a wide variety of process flows with minimal risk of human error and also to provide a high degree of visibility of batch status to anyone within the 400 strong user group. A natural consequence of the use of PROMIS is total traceability of material from incoming material to finished devices.

Product Assembly

The assembly capability is contained within the Lincoln (UK) facility except for plastic encapsulation (offshore) and tin plating (Power Division, Lincoln). The preseal assembly facility is enclosed in cleanroom conditions. Space products have been isolated in their own module to provide additional focus on these high quality components. The area offers total facilities for military and space manufacture of integrated circuits on one site. Current product being produced to these levels of quality include static RAMS, MIL-STD-1750 processors, standard logic circuits, MIL-STD-1553 databus products, and ASICs.

The present capacity of this assembly area is 10,000 units per week. Expansion over the next 12 months will increase the space capacity. The area also offers an engineering quick turnaround route for development prototypes and engineering experiments.

The assembly area has facilities for the production of bulk silicon CMOS and silicon on sapphire devices in numerous package styles, including custom designed packages for special applications. Current capability includes:

Dual in line - Sidebrazed and Cerdip, Leaded Flatpack, Cerpac, Leadless Chip Carrier, Pin Grid Arrays, Cerquads (J Lead and Gullwing), and Small Outline Packages (SO). Sealing methods include solder seal with Kovar or ceramic lids, glass seal and conformal coatings.

A surface mounting facility has been established to mount Class S leadless chip carriers onto motherboards to produce 1750 processor and RAM modules.

The company offers a manufacturing flow capable of screening to MIL-STD-883C class S and B, European Space Agency and British Standard quality levels.

Basic Structures Characterisation

DC measurements can be performed on a range of test systems all with pA current and mV voltage resolution.

A KEITHLEY 250 is utilised for routine wafer assessment, where large quantities of data can be stored and analysed using the KEITHLEY database analysis routines. For more detailed manipulation/analysis, data can be easily transferred to the VAX system where GPS developed routines are available.

More rigorous and detailed testing can be achieved using a HP4145 parametric analyser controlled by a HP310 computer. Connection via a 40-channel relay matrix to an autoprober enables any specific parameter to be measured across the whole area of a wafer.

Software has been developed for instrument control as well as for data manipulation and analysis to produce colour histogram/wafermap outputs. Data can be transferred from the HP computer to the VAX, using terminal emulator software, where analysis using existing statistical software programs can be performed Radiation effects can be studied using another HP4145/matrix/computer configuration linked to an ARACOR x-radiation system.

The 10-keV x-rays are produced within a lead-lined cabinet, which also contains an autoprober and dosimeter. Connecting wires are passed through a shielded orifice which enables devices to be biased or measured during irradiation. Software can be developed to repeat a cycle of test, bias, and irradiate for assessment of total dose effects, without the need to open the cabinet. Facilities are available to test devices either in package or wafer form Dose rates are determined by a suitable choice of tube current and voltage, within the range 0 25 to 160 Krads (Si02)/min.

Measurements of capacitance parameters use a HP4192 impedance analyzer, which has a resolution down to 10fF and a frequency range of 5Hz to 13MHz. A built-in power supply enables a bias of up to +35V to be applied to the device under test. A conductance value can also be obtained within the range 1 ns to 10 S. It has a four terminal configuration making precise measurements possible when using a correctly designed test-box. Wafer measurements utilise two coaxial probes situated on a manual prober within a screened light-proof cabinet, keeping strays and external EM interference to a minimum. This equipment can be controlled by a computer where specific software can easily be written to set up, trigger and return results from the instrument.

Test Capability

The test area consists of some six digital testers with capabilities up to 100MHz and 256 pins. A Fairchild 5588 Memory Tester is used to test memory devices up to speeds of 25MHz.

This ATE is supported by a wide range of automatic probers and environmental handlers, coupled with temperature sources, enabling full military and space level testing to be carried out Control of the calibration of equipment, test programs, test hardware, test methodology, practices, and device flow is maintained by an extensive quality control system, ensuring compliance to the various commercial, military, and space quality screening levels. Procedures for handling static sensitive device within the area

The computer-aided manufacturing (CAM) system, using PROMIS software, is installed in this area to control work progress, provide traceability and return results from analysis.

Burn-in/Life Test

Extensive burn-in facilities offer screening at any temperature up to 150°C Burn-in voltages can be provided up to +15 volts for particular devices. The ovens have continuous monitoring of both temperature and voltage to ensure complete reliability Sequential switching of device supplies and controlled cooling is incorporated into the device flow wherever necessary. Both static and dynamic burn-in is carried out in this area to MIL-STD-883C, ESA 9000, BS9000, and commercial standards.

High volume standard products have dedicated burn-in modules, but reconfigurable modules are available for rapid response, covering a wide range of standard packages, DIP, PGA, LCC, Cerquads, etc.

Burn-in times may vary from 1 hour to 500 hours for production screening, 100 to 200 hours for QCI testing and 2000 to 6000 hours for specific qualification exercises. Specific areas are used for engineering investigations and specialised exercises demanding modified equipment/monitoring.

The SOS Product Range

A range of products and capabilities has been developed to ensure that all the major elements in a radiation hard system are available and fully supported. The product strategy is to continue to develop products to increase the performance of the following families and release them to the appropriate military and space quality levels.

Microprocessors

The key microprocessor product is the high performance (2 MIPs) 1750 microprocessor. Designated as the MA31750, it meets the requirements for higher speed processing of both 1750A and 1750B instruction sets in space and military applications.

Also in the processor range is the MAS281 MIL-STD-1750A microprocessor. Based on the McDonnell Douglas MDC281, the GPS version has been enhanced to make it what was for a number of years the only viable radiation hard, space grade, 1750A microprocessor. It is supported by a range of standard peripheral devices to satisfy standard system functions.

Memories

A range of static random access memories (RAM) has been developed specifically for radiation hard applications. As the products have evolved from 1K bits to 64K bits, process and design techniques have been refined resulting in progressively harder and faster components.

Read Only Memory (ROM) is offered as a capability with either base or metal programming ROM is also used in standard products such as microcode ROM and databus protocol look-up tables.

Simple logic functions and octal transceivers, latches, buffers, decoders and multipliers have been included in the SOS product range to allow non-standard functions to be configured which do not justify a semicustom development. Innovative techniques allow new products to be rapidly introduced and a wide range of devices to be manufactured with minimal lead time and cost penalties.

Databus

GPS has been a leading supplier of MIL-STD-1553 products for more than a decade. In 1982, the first full protocol LSI chip set was demonstrated. A more powerful, radiation hard chip set has now been produced.

The MIL-STD-1553B protocol was originally defined for military avionic systems but is now used in other military systems and is being designed into future space projects.

Semicustom

Gate arrays ranging in complexity from 700 to 60,000 gates provide rapid access to the SOS technology for non standard functions. For more complex designs, an extensive standard cell library enables design engineers to quickly and consistently produce radiation hard circuits to meet customers' specific requirements.

Mixed Analogue and Digital

Standard products and standard cells have been produced for such functions as analogue to digital, and digital to analogue converters, comparators and operational amplifiers.

Radiation Performance

An integrated circuit is said to be radiation hard if it can continue to function within its specifications after exposure to a stated amount of radiation. On Earth, the atmosphere shields systems at ground level from most gamma and x-rays, electrons and heavy ions which occur in space, can change the electrical properties of integrated circuits and adversely affect system performance. Defence applications are also demanding increasing tolerance to a variety of radiation effects. Although all semiconductors have some intrinsic resistance to radiation, CMOS SOS is the only technology which is tolerant to all radiation effects.

Accumulated Total Dose

The total dose hardness of an integrated circuit is a measure of its ability to withstand accumulated doses of high energy radiation in the form of gamma or x-rays. In the space environment, the ionising radiation that is absorbed by a device is accumulated over a long period of time; typically 100KRad (Si) over a 10 year operating life, but may be significantly higher depending on mission.

Ionizing radiation causes electron-hole pair generation in the oxide Recombination occurs immediately, but under a positive bias electrons are swept to the gate electrode within pico seconds. The less mobile holes move towards and eventually are trapped in the silicon silicon dioxide interface region, causing a negative threshold voltage shift. The effect of these changes to the core elements of the circuit range from input threshold degradation to functional failure and high static supply leakage.

Total dose hardness up to the 1M Rad(Si) level is only achieved by a constrained design system and special attention to critical process steps ,especially gate oxide growth. Detailed knowledge and analysis of radiation effects using the in-house gamma and x-ray facilities is also required.

Transient Dose

One well known problem with most technologies is their vulnerability to high transient doses of ionising radiation. These pulses have been shown to induce the latch up. CMOS circuits have certain parasitic transistors associated with adjacent P and N channel devices .These parasitics are configured so as to approximate a silicon controlled rectifier (SCR). The photo-current induced in these structures by a severs burst of ionising radiation can be sufficient to turn on the SCR. This then initiates a large, self perpetuating current flow capable of causing great damage to the device Once latched, a circuit can only be returned to correct operation (if not permanently damaged), by a power down/power up procedure.

It is physically impossible for a SOS device to suffer from latch up. In SOS, each transistor is made on an individual silicon island. These islands are isolated from each other by removing all epitaxial silicon from non-active areas, leaving only insulating sapphire substrate. This removes the possibility of any parasitic structures existing between transistors, and thus completely prevents latch up.

The other effect of transient radiation is to cause data corruption in stored cell elements. This corruption is caused by the inability of the power rail to hold up the voltage on a node sufficiently to maintain the data (power rail collapse). The voltage drop is as a result of the transient burst generating a photocurrent, the magnitude of which is proportional to total junction area. The CMOS SOS technology gains its high tolerance to transient radiation from the fact that much smaller photocurrents flow and hence voltage drop along

the supply is lower. This is due to the fact that the junction area is confined to only the thin epitaxial layer rather than the much larger junction and well depletion volumes which occur on conventional CMOS processes.

Evaluations have shown corruption levels of up to $1x10^{12}$ Rad(Si) Sec-1 and will survive without permanent degradation levels of $>1x10^{13}$ Rad(Si) Sec-1 on RAMS fabricated on the 1.5 micron SOS process.

Single Event Upset

SEU within a memory cell can be defined as the corruption of data caused by the creation of a charge in a circuit by a heavy particle ion. There is no permanent or long term damage to the circuit, data becoming valid again after the next write operation.

As a charged particle passes through a semiconductor, it will lose energy by ionisation. If a charged particle passes through a reverse-biased p-n junction, the electron-hole pairs generated in the device depletion region will be separated by the high electric field. The high carrier density created along the particle's track will distort the electric field of the junction depletion region. The field will be spread along the particle track and create a field funnel. The charges in this funnel will be collected by drift and will add to the charge collected in the junction depletion region.

If sufficient charge is deposited on the parasitic gate and junction capacitance, a voltage transient will appear. The voltage transient created by an event on a node can then cause the logic state of the cell to be inverted. The charge required to invert the state of the memory cell is referred to as the critical charge

Silicon on Sapphire technology offers significant advantages in this area. The physical structures of SOS transistors with their individual, totally isolated silicon islands, lead to much smaller 'junction depletion region' volumes than bulk CMOS technologies.

The charged particle can also induce latch up in bulk CMOS circuits. For the reasons outlined in the previous section this is not possible on CMOS SOS.

Evaluations carried out on a Cyclotron by the European Space Agency have shown a threshold LET of 59.4 Mev/(mg/sq. cm) for a 64K memory. The MA31750 has been evaluated on a Van de Graaff facility and found to just start upsetting at the 170 Mev/(mg/sq. cm) level. Both these devices are fabricated on the 1.5 micron process.

Neutron Radiation

CMOS SOS is inherently hard to neutron radiation. The main effect of neutrons are to degrade the silicon lattice giving rise to recombination sites. This has the effect of reducing minority carriers lifetime which has a significant effect on bipolar technologies.

CMOS SOS in common with all MOS is a majority carrier technology and is therefore largely unaffected. SOS Devices have been proven to with stand neutron radiation to greater than 10^{15} neutrons/cm^2 (the limit of the equipment used) without significant degradation of critical device parameters.

Section 1

Microprocessors

GEC PLESSEY

SEMICONDUCTORS

MA31750

HIGH PERFORMANCE MIL-STD-1750 MICROPROCESSOR

The GEC Plessey MA31750 is a single-chip microprocessor that implements the full MIL-STD-1750A instruction set architecture, or Option 2 of Draft MIL-STD-1750B. The processor executes all mandatory instructions and many optional features are also included. Interrupts, fault handling, memory expansion, Console, timers A and B, and their related optional instructions are also supported in full accordance with MIL-STD-1750.

The MA31750 offers a considerable performance increase over the existing MAS281. This is achieved by using a 32-bit internal bus structure with a 24 x 24 bit multiplier and 32-bit ALU. Other performance-enhancing features include a 32-bit shift network, a multi-port register file and a dedicated address calculation unit.

The MA31750 has on-chip parity generation and checking to enhance system integrity. A comprehensive built-in self-test has also been incorporated, allowing processor functionality to be verified at any time.

Console operation is supported through a parallel interface using command/data registers in I/O space. Several discrete output signals are produced to minimise external logic.

Control signals are also provided to allow inclusion of the MA31750 into a multiprocessor or DMA system.

The processor can directly access 64KWords of memory in full accordance with MIL-STD-1750A. This increases to 1MWord when used with the optional MA31751 memory management unit (MMU). 1750B mode allows the system to be expanded to 8MWord with the MMU.

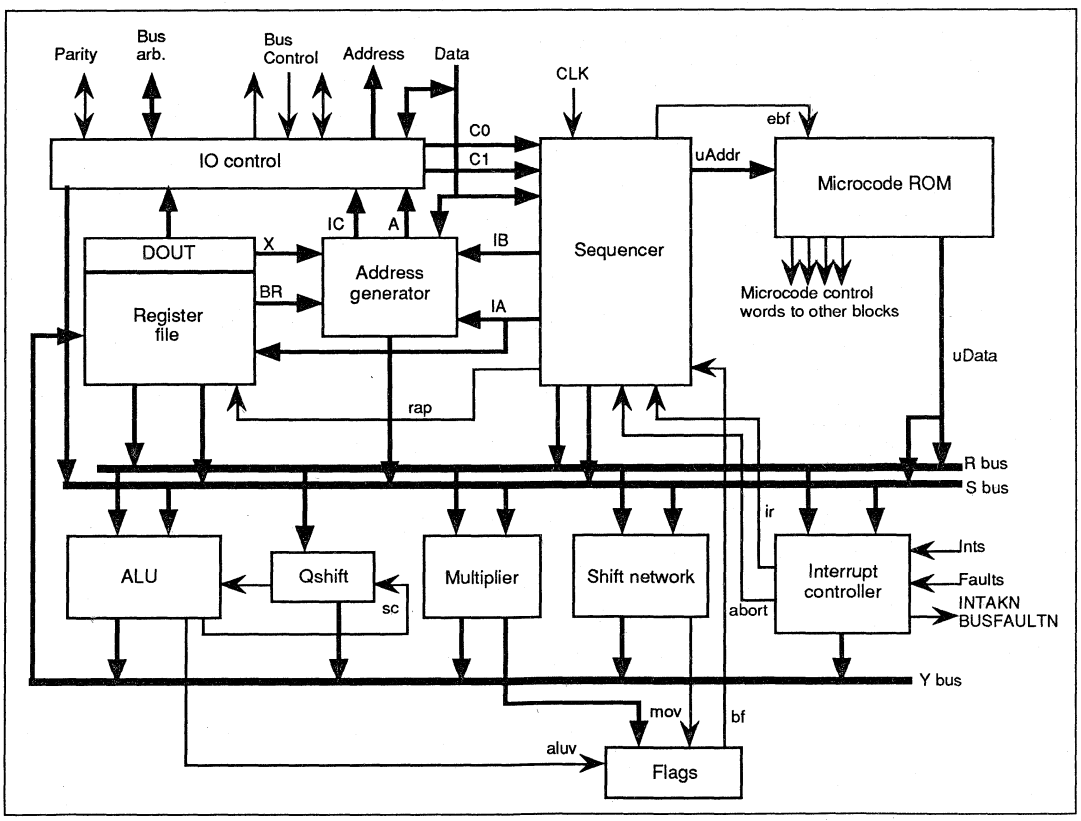


Figure 1: Architecture

1. ARCHITECTURE

The GEC Plessey MA31750 Microprocessor is a high performance implementation of the MIL-STD-1750A (Notice 1) Instruction Set Architecture. Figure 1 depicts the architectural details of the chip. Two key features of this architecture which contribute to the overall high performance of the MA31750 are a 32-bit shift network and a 24-bit parallel multiplier. These sub-systems allow the MA31750 to perform multi-bit shifts, multiplications,divisions and normalisations in a fraction of the clock cycles required on machines not having such resources. This is especially true of floating-point operations, in which the MA31750 excels. Such operations constitute a large proportion of the Digital Avionics Instruction Set (DAIS) mix and generally a high percentage of many signal processing algorithms, therefore having a significant impact on system performance.

Key features include:

1) A three-bus (R, S, and Y) datapath consisting of an arithmetic/logic unit (ALU), three-port register file, shift network, parallel multiplier and flags block;
2) Four instruction fetch registers C0,C1, IA, and IB;
3) Two operand transfer registers DI, and DO;
4) Two address registers IC and A;
5) A state sequencer;
6) Micro-instruction decode logic.

The relationship between these functional blocks is shown in Figure 1.

2. ADDITIONAL FEATURES

The MA31750 may be operated in one of two basic user selectable modes. 1750A mode follows the requirements of MIL-STD-1750A (Notice 1) and implements all of the mandatory features of this standard. In addition, many of the optional features such as interval timers A and B, a watchdog timer and parity checking are included. 1750B mode, when selected, allows the user access to a range of new instructions and features as described in the Draft MIL-STD-1750B, Option 2. These include a range of unsigned arithmetic operations and expanded addressing support instructions.

2.1. MIL-STD-1750 OPTIONAL FEATURES

In addition to implementing all of the required features of MIL-STD-1750A and the Draft standard MIL-STD-1750B, the MA31750 also incorporates a number of optional features. Interval timers A and B as well as a trigger-go counter are provided. Most specified XIO commands are decoded directly on the chip and an additional set of commands, associated with MMU and BPU operations, are also decoded on chip.

2.2. BUS ARBITRATION

The MA31750 has a number of extra control lines to allow its use in a system utilising multiple processors. A bus request and grant system coupled with external arbitration logic allows common data and address buses to be used between devices. A lock request pin is also provided to allow the processor to maintain control of the buses when modifying areas of shared memory.

2.3. MEMORY BLOCK PROTECTION

The basic MMU function allows write or execute protection to be applied on 4KWord block boundaries. This may be further resolved to 1kWord blocks by the inclusion of a Block Protect Unit (BPU). The MA31751 can act as both an MMU and a BPU in 1750A mode, operating with the full compliment of 1MWord of memory. It will also support expansion to 8MWord in accordance with Draft MIL-STD-1750B.

3. MODES OF OPERATION

MA31750 operating modes include: (1) initialisation, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) timer operations and (6) console operation.

3.1. INITIALISATION

The MA31750 executes a microcoded initialisation routine in response to a hardware reset or power-up. Figure 3 shows a cycle-by-cycle breakdown of this routine. The operations performed are dependent on the system configuration read by the processor during startup. Figure 2 summarises the resulting initialisation state.

MA31750	
Instruction Counter	Zero
Status Word	Zero
Fault Register Zero	Zero
Fault Mask Register (1750B)	All ones
Pending Interrupt Register	Zero
Interrupt Mask Register	Zero
General Registers	Undefined
Interrupts	Disabled
Timers A and B	Zeroed and started
Timer Reset Registers (1750B)	Zero
Trigger-Go Counter	Reset and started
TGON Line	High
Start-Up ROM	Enabled
DMA	Disabled
MMU	
Page Registers AL/W/E fields	Zero
Page Register PPA field	Logical to physical
BPU	
Memory Protect RAM	Zero (disabled)
Global Memory Protect	Enabled

Figure 2: Initialization State

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero with AS = 0, PS = 0 and PB = 0 and will be from the Start-Up ROM (SUR) if implemented. Whether BIT passes or not, the processor will begin instruction execution at this point. The system start-up code may include a routine to enable and unmask interrupts in order to detect and respond to a BIT failure if required.

Addr	Operation
0	PIC initialised
1	A<-- 0x8410
*2	Read external configuration register from 8410H (CONFWN asserted low)
3	-
1F	-
20	If BPU, N<-- 128 else N<-- 0
21	Decrement N; branch to 21 if N >= 0
4	Write internal configuration register
5	-
6	If no MMU, br to 7
13	-
14	-
15	N <-- 256
16	Decrement N
*17	Write MMU Instruction Page Register N
*18	Write MMU Operand Page Register N; branch to 16 if N > 0
19	A <-- 0400H
1A	N <-- 16
1B	PBSR <-- N
1C	-
*1D	Write Memory control register to MMU with PB = N
1E	Decrement N; branch if N >= 0 to 1B
7	A <-- 0
8	IC <-- A
9	Br to BIT if required
A	-
B	Br if no SUR to 00D
C	-
D	Re-init PIC
E	-
*F	Zero SW
10	-
32	-
33	Br to 011 if BIT passed (or not run)
34	
35	
36	Set FT bit 13
11	Init DMAE, SUREN, NPU
12	
*3F8	Fetch first word from 0
*3F9	Fetch second word from 1 First instruction first cycle

* Indicates an external cycle

Figure 3: Initialization Sequence

3.1.1. CONFIGURATION REGISTER

The system configuration register allows the MA31750 to function with a variety of different system designs. Implemented features such as a BPU should be indicated as present by setting bits in an externally-implemented 16-bit latch - see figure 4 for bit assignments. The latch must be placed in IO space at the address defined by XIO RCW (8410) shown in the table of XIO commands, Figure 20c. The processor decodes this command internally and produces a discrete output signal CONFWN which may be used as the external register Output Enable control.

Bit	Function
0	MMU Select 0
1	BPU Select 0
2	1 = Console operation enabled
3	MMU Select 1
4	Interrupt sensitivity (1 = level, 0 = edge)
5	MMU Select 2
6	Parity sense (1 = odd, 0 = even)
7	1= BIT on power-up
8	1 = Start-Up ROM present
9	1 = DMA device present
10	1=1750A mode, 0=1750B mode
11	1=Instruction set expansion enabled
12	BPU Select 1
13	BPU Select 2
14-15	Reserved for future expansion

Figure 4: Configuration Word Bits

The processor maintains an internal configuration register which is updated from the external register during initialisation and during the execution of a NOP/BPT (No-op/Breakpoint) instruction. The internal configuration register is used to control the CPU. Note that although the external register can be read using XIO RCW, this does not affect the internal configuration. Note: if the interrupt level/edge trigger select bit - (bit 4) is changed in the internal register during normal operation of the device, one or more spurious interrupts may occur.

When in 1750B mode, the processor needs to know how many Page Banks are implemented in the external system so that Status Word changes can be protected properly. MIL-STD-1750B allows the options 0,1,2,4,8 or 16. The actual selection should be coded into the three configuration register bits MMU0, MMU1 and MMU2 as shown in figure 5.

In 1750A mode, setting any of the MMU select bits indicates the presence of an MMU, the actual code is unimportant in this mode.

BPU selects bits 2:0 should be set to indicate how much BPU-protected memory exists on the system. If no BPU is present, all three bits should be zero.

Selected bit			Function
MMU2	MMU1	MMU0	
0	0	0	No MMU in system
0	0	1	1 Page Bank (PB0)
0	1	0	2 Page Banks (PB0-1)
0	1	1	4 Page Banks (PB0-3)
1	0	0	8 Page Banks (PB0-7)
1	0	1	16 Page Banks (PB0-15)
1	1	X	16 Page Banks (PB0-15)

Note: In 1750A mode, setting any or all of the MMU select bits indicates the presence of an MMU.

Figure 5: MMU Selection Bits

3.1.2. BUILT-IN TEST (BIT)

BIT consists of ten subroutines, as outlined in Figure 6. If all ten subroutines execute successfully, or no BIT is selected in the configuration word, a BIT pass is flagged (seen externally as NPU raised high by the initialization routine). If any part of BIT fails, a corresponding bit identifying the failed subroutine is set in General Register R0, Fault Bit 13 is set in the Fault register (FT) and NPU is left in the low state. Figure 6 defines the coding of BIT results in R0. In the event of such a failure, the resulting processor reset state will be dependent on where in BIT the error occurred and may not be the same as that shown in figure 2. A BIT failure indication in FT will set the level 1 interrupt request bit of the Pending Interrupt (PI) register. Since initialisation disables and masks interrupts, this interrupt request will not be asserted. Any external interrupts or faults occurring during BIT will be cleared before program execution begins and will not be serviced.

Test Coverage	Machine Cycles	Bit set on fail
Temporary Registers (T0-T11)	47	7
General Registers (R0-R15)	79	7
Flags Block	18	8
Sequencer Operation and ROM checksum	5632	9
Divide routine Quotient Shift Network	12	10
Multiplier and ALU	13	11
Barrel shift Network	13	12
Interrupts and fault handling and detection	17	13
Address generator block	13	14
Instruction pipeline	15	15

Note: BIT pass is indicated by all zeros in FT bits 13,14, and 15

Figure 6: Built-In Test Coverage

3.2. INSTRUCTION EXECUTION

Once initialisation has been completed, the processor will begin instruction execution. Instruction execution is characterised by a variety of operations, each is one machine cycle in duration (two or more system CLK periods). Depending on the instruction being executed at the time, these operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by an interrupt or Console request. Internal cycles are always two CLK periods long, whilst the other cycle types are a minimum of two CLK periods - extendable by inserting waitstates. In all cycles except internal cycles, RDN, WRN, DSN and AS strobes are produced to control the transfer and latching of data and address around the system.

Cycle Type	RD/WRN	O/IN	M/ION	Description
Internal Cycle	H	L	H	Used to perform all CPU data manipulation operations where bus activity is not required.
Instruction Fetch	H	L	H	Used to keep the instruction pipeline full with instructions and/or their postwords. At least one instruction is always ready for execution when the preceding instruction is completed. During jump and branch instruction execution the pipeline is refilled by two consecutive instruction fetches starting at the new instruction location. It is also refilled as part of interrupt request processing.
Operand Read Operand Write	H L	H H	H H	Used to read in data from the external system and to write results to the system.
IO Read IO Write	H L	H H	L L	Input/Output transfers utilize the MIL-STD-1750 XIO and VIO instructions. RD/WN defines the direction of the transfer. IO transfers may be divided into three groups; those commands which are implemented internally by the CPU, those commands which are implemented by external system hardware and those commands defined as illegal by MIL-STD-1750A and B.

Figure 7: External Cycle Types

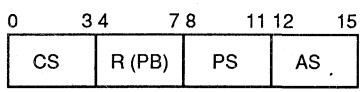
3.3. IO OPERATION

The MA31750 supports a 64KWord addressing space dedicated to IO control and communication in accordance with MIL-STD-1750. The control line MION is asserted low when accessing IO space (see figure 7 above for other strobe states). One of the two commands XIO or VIO is used to specify both data for the transfer and the port address (referred to as an XIO Command in 1750). The CPU contains logic which decodes all internally supported XIO commands and generates the control signals necessary to carry out the commanded action. In addition, the validity of a command not implemented internally is verified. Figure 20c identifies the XIO commands which are internally supported by the MA31750.

3.4. INTERRUPT AND FAULT HANDLING

3.4.1. STATUS WORD (SW)

Figure 8 depicts the status register format. This 16-bit word is divided into four, 4-bit sections. Three of these sections [AS, PS and, (1750B mode) PB] are control bits for implementing expanded memory with an external MMU. The fourth section, CS, is used to hold the carry, positive, zero and negative condition flags set by the result of the previous arithmetic operation.



Field	Bits	Description
CS	0 1 2 3	CONDITION STATUS C- Carry from an addition or no borrow from a subtraction. P- Result > 0 Z- Result = 0 N- Result < 0
R PB	4-7	RESERVED (=0) in 1750A mode Page Bank Select in 1750B mode
PS	8-11	PROCESSOR STATE: (a)- Memory access to key code (b)- Priviledged instruction enable
AS	12-15	ADDRESS STATE: Page register sets for expanded memory addressing.

Figure 8: Status Word Format

The AS field is used during expanded memory access to define the page register set to be used for instruction and operand memory references. The PS field is used during memory protect operations to define the access key used for memory accesses. The PS field is also used during execution of privileged Instructions - PS must be zero for such operations to be legal. See Section 4.3 for further information on the use of this field. The PB field is used in conjunction with the AS field in 1750B mode to expand the number of page registers available. Note that attempting to set AS or PB to a non-zero value with no MMU, or setting PB to a non-zero value in 1750A mode is illegal. This will be aborted and a fault 11 will be generated (SW will remain unchanged).

3.4.2. PENDING INTERRUPT REGISTER (PI)

This 16-bit register is used to capture and hold interrupts until they can be processed by microcode and user software. A logic 1 is used to represent an active pending interrupt. The PI register supports three dedicated external, six user-definable external, and seven dedicated internal interrupts. Level-sensitive interrupts are sampled on each rising CLK edge, whilst edge sensitive interrupts are captured immediately.

System Interrupts		Internal Interrupts
PWRD	0	(Cannot be disabled or masked)
	1	Machine Error (Cannot be disabled)
INT02	2	
	3	Floating-Point Overflow
	4	Fixed-Point Overflow
	5	Executive call (Cannot be disabled or masked)
	6	Floating-Point Underflow
	7	Timer A Overflow
INT08	8	
	9	Timer B Overflow
INT10	10	
INT11	11	
IOI1	12	
INT13	13	
IOI2	14	
INT15	15	

Figure 9: Pending Interrupt Bit Assignments

System Faults		Internal Faults
MPROE (CPU)	0	
MPROE (DMA)	1	
PE (CPU memory)	2	
PE (CPU IO)	3	
PE (DMA)	4	
EXADE or Bus Timeout (CPU IO)	5	
	6	Parallel IO Transfer Error
FLT7	7	
EXADE or Bus Timeout (CPU memory)	8	
	9	Illegal Instruction Opcode
	10	Priviledged Instruction
	11	Unimplemented Address State
Reserved	12	
SYSF	13	MA31750 BIT Fail
EXADE (DMA)	14	
SYSF	15	

Figure 10: Fault Register Bit Assignments

3.4.3. MASK REGISTER (MK)

This 16-bit register is used to store the interrupt mask. Interrupts are masked by ANDing each mask bit with its corresponding PI register bit. ie. A logic zero in a given bit position indicates that the corresponding bit in the PI register will be masked. Interrupts which are masked will be captured in the PI register but will not be acted on until unmasked. Interrupt level zero can not be masked.

3.4.4. PRIORITY ENCODER

This encoder generates an interrupt request to the sequencer block whenever one or more unmasked interrupts are pending and enabled in the PI. The highest priority unmasked pending interrupt is encoded as a 4-bit vector. This vector is used during interrupt servicing in order to create the interrupt linkage and service pointers.

3.4.5. FAULT REGISTER (FT)

This 16-bit register is used to capture and hold both internal and user implemented external faults using positive logic, i.e., a logic one represents a fault. Bus cycle faults are captured at the end of each machine cycle whilst the two general purpose faults SYSFN and FLT7N are set when the low time exceeds the minimum pulse width. Setting any one or more faults in FT will cause a level 1 (machine error) interrupt request. Once a fault is set in FT, it may only be cleared via an XIO command.

In 1750B mode, a fault mask register is provided to allow selective masking of fault conditions. Section 4 (Software Considerations) contains further information. Figure 27 shows the fault register assignments.

3.4.6. MEMORY FAULT PAGE AND ADDRESS REGISTERS

These registers capture the page and address information at the end of each external cycle until a memory fault occurs. Faults setting bits 0, 1, 2 and 8 in the fault register cause the registers to stop latching new address information, so retaining information about the address at which the fault occured. The registers can be read (using the GPS defined XIOs RMFP and RMPA). The fault register must be cleared and both memory fault registers read before latching can restart.

The information stored in the memory fault registers is as follows:

MFPR[0:3]	**MFPR[4:7]**	**MFPR[8:10]**	**MFPR[11]**
A[0:3]	PB[0:3](ASOB)	Res	ION
MFPR[12:15]	**MFAR[0:15]**	Note:	MFPR[11] is the inverse of OIN.
AS[0:3]	A[0:15]		

These registers are only available if there is an MMU in the system. If there is no MMU present, then the RMFP and RMFA XIO commands become illegal.

The address information held in these registers can be used to restart code after a memory fault has occurred. Bits [6:7] of the OAS register store information on the type of instruction which was being executed when the fault occured:

00 → branch that was taken
01 → single word instruction
10 → double word instruction

(Subtracting this value from the saved address will give the address of the failed instruction unless it was a branch that was taken).

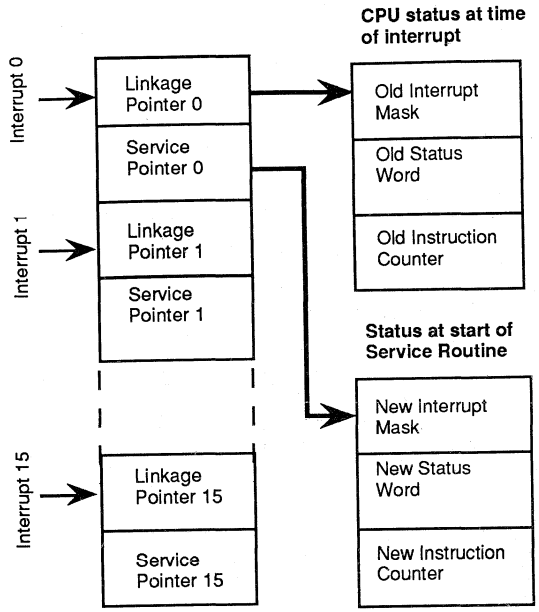


Figure 11: Interrupt Vectoring

3.4.7. INTERRUPT SERVICING

Nine user interrupt request inputs are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the rising edge of CLK (level sensitive interrupts only) and latched into the Pending Interrupt (PI) register on the falling edge of CLK at the end of the current CPU cycle. This sequence occurs whether interrupts are enabled or disabled or whether the specific interrupt is masked or unmasked. More details of interrupt operations are available in Applications Note 4.

All of the user interrupts PWRDN, INT02N - INT15N may be programmed to be either level or edge sensitive by setting or clearing the appropriate bit in the system configuration register. If edge sensitivity is selected then an interrupt request input must return to the high state before a subsequent request on that input will be detected. If level sensitivity is selected then holding an interrupt input low will cause a new interrupt to be latched following each service. Note that interrupts IOI1N and IOI2N are level sensitive only.

In order that the system may recognise when a service has been started, an interrupt acknowledge pin is provided. During the microcoded interrupt service routine execution, the processor will read the Linkage Pointer address in memory. During this operand read cycle, the processor will also assert INTAKN low, which may be used in conjunction with AS and address bus bits A[11:14] to reveal the priority level of the interrupt being serviced. (A[11:14] = 0 indicates level 0 interrupt, A[11:14] = 1 indicates level 1 interrupt, and so on). INTAKN should also be used to remove level-sensitive interrupt requests to ensure that repeated requests are not generated.

	Interrupt No.	LP Address	SP Address
PWRD	0	20	21
ME	1	22	23
INT02	2	24	25
FI.P o/f	3	26	27
Fx.P o/f	4	28	29
BEX	5	2A	2B
FI.P u/f	6	2C	2D
Timer A	7	2E	2F
INT08	8	30	31
Timer B	9	32	33
INT10	10	34	35
INT11	11	36	37
IOI1	12	38	39
INT13	13	3A	3B
IOI2	14	3C	3D
INT15	15	3E	3F

Note: Addresses (in hex) are in operand space

Figure 12: Interrupt Pointer Address

When an interrupt request is latched into PI, it is ANDed with its corresponding mask bit in the mask register (MK). NOTE: Interrupt level 0 is non-maskable. Any unmasked pending interrupts are output to the priority encoder where the highest priority is encoded as a 4-bit vector. If interrupts are enabled and an unmasked interrupt is pending, the priority encoder will assert an interrupt request to the sequencer. 1 or 2 extra CLKs will be inserted into the machine cycle on which the interrupt request is asserted.

Upon completing execution of each MIL-STD-1750A or B instruction, the sequencer checks the state of the priority encoder interrupt request. If a request is asserted, the sequencer branches to the microcode interrupt service routine. This routine reads the 4-bit pending interrupt vector and then uses this value to calculate the appropriate interrupt linkage (old processor context save area) and service (new context load area) pointers. Figure 11 depicts this relationship. Figure 12 defines the pointer values.

Using the linkage and service pointers, the microcode interrupt service routine performs the following: (1) the current contents of the status word, mask register, and instruction counter are saved; (2) a write status word (WSW) I/O command is executed with an all zero data word; (3) the new mask is loaded into MK and interrupts are disabled; (4) the new status word is read and checked for a valid Address State (AS[0:3]) field - If the address state is non-zero and an MMU is not present, AS[0:3] is set to zero and fault 11 (address state error) is set in the fault register FT); (5) a write status word command using the new status word is performed; and (6) the new IC value is loaded into IC, the instruction pipeline is flushed and refilled starting at the new address, and instruction execution begins.

[NOTE: The steps listed above represent a summary of actions performed during interrupt servicing and do not necessarily reflect the actual order in which these events take place.]

If an address state fault occurs during the service routine, interrupt level 1 will be set. This interrupt will be serviced when interrupts are re-enabled unless it is masked by the new value in MK.

3.4.8. FAULT SERVICING

Five user fault inputs are provided. A low on any of the three bus-cycle-related fault inputs, EXADEN, MPROEN or PEN, will be latched into the Fault Register (FT) on the next falling edge of AS. A low on either of the two general purpose fault inputs, FLT7N or SYSFN, will be latched immediately and will be sampled into the appropriate bit of FT on the falling edge of AS.

Any fault which sets a bit in the FT immediately causes a level 1 pending interrupt to be entered into the PI register. This interrupt is maskable but may not be disabled.

This interrupt will be serviced at the end of the currently executing 1750 instruction if not masked. The microcoded interrupt service routine reads the interrupt priority vector and clears the bit relating to the serviced interrupt from the PI. However, the FT retains the set fault bits until the FT is cleared using the XIO RCFR command. (A non-destructive read of the FT is provided by the XIO RFR command.) Anti-repeat logic between the FT and the PI prevents the same fault being latched and serviced twice. However, as all FT bits are ORed together and input to PI bit 1, this also prevents any other faults being serviced until the fault register has been cleared. It is imperative, therefore, that the fault service routine executes a RCFR XIO before exiting. Different types of faults are serviced slightly differently as follows:

3.4.8.1. MPROEN and EXADEN

If MPROEN and/or EXADEN are low on a falling clock edge with AS and DSN high (see figure 23a), the processor will wait in this state. If either fault input remains low during two falling edges of TCLK, the cycle is forced to complete but RDN/WRN and DSN are inhibited (see figure 24b). This allows the processor to prevent erroneous accesses. An access fault will be registered as AS falls at the end of the cycle.

3.4.8.2. PEN

External parity errors are latched into the FT on the falling edge of AS. The fault bit set is dependant upon the type of transfer taking place (memory, IO or DMA).

3.4.8.3. FLT7N and SYSFN

These faults are latched immediately, but are not sampled into the fault register until the following falling edge of AS.

3.4.9. PARITY GENERATION AND CHECKING

The MA31750 features on-chip parity generation and checking on all data bus transfers. Data generated by the processor has a parity bit attached to it to allow external logic to verify write transfers. On read transfers, the processor will check the incoming parity (if enabled) and will generate the appropriate parity error fault if detected. However, the data to be checked is only available as DSN rises at the end of the cycle so the error flag is generated and latched in the cycle following the erroneous cycle. Parity checking may be

disabled when operating with devices which do not support parity generation by asserting the DPARN (Disable Parity) input low. The checking polarity (odd or even) is selectable with Configuration Register bit 6.

3.5. TIMER OPERATIONS

The MA31750 implements interval timers A and B, a trigger-go counter, and a bus fault timer. A discussion of each follows:

3.5.1. TIMERS A AND B

Two general-purpose, 16-bit timers are provided in the processor. Timer A is clocked by the TCLK input; timer B is clocked by an internally generated TCLK/10. The divider circuit is reset when Timer B is reset to give deterministic processor operation. MIL-STD-1750 requires TCLK to be a 100kHz pulse train. If allowed to overflow, timers A and B will set level 7 and level 9 interrupt requests respectively. Each timer can be read, loaded, started and stopped by using XIO commands as identified in figure 20c.

Each timer has associated with it a reset register from which the timer is automatically loaded following a software reset or overflow. These registers are initially loaded with zero but may be reloaded from software (using the XIO instructions OTA and OTB) to provide greater control over the count period.

The MA31750 timers A and B will be disabled when the device enters Console mode, as required by MIL-STD-1750A Notice 1.

3.5.2. TRIGGER-GO COUNTER

This 16-bit counter is clocked by the TCLK input and is typically used as a system "watchdog" timer. It is enabled during system initialisation and may be preset under software control to give a wide range of timeout intervals. In order that the count period may be controlled, a reset register is provided. On reset, this register is loaded with zero, but can be reloaded under software control to take any value between 0 and $FFFF_{16}$ (a value of zero gives the maximum count period). This allows the timeout period to be varied between 20us and 0.65s. Note that there is no value which disables the timer.

The counter is incremented on each TCLK falling edge. Whenever the trigger-go counter overflows, TGON drops low and remains low until the counter is reloaded from the reset register via the GO internal XIO command. TGON low would typically be used to initiate a user-defined system recovery action such as a system reset.

3.5.3. BUS FAULT TIMER

All bus operations are monitored to ensure timely completion. A hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition) and is reset upon receipt of the external ready (RDYN) signal. If this circuit fails to reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 8 (if the transaction is with memory) or bit 5 (if the transaction is with I/O) of the Fault Register (FT) is set. This sets Pending Interrupt level 1 and causes the strobes to be suppressed and the current bus cycle to be aborted. The MIL-STD-1750 instruction is aborted, and control passes to the level 1 interrupt service routine (if the level 1 interrupt is unmasked). The timeout mechanism is disabled and reset if DTON is asserted low.

3.6. CONSOLE OPERATION

The MA31750 is capable of interfacing directly to an external console, allowing the developer to: examine and change the contents of internal registers, memory and IO devices; single step code and halt the processor. Applications Note 3 provides a full description of the Console interface, its implementation and operation.

3.7. MULTIPROCESSOR SUPPORT

Once initialisation has been completed, the processor will begin instruction execution by executing a sequence of micro-instructions, each one machine cycle (two system clock periods) long. Each machine cycle may perform either an internal or an external operation; if the operation is purely internal then the system busses will not be in use and may be reassigned to another processor.

An external machine cycle (indicated by REQN low during the second half of the previous cycle) will cause the processor to stall upon completion of the current microcycle, awaiting GRANTN asserted low. Whilst GRANTN is high the busses remain undriven.

In simple, single processor systems which use no DMA devices the GRANTN line should be tied to GND to allow the processor to retain control of the busses. The LOCKN and REQN pins can be left open-circuit in this case. Applications Note 11 provides further information for designers of systems with more than one bus master.

4. SOFTWARE CONSIDERATIONS

4.1. OPERATING MODES

The MA31750 is capable of being operated in one of two basic modes as previously mentioned. These are described in detail below:

4.1.1 1750A MODE

1750A mode is a full implementation of MIL-STD-1750A (Notice 1) and includes some of the optional features mentioned in this standard.

4.1.2 1750B MODE

1750B mode is an implementation of the proposed MIL-STD-1750B, Option 2, Draft of 17th July 1988. This mode extends the basic 1750A mode operation. Note that the transcendental functions SIN, COS, LN etc. (Option 3 of MIL-STD-1750B) are not supported. Features new to MIL-STD-1750B which are in violation of MIL-STD-1750A are only enabled in 1750B mode. The additional instructions available in 1750B mode are detailed in figure 20b.

4.2. ACCESSING IO USING XIO AND VIO COMMANDS

MIL-STD-1750 defines a 64KWord addressing space which is available exclusively for accessing IO resources. Two special commands, XIO and VIO, are provided as part of the instruction set for accessing this space. Port addresses are specified as a 16-bit Command word which is supplied as a parameter to the XIO/VIO instruction. The MSB of the Command word indicates the direction of data transfer between the port and the register specified in the XIO command (a 1 in the MSB indicates that the port is being read, whilst 0 indicates a write to the port).

Output	Input	Usage
0000-03FF	8000-83FF	PIO
0400-1FFF	8400-9FFF	Spare
2000-20FF	A000-A0FF	CPU and auxiliary register control
2100-2FFF	A100-AFFF	Reserved
3000-3FFF	B000-BFFF	Spare
4000-40FF	C000-CFFF	CPU and auxiliary register control
4100-4CFF	C100-CCFF	Reserved
4D00-4FFF	CD00-CFFF	Extended memory protect RAM
5000-50FF	D000-D0FF	Memory protect RAM
5100-51FF	D100-D1FF	MMU Instruction Page Registers
5200-52FF	D200-D2FF	MMU Operand Page Registers
5300-7FFF	D300-FFFF	Spare

Figure 13: XIO Command Channel Grouping

XIO command addresses are grouped by the Standard according to function. Certain groups are 'reserved' and must not be implemented. Attempts to read or write these areas will be prevented by the processor and a fault will be logged in the fault register. Other groups are designated 'spare' and may be implemented as required by the system designer. Note, however, that there is a third group which access system resources such as MMU page registers and interrupt control registers which are not available to the user to implement. A summary of the XIO map is provided in figure 13, whilst the detailed list of implemented command addresses is shown in Figure 20c.

The VIO (Vectored IO) command allows a number of IO operations to be executed in a sequence from a table. Applications Note 8 gives further information on the use of this command.

Both XIO and VIO are priveleged commands and as such can only be executed when the Status Word PS field is zero.

4.3. PROCESSOR STATE AND PRIVILEGED INSTRUCTIONS

The Processor State is defined by a 4-bit value held in the processor Status Word. If the value is made non-zero then attempts to execute the commands XIO, VIO or LST will be aborted and a fault will be raised. This is intended to deny direct access to the hardware from user applications (running in PS≠0), whilst allowing the Operating System (operating with PS=0) access to the system IO and interrupt resources.

If an MMU is present on the system the PS field is used in conjunction with the page register Access Key field to provide a further level of protection to the system. When PS=0 access is granted to all pages, irrespective of their key value. If PS is non-zero, access is only permitted if the Access Key is equal to the PS value, or the Access Key is 15. Access Key 15 should be applied to a shared area of code or data, and is accessable to all PS values.

4.4. USING START-UP ROM

The transition between code execution from Start-up ROM and system RAM must be made with care. If a system overlays RAM with the Start-Up ROM and the transition is made by simply executing XIO DSUR from the ROM, then the instruction pipeline will contain the value stored in the ROM location immediately following the XIO DSUR command. This value will be treated as an instruction and the processor will attempt to execute it. In such cases, it is recommended that DSUR be followed by an unconditional branch instruction with offset, i.e. the BR instruction. An alternative approach is simply to jump to a portion of RAM not overlaid by the Start-Up ROM and execute DSUR from RAM.

4.5. USING SOFTWARE TIMERS A AND B

The MA31750 implements the two software timers, A and B as defined in the MIL-STD 1750A specification. These are general purpose timers which are clocked at 100kHz and 10kHz respectively, giving clock 'tick' intervals of 10us and 100us respectively. They may be started using the XIO TAS and XIO TBS instructions, and stopped using XIO TAH and XIO TBH. If a timer is allowed to overflow ($FFFF_{16}$ - 0000_{16}) it will generate pending interrupt levels 7 (A) or 9 (B).

In 1750B mode each timer has associated with it a reset register which may be loaded with any 16-bit value from software. If a timer is allowed to overflow, an automatic reset will take place which will reload the timer with the value held in its on-chip reset register, provided that the timer had previously been loaded using XIO OTA/OTB. If this is not the case, then the timers will reset to zero on overflow. Each of the reset registers is initialised to zero but may be changed using XIO OTAR or XIO OTBR.

4.6. FAULT MASK REGISTER

A fault mask register is accessible in 1750B mode. Its function is similar to that of the Interrupt Mask register and allows selective enabling and disabling of all bits in the Fault Register. All faults are maskable. Setting a bit in this register allows the corresponding fault bit to be seen by the system. The mask register is loaded with $FFFF_{16}$ on initialisation.

4.7. GENERAL REGISTERS R0-R15

There are 16 general purpose registers defined by MIL-STD-1750; each is 16-bits wide. Adjacent registers may be concatenated to provide storage for the larger data formats (Double Integer and Float - 32-bit; Extended Float - 48-bit). The first register in the set stores the most significant data word and is the register specified when referring to the value. Wrap-around occurs between R15 and R0.

Although generally all registers are the same, certain registers are notionally assigned to particular tasks, see figure 15.

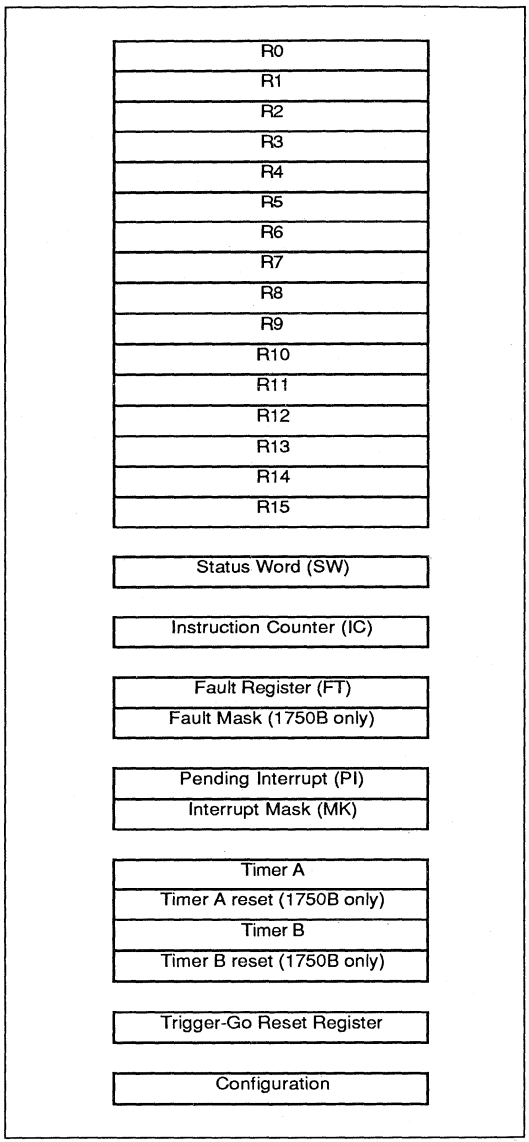


Figure 14: Register Set Model

4.8. MIL-STD-1750 DATA TYPES

The MA31750 fully supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended precision floating- point data types. Figure 16 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. All floating-point operands are expected to be normalised. If not normalised, the results from an instruction are not defined.

4.9. MIL-STD-1750 ADDRESSING MODES

The MA31750 supports the eight basic addressing modes specified in MIL-STD-1750A. These addressing modes are depicted in Figure 18 and are defined below. In binary operations one operand is assumed to be in a register (specified as part of the opcode) whilst the second operand (the Derived Operand, DO) is taken from a source which is dependent upon the addressing mode, see figure 17. Many adddressing modes may be specified as indexable: the index register may be any of the general purpose registers R1-R15 (if 0 is specified then the non-indexable form is used). For Base Relative addressing modes the first operand is fixed as part of the instruction (either R0 for Double Integer operations, or R2 for Single Integer operations).

4.10. MEMORY ADDRESSING CAPABILITY

In accordance with MIL-STD-1750A, the MA31750 can access a 64KWord address space directly. With the addition of a single external GEC Plessey MA31751 chip, configured as a Memory Management Unit (MMU), this address space may be expanded to 1MWord (1750A mode) or 8MWord (1750B mode). The MA31751 data sheet gives further information on the MMU/BPU chip and on the memory management scheme employed. Note that whilst one MMU can be used to provide the full range of physical addresses to the system memory, the logical addressing capability may also be expanded by adding further MMU devices up to a maximum of 16.

Register(s)	Notional Use or Restriction on Use
R0	Cannot be used as an index register With R1: Implied register in Double mode Base Relative addressing
R2	Implied register in Single mode Base Relative addressing
R3-R11	General purpose
R12-R15	Base relative registers
R15	Stack pointer in PSHM and POPM operations

Figure 15: General Register Usage

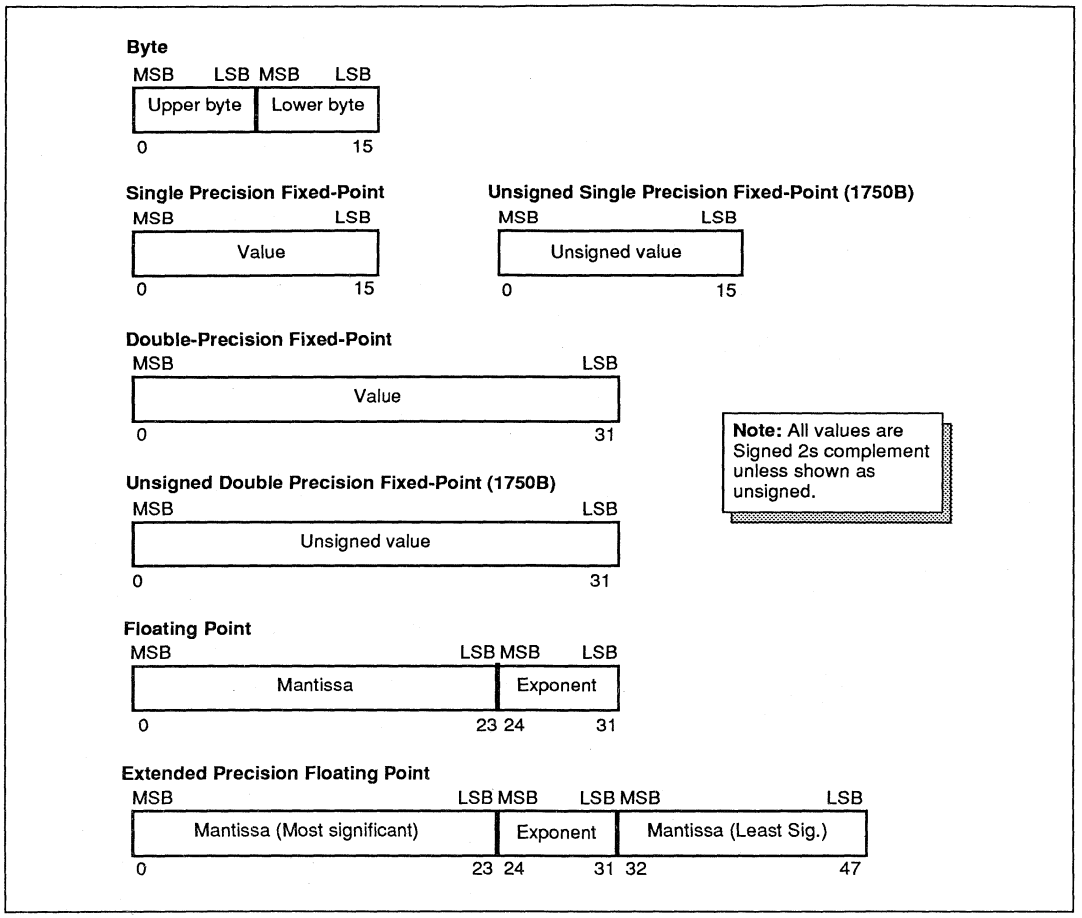


Figure 16: Data Formats

Mode	Name	Derived Operand
R	Register Direct	The operand is contained in a regular specified by the instruction.
D, DX	Memory Direct	The instruction postword (plus RX if RX ≠ 0), contains the memory address of the operand.
I, IX	Memory Indirect	The instruction postword (plus RX if RX ≠ 0) contains the address of the address which holds the operand.
IM, IMX	Immediate Long	The instruction postword (plus RX if RX ≠ 0) holds the operand.
ISP	Immediate Short Positive	The operand value is specified as part of the instruction. (ISP specifies values between 0001_H and 0010_H, ISN specifies values between $FFFF_H$ and $FFEF_H$).
ISN	Immediate Short Negative	The operand value is specified as part of the instruction. (ISP specifies values between 0001n and 0010n, ISN specifies values between FFFFn and FFEFn).
ICR	Instruction Counter Relative	A 2s-complement, 8-bit displacement which is sign-extended and added to the Instruction counter to provide an offset of -128 to +127.
B	Base Relative	Data at address given by: contents of specified base register (R12-R15, specified by opcode), plus unsigned 8-bit displacement field from opcode.
BX	Base Relative Indexed	Data at address given by contents of specified base register (R12-R15, specified by opcode), plus contents of RX register if RX ≠ R0
S	Special	See instruction for details.

Figure 17: Address Mode Summary

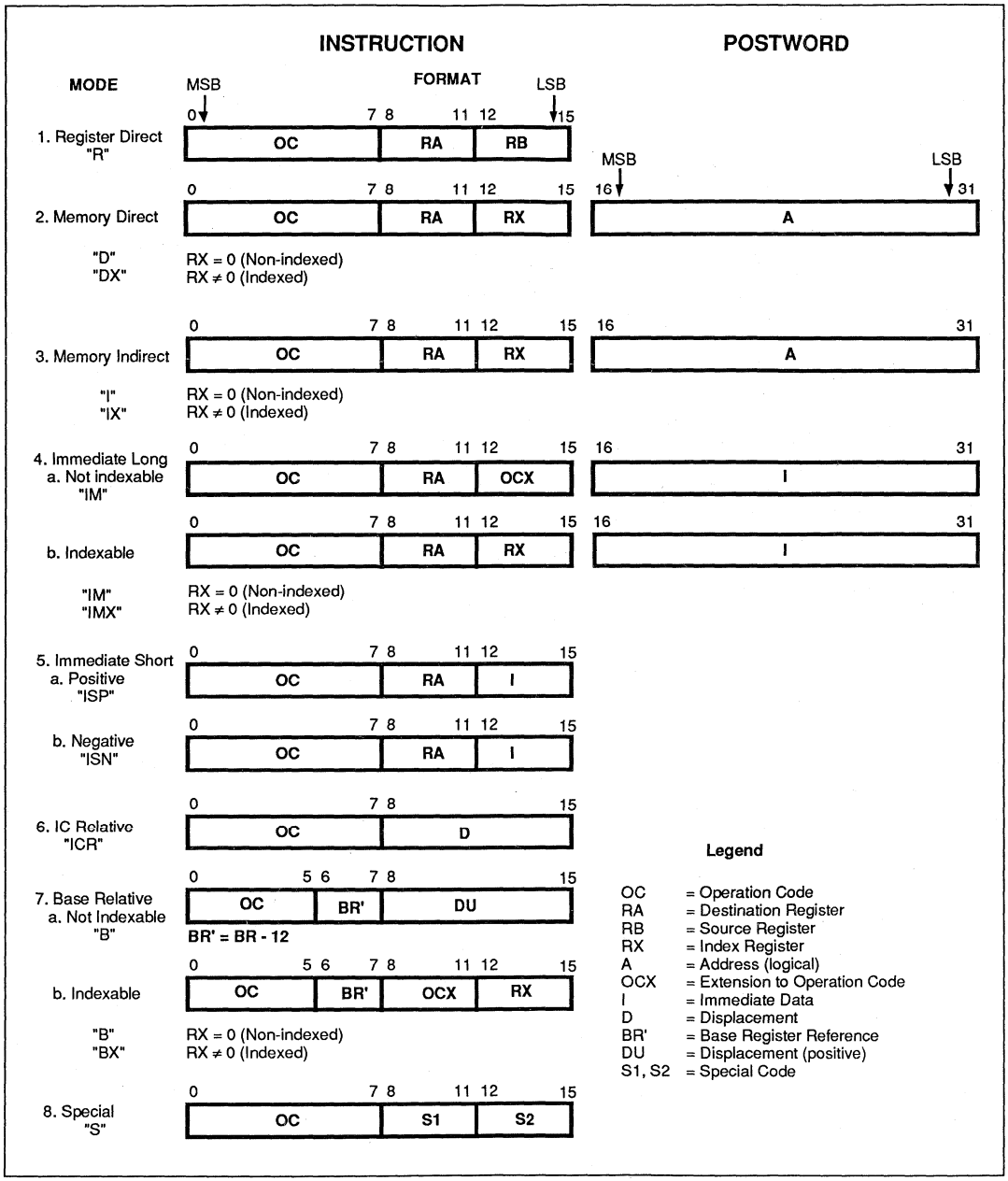


Figure 18: Addressing Modes

5. PERFORMANCE

5.1. BENCHMARKING

Figure 20a defines the number and type of machine cycles associated with each MIL-STD-1750 instruction. This information may be used when benchmarking MA31750 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix is that it does not reflect the impact of data dependencies on system performance. E.g. a multiplication in which the operand is zero may be performed much faster than one with two non-zero operands.

Realistic benchmarks must therefore take both the instruction mix and data dependencies into account. To this end, machine cycle counts in figure 20a which have data dependencies are annotated with either an "a" or "wa" suffix.

An "a" suffix reflects an average number of machine cycles (where each of several possibilities is equally likely) and a "wa" suffix reflects a weighted average number of machine cycles (where some data possibilities are more likely than others).

Weighted averages are only applicable to floating-point operations. Normalisation and alignment operations are also represented. Figure 19 shows MA31750 throughput, at various frequencies and wait states, for the floating point DAIS mix.

5.2. EXPANDED MEMORY PERFORMANCE

The inclusion of an MMU (Memory Management Unit) will degrade the throughput performance of the processor in two ways. Firstly, each memory access will have an additional overhead associated with the formation of the extended address from the MMU. This may require that the processor inserts wait states to lengthen each external cycle. Secondly, the MMU itself may require that some 'housekeeping' work be done by the processor, which will lengthen the program execution time. There are no widely accepted benchmarks which may be used to measure the resultant decrease in throughput.

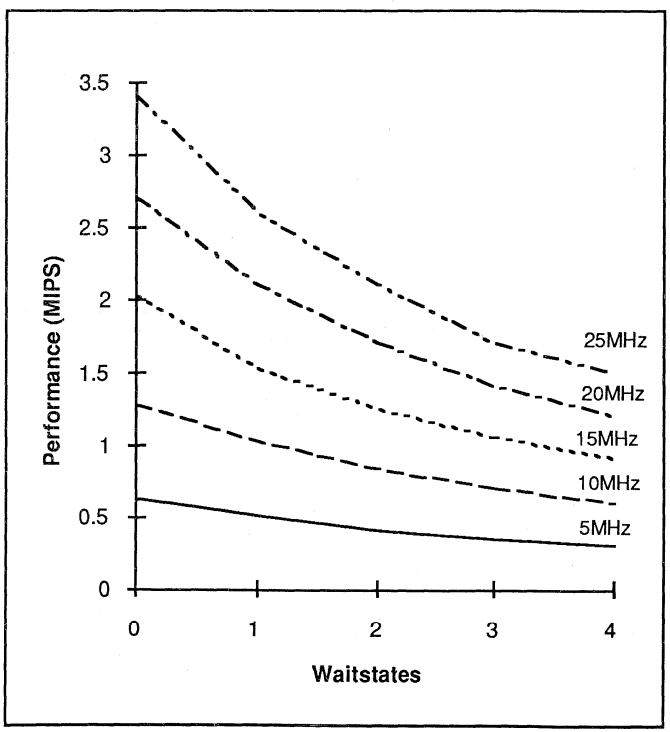


Figure 19: Throughput (MIPS) with Waitstates

5.3. INSTRUCTION SUMMARY

OPERATION	Mnem.	Format	Opcode (Ext)	Memory cycles	Internal Cycles
SINGLE LOAD/STORE					
Single Precision Load	LR	R	81	1	0
	LB	B	0X	2	1
	LBX	BX	4X 0	2	1
	LISP	ISP	82	1	0
	LISN	ISN	83	1	0
	L	D,DX	80	3	0
	LIM	IM,IMX	85	2	0
	LI	I,IX	84	4	0
Double-Precision Load	DLR	R	87	1	0
	DLB	B	0X	3	1
	DLBX	BX	4X 1	3	1
	DL	D,DX	86	4	0
	DLI	I,IX	88	5	0
Single-Precision Store	STB	B	0X	2	0
	STBX	BX	4X 2	2	1
	ST	D,DX	90	3	0
	STI	I,IX	94	4	0
Store Non-Negative Constant	STC	D,DX	91	3	0
	STCI	I,IX	92	4	0
Double-Precision Store	DSTB	B	0X	3	0
	DSTX	BX	4X 3	3	1
	DST	D,DX	96	4	0
	DSTI	I,IX	98	5	0
Load Multiple Registers	LM	D,DX	89	3+n	0
Store Multiple Registers	STM	D,DX	99	2+n	1
COMPARE					
Single-Precision Compare	CR	R	F1	1	0
	CB	B	3X	2	1
	CBX	BX	4X C	2	1
	CISP	ISP	F2	1	1
	CISN	ISN	F3	1	0
	C	D,DX	F0	3	0
	CIM	IM	4A A	2	0
Compare Between Limits	CBL	D,DX	F4	4	2.7a
Double-Precision Compare	DCR	R	F7	1	0
	DC	D,DX	F6	4	0
BYTE					
Load From Upper Byte	LUB	D,DX	8B	3	1
	LUBI	I,IX	8D	4	1
Load From Lower Byte	LLB	D,DX	8C	3	0
	LLBI	I,IX	8E	4	0
Store Into Upper Byte	STUB	D,DX	9B	4	0
	SUBI	I,IX	9D	5	0
Store Into Lower Byte	STLB	D,DX	9C	4	1
	SLBI	I,IX	9E	5	1
Exchange Bytes in Register	XBR	S	EC	1	0

Figure 20a: Instruction Summary

OPERATION	Mnem.	Format	Opcode (Ext)	Memory cycles	Internal Cycles
INTEGER ARITHMETIC					
Single-Precision Integer Add	AR	R	A1	1	0
	AB	B	1X	2	1
	ABX	BX	4X 4	2	1
	AISP	ISP	A2	1	0
	A	D,DX	A0	3	0
	AIM	IM	4A 1	2	0
Increment Memory by a Positive Integer	INCM	D,DX	A3	4	0
Single-Precision Absolute Value	ABS	R	A4	1	1.5a
Double-Precision Absolute Value	DABS	R	A5	1	1.5a
Double-Precision Integer Add	DAR	R	A7	1	0
	DA	D,DX	A6	4	0
Single Precision Integer Subtract	SR	R	B1	1	0
	SBB	B	1X	2	1
	SBBX	BX	4X 5	2	1
	SISP	ISP	B2	1	1
	S	D,DX	B0	3	0
	SIM	IM	4A 2	2	0
Decrement Memory by a Positive Integer	DECM	D,DX	B3	4	0
Single-Precision Negate	NEG	R	B4	1	1
Double-Precision Negate	DNEG	R	B5	1	1
Double-Precision Integer Subtract	DSR	R	B7	1	0
	DS	D,DX	B6	4	0
Single-Precision Integer Multiply with 16-Bit Product	MSR	R	C1	1	2
	MISP	ISP	C2	1	2
	MISN	ISN	C3	1	3
	MS	D,DX	C0	3	2
	MSIM	IM	4A 4	2	2
Single-Precision Integer Multiply with 32-Bit Product	MR	R	C5	1	1
	MB	B	1X	2	2
	MBX	BX	4X 6	2	2
	M	D,DX	C4	3	1
	MIM	IM	4A 3	2	1
Double-Precision Integer Multiply	DMR	R	C7	1	16.5a
	DM	D,DX	C6	4	16.5a
Single-Precision Integer Divide with 16-Bit Dividend	DVR	R	D1	1	23.5a
	DISP	ISP	D2	1	23.5a
	DISN	ISN	D3	1	23.5a
	DV	D,DX	D0	3	23.5a
	DVIM	IM	4A 6	2	23.5a
Single-Precision Integer Divide with 32-Bit Dividend	DR	R	D5	1	28a
	DB	R	1X	2	29a
	DBX	BX	4X 7	2	29a
	D	D,DX	D4	3	28a
	DIM	IM	4A 5	2	28a
Double-Precision Integer Divide	DDR	R	D7	1	41a
	DD	D,DX	D6	4	41a

Figure 20a (continued): Instruction Summary

OPERATION	Mnem.	Format	Opcode (Ext)	Memory cycles	Internal Cycles
LOGICAL					
Inclusive Logical-OR	ORR	R	E1	1	0
	ORB	B	3X	2	1
	ORBX	BX	4X F	2	1
	OR	D,DX	E0	3	0
	ORIM	IM	4A 8	2	0
Logical-AND	ANDR	R	E3	1	0
	ANDB	B	3X	2	1
	ANDX	BX	4X E	2	1
	AND	D,DX	E2	3	0
	ANDM	IM	4A 7	2	0
Exclusive Logical-OR	XORR	R	E5	1	0
	XOR	D,DX	E4	3	0
	XORM	IM	4A 9	2	0
Logical NAND	NR	R	E7	1	0
	N	D,DX	E6	3	0
	NIM	IM	4A B	2	0
Set Bit	SBR	R	51	1	0
	SB	D,DX	50	4	0
	SBI	I,IX	52	5	0
Reset Bit	RBR	R	54	1	0
	RB	D,DX	53	4	0
	RBI	I,IX	55	5	0
Test Bit	TBR	R	57	1	0
	TB	D,DX	56	3	0
	TBI	I,IX	58	4	0
Test and Set Bit	TSB	D,DX	59	2	2.5a
Set Variable Bit	SVBR	R	5A	1	0
Reset Variable Bit	RVBR	R	5C	1	0
Test Variable Bit	TVBR	R	5E	1	0
Store Register Through Mask	SRM	D,DX	97	4	1

JUMP/BRANCH					
Jump on Condition	JC	D,DX	70	3a	0
	JCI	I,IX	71	3.5a	0
Jump to Subroutine	JS	D,DX	72	2	1
Subtract One and Jump	SOJ	D,DX	73	3a	0
Branch Unconditionally	BR	ICR	74	2	1
Branch if Equal to (Zero)	BEZ	ICR	75	2a	0
Branch if Less than (Zero)	BLT	ICR	76	2a	0
Branch to Executive	BEX	S	77	11	14
Branch if Less than or Equal to (Zero)	BLE	ICR	78	2a	0
Branch if Greater than (Zero)	BGT	ICR	79	2a	0
Branch if Not Equal to (Zero)	BNZ	ICR	7A	2a	0
Branch if Greater than or Equal to (Zero)	BGE	ICR	7B	2a	0

Figure 20a (continued): Instruction Summary

OPERATION	Mnem.	Format	Opcode (Ext)	Memory cycles	Internal Cycles
EXTENDED PRECISION					
Extended-Precision Floating-Point Load	EFL	D,DX	8A	5	0
Extended-Precision Floating-Point Store	EFST	D,DX	9A	5	0
Floating-Point Absolute Value of Register	FABS	R	AC	1	2wa
Floating-Point Negate Register	FNEG	R	BC	1	3wa
Floating-Point Compare	FCR	R	F9	1	3.7wa
	FCB	B	3X	3	3.7wa
	FCBX	BX	4X D	3	3.7wa
	FC	D,DX	F8	4	3.7wa
Extended-Precision Floating-Point Compare	EFCR	R	FB	1	4wa
	EFC	D,DX	FA	5	2wa
Floating-Point Add	FAR	R	A9	1	7wa
	FAB	B	2X	3	8.5wa
	FABX	BX	4X 8	3	8.5wa
	FA	D,DX	A8	4	8.5wa
Extended-Precision Floating-Point Add	EFAR	R	AB	1	21wa
	EFA	D,DX	AA	5	20wa
Floating-Point Subtract	FSR	R	B9	1	9wa
	FSB	B	2X	3	10wa
	FSBX	BX	4X 9	3	10wa
	FS	D,DX	B8	4	9wa
Extended-Precision Floating-Point Subtract	EFSR	R	BB	1	23wa
	EFS	D,DX	BA	5	22wa
Floating-Point Multiply	FMR	R	C9	1	1
	FMB	B	2X	3	2
	FMBX	BX	4X A	3	2
	FM	D,DX	C8	4	1
Extended-Precision Floating-Point Multiply	EFMR	R	CB	1	33wa
	EFM	D,DX	CA	5	32wa
Floating-Point Divide	FDR	R	D9	1	42.8wa
	FDB	B	2X	3	43.8wa
	FDBX	BX	4X B	3	43.8wa
	FD	D,DX	D8	4	42.8wa
Extended-Precision Floating-Point Divide	EFDR	R	DB	1	112.6wa
	EFD	D,DX	DA	5	112.6wa
STACK					
Stack IC and Jump to Subroutine	SJS	D,DX	7E	3	1
Unstack IC and return from Subroutine	URS	S	7F	3	1
Pop Multiple registers off the Stack	POPM	S	8F	1+n (n=0 to 15)	4
Push Multiple Registers onto the Stack	PSHM	5	9F	1+n (n=0 to 15)	8

Figure 20a: Instruction Summary

OPERATION	Mnem.	Format	Opcode (Ext)	Memory cycles	Internal Cycles
CONVERT					
Convert Floating-Point to 16-Bit Integer	FIX	R	E8	1	7.1a
Convert 16-Bit Integer to Floating-Point	FLT	R	E9	1	3
Convert Extended-Precision Floating-Point to 32-Bit Integer	EFIX	R	EA	1	8.5a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EFLT	R	EB	1	9
SHIFT					
Shift Left Logical	SLL	R	60	1	0
Shift Right Logical	SRL	R	61	1	0
Shift Right Arithmetic	SRA	R	62	1	0
Shift Left Cyclic	SLC	R	63	1	0
Double Shift Left Logical	DSLL	R	65	1	0
Double Shift Right Logical	DSRL	R	66	1	0
Double Shift Right Arithmetic	DSRA	R	67	1	0
Double Shift Left Cyclic	DSLC	R	68	1	0
Shift Logical, Count in Register	SLR	R	6A	1	2
Shift Arithmetic, Count in Register	SAR	R	6B	1	5a
Shift Cyclic, Count in Register	SCR	R	6C	1	2
Double Shift Logical, Count in Register	DSLR	R	6D	1	2
Double Shift Arithmetic, Count in Register	DSAR	R	6E	1	5
Double Shift Cyclic, Count in Register	DSCR	R	6F	1	2
I/O (See I/O Command Summary)					
Execute I/O	XIO**	IM,IMX	48	3	4.3a
Vectored I/O (n transfers)	VIO**	D,DX	49	***	***
SPECIAL					
Move Multiple Words, Memory-to-memory (n-words moved)	MOV	S	93	1+2n	7
Exchange Words in Registers	XWR	R	ED	1	2
Load Status	LST**	D,DX	7D	6	1
	LSTI**	I,IX	7C	7	1
No Operation	NOP	S	FF 00	1	2
Break Point	BPT	S	FF FF	1	6

Figure 20a (continued): Instruction Summary

OPERATION	Mnem.	Format	Opcode (Ext)	Memory cycles	Internal Cycles
1750B MODE INSTRUCTIONS The following instructions may only be executed in 1750B mode and are illegal in 1750A					
'LONG' LOADS AND STORES					
Long Load Single	LSL	S	CC	3	11
Long Load Double	LDL	S	CD	4	20
Long Load Extended Precision Floating-Point	LEFL	S	CE	5	27
Long Store Single	LSS	S	DC	4	9
Long Store Double	LDS	S	DD	6	16
Long Store Extended Precision Floating-Point	LEFS	S	DE	8	23
UNSIGNED ARITHMETIC					
Unsigned Integer Add	UAR	R	AD	1	4
	UA	D,DX	AE	3	4
Unsigned Integer Subtract	USR	R	BD	1	4
	US	D,DX	BE	3	4
Unsigned Integer Compare	UCR	R	FC	1	5
	UC	D,DX	FD	3	5
	UCIM	IM	4A 0	2	5
BYTE LOADS AND STORES					
Load Byte	LBY	S	BF	2	3
Load Byte With Increment	LBYI	S	AF	2	3
Store Byte	SBY	S	DF	2	3
Store Byte With Increment	SBYI	S	CF	2	3
BIT OPERATION					
Search First Bit Set	SFBS	R	95	1	3.75a

Notes:

a	Average if more than one alternative exists.
wa	Weighted average where data dependency exists.
**	Privileged instruction - illegal if PS≠0.
***	VIO execution time dependent on number and type of transfer.

Figure 20b: MIL-STD-1750B Instruction Summary

5.4 I/O COMMAND SUMMARY

Operation	Mnem	Code	Ext[1]
Implemented in CPU 1750A or B mode			
Set Interrupt Mask	SMK	2000	No
Clear Interrupt Request	CLIR	2001	No
Enable Interrupts	ENBL	2002	No
Disable Interrupts	DSBL	2003	No
Reset Pending Interrupt	RPI	2004	No
Set Pending Interrupt Reg.	SPI	2005	No
Write Output Discrete Reg.	OD	2008	Yes
Reset Normal Power Up Line	RNS	200A	No
Write Status Word	WSW	200E	Yes
Enable Start-Up ROM[3]	ESUR	4004	No
Disable Start-Up ROM[3]	DSUR	4005	No
Direct Memory Access Enable[3]	DMAE	4006	No
Direct Memory Access Disable[3]	DMAD	4007	No
Timer A Start	TAS	4008	No
Timer A Halt	TAH	4009	No
Output Timer A	OTA	400A	No
Reset Trigger-Go	GO	400B	No
Timer B Start	TBS	400C	No
Timer B Halt	TBH	400D	No
Output Timer B	OTB	400E	No
Read Interrupt Mask	RMK	A000	No
Read Pending Interrupt Reg.	RPIR	A004	No
Read Output Discrete Reg.	RDOR	A008	Yes
Read Status Word	RSW	A00E	No
Read and Clear Fault Reg.	RCFR	A00F	No
Input Timer A	ITA	C00A	No
Input Timer B	ITB	C00E	No
Read Memory Fault Status	RMFS	A00D	No

GPS Defined XIOs			
Set Fault Register	SFR	0401	No
Load OAS register	LOS	0406	No
Output Trigger-Go Reset Reg.	OTGR	040E	No
Write Page Bank Select	WPBS	200C	No
Read Fault Register (No clear)	RFR	8401	No
Read Linkage Pointer	RLP	8404	No
Read Processor Status	RPS	8405	No
Read OAS register	ROS	8406	No
Read Memory Fail Address	RMFA	8407	No
Read Memory Fail Page	RMFP	8408	No
Read Internal Config. Word	ICW	840C	No
Run Built In Test	BIT	840D	No
Input Trigger-Go Reset Reg.	ITGR	840E	No
Read External Configuration	RCW	8410	Yes

Implemented in CPU, 1750B mode only.			
Output Timer A Reset Reg.	OTAR	4002	No
Output Timer B Reset Reg.	OTBR	400F	No
Input Timer A Reset Register[2]	ITAR	C002	No
Input Timer B Reset Register[2]	ITBR	C00F	No
Set Fault Mask	SFMK	2006	No
Write Page Bank Select	WPBS	200F	No
Read Page Bank Select	RPBS	A00C	No
Read Fault Mask	RFMK	A006	No

Implemented in BPU			
Memory Protect Enable[3]	MPEN	4003	Yes
Load Memory Protect RAM[3]	LMP	50XX	Yes
Read Memory Protect RAM[3]	RMP	D0XX	Yes
Load Ext Mem. Protect RAM[3,5]	LXMP	4XXX	Yes
Read Ext. Mem. Protect RAM[3,5]	RXMP	CXXX	Yes

Implemented in MMU			
Write Instruction Page Reg.[3]	WIPR	51XY	Yes
Write Operand Page Reg.[3]	WOPR	52XY	Yes
Read Instruction Page Reg.[3]	RIPR	D1XY	Yes
Read Operand Page Reg.[3]	ROPR	D2XY	Yes

Implemented in Console[6]			
Console Data Output[4]	CO	4000	Yes
Console Command[4]	CC	8402	Yes
Console Data Input[4]	CI	C000	Yes

Reserved by GPS (Unavailable to the user)			
Initialise Interrupt Logic	PINIT	0403	No
Set NPU	RNPU	040A	No
Write Internal config word	WCW	040C	No
Write Memory Config. Reg.	WMCR	0400	Yes
FMCR	FMCR	A010	No

Spare and Reserved Addresses		
Output	**Input**	
04XX-1FXX	84XX-9FXX	Spare
21XX-2fXX	A1XX-AFXX	Reserved
30XX-3FXX	B0XX-BFXX	Spare
41XX-4FXX	C1XX-CFXX	Reserved
53XX-7FXX	D3XX-FFXX	Spare

[1] External cycles output on the address bus
[2] GPS defined 1750B XIO's **Reserved Addresses**
[3] Command illegal if device not implemented in config word
[4] External cycle needing external ready generation
[5] Only implemented in 1750B
[6] The address 4001 and C001 are implemented but have no effect in the 31750.

Figure 20c: Internal I/O Command Summary

6. TIMING DIAGRAMS

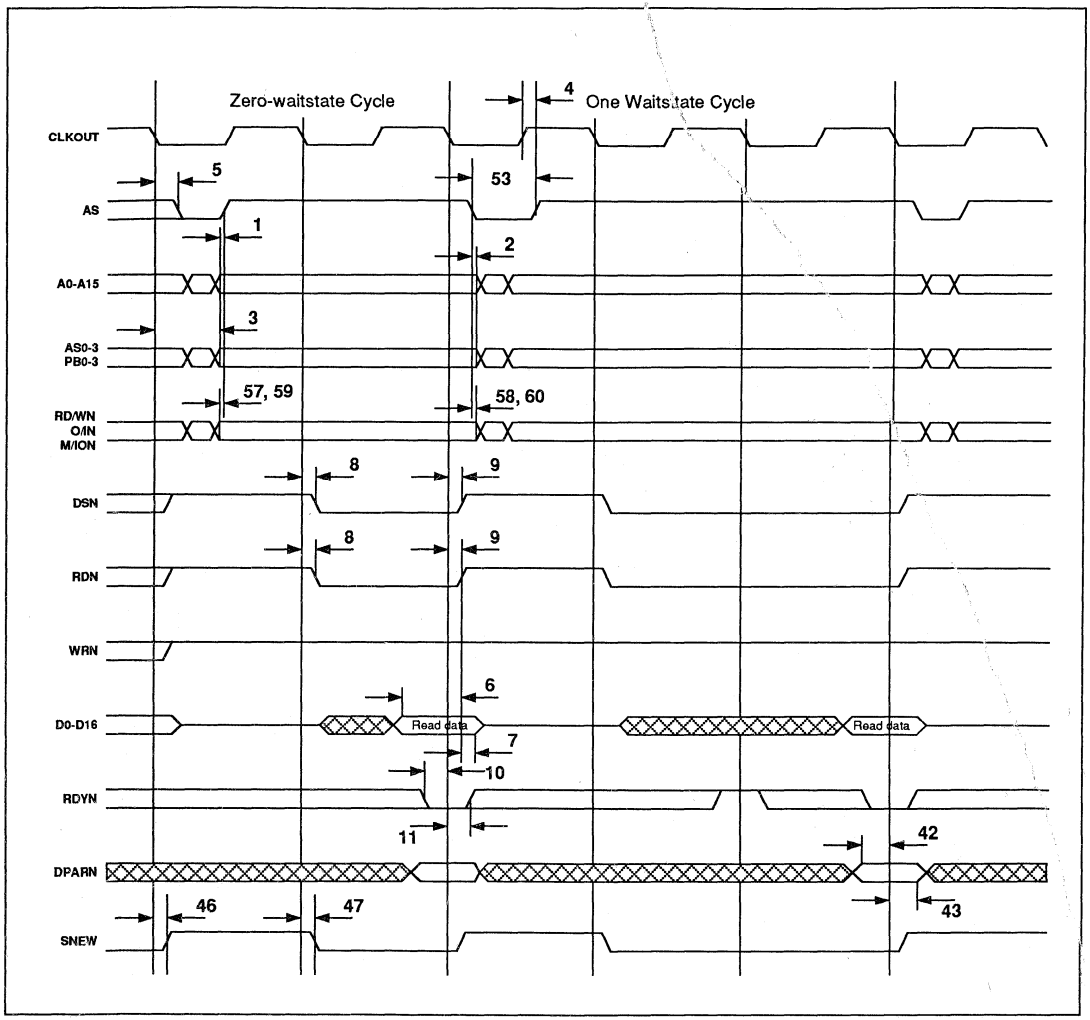
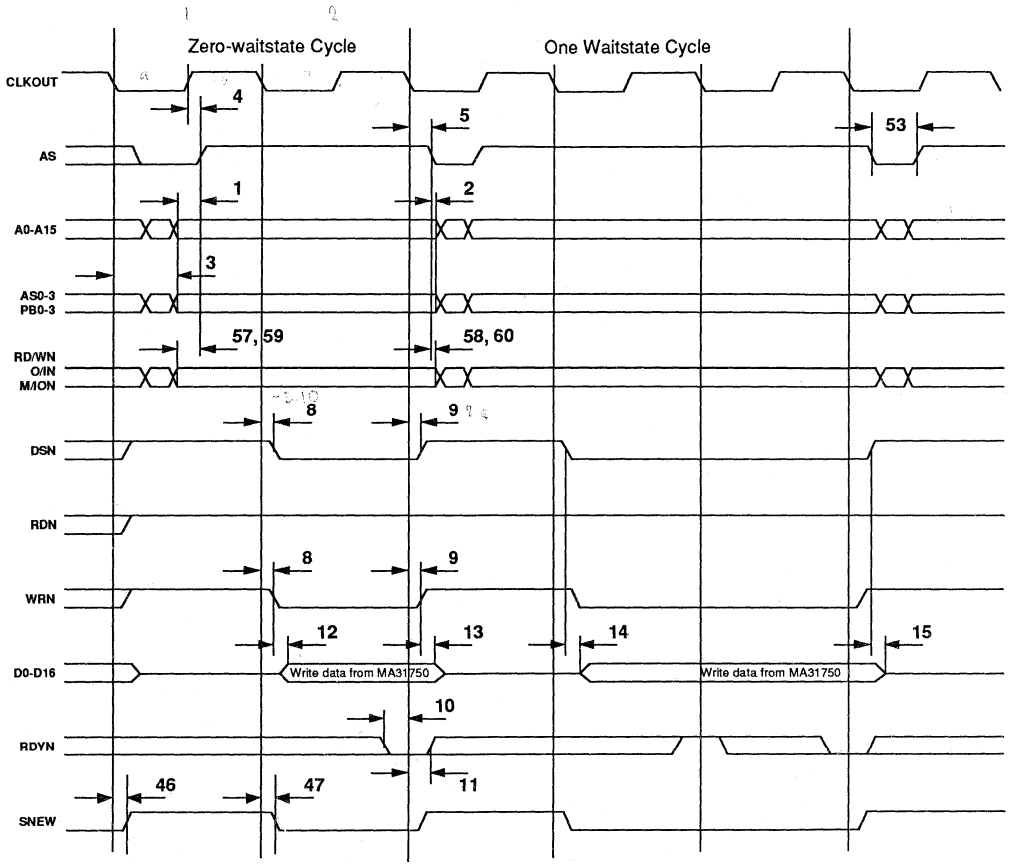
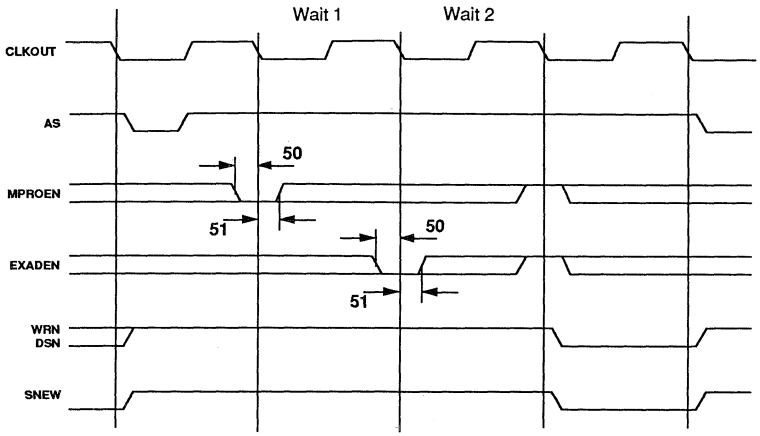


Figure 21: Read Cycle Timings



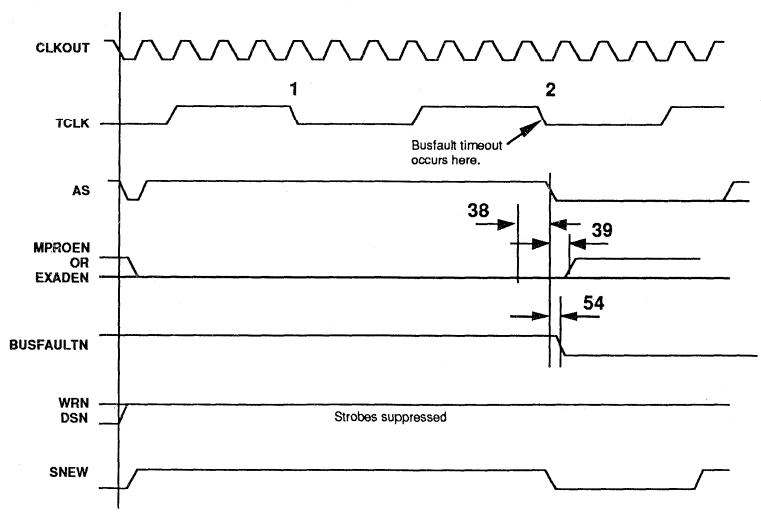
Note: Write data is guaranteed valid after DSN and WRN rise (timing 13)

Figure 22: Write Cycle Timings



Notes:
Diagram shows a WRITE cycle but is also applicable to READ cycles.
Cycle 'Wait 1' is introduced by MPROEN low.
Cycle 'Wait 2' is introduced by EXADEN low.
Strobes RDN/WRN and DSN are not asserted until faults are clear.
If either MPROEN or EXADEN remains low for two successive falling edges of TCLK, the relevant fault is logged in the fault register.

Figure 23a: MPROEN and EXADEN Timings



Notes:
Bus fault timeout occurs after two consecutive TCLK falling edges.
Strobes are suppressed for the duration of the erroneous cycle.
Normal operation resumes with the following cycle.

Figure 23b: Bus Fault Timeout

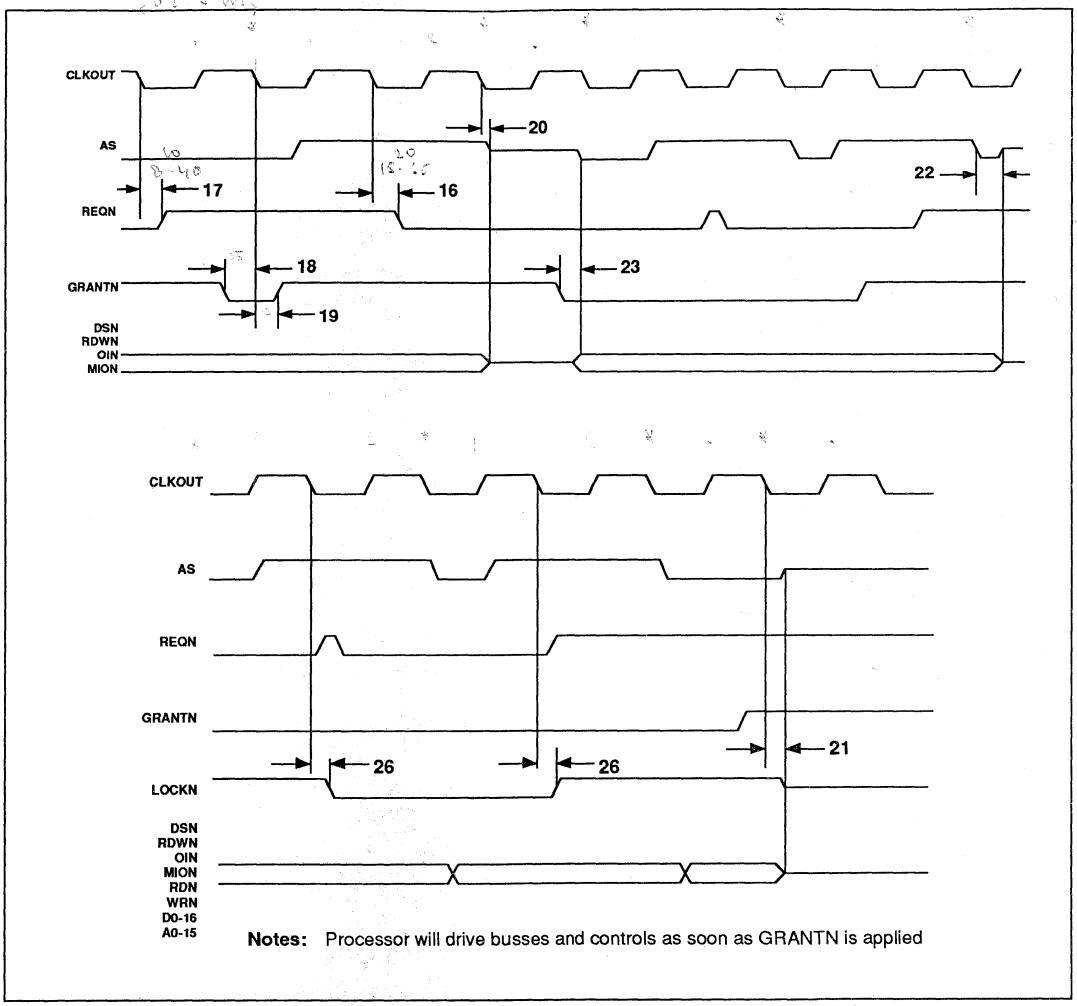


Figure 24: Bus Arbitration Timing

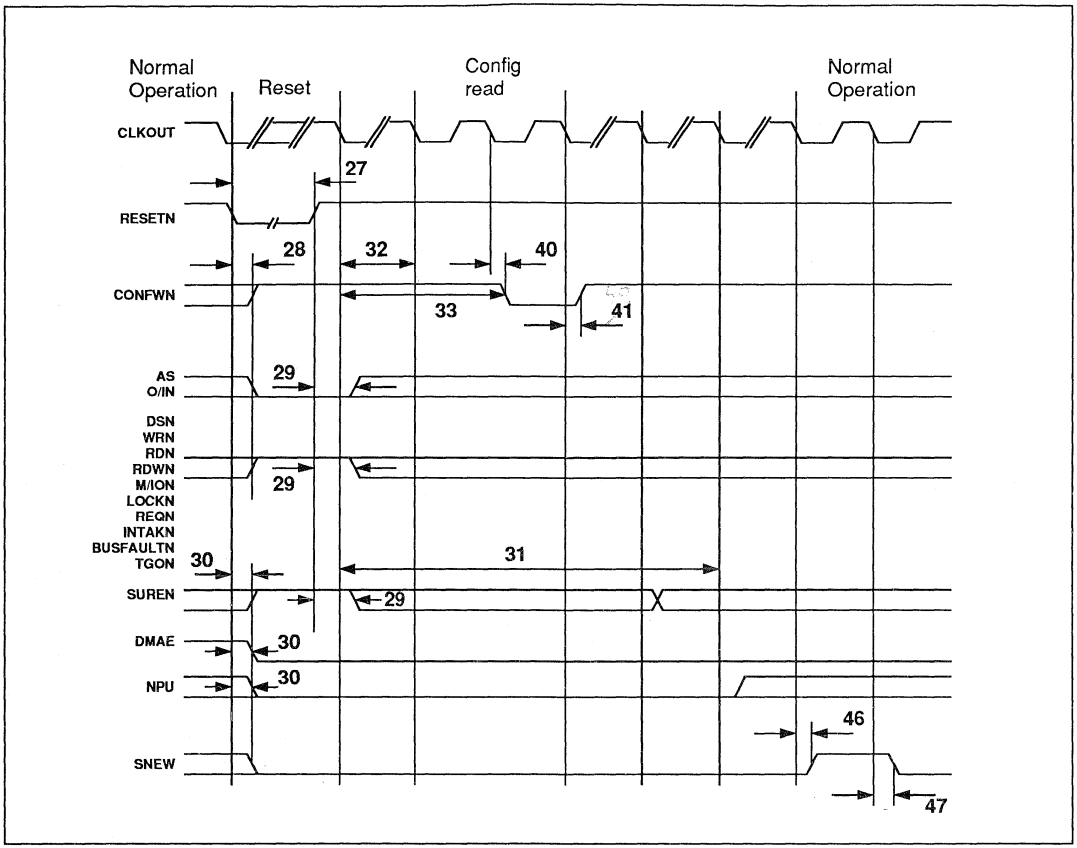


Figure 25: Reset Timing

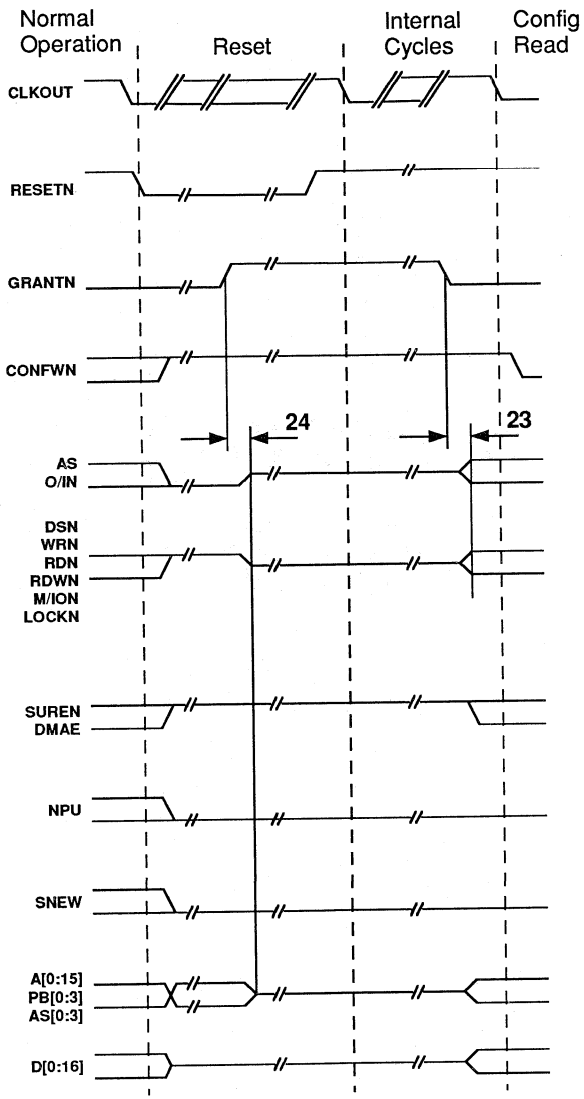
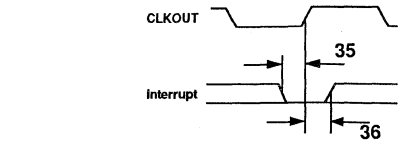
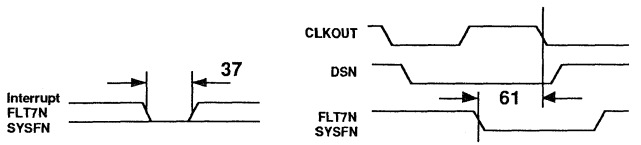


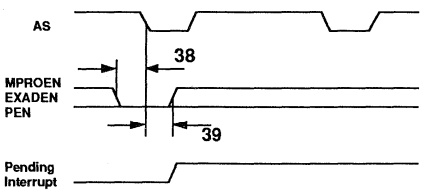
Figure 26: GRANTN during RESETN Low



Level-sensitive Interrupts



Edge-sensitive Interrupts and Asynchronously Captured Faults



Level-sensitive Faults

Notes: A fault causes an internal Pending Interrupt request shortly after the fault has been latched into the fault register (on AS ↓)

Figure 27: External Interrupt and Fault Timing

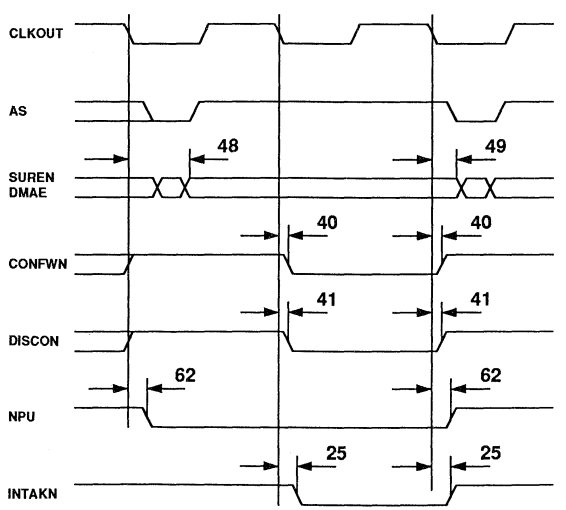


Figure 28: Discrete Timings

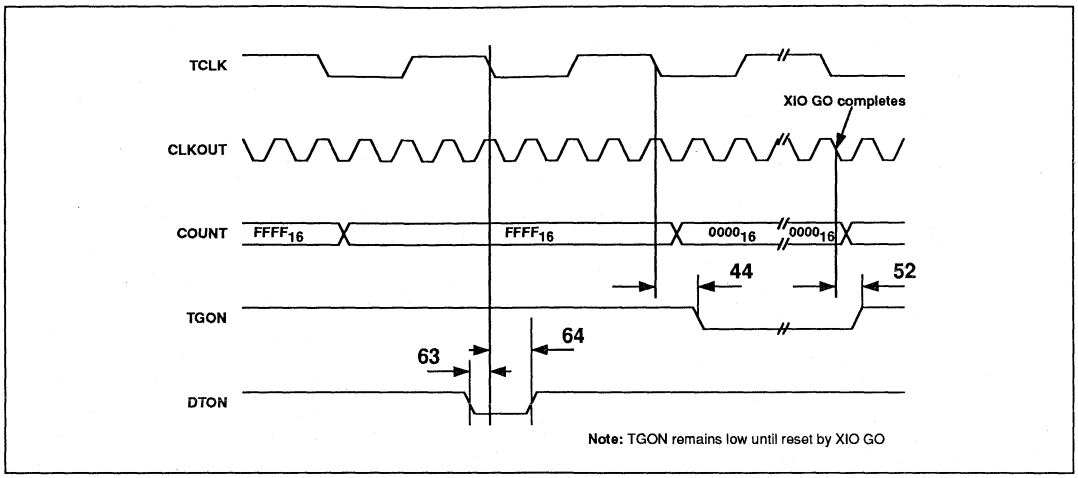


Figure 29: Trigger Go Timing

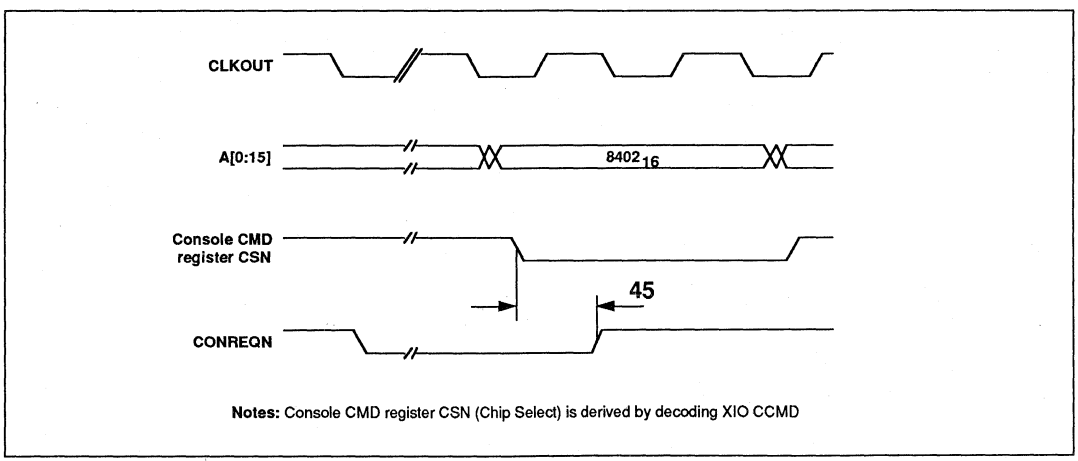


Figure 30: Console Request Timings

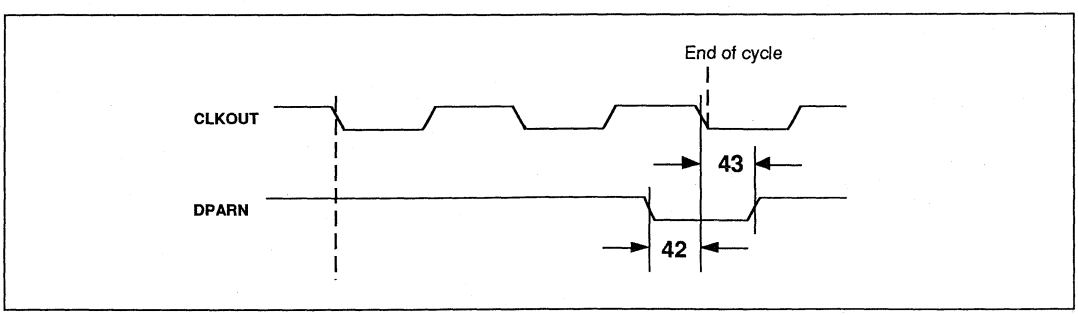


Figure 31: DPARN Timing

No.	Parameter	Min.	Max.	Units
1	ADDRESS valid to AS rising	TL-25	-	ns
2	ADDRESS valid after AS falling	5	25	ns
3	CLKOUT low to ADDRESS valid	-	40	ns
4	CLKOUT rising to AS rising	-	20	ns
5	CLKOUT falling to AS falling	-	15	ns
6	Data setup to RDN rising	15	-	ns
7	Data hold after RDN rising	0	-	ns
8	CLKOUT falling to DSN, RDN, WRN falling	-5	10	ns
9	CLKOUT falling to DSN, RDN, WRN rising	-5	10	ns
10	RDYN setup to CLKOUT falling	25	-	ns
11	RDYN hold after CLKOUT falling	0	-	ns
12	WRN falling to write data valid	5	35	ns
13	Write data valid after WRN rising (Test Load 2)	5	40	ns
14	DSN falling to data bus driven (write) (Test Load 2)	5	35	ns
15	DSN rising to data bus hi-Z (write) (Test Load 2)	-	40	ns
16	CLKOUT falling to REQN falling	15	55	ns
17	CLKOUT falling to REQN rising	8	40	ns
18	GRANTN setup to CLKOUT falling	15	-	ns
19	GRANTN hold after CLKOUT falling	0	-	ns
20	CLKOUT falling to control, strobes and busses hi-Z (GRANTN removed) (Test Load 2)	2	25	ns
21	CLKOUT falling to control, strobes and busses hi-Z (GRANTN removed) (Test Load 2)	10	50	ns
22	AS falling to control, strobes and busses hi-Z (GRANTN removed) (Test Load 2)	4	40	ns
23	GRANTN falling to control, strobes and busses driven	4	25	ns
24	GRANTN rising to control, strobes and busses undriven (RESETN = LOW)	10	50	ns
25	CLKOUT falling to INTAKN changing	4	30	ns
26	CLKOUT falling to LOCKN valid	4	35	ns
27	RESETN low pulse width	10	-	ns
28	RESETN low to strobes inactive (GRANTN = LOW)	10	55	ns
29	RESETN high to strobes valid (GRANTN = LOW)	4	30	ns
30	RESETN falling to DMAE, NPU low, SUREN high	-	50	ns
31	RESETN rising to DMAE, SUREN, NPU initialized	28	13960†	CLK
32	RESETN rising to first bus cycle (configuration word read)	6	6	CLK
33	RESETN rising to CONFWN low	7	7	CLK
34	RESETN rising to first instruction fetch	T31+16	T31+16	CLK
35	Interrupt setup to CLKOUT rising (level sensitive)	15	-	ns
36	Interrupt hold after CLKOUT rising (level sensitive)	20	-	ns
37	Interrupt pulse width (edge-sensitive)	10	-	ns
38	MPROEN/EXADEN/PEN setup to AS falling (MPROEN and EXADEN sampled on early time-out)	5	-	ns
39	MPROEN/EXADEN/PEN hold after AS falling (MPROEN and EXADEN sampled on early time-out)	15	-	ns
40	CLKOUT falling to CONFWN changing	2	25	ns
41	CLKOUT falling to DISCON changing	8	45	ns
42	DPARN setup to CLKOUT falling	10	-	ns
43	DPARN hold after CLKOUT falling	5	-	ns
44	TCLK falling to TGON low	5	45	ns
45	CONREQN hold after Console Command Chip Selection	-	3	CLK
46	CLKOUT falling to SNEW rising	4	30	ns
47	CLKOUT falling to SNEW falling	4	30	ns
48	CLKOUT falling to SUREN/DMAE valid	4	30	ns
49	CLKOUT falling to SUREN/DMAE invalid	4	30	ns
50	MPROEN/EXADEN setup to CLKOUT falling (to insert early wait states)	40	-	ns
51	MPROEN/EXADEN hold after CLKOUT falling (to insert early wait states)	0	-	ns
52	CLKOUT falling to TGON rising (following XIO GO)	20	80	ns
53	AS low pulse width	0.5T-5	0.5T+10	ns
54	AS falling to BUSFAULTN valid	-	45	ns
55	CLK rising to CLKOUT rising	5	25	ns
56	CLK falling to CLKOUT falling	5	25	ns
57	MION valid to AS rising	TL-20	-	ns
58	MION valid after AS falling	1	25	ns
59	OIN/RDWN valid to AS rising	TL-20	-	ns
60	OIN/RDWN valid after AS falling	1	25	ns
61	SYSFN/FLT7N setup to CLKOUT (at end of cycle)	10	-	ns
62	CLKOUT falling to NPU changing	-	30	ns
63	DTON setup to TCLK falling	10	-	ns
64	DTON hold after TCLK falling	10	-	ns

† This timing includes MA31751 Setup Cycles and Built In Test Cycles.
Mil-Std-883, Method 5005, Subgroups 9, 10, 11.
TL = Low CLK period (ns), TH = High CLK period (ns).
Test Conditions: Vdd = 5.0V ±10%, Temperature = -55°C to 125°C, Vil = 0.0V, Vih = Vdd.
Output loads: All test load 1 unless otherwise specified.
Output Threshold: 50% Vdd (Load 1), Vss+1V, Vdd-1V (Load 2).

Figure 32a: Timing Parameters for MA31750

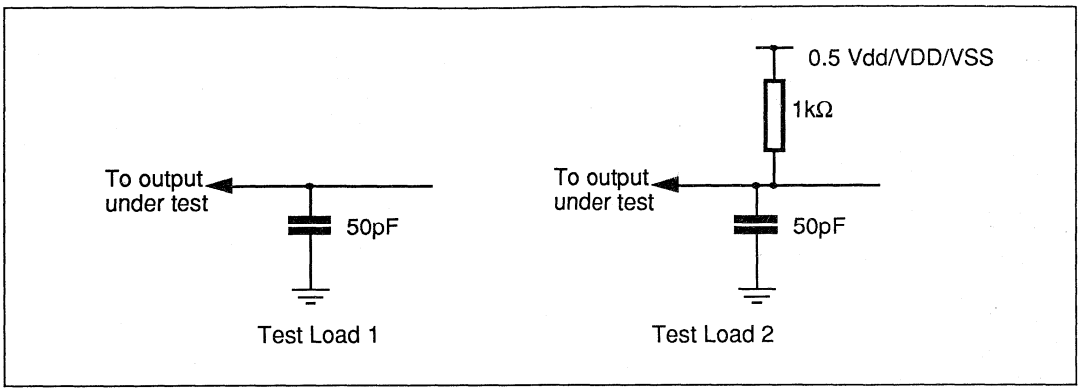


Figure 32b : Output Loads for AC measurements

8. TYPICAL SMALL SYSTEM CONFIGURATION

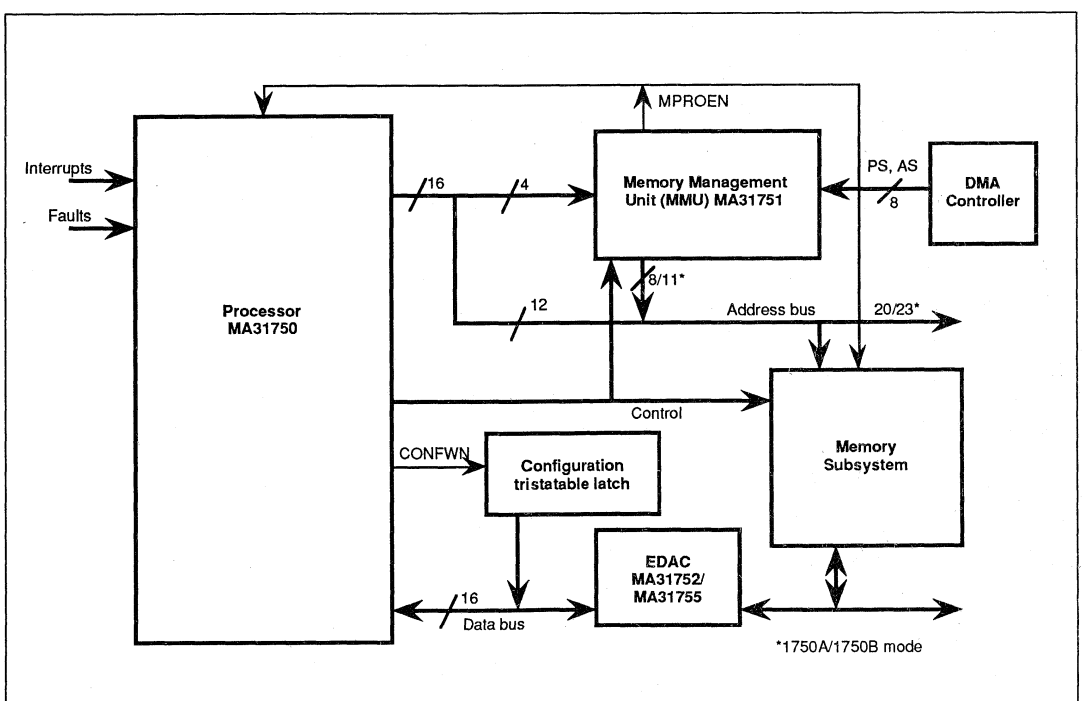


Figure 33: Typical Small System Configuration

A Single Board Computer is available to developers. Please call GPS for details.

9. RATING AND CHARACTERISTICS

Parameter	Min.	Max.	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	VDD+0.3	V
Current through any I/O pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Figure 34: Absolute Maximum Ratings

Parameter	Min.	Max	Units
Clock Frequency (CLK)	0	16	MHz
TCLK Frequency	0	f_{CLK} / 9 †	Hz
Recommended Clock duty cycle	45	55	%

† MIL-STD-1750 mandates that TCLK be 100kHz
Vdd=5V±10% over full operating temperature range
Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Figure 35: Operating AC Electrical Characteristics

			Total dose radiation not exceeding $3x10^5$ Rad(Si)			
Symbol	Parameters	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	80% V_{DD}	-	-	V
V_{IL}	Input low voltage	-	-	-	20% V_{DD}	V
V_{CKH}	CLK & TCLK input high voltage	-	V_{DD}-0.5	-	-	V
V_{CKL}	CLK & TCLK input low voltage	-	-	-	V_{SS}+0.5	V
V_{OH}	Output high voltage	I_{OH}=-3mA	V_{DD}-0.5	-	-	V
V_{OL}	Output low voltage	I_{OL}=5mA	-	-	V_{SS}+0.4	V
I_{IH}	Input high current (Note 1)	-	-	-	10	µA
I_{IL}	Input low current (Note 1)	-	-	-	-10	µA
I_{OZH}	I/O tristate high current (Note 1)	-	-	-	50	µA
I_{OZL}	I/O tristate low current (Note 1)	-	-	-	-50	µA
I_{DDYN}	Dynamic supply current @ 16MHz	-	-	-	80	mA
I_{DDS}	Static supply current	-	-	-	10	mA

Vdd=5V±10% over full operating temperature range
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not tested at low temperature (-55°C)

Figure 36: Operating DC Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Table 36 at +25°C
2	Static characteristics specified in Table 36 at +125°C
3	Static characteristics specified in Table 36 at -55°C
7	Functional characteristics specified in Table 35 at +25°C
8A	Functional characteristics specified in Table 35 at +125°C
8B	Functional characteristics specified in Table 35 at -55°C
9	Switching characteristics specified in Table 32a at +25°C
10	Switching characteristics specified in Table 32a at +125°C
11	Switching characteristics specified in Table 32a at -55°C

Figure 37: Definition of MIL-STD-883, Method 5005 Subgroups

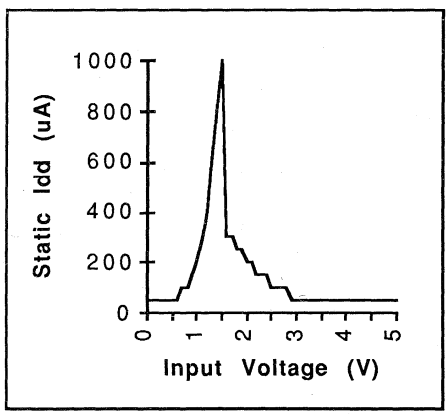


Figure 38: Input Characteristic

10. PIN DESCRIPTIONS

A description of each pin function appears in Figure 39. The acronym is presented first, followed by its function and description. Timing characteristics of each of the functions are shown in section 6.

All signals - with the exception of CLK and TCLK are CMOS compatible, and are protected by an Electrostatic Discharge (ESD) protection circuit. All output signals are also TTL compatible. CLK and TCLK are Schmitt inputs.

Throughout this data sheet, active low signals are denoted by following the signal name with an "N" suffix, e.g.,DSN. If a signal has a dual function, both function names will be used separated by a "/". The function name to the left of the "/" will be active high while the function to the right will be active low, again with an "N" suffix, e.g., RD/WN.

All unused inputs should be connected to their inactive state and should not be allowed to float.

Pin Name	Function	Description
POWER		
VDD	Power Supply	DC power supply input - nominally +5V.
GND	Ground	0V reference point.
CLOCK SIGNALS		
CLK	System Clock	Schmitt Input clock signal. For correct operation of the timers the CLK frequency should be at least 9 times that of TCLK.
CLKOUT	Clock Out	Buffered reference clock derived directly from the internal clock. This signal is used to reference all of the external strobes and internal timing events and may be used to synchronise an external system to the processor.
TCLK	Timer Clock *100kHz sq. wave*	This Schmitt input clock is used by the internal 16-bit timers A and B and by the Trigger-Go-counter. MIL-STD-1750 requires this signal to have a frequency of 100kHz.
SYSTEM BUSES		
A00-A15	Address bus *A00 is MSB*	An active-high address bus which is input during bus cycles not assigned to this CPU. A00 is the most significant bit.
D00-D16	Data bus *D00 is MSB*	An active-high data bus which is tristate during bus cycles not assigned to this CPU. D00 is the most significant bit. D16 is the optional parity check bit.
BUS CONTROL		
AS	Address Strobe *Active HIGH*	This active-high bidirectional signal establishes the beginning and end of each bus cycle. The trailing edge (high to low transition) is used to sample bus cycle-related faults into the fault register. The leading edge guarantees that a valid address is on the address bus. During cycles not assigned to this CPU the AS line is an input to allow the falling edge to continue to latch bus cycle related faults into the fault register.
DSN	Data Strobe *Active LOW*	This active-low signal indicates the presence of data on the system data bus. During a read cycle DSN goes low to indicate that the processor is requesting data from the bus, whilst in a write cycle DSN indicates that data is present on the bus. This signal is tristate in bus cycles not assigned to this CPU.
M/ION	Memory/IO Select *Memory=HIGH* *IO=LOW*	This signal indicates whether the current bus cycle is accessing memory (high) or IO (low) addressing space. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. M/ION becomes an input on cycles not assigned to the CPU to ensure that faults are latched into the correct bit of the fault register.
RD/WN	Read/Write Select. *Read=HIGH* *Write=LOW*	This signal indicates the direction of data transfer on the system data bus. Data is read in by the processor when high, and written out when low. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. RD/WN is tristate during cycles not assigned to this CPU.
O/IN	Operand/Instruct Select. *Operand=HIGH* *Instr.=LOW*	This signal indicates whether the current bus cycle is accessing operand (high) or instruction (low) addressing space. This signal becomes valid shortly after the start of a machine cycle and remains valid throughout. O/IN is an input during cycles not assigned to this CPU, to ensure correct operation of the MFPR and the MFAR.
RDN	Read Strobe. *Active LOW*	This active-low output is asserted low with DSN during read cycles. It is driven high on the same clock edge as that used by the processor to latch the input data. This signal is tristate in bus cycles not assigned to this CPU.
WRN	Write Strobe. *Active LOW*	This active-low output signal is asserted low with DSN during write cycles. The rising edge should be used by the system to latch data from the data bus. This signal is tristate in bus cycles not assigned to this CPU.
RDYN	Ready. *Active LOW*	This input signal allows the basic machine cycle of the processor to be extended to accommodate slower peripheral or memory devices. Ready may be asserted high to add an integer number of CLK cycles (wait states) to the machine cycle. The line must be asserted low to allow processing to proceed. RDYN has no effect on cycles dedicated to internal operations. **Note:** If RDYN is held high during two consecutive TCLK high-to-low transitions (with DSN low), a bus timeout fault will occur and will be indicated in the appropriate bit in the fault register. The occurrence of this fault will cause the state sequencer to terminate the current machine cycle and begin the next. At the end of the current macro-instruction execution will branch, unless masked, to the machine error interrupt (level 1) software routine. The DTON signal may be used to override this feature.

Figure 39: Pin Descriptions

Pin Name	Function	Description
BUS ARBITRATION		
LOCKN	Bus Lock Request. *Active LOW*	This active-low output signal indicates to the bus arbiter that the processor is performing an atomic instruction which should not be interrupted. External bus accesses should be denied whilst LOCKN is low. The CPU will lock the bus during read-modify-write instructions such as DECM (Decrement Memory) and TSB (Test & Set Bit). LOCKN remains high during non-locked cycles. This signal is tri-stated on cycles not assigned to this CPU. **Note:** LOCKN is advisory only - it may be ignored by the arbiter if neccessary.
REQN	Bus Request. *Active LOW*	This active-low output signal is driven low when the CPU requires the bus in the next cycle. This signal may be used as an input to an external bus arbiter. The signal becomes invalid once the CPU has started the requested cycle.
GRANTN	Bus Grant. *Active LOW*	This active-low signal is asserted by an external bus arbiter to indicate that the CPU currently has the highest priority bus request. The CPU will begin a bus cycle (if one is pending) commencing with the next CPU clock cycle.
INTERRUPTS		
PWRDN	Power-Down Interrupt. *Active LOW*	A low on this active low input will be captured in the PI register and sets Pending Interrupt 0. This is the highest priority interrupt and cannot be masked or disabled.
INT02N, INT08N, INT10N, INT11N, INT13N, INT15N	Interrupt Inputs. *Active LOW*	A low on any of these active low inputs will be captured in the PI register and will set Pending Interrupt levels 2, 8, 10, 11, 13, and 15, respectively. Level 2 is the highest priority user level, while level 15 is the lowest priority. These interrupts are maskable and can be disabled. If edge sensitivity has been selected, interrupts will be captured on the falling edge of the interrupt input, otherwise the interrupt will be latched by the falling edge of CLK at the end of the machine cycle. **Note:** Interrupt levels 1, 3, 4, 5, 6, 7 and 9 are dedicated to internal machine interrupts.
IOI1N, IOI2N		A low on either input will set Pending Interrupt levels 12 or 14 respectively. These inputs are level sensitive only and are captured by the falling edge of CLK at the end of a machine cycle. These inputs can be masked and disabled.
INTAKN	Interrupt Acknowledge Strobe. *Active LOW*	This active-low output indicates the start of an interrupt service. When low, the processor outputs the Linkage Pointer (LP) address to the system. The INTAKN signal may be used to remove level-sensitive interrupt inputs: the current interrupt priority can be ascertained by reading the address bus during the cycle in which this output is low.
FAULTS		
MPROEN	Memory Protect Fault. *Active LOW*	A low on this input, sampled on falling AS, indicates that an execute protect or write protect fault has been detected. Bit 0 of the fault register is set if this signal is applied during a CPU cycle; bit 1 is set if the line goes low during a DMA cycle. Either condition sets Pending Interrupt level 1. The CPU will prevent access to memory (by inhibiting strobe production) whilst this input is LOW. See 3.4.7.1. To effectively use this feature, MPROEN should be pulled low prior to the start of the next machine cycle.
PEN	Parity Error *Active LOW*	A low on this active-low input, sampled on falling AS, informs the CPU that an external parity error has occurred. Bit 2 (memory), 3 (IO) or 4 (DMA) of the Fault Register is set, depending upon the type of transfer taking place. This asserts a level 1 Pending Interrupt.
EXADEN	External Address Error *Active LOW*	A low on this active-low input, sampled on falling AS, informs the CPU that an external address error has occurred. Bit 8 of the fault register is set if this signal goes low during a memory cycle; bit 5 is set if the signal goes low during an IO cycle and bit 14 is set if a DMA has control of the system. Either error condition asserts a level 1 pending interrupt. As with MPROEN, the CPU will prevent access to memory (by inhibiting strobe production) whilst this input is LOW. See 3.4.8.1
FLT7N	Fault Level 7 *Active LOW*	A low at any time on this active-low input sets bit 7 of the fault register, causing a level 1 pending interrupt. This fault is user-definable.
SYSFN	System Fault *Active LOW*	A low at any time on this active-low input sets bits 13 and 15 of the fault register, causing a level 1 pending interrupt. This fault is user definable.
BUSFAULTN	Illegal address *Active LOW*	This active-low output drops low if any bus-related fault (MPROEN, EXADEN or PEN) is detected low or if the bus fault timeout circuit causes an interface timeout.

Figure 39 (continued): Pin Descriptions

Pin Name	Function	Description
MMU CONTROL		
AS[0:3]	Address State Active HIGH *AS0 is MSB*	This active-high bus indicates the current address state of the CPU. The value on this bus is copied from the Status Word register within the CPU. These lines are inputs during bus cycles not assigned to this CPU, so that the MFPR and the MFAR can store the relevant failure information if a remote failure occurs.
PB[0:3]	Page Bank Select Active HIGH *PB0 is MSB*	In 1750B mode, this active-high bus indicates the current CPU Page Bank. The value on this bus is copied from the Status Word register within the CPU. These lines are inputs during bus cycles not assigned to this CPU, so that the MFPR and the MFAR can store the relevant failure information if a remote failure occurs.
DISCRETES		
CONFWN	Configuration Register Read Strobe *Active LOW*	This active-low output signal is driven low when the processor reads the external configuration register. The line may be used as an output enable for this register. The configuration register is read during initialisation and during the execution of a BPT instruction to determine the system configuration.
SNEW	Start of New Cycle Strobe *Active HIGH*	This active-high output will be asserted high during the first phase of each machine cycle.
DISCON	Discretes Output Strobe *Active LOW*	This active-low output will be asserted low by the processor during an XIO OD or XIO RDOR command. It may be used as the enable signal for an external discrete output register.
DMAE	DMA Enable *Active HIGH*	This active-high output indicates that an external DMA device is enabled. It is disabled (low) following reset and can be toggled under program control using XIO DMAE and XIO DMAD, (if a DMA device is set as present in the configuration register).
CONREQN	Console Request *Active LOW*	This active-low input initiates and controls Console operation following the end of a 1750 instruction. Commands and data are passed to the processor in this mode via three dedicated registers in IO space. Console operation takes precedence over Interrupts.
SUREN	Start-Up-ROM Enable *Active LOW*	This active-low output indicates that start-up ROM is enabled. The signal is asserted low following initialisation or by XIO ESUR. The signal remains asserted until removed with XIO DSUR. When a start-up ROM is present on the system indicated in the configuration word, this signal should be used to qualify its chip select or output enable such that the ROM may be accessed only when SUREN is low. **Note:** Instruction pipelining must be considered in moving from Start-Up ROM to RAM. See Section 4 on Software Considerations.
NPU	Normal Power-Up Discrete *Active HIGH*	This output is asserted to indicate that the Built-In-Test (BIT), performed on reset or power-up, has passed. The line is asserted low following an external reset and may also be reset by software using the XIO RNS command.
TGON	Trigger-Go Output Discrete *Active LOW*	This active-low output is asserted low whenever the Trigger-Go counter overflows (rolls over to 0000). It returns to the high state when the counter is reset by software (using the XIO GO command).
DTON	Disable Timeout *Active LOW*	A low on this input will reset and disable the bus fault timeout circuit.
DPARN	Disable Parity *Active LOW*	A low on this input will reset and disable the on-chip parity verification. **Note:** Parity *generation* on write data is not disabled by this pin.
RESETN	CPU reset *Reset=LOW*	This active-low input should be asserted low to reset the processor. The low to high transition will start the initialisation sequence which will perform a Built-In-Test (if selected), initialising the processor in accordance with MIL-STD-1750 (see figures 2 and 3).

Figure 39 (continued): Pin Descriptions

11. PIN ASSIGNMENTS AND OUTLINES

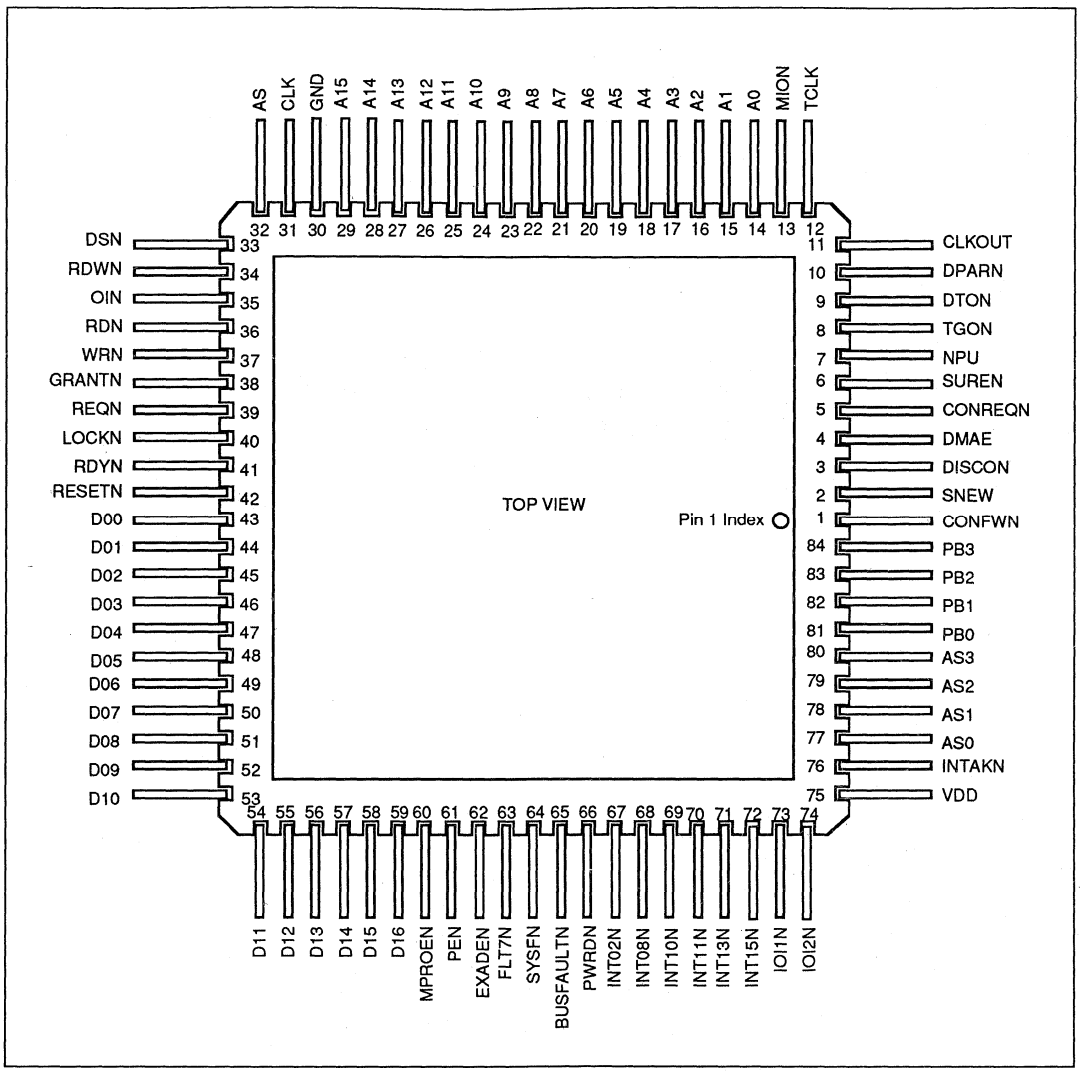
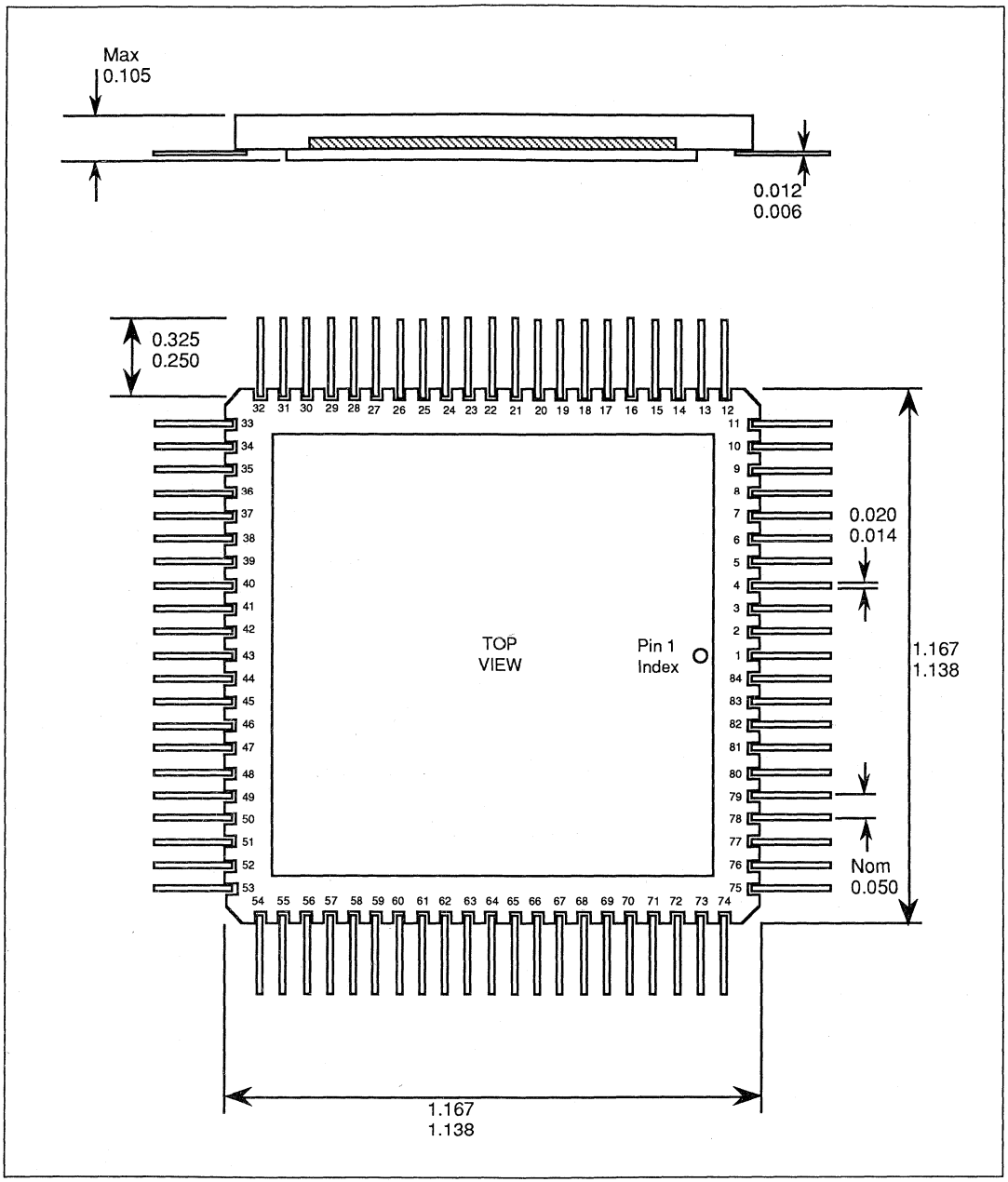
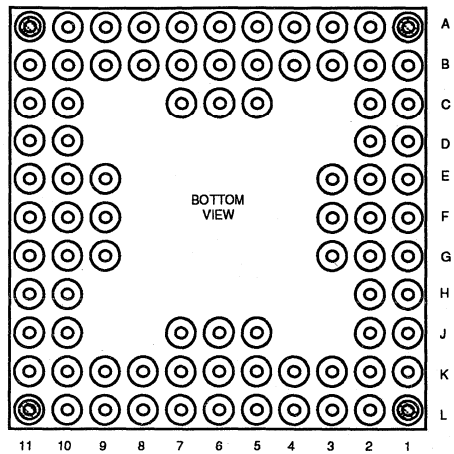


Figure 40a: 84-Lead Flatpack - Package Style F



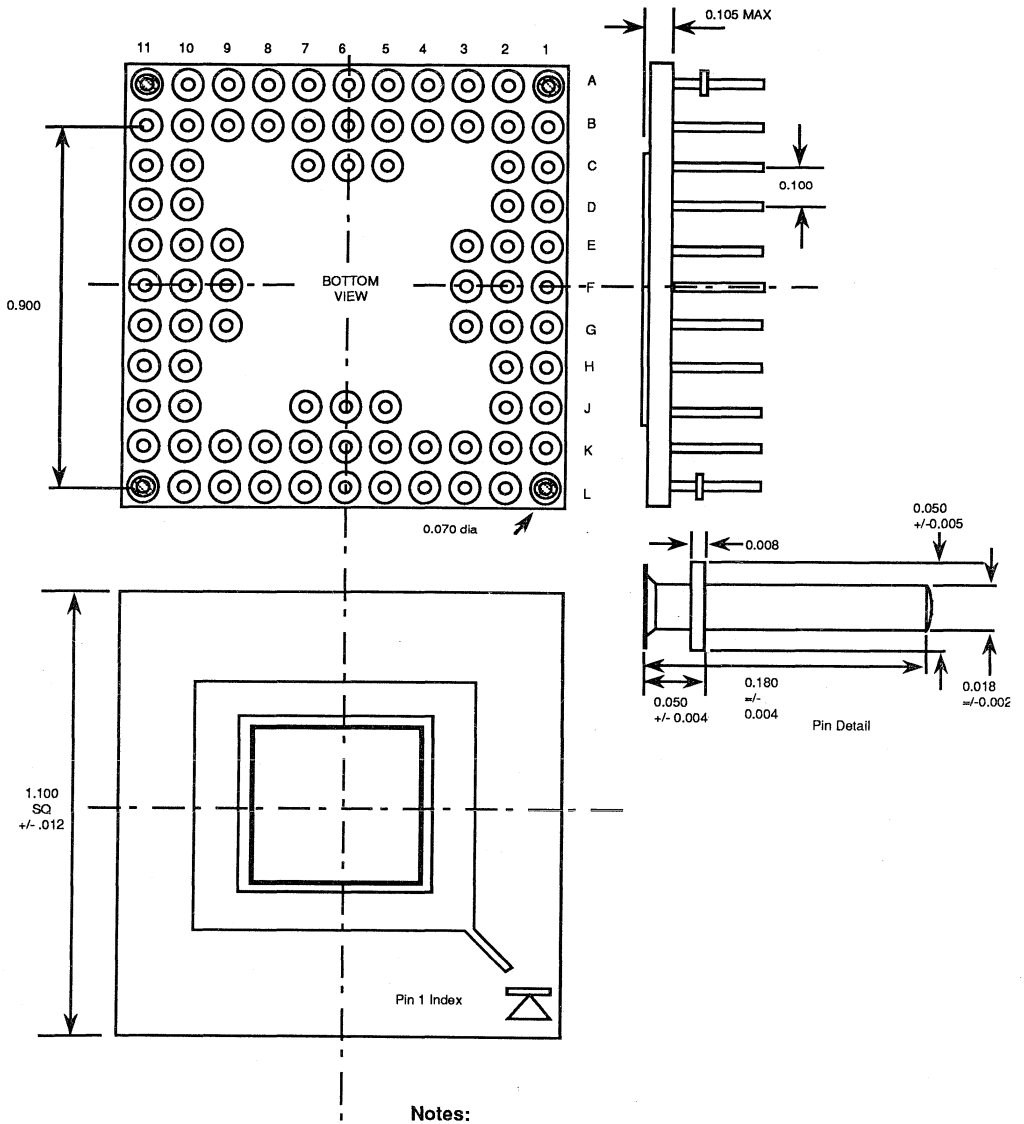
NOTE: All dimensions shown in inches

Figure 40b: 84-Lead Flatpack - Package Style F



A1	IOI2N	B11	D08	F9	D00	K2	TCLK
A2	INT15N	C1	AS1	F10	RESETN	K3	MION
A3	INT13N	C2	INTAKN	F11	D04	K4	A02
A4	INT10N	C5	BUSFAULTN	G1	DISCON	K5	A05
A5	PWRDN	C6	SYSFN	G2	DMAE	K6	A04
A6	INT08N	C7	MPROEN	G3	CONREQN	K7	A11
A7	EXADEN	C10	D09	G9	REQN	K8	A14
A8	D16	C11	D07	G10	LOCKN	K9	CLK
A9	D14	D1	AS3	G11	RDYN	K10	DSN
A10	D13	D2	AS2	H1	SUREN	K11	OIN
A11	D10	D10	D06	H2	NPU	L1	CLKOUT
B1	AS0	D11	D05	H10	WRN	L2	A00
B2	VDD	E1	PB2	H11	GRANTN	L3	A01
B3	IOI1N	E2	PB1	J1	TGON	L4	A03
B4	INT11N	E3	PB3	J2	DPARN	L5	A06
B5	INT02N	E9	D01	J5	A07	L6	A09
B6	FLT7N	E10	D03	J6	A08	L7	A10
B7	PEN	E11	D02	J7	A12	L8	A13
B8	D15	F1	SNEW	J10	RDWN	L9	A15
B9	D12	F2	PB0	J11	RDN	L10	GND
B10	D11	F3	CONFWN	K1	DTON	L11	AS

Figure 41a: 84-Pin Grid Array - Package Style A



Notes:

1. ▨ represents gold plating 50 microns min. over 100 microns nominal nickel.
2. All dimensions are in inches.
3. Default tolerances ±1% not less than 0.005
4. Ceramic is 92% Alumina.

Figure 41b: 84-Pin Grid Array - Package Style A

12. RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to total dose radiation levels, each wafer lot will be approved when all sample devices pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL STD 883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$1x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request
** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

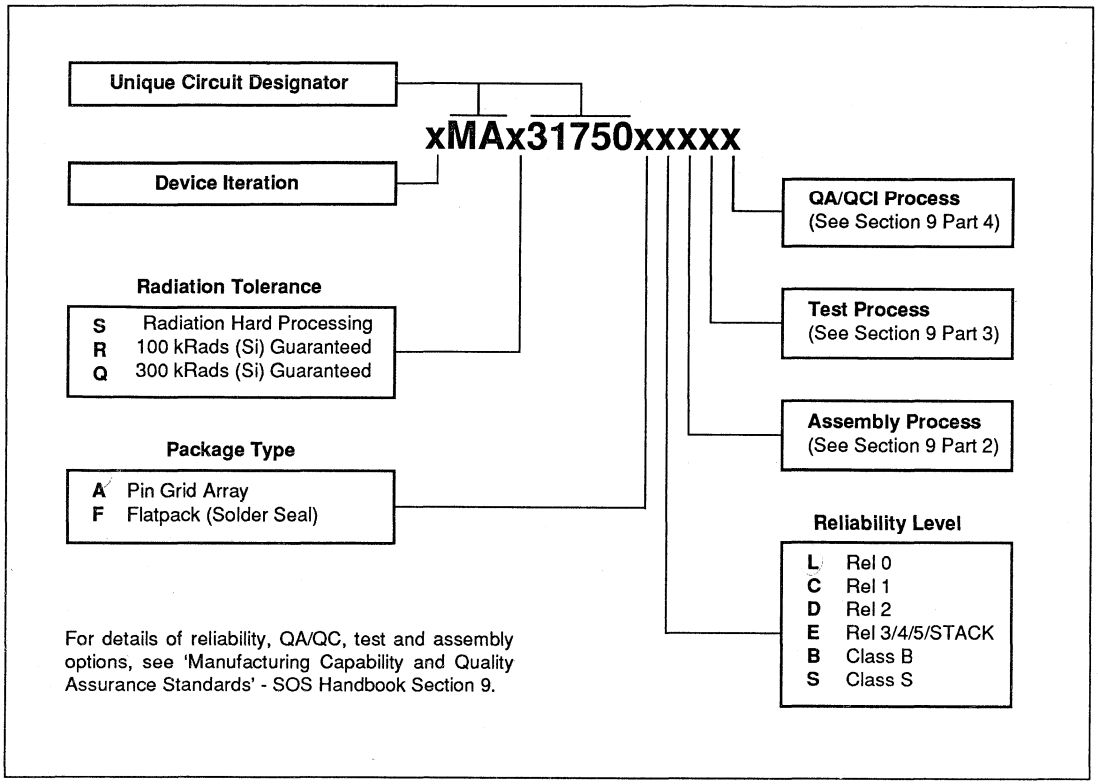
Figure 42: Radiation Hardness Parameters

13. RELATED DOCUMENTATION

A number of Applications Notes are available to support the information in this data sheets. Please call for details:

Application Note	Describes
No. 2	1750B Mode
No. 3	Use of Console Mode
No. 4	Use of Interrupts
No. 8	Use of VIO Instructions
No. 11	Bus Arbitration
No. 14	Use of NMA31750 Samples
No. 15	Pipelining Instructions

14. ORDERING INFORMATION



MA31750 - Application Note 2

MIL-STD-1750B FEATURES

The following Applications note describes the implementation of MIL-STD-1750B in the MA31750:

On the MA31750, a single chip pin is used to select between 1750A and 1750B modes of operation. In 1750A mode the processor conforms fully to the MIL-STD-1750A (Notice 1). In 1750B mode the MA31750 conforms to Option 2 of the Draft standard MIL-STD-1750B dated 17-Jul-1989.

MIL-STD-1750B FEATURES (Illegal in 1750A Mode)

In 1750B mode the following features are enabled in addition to those of MIL-STD-1750A:

- Extended addressing to 8MWords each of instruction and operand space (with MMU)
- Up to 16 Page register Banks (with MMU)
- 'Long' load and store instructions allowing direct access to data anywhere in the physical memory space
- Unsigned add, subtract and compare instructions
- 'Search first bit set' (SFBS) instruction
- Load and store byte instructions
- Reset registers for the two software timers, A & B
- Fault mask register
- Modified overflow detection in floating-point multiply and divide (see below)

1750B UNSIGNED SUBTRACT

The MA31750 operates primarily on signed quantities. This leads to a potential problem when generating flags for unsigned operations in 1750B. The operation of the carry flag is undefined in 1750B when executing an unsigned subtract (US or USR) operation. The operation will be to produce the same carry flag as would the equivalent signed operation.

OVERFLOW HANDLING

There are differences between 1750A and B in the way in which overflows are handled. These differences only occur in multiplication and division of floating point and extended floating point numbers. Furthermore, the difference only affects operations when one of the operands is at the extreme end of the number range.

In MIL-STD-1750A, a multiplication overflows if the sum of the exponents of the multiplicand and multiplier exceeds the 8-bit number range. Similarly, a division overflows if the difference between the divisor and dividend exponents exceeds the 8-bit range.

In MIL-STD-1750B, an overflow on multiplication or divide only occurs if the exponent of the result is outside the exponent (8-bit) number range.

An example of this difference in operation is set out below. Here we are performing the multiplication of a large positive number by one:

Decimal: $(\frac{1}{2} \times 2^{127}) \times (\frac{1}{2} \times 2^{1})$
Hex: (4000 007F) x (4000 0001)

The 1750A solution adds the two exponents to yield an overflow in 8 bits. This forces the entire operation to be treated as an overflow:

7F + 01 = 80 (Overflow in 8-bits)

In 1750B, the remainder of the calculation is performed, and the result is normalised:

$0.5 \times 0.5 = 0.25$
$= 0.5 \times 2^{-1} (2^{FF})$

The normalising factor is added to the overflowed exponent sum to bring the value back into range and yield no overflow:

7F + 01 + FF = 7F (no overflow)

ADOPTION OF MIL-STD-1750B

It now appears unlikely that the draft MIL-STD-1750B will be issued as a MIL standard and for this reason there can be no formal verification of the 1750B mode of operation. However, it is anticipated that some users will use the 1750B mode in order to take advantage of the extended addressing capability provided in this mode.

MA31750 - Application Note 3

USE OF CONSOLE MODE

The following information applies to the N- iteration of the MA31750.

Console Mode is an optional feature of MIL-STD-1750 processors in general and is mentioned in MIL-STD-1750. The mode is provided within the MA31750 to allow the system designer to control, monitor and modify internal operation of the processor without having to substantially rewrite system software. This Applications Note describes this mode in detail, giving information on the commands available and the external hardware required to support the Console. This Note updates and corrects the previous issues for the relevant iterations.

OVERVIEW

The processor can operate in one of a number of different modes. One of these is Console mode where the normal MIL-STD-1750 operation is suspended and a special debugging interface is presented instead.

Console mode may be entered by either hardware or software means. When in Console mode the processor receives its instructions from a fixed IO-mapped location. Operands and results (as appropriate) associated with these instructions are passed between system and processor via two other fixed locations in the IO map. Any number of Console commands may be performed before issuing a special command which returns control back to the interrupted 1750 program.

Note that the two interval timers, Timer A and Timer B, are stopped on entry to Console mode, in accordance with MIL-STD-1750.

ENTERING CONSOLE MODE USING CONREQN

Asserting CONREQN low for 2 machine cycles during normal operation will cause the processor to enter Console mode following the completion of the current instruction (but see note on Console inhibit). Whilst CONREQN is low, the device will loop round three machine cycles, one of which will perform a read of the command register (8402_{16}). The command is not executed whilst CONREQN remains low. CONREQN may stay low for as long as required. The user should load the system Console Command register with the desired command before asserting CONREQN high, at which point the requested command will be executed. The flowchart shows the remainder of the command operation. See Table 1 for command information.

ENTERING CONSOLE MODE WITH BPT

If the processor encounters a BPT instruction the processor will enter Console mode (but see note on Console inhibit) and will immediately process the Console command contained in the Command register. It is important, therefore, that the Command register is loaded before any BPT instructions may be encountered. Operation then continues as for CONREQN-initiated commands (see flowchart).

CONSOLE INHIBIT

When CONREQN is asserted low, the CPU checks its internal copy of the configuration register to see if a console is present. If console is entered via the BPT instruction, the CPU reads the system configuration word, hence giving dynamic control over console entry by BPT. If no console is declared in the configuration, CONREQN is ignored and BPT instructions are treated as NOPs.

CONTROLLING THE PROCESSOR IN CONSOLE MODE

When in Console mode the processor communicates with the system console via a number of locations in IO space, as listed below:

Address	Function
8402_{16}	Console command input
$C000_{16}$	Data input
4000_{16}	Data output
$C001_{16}$	Read Console Status (not used in MA31750)
4001_{16}	Clear Console (not used in MA31750)

The user should provide a method of supplying values when these addresses are polled by the processor. A typical approach is to implement three IO-mapped registers which respond to the above addresses and which may be loaded from an external controller or banks of switches.

The required action is communicated to the processor by placing the appropriate command at IO location 8402_{16} and asserting CONREQN high. If the command takes an operand (such as a value to Write Register) then this should first be placed at location $C000_{16}$. Following completion of the command, any results are returned via location 4000_{16}. Note that during XIO and Next XIO operations, external read XIO commands execute an extra read of the Data input register. This does not affect the operation in any way. Also note that the IO addresses $C001_{16}$ and 4001_{16} are enabled when Console mode is selected, but is not used as part of the Console Mode operation.

Following the execution of the first command, the processor will halt (provided the command is not 'continue') and wait for a further negative edge on CONREQN. The next command to be executed should be set at address 8402_{16} before the rising edge of CONREQN. Any number of commands may be issued in this way, using CONREQN to control execution and to signal the presence of a new command code to the processor.

LEAVING CONSOLE MODE

To release the MA31750 from Console mode, a 'continue' command should be issued. The instruction pipeline will be refilled with the 1750 instruction immediately following the point at which the Console request or BPT was registered; normal instruction execution then resumes from that point.

SINGLE STEP

Single step operation is also accomplished using a 'continue' command. Once Console mode has been entered, raising CONREQN will cause the processor to execute the command and leave Console mode. If the user reasserts CONREQN low after the 2nd internal cycle after the read and before the 2nd pipe-line pre-fetch, then exactly one 1750 instruction will be executed before the processor returns to Console mode. This allows the processor to step through the 1750 code one instruction at a time.

COMMAND SUMMARY

Table 1 shows a summary of all commands available in Console mode, with a description of their function. Commands should be constructed according to Figure 1. It should be noted that although many of the internal registers are made available in Console mode, attempting to change them may produce predictable but unexpected results. In particular, temporary registers T0, T1 and T9-T11 are used by the Console interface to store operands such as the IC register prior to Console Mode entry.

Command	Function	Code
Continue	Resumes normal MIL-STD-1750 operation. This command is also used for single stepping instructions.	0
Read Register	Places the contents of a specified internal register into the Console Output register (IO address 4000). The register to be accessed is specified as a value placed in the lower 12 bits of the Command register according to Table 2.	1
Write Register	Places the contents of the Console Input register (IO location C000) into a specified internal register. The register to be accessed is specified as a value placed in the lower 12 bits of the Command register according to Table 2.	2
Read and Clear Fault Register	Places the contents of the 1750 Fault register into the Console Output register and then clears the Fault Register.	3
Write Status Word	Copies the contents of the Console Input register to the 1750-defined Status Word register. Note that the A reg is changed to 200E.	4
Read memory	The contents of operand memory space at address A (the contents of the Alternate Address register) are placed in the Console Output register.	5
Write memory	The contents of the Console Input register are placed in operand memory space at address A.	6
Read next memory	The contents of the A register is incremented. The contents of operand memory space at address A are then placed in the Console Output register.	7
Write next memory	The contents of the A register is incremented. The contents of the Console Input register are then placed in operand memory space at address A.	8
XIO	The XIO command specified by the content of the A register is performed using data read from the Console Input register. If the XIO command is illegal the command is ignored. No Status Word Processor State checking is performed.	9
Next XIO	As above, but the command in A is incremented before the XIO is attempted.	A
Disable	Console operation is suspended pending a new Console request or an interrupt. If an interrupt occurs then the Instruction Counter will be restored and normal MIL-STD-1750 operation will be resumed with the interrupt service routine.	B
Reserved	Reserved for internal use by GPS - do not use.	C
Other...	Any other command not described above is ignored and has no action. User should reload Command register with correct value as for a new instruction.	X

Table 1: Console Instructions

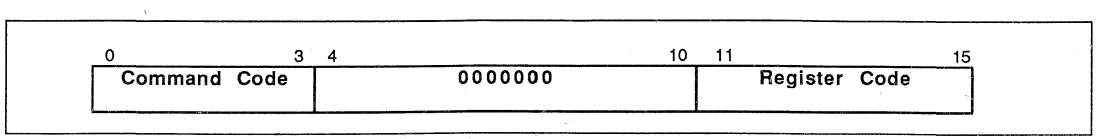


Figure 1: Command Register Format

Register	Register Description	Code (bottom 12 bits)
R0-R15	General purpose register R0-R15	000-00F
T0-T11	Microcode registers T0-T11	010-01B
A	Operand or alternate address register	01C
IC	Instruction Counter (take great care when modifying this value)	01D

Table 2: Register Map

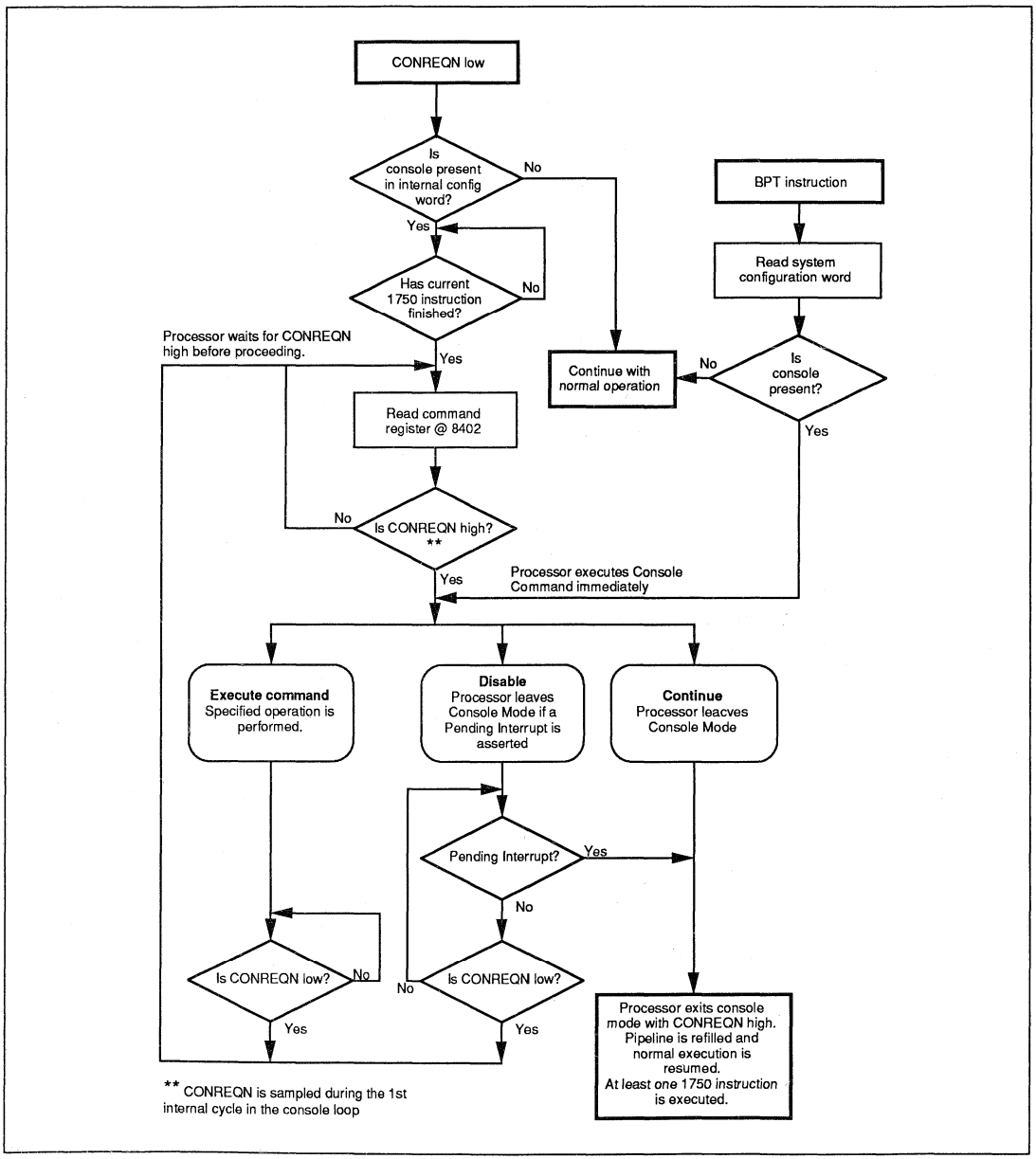


Figure 2: Console Operation Flowchart

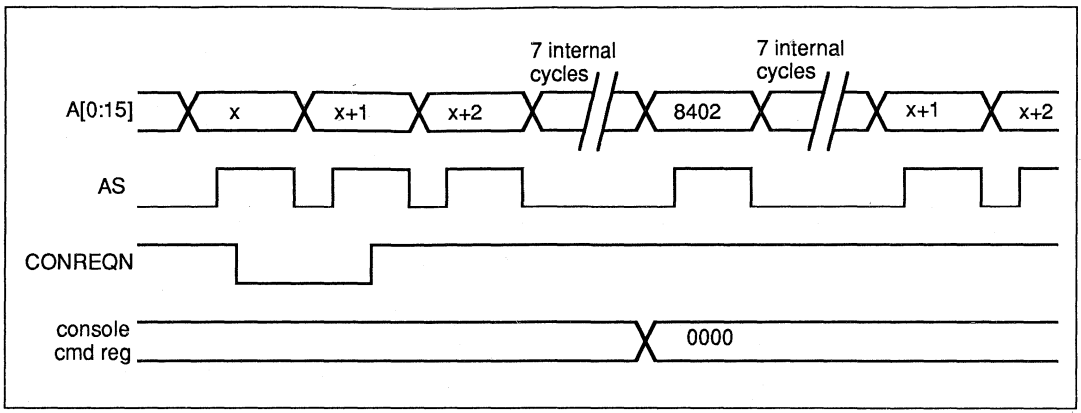


Figure 3: Entering Console Mode

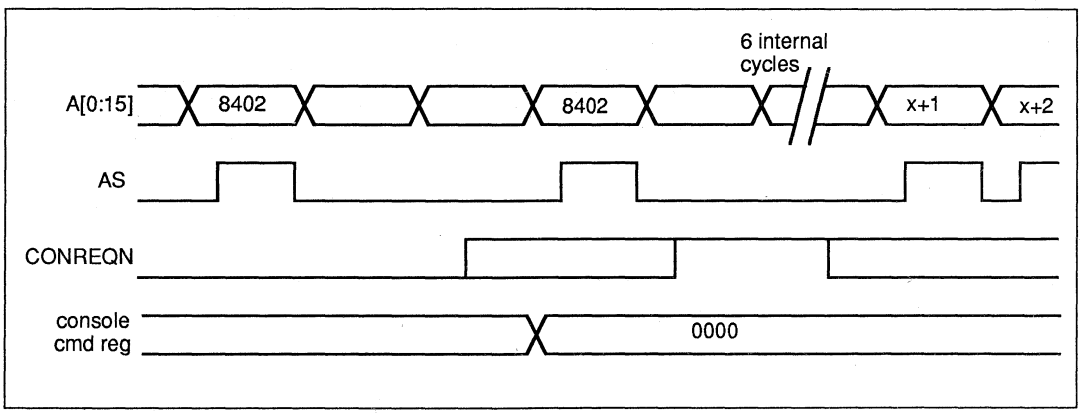


Figure 4: Exiting Console Mode

MA31750 - Application Note 4

INTERRUPT OPERATIONS

This applications note details the interrupt handling operations of the NMA31750.

INTRODUCTION

The MA31750 has 16 interrupts: 9 of these interrupts are available to the system as external interrupts to the processor, The remaining 7 are internally generated by the MA31750. Interrupts can occur at any time and are latched into the Pending Interrupt register (PI). However, they are not serviced until completion of the currently executing MIL-STD1750 instruction.

MIL-STD-1750 makes provision for interrupt software control via I/O commands. These I/O commands are internally implemented by the MA31750. They provide an enable/ disable facility (without preventing the latching of interrupt requests into the PI) and a means of manipulating the interrupt Mask Register (MK), the PI and the Fault Register (FT) contents.

HARDWARE CONSIDERATIONS

The user interrupts, PWRDN and INT02N-INT15N, can be defined as being edge or level sensitive by the State of bit 4 in the configuration word. If edge sensitivity is selected, an interrupt pulse exceeding the minimum width (specified in the data sheet), appearing at any time in the cycle, will latch an interrupt request. Another interrupt request cannot be detected on that interrupt line until the previous one has cleared.

If level sensitivity is selected, an interrupt will be requested whenever the interrupt signal is active as the PI latches (ie. the same interrupt could be latched multiple times). It is the user's responsibility to deactivate any unwanted external interrupts. INTAKN is asserted low whilst the processor reads the interrupt service pointer (part of the microcoded interrupt service routine). This event may be used to identify and release the interrupt currently being serviced. Figure 1 is a representation of the CPU interrupt latching circuitry.

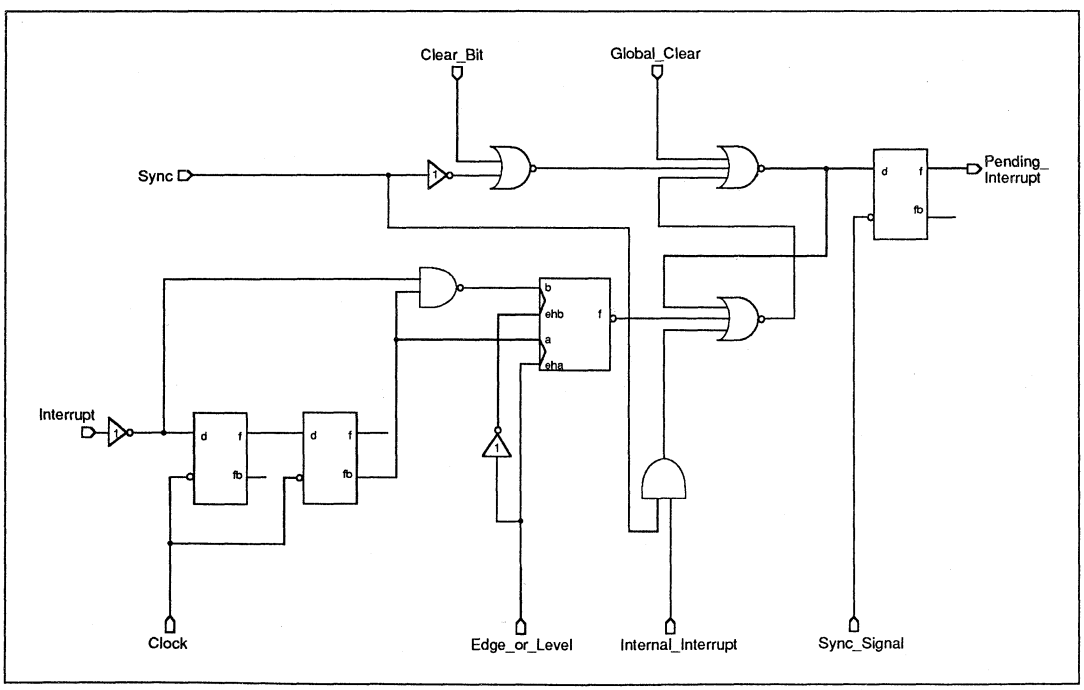


Figure 1: Edge and Level Interrupt Latching Circuit

The internal interrupts are always level sensitive, therefore their latching circuitry does not have the edge detection option. This removes the need for the multiplexer. The cross-coupled NOR gates are also surplus as the asynchronous edge detection has been removed.

As part of the service routine, microcode clears the bit in the PI register asociated with the current interrupt. There are 7 internal interrupts. Interrupt 1, the machine error interrupt signal, differs from the others as it cannot be disabled. It becomes active whenever any of the bits in the Fault Register (FT) are set. There is anti-repeat logic between the FT output and the PI as FT is not cleared when the interrupt is serviced (and re-latching has to be prevented). The FT must be cleared by the user, in the interrupt service routine (by reading and clearing FT) before another machine error can be detected. See Figure 2.

INTERRUPT PROCESSING

Detecting any active interrupt or fault causes a 4 CLK machine cycle to occur on the next machine cycle, (2 early wait states are added). This allows the processor enough time to enter the service routine directly after the currently executing 1750 instruction, even if the interrupt/fault was set as that instruction was completing.

Once an interrupt signal has been set internally, it is ANDed together with the appropriate bit in the Mask Register (MK). If the interrupt has not been masked (only 1-15 can be masked) then the interrupt signal is input to the Priority Encoder. This prioritises the unmasked and enabled interrupts, giving highest priority to the lowest interrupt numbers ie. interrupt 0 is the highest possible priority. The priority encoder outputs a 4-bit interrupt vector and signals to the microcode sequencer that there is an interrupt awaiting processing (service begins when the present 1750 instruction has completed). The vector is read during the interrupt service routine and is used to derive the Linkage Pointer and Service Pointer addresses for the interrupt being processed. Reading the vector also clears the appropriate bit of the Pending Interrupt Register.

INTERRUPT VECTORING

When an interrupt request signal has been received and the processor starts the Microcode Interrupt Service Routine (MISR), the old status of the device has to be stored so that processing can be resumed once the interrupt has been serviced. This old status is stored in a fixed memory location (there is a unique location for each interrupt). The address of this memory location is known as the Linkage Pointer (LP). It references the old mask register (MK), the old status word (SW) and the old instruction counter (IC).

Before execution of the User Interrupt Service Routine (UISR), the context relating to this routine is loaded. The processor loads new values for MK, SW and IC from a three word memory block whose address is held at the Service Pointer (SP) location for that interrupt.

The addresses of the LP and SP for each interrupt are derived from the interrupt vector generated by the priority encoder.

PROCESSING INTERRUPT 5 - BEX

The BEX interrupt is one means of changing the address or processor state of the CPU via software. This allows protected calls to be made to routines in other address states. BEX is called with a number in the range 0-15. This number maps the Instruction Counter onto one of 16 possible new addresses, taken from the memory area pointed to by the SP. Figure 6 shows how the vectoring works for any interrupt.

Note: Most interrupt routines can be called in either of two ways. The interrupt request signal can be activated or the relevant bit in the Pending Interrupt register can be set. However, in 1750B mode, setting bit 5 of the PI (corresponding with BEX) will not generate an interrupt request. In 1750A mode, setting bit 5 in the PI causes BEX 0 to be called.

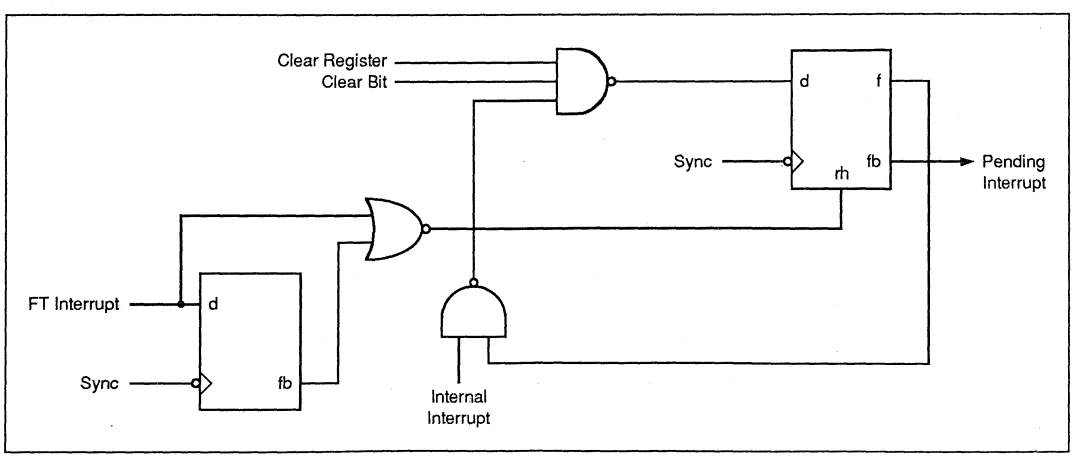


Figure 2: Interrupt 1 Latching Circuitry

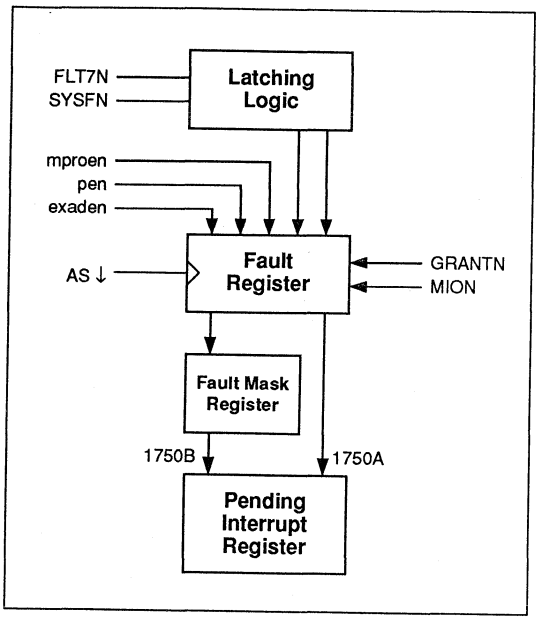


Figure 3: Machine Error Interrupt Capture

MACHINE ERROR FAULTS

Figure 3 shows the latching logic for machine errors. The Fault Register is loaded on the falling edge of the address strobe, AS. This provides synchronicity with the peripherals in the system as they may have control at the time of interrupt generation. The output from the fault register is asynchronously fed into the pending interrupt register (via the fault mask if in 1750B mode). Bit 1 of the PI is set asynchronously as can be seen in Figure 2. This is to ensure that faults are serviced directly after the erroneous instruction. (If the OAS register remains unchanged after initialisation, then abort is enabled. MPROEN and EXADEN will cause the erroneous instruction to be aborted before entering the ME service routine. PEN will cause the next instruction to be aborted if it is an external cycle. The ME is then serviced).

ENDING THE INTERRUPT SERVICE ROUTINE

The software interrupt handling routine is typically ended by using the LST (Load Status) 1750 instruction with the appropriate LP value in (or pointed to by) the address field. LST restores the processor to the state prior to interrupt servicing.

LST is a priviledged instruction, therefore the Processor State (PS) must be set to zero in order for LST to execute. If PS does not equal zero, then the instuction is aborted and the priviledged instruction fault (FT10) is set. This causes a machine error interrupt. If this interrupt is disabled, processing will continue with the 1750 instruction following the aborted LST.

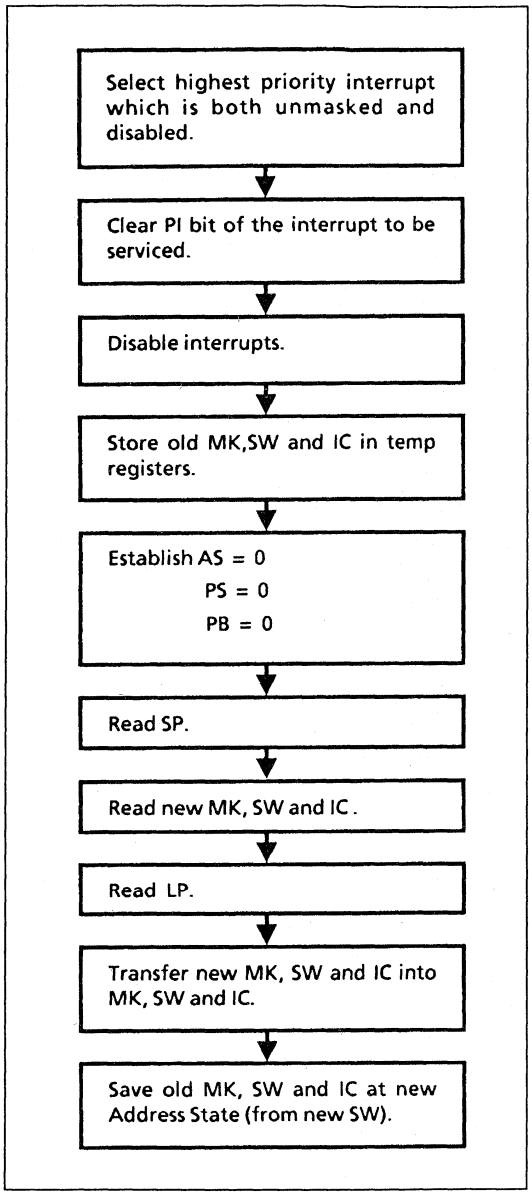


Figure 4: General Description of the Microcode Interrupt Handling Routine

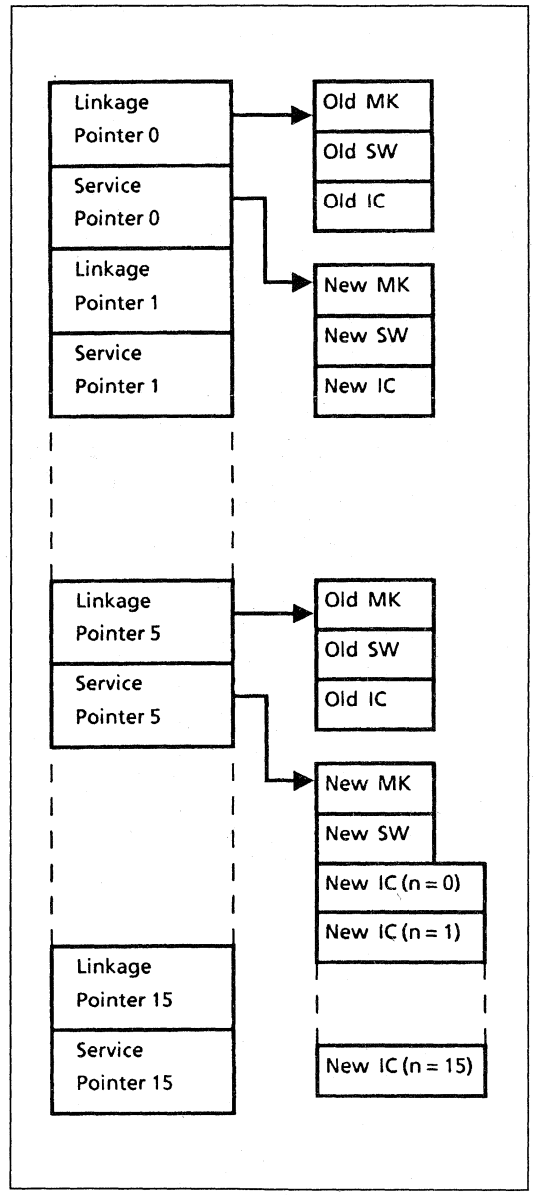


Figure 5: Interrupt Vectoring

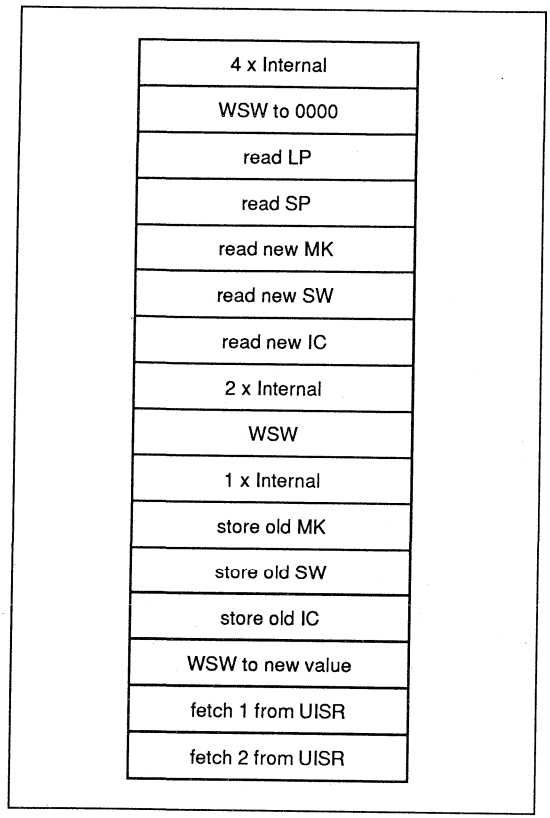


Figure 6: Machine Cycle Description of Interrupt Initialisation

MA31750 - Application Note 8

USE OF VIO INSTRUCTION

This Applications Note is intended as a guide to assist the user to program using the vectored interrupt command. This 1750 instruction executes a table of XIO commands and is described fully below.

A vectored input/output (VIO) is a 1750 instruction which performs the IO operations defined in a vector table in memory.

A VIO is written as 1750 assembly code in the form:

VIO RA, ADDR, RX

RA is the increment applied to the XIO command address between each transfer, and ADDR + RX form the start address of the vector table. (ADDR is the base address and register RX is the optional index register.)

The first entry in the vector table is the command word, the second is the mask word. Data follows after these. See Fig 1.

The IO operation (device address) is defined as:

[ADDR + RX] + ([RA] * n)
= ((command word) + (increment factor * n))

where n = the bit number of the bit set in the mask word and [ ] means that the contents of that memory location should be used.

The mask word, in address [ADDR + RX + 1], determines which instructions in the table are executed. If the mask bit is set high, then the transfer takes place. If the mask bit is set to zero, no XIO command is generated. n always increments as the next bit in the mask word is considered. i does not increment if no transfer occurs.

The device address, if unmasked, is then interpreted by the microprocessor as an XIO command and treated accordingly. The only difference is that, instead of using data from RA, the command gets its data from ([ADDR + RX] + 2 + i) where i starts at zero and is incremented after each transfer ie. each data word in turn is accessed.

VIO is a privileged instruction. If the privilege status (PS)!=0 when the VIO starts, no commands are executed and a fault is caused. If the PS changes during the execution of a chain of commands, it is ignored until the next privileged instruction is called.

If an illegal XIO command is encountered whilst the table is being executed, the following actions will occur.

1. The illegal IO bit is set in the fault register (bit 5)
2. The VIO chain is terminated, and the illegal XIO command is treated as a NOP. This termination does not affect the execution of the preceding XIO commands in the VIO chain.

The mask word, in address [ADDR + RX + 1], determines which instructions in the table are executed. If the mask bit is set high, then the transfer takes place. If the mask bit is set to zero, no XIO command is generated. n always increments as the next bit in the mask word is considered. i does not increment if no transfer takes place.

The example below shows a typical piece of 1750 assembly code for executing VIO instructions.

(A table has been loaded at address 2000 with a command word of 6000, a mask word of C001 and 3 data words to correspond to the 3 bits set in the mask word. See Fig 2.)

```
LIM  R0, 2          (R0 will be used as RA)
VIO  R0, 2000
```

Bit 0 is considered: The first mask bit (bit 0) is set to 1 therefore data is to be transferred. The number of the bit, n, equals 0. This is multiplied by the contents of RA → 0 * 2. This is then added to the command word to give 6000. The XIO command to be executed is therefore 6000. As a general convention, any XIO command which has it's MSB set to 0 is a read from memory and write to IO. Therefore, the data is to be transferred from memory address 2002 (base address of table + 2 to allow for the command and mask words) to IO address 6000. The transfer takes place, then n and i are incremented.

Next, bit 1 is considered: The second mask bit is set to 1 therefore data will be transferred from memory address 2003 (base address + 2 + i) to IO address 6002. ((1*2) + 6000). After the completion of the transfer, n and i are incremented.

The third bit is masked out, as are the rest of the bits, until case 15 is reached. i has remained set to 2 as only 2 transfers have occured. n has incremented to 15. Data transfer will take place from memory address 2004 ([ADDR + RX] + 2 + i) to IO address 601E ((n*2) + 6000).

As it can be seen, the VIO command is useful for accessing IO addresses which do not have to be consecutive (as long as they are regularly spaced). However, the instruction is slow to execute as each time round the loop takes 4 machine cycles for no transfer and 9 (write) or 10 (read) machine cycles when an external transfer occurs. If speed of transfers is required, the IO devices can be located in consecutive memory space. Then the MOVE command can be used to transfer data from one area of memory to another.

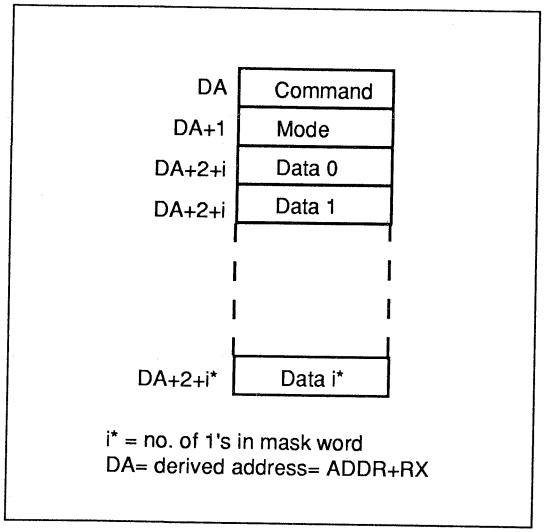


Figure 1: General Vector Table

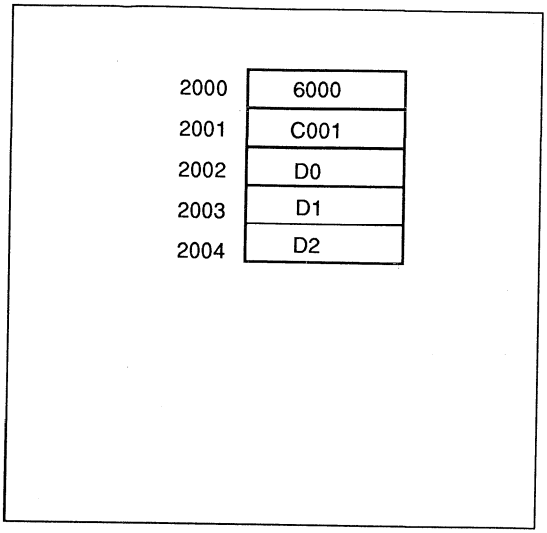


Figure 2: Example Vector Table

MA31750 - Application Note 11
BUS ARBITER

1.0 INTRODUCTION

This application note presents a possible solution for a bus arbiter in a multiple-controller MA31750 system. Such an arbiter can be used to arbitrate between the primary MA31750 system and 1 or more other bus masters. These bus masters can be other MA31750 systems, DMA controllers such as the MA31753, or external interfaces.

2.0 PROCESSOR CONSIDERATIONS

When designing a bus arbiter for an NMA31750 system, the following points need to be taken into account:

2.1 LOCKN PULL-UPS

The LOCKN signals should be pulled up because they go tristate when the processor is degranted. Pull-ups are not shown in the arbiters that are described in the next sections, but they must be incorporated.

2.2 PROTECTED CYCLES

The processor internally latches GRANTN on AS falling to ensure that, when GRANTN is removed, the processor continues driving the busses, strobes and control signals until the cycle has completed. However, on the first external cycle after being granted, or the first external cycle after an internal cycle, this latch has not yet been clocked, and there is a danger, when removing GRANTN during these types of cycles, that the processor stops driving whilst strobes are still active. To prevent this from happening, these cycles must be protected from being degranted, or if grant is taken off during a protected cycle, it must be reasserted before AS falling.

2.3 GRANTN TIMING

The processor samples GRANTN on falling CLKOUT, so an arbiter should not allow set-up and hold times to be violated. This can be achieved by latching out the GRANTN signals off the falling edge of CLKOUT of the relevant system. In addition, note that as GRANTN falls to drive the address bus and strobes, the AS can rise off a falling CLK edge. This can erode the address set-up time to AS rising. If this affects the system, then GRANTN must be asserted low to drive the address bus valid and provide the set-up time before the CLK falling edge (and the AS rising edge).

2.4 TCLK TIMING

If the MA31750 is degranted for long periods, a problem can occur: If after degranting the processor, the TCLK falling edge is close to the falling CLK edge at the end of the machine cycle, and then grant is not returned to that system until after another falling edge of TCLK, a cycle may be aborted. (The time-out circuitry is disabled a short time after the end of the degranted cycle. If a TCLK falling edge occurs between the end of the cycle and the disabling of the time-out circuit, then the time-out count remains active. This problem can occur irrespective of the state of DTON.) This can be prevented by synchronising TCLK to CLK to ensure that TCLK only changes during CLKOUT high. This can be achieved by putting TCLK through a D-type that is clocked by CLKOUT from the same system (to be safe, 2 D-types should be used to prevent metastability problems). This is not shown in the next sections.

3.0 2 CHANNEL SYNCHRONOUS BUS ARBITER

The following is an explanation of a bus arbiter that arbitrates between 2 systems, one of which is the default system (system1), but the other having priority over the first (system2). Only the request from system2 is monitored - if it is asserted then grant is given to system2, otherwise grant is given to system1. The lock signals are also monitored to ensure that either system can keep grant during atomic instructions which should not be interrupted. Both systems and the arbiter run off the same clock. An example of such a scheme would be an MA31750 system which gets the bus by default, and a DMA controller which has priority over the processor.

3.1 BUS ARBITRATION LOGIC

The circuit is shown in figure 1. Falling CLKOUT is used to latch in requests and latch out grants to ensure sufficient set-up and hold time of GRANTN to CLKOUT falling (see section 2.3). If the latched request changes state (and LOCKN is inactive), the active grant will be deasserted. Although grant may be taken away immediately, no grant is given until activity on the bus has finished. The signal PRESETN, which prevents a new grant being assigned, is generated from AS or ACTIVE asserted with no grants (ACTIVE comes from the cycle protect logic described in section 3.2). Note that the arbitration logic can be overridden by PROTECT, the other signal from the cycle protect logic (section 3.2), which keeps grant on or reassigns grant to the last system granted.

3.2 CYCLE PROTECT LOGIC

The circuit is shown in figure 2. The cycle protect logic detects activity on the bus by sampling AS on CLKOUT falling. If AS is sampled low, the cycle is inactive and the ACTIVE signal is deasserted (low). ACTIVE high inhibits granting i.e. grants can only be asserted on inactive cycles. This circuit also detects the first external cycle following inactivity on the bus, and from this it generates the signal PROTECT which lasts until AS falling i.e. until the end of the cycle to be protected. This signal is used to prevent degranting of either system if that system is executing the first external cycle. Protecting this cycle from degranting is important for the correct operation of the processor (see section 2.2). Note that the protected cycle can be either the first external cycle after grant has been asserted, or an external cycle following a granted internal cycle.

It can happen that grant is taken off system1 while it is performing internal cycles but just as it is about to perform an external cycle. As soon as AS goes high, the PRESETN signal, which is generated from AS high with no grants, is asserted and prevents granting of system2. At the same time, the PROTECT signal will become asserted and will reassign grant to system1 until the cycle is complete.

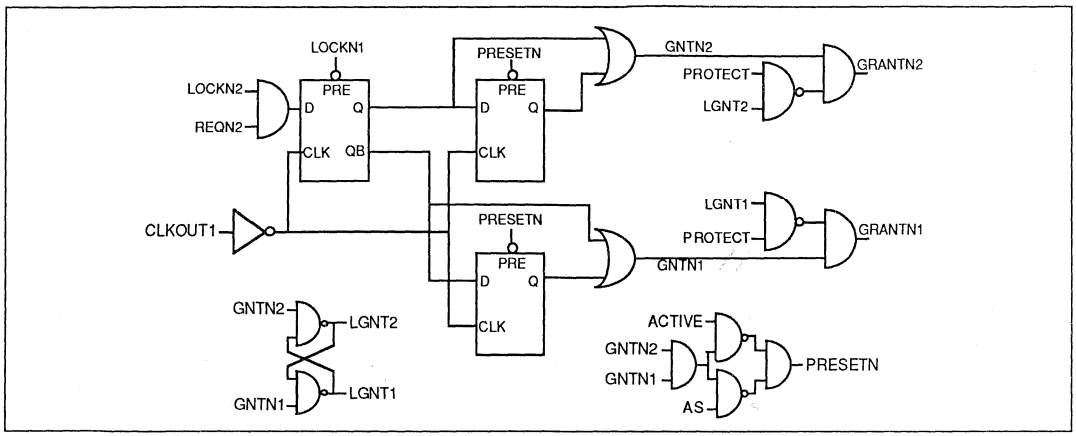


Figure 1: 2 Channel Synchronous Bus Arbitration Logic

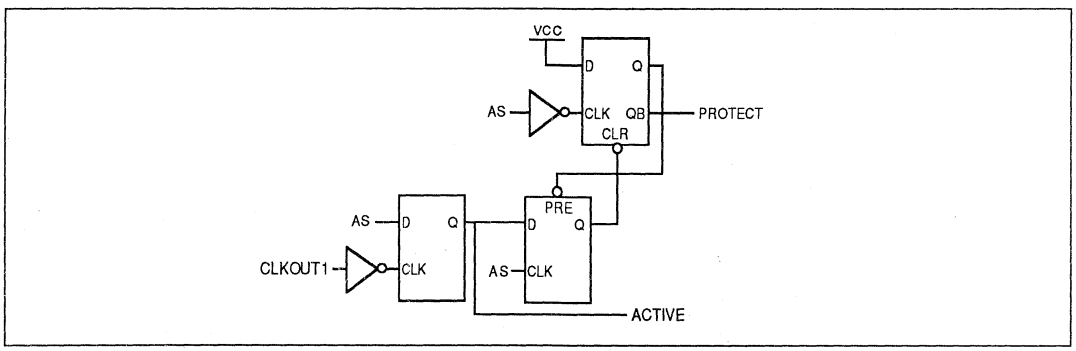


Figure 2: Synchronous Cycle Protect Logic

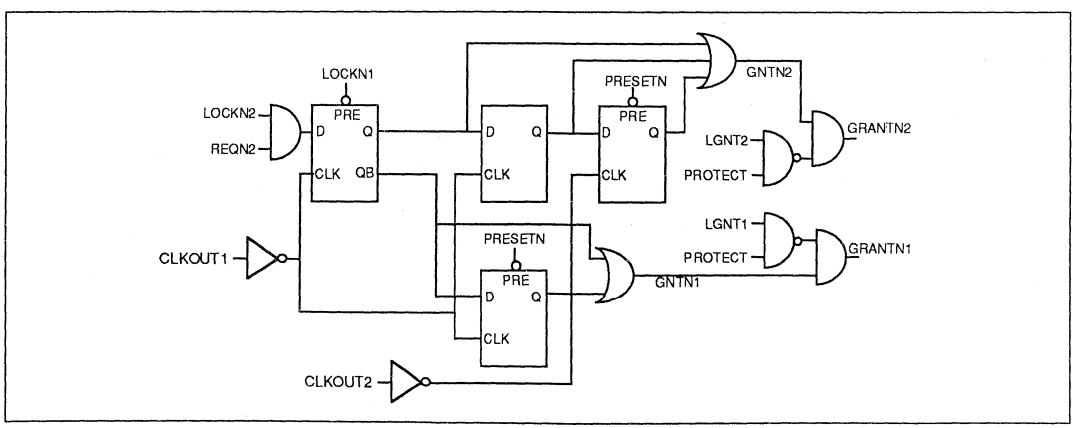


Figure 3: 2 Channel Asynchronous Bus Arbitration Logic

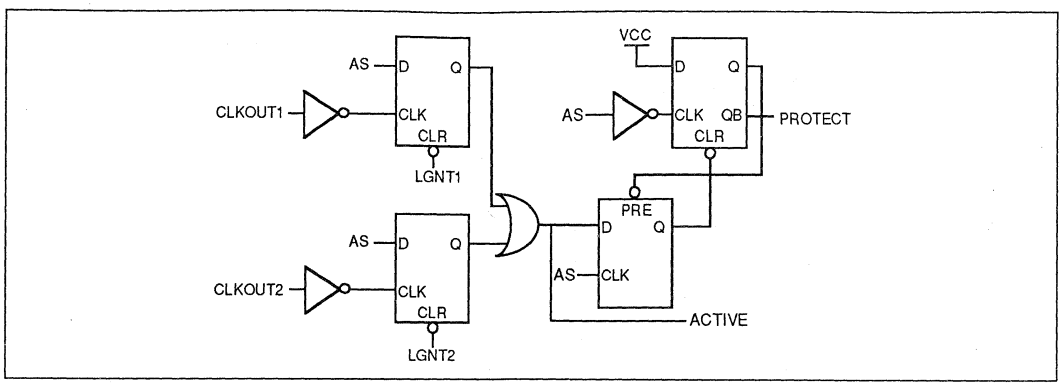


Figure 4: 2 Channel Asysnchronous Cycle Protect Logic

4.0 2 CHANNEL ASYNCHRONOUS BUS ARBITER

This section describes a bus arbiter that is required to arbitrate between 2 systems having separate asynchronous clocks e.g. a processor with an external interface.

4.1 BUS ARBITRATION LOGIC

The bus arbitration logic is shown in figure 3 (the grant latch and preset logic are the same as in figure 1). It is similar to the synchronous case except for the addition of another D-type clocked by CLKOUT2 falling to synchronise GRANTN2 to system2.

4.2 ASYNCHRONOUS CYCLE PROTECT LOGIC

The cycle protect logic is similar to the synchronous case, but now the CLKOUT signals from both system1 and system2 are used to detect activity on the bus. The circuit is shown in figure 4. Note that the latched grant signals LGNT1 and LGNT2 from the arbitration logic are used to select the clock from the system that was last granted.

5.0 3 CHANNEL SYNCHRONOUS BUS ARBITER

This section describes a 3 channel synchronous bus arbiter where system1 is again the default system, system2 has priority over system1 and system3 has priority over both of the other 2 systems (e.g. a processor and 2 DMA controllers).

5.1 BUS ARBITRATION LOGIC

Figure 5 shows the bus arbitration logic which is simply an extension of the 2 channel case.

5.2 CYCLE PROTECT LOGIC

This is exactly the same as for the 2 channel synchronous bus arbiter (figure 2).

6.0 3 CHANNEL ASYNCHRONOUS BUS ARBITER

This section describes a bus arbiter that is required to arbitrate between 3 systems having separate asynchronous clocks e.g. a processor with 2 external interfaces.

6.1 BUS ARBITRATION LOGIC

The bus arbitration logic is shown in figure 6 (the grant latch and the preset logic are the same as in figure 5). It is similar to the synchronous case except for the addition of 2 D-types clocked by CLKOUT2 and CLKOUT3 falling to synchronise GRANTN2 and GRANTN3 to systems 2 and 3 respectively.

6.2 ASYNCHRONOUS CYCLE PROTECT LOGIC

The cycle protect logic is similar to figure 4, but now the CLKOUT signals from all 3 systems are used to detect activity on the bus. The circuit is shown in figure 7.

6.3 WAVEFORMS

Figure 8 shows typical waveforms for the 3 channel asynchronous arbiter described above. The sequence of events is as follows:

1) System 3 executes an external cycle during which it deasserts REQN3.
2) GRANTN3 is deasserted when REQN3 high is latched.
3) ACTIVE goes low followed by GRANTN1 being asserted.
4) System1 executes 2 external cycles followed by an internal cycle, REQN2 is asserted during the internal cycle.
5) REQN2 low is latched and GRANTN1 is deasserted.
6) System 1 executes another external cycle so PROTECT is asserted and GRANTN1 reasserted.
7) GRANTN1 is deasserted at the end of this cycle.
8) When ACTIVE has gone low, GRANTN2 is asserted.
9) System 2 starts executing external cycles, starting with a protected cycle.

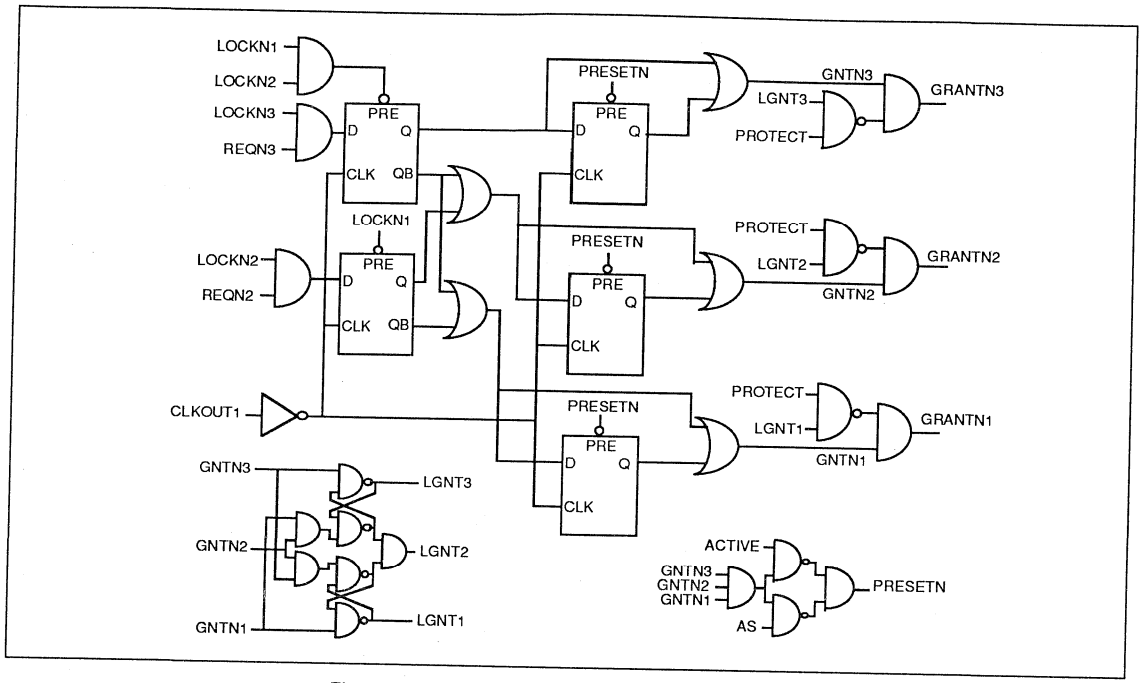


Figure 5: 3 Channel Synchronous Bus Arbitration Logic

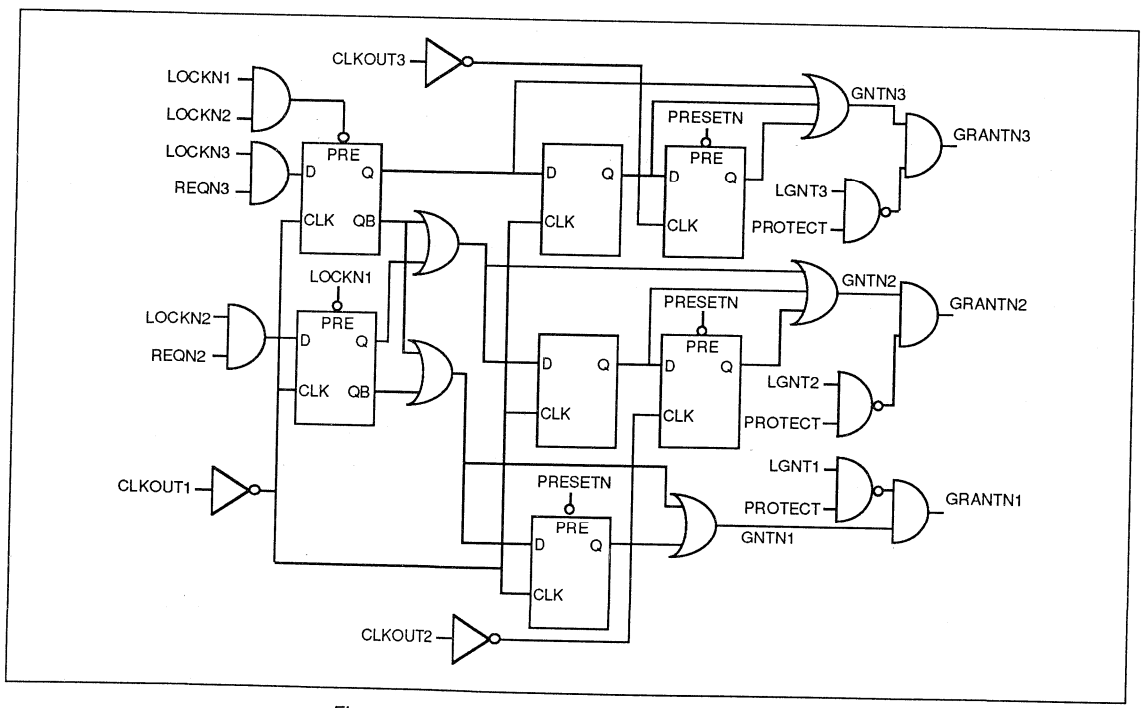


Figure 6: 3 Channel Asynchronous Bus Arbitration Logic

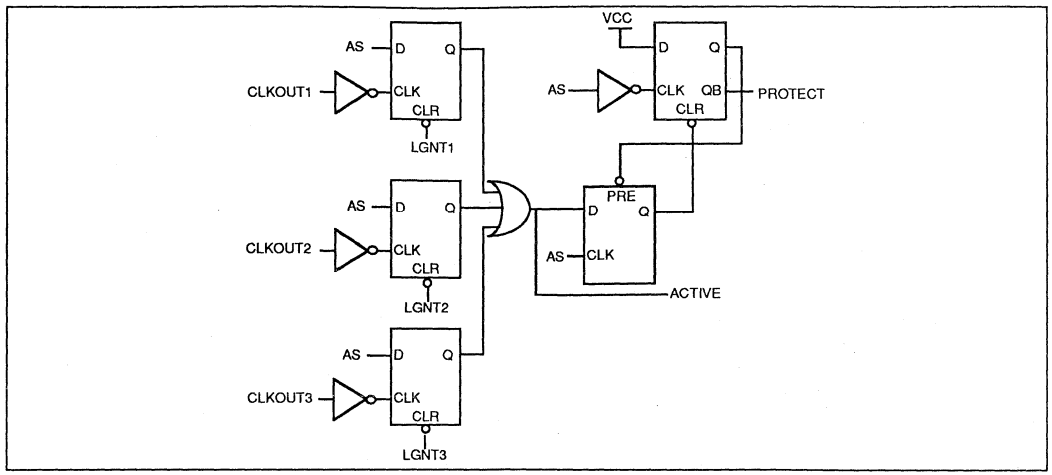


Figure 7: 3 Channel Asynchronous Cycle Protect Logic

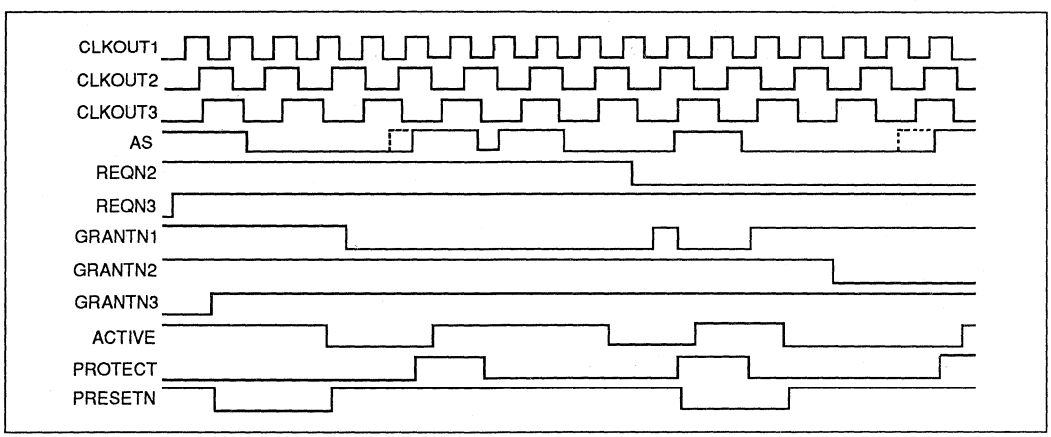


Figure 8: Typical Waveforms for 2 Channel Asynchronous Arbiter

MA31750 - Application Note 14

USE OF NMA31750 SAMPLES

The following Applications Note presents information which will be of use to design engineers who are evaluating the N iteration of the MA31750 microprocessor. In particular, it defines the aspects of the current device operation which do not fully meet the requirements of the specification. This note covers all of the known problems found to date with the N iteration parts.

1. LONG LOADS AND STORES IN 1750B MODE

When using the long load instructions in 1750B mode, the status word does not update the flags bits according to the data just loaded. If a conditional branch or jump is to be determined on the data long loaded, then an explicit compare must be executed before the branch or jump instruction.

During long load and store instructions, the status word is written between each memory access. In the status word written during the loads / stores the PS bits mimic the AS bits. This can be a problem if there is an MMU present in the system as it may cause illegal memory accesses due to access locks and keys no longer matching.

2. EXTENDED MULTIPLICATION IN 1750B MODE.

In 1750B mode, when using EFM / EFMR to multiply 2 numbers, both with an exponent of 0x80, the normalisation method incorrectly determines that an overflow has occurred. The result is forced to the largest positive value (7FFF FF7F FFFF) if the signs of the multiplicands were the same, and to the largest negative number (8000 007F 0000) if the signs of the multiplicands were different. In both cases, the overflow flag is set. A workaround within the overflow interrupt service routine would be to check the exponent of the multiplicand that has not been overwritten. If the exponent value is 0x80, then an overflow result must be erroneous and appropriate action can be taken if required. This problem does not occur in 1750A mode.

3. UNSIGNED SUBTRACT IN 1750B

If a negative flag is set as the result of an unsigned subtract, the carry flag will also be set. This may be incorrect.

4. FAULT MASK WRITES IN 1750B MODE

The fault mask is permanantly stuck at $FFFF_H$. The fault mask write XIO is legal in 1750B mode, but has no effect on the contents of the mask register.

5. BUS TIMEOUTS AND THE FAULT REGISTER

When RDYN stays high during an external memory or IO access (ie. DSN is low), then a timeout fault (either bit 5 or bit 8), will be logged in the fault register. Internally, the CPU sets a timeout flag. This timeout flag is only cleared by servicing the machine error interrupt or by executing the CLIR XIO instruction. Normally, when a fault is activated, the ME interrupt is serviced immediately and the timeout flag is cleared. However, if the ME interrupt is masked, any further external cycles will be flagged as having a timeout fault. This could erroneously set either bit 5 or bit 8 in the fault register. This is also a problem in console mode when console has priority over interrupts.

6. DE-GRANTING THE PROCESSOR

It is strongly recommended that users should reference Application Note 11 for the MA31750, if the CPU is ever to be de-granted.

MA31750 - Application Note 15

PIPELINING INSTRUCTIONS ON THE MA31750

When analysing the behaviour of the MA31750, the pipelining of instructions must be considered.

1.0 PIPELINING INSTRUCTIONS

Instructions are pre-fetched from system memory and are stored in the pipeline of the processor. They are then pulled from the pipeline to be executed. Whilst the instructions are being executed, the pipeline has emptied and the pre-fetch of the next instruction can take place. This pre-fetch is limited to times when the system address and data busses are free as it utilises these busses to access the system memory. See Figure 1.

2.0 PIPELINING ON THE MA31750

The pipeline on the MA31750 always holds 2 16-bit words. If the instruction being executed is a single word instruction, then only one word has been removed from the pipeline. The second word in the pipeline moves up to the first position and one extra word is pre-fetched from system memory. If the instruction being executed is a double word instruction, then the pipeline has emptied and two pre-fetches are necessary to fill it up again.

Occasionally the pipeline needs emptying and reloading, eg. after initialisation or after an interrupt service routine or if a branch or jump is executed. This will take 2 machine cycles dedicated to pre-fetching the new pipeline. Execution can then resume.

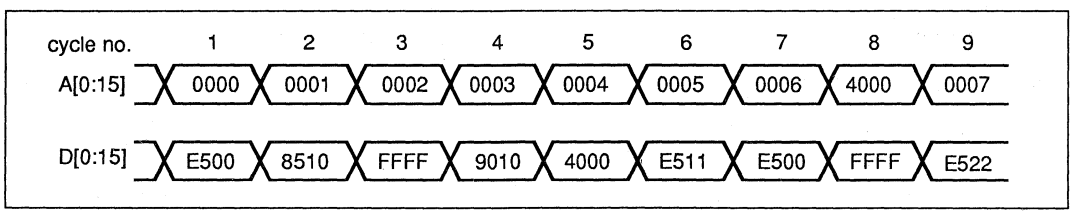


Figure 1: Example of Operation

3.0 EXAMPLE

Figure 1 shows the address and data busses for the following code:

```
0000    E500:       XORR R0,   R0
0001    8510 FFFF:  LIM  R1,   FFFF
0003    9010 4000:  ST   R1,   4000
0005    E511:       XORR R1,   R1
0006    E500:       XORR R0,   R0
0007    E522:       XORR R2,   R2
```

Cycles 1 and 2 are used to fill the pipeline. No instruction execution occurs.

On cycle 3, the XORR instruction is taken from the pipeline and the registers are exor'ed internally. At the same time, the data from address 0002 is loaded into the pipeline.

The next instruction in the pipeline is a double word instruction, therefore cycles 4 and 5 are both needed to refill the pipeline. Whilst the data from addresses 0004 and 0005 are being pre-fetched, register 1 is loaded across internal busses with data FFFF.

Again, the pipeline contains a double word instruction, so cycles 6 and 7 are both needed to refill the pipeline. However, the store instruction needs to use the external address and data busses. This is done on cycle 8 after the pre-fetches have finished.

Once the store has completed, the next instruction is executed. This is a single word instruction (XORR), hence cycle 9 is used for the pre-fetch, as the exor instruction is executed internally.

DS3822-5.3

MA31750SBC

SINGLE BOARD COMPUTER

The MA31750 single board computer (SBC) is a fully featured MIL-STD-1750 compliant system based around the microprocessor from GPS. The board also features a fully implemented MMU/BPU, 64K words of fast SRAM, twin serial ports and a parallel port. All can be implemented in GPS's proprietary CMOS/SOS latchup immune, radiation hard technology if required.

The SBC can be used as a hardware and software development and evaluation platform or as a solution to a specific target application. GPS provide a suite of assembly and debugging tools with each board, aimed at simplifying the development of software code. These tools can be hosted on a VAX, SUN, Apple Macintosh or PC based workstations.

The SBC has been designed to enable all on board logic to be implemented in radiation hard technology, thus offering a complete solution to a system designers needs. If necessary the SBC can be easily expanded via the 96-way expansion bus to fulfil almost all development system requirements.

Implemented on a high quality 6 layer PCB, with dedicated power planes and decoupling, the SBC offers a high level of system integration. The SBC system comprises MA31750 CPU, MA31751 MMU/BPU, 64kWords of fast SRAM - MA9287's, MA8251 USARTs, MA8255 PPI and all the necessary glue logic for system interfacing.

FEATURES

- MA31750 and MA31751 in CMOS/SOS
- Operates to Maximum Speed of CPU
- 64K SRAM System with MMU/BPU (SOS if Required)
- Peripherals (Radiation Hard SOS if Required)
- Supports All Mandatory MIL-STD-1750A Requirements
- Supports Option 2 1750B Instructions (User Selectable 1750A or 1750B Modes)
- Standard Edge Connector Provides For Future Expandability
- Supplied with Powerful MIL-STD-1750 Assembler and Tools to Link the Board to a VAX, SUN or PC Based Workstation.
- Built in ROM BIOS Aids Software Development
- Standard Rack Mountable Card Format

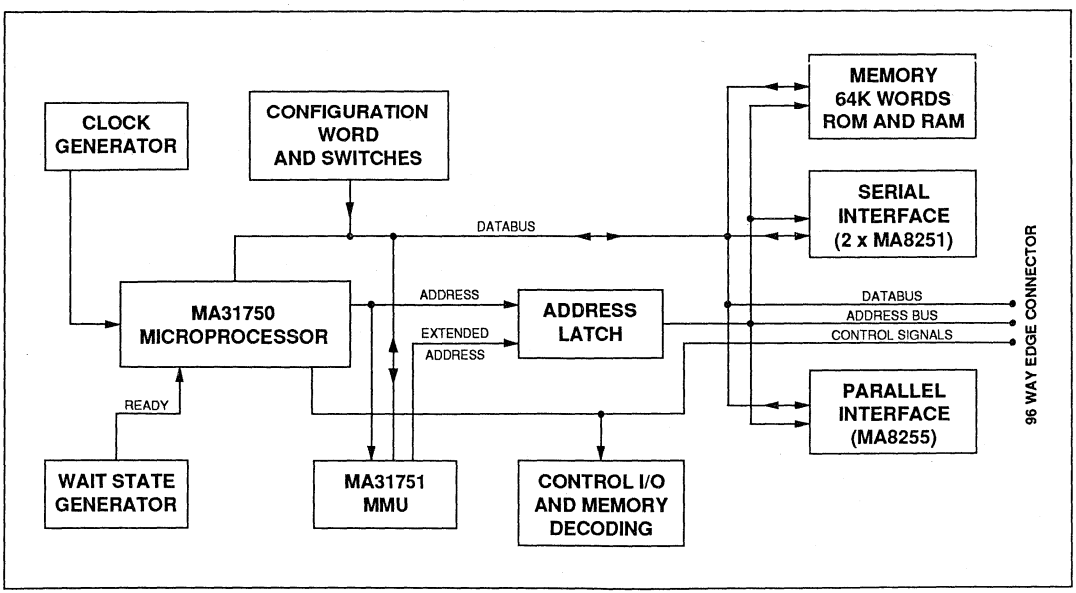


Figure 1: Block Diagram

The board can be used in two main configurations:

i) With a IMA31750 and no MMU.

ii) With a NMA31750 and a B/CMA31751

If the first configuration is used, the CPU accesses the 64K of memory directly. If the second configuration is set (by selecting the appropriate jumper option) then the MA31750 can access the full 64kWords of memory implemented on the SBC via the MA31751 MMU/BPU. The MA31751 also provides the full additional memory expansion of 1750A to allow access to a full 1MWord of memory (most of this expanded memory must be accessed via the external expansion bus).

The MA31751 is capable of working in either MMU only, BPU only or combined MMU/BPU mode which is selected under user control via the system configuration register. The MA31751 automatically traps all MIL-STD-1750A/B XIO instructions which control memory management and protection functions and processes them as required. A simple bus interface between the MA31750 and MA31751 allows the system to be implemented with only a handful of gates.

The SBC incorporates several different ways of interfacing to external devices. Serial communications are provided by two MA8251 IC's. The MA8251 is based upon the industry standard 8251A Universal Synchronous Asynchronous Receiver/Transmitter (USART). Upon reset the built in ROM BIOS sets up the two 8251's as simple 9600 baud terminal ports - one of which is intended to be connected to a terminal (VT100 or compatible) and the other is intended for communicating serially to a host computer (VAX, SUN or PC). The MA8251's can, however, be re-programmed by the user to fulfil virtually any serial data link needs. The SBC also incorporates a set of RS232 level translators to facilitate connection to any RS232 conformant system.

Parallel communications on and off the SBC are governed by an MA8255. The MA8255 is a general purpose programmable I/O device. It is capable of driving up to 24 I/O pins in 3 different modes of operation. The MA8255 accepts 8 bits of parallel data from the CPU and outputs this data on the parallel link bus. Conversely the MA8255 can accept parallel data via the link and formats this data ready for transfer to the CPU. Upon reset the MA8255 is set up for bi-directional communications over a PC compatible parallel port link. Again this device may be re-programmed to suit the user's needs.

1. INVENTORY

The following items are supplied as part of the SBC package:

Single Board Computer.

An IBM diskette contains the following software:

CASM.EXE - an in-house Mil-Std-1750 assembler,
PROMBLOW.EXE - a PC to EPROM programmer downloader,
DOWNLOAD.EXE - a PC to MA31750 board downloader,
DOWNLD.SFS - the MA31750 board part of DOWNLOAD,
ROM500.SFS - MA31750 Monitor ROM as implemented in the SBC.

Full set of circuit diagrams for the SBC.

2. GETTING STARTED WITH THE SBC

2.1. EQUIPMENT REQUIRED

In addition to the SBC you need the following equipment:

a) +5v supply.
b) VT220.Connect to PORT 2 (labelled P2)
NO XON/XOFF
9600 baud, 8 Bits,1 Stop bit

2.2. JUMPER AND LINK OPTIONS

The SBC has been organised to permit various system configurations, using different iterations of the MA31750.

a) IMA31750 in 1750A or 1750B mode with no MMU
b) NMA31750 in 1750A or 1750B mode with or without an MMU (B/CMA31751)

SBC 9 WAY SOCKET(PORT 1)	VAX 25 WAY PLUG
2	2
3	3
5	7

SBC 9 WAY SOCKET(PORT2)	TERMINAL 25 WAY SOCKET
2	2
3	3
5	7

Figure 2: RS232 Socket Connections

To configure the SBC, view the board from the component side with the MA31750 furthest away (North), the 96 way edge connector on the right (East), and the RS232 connectors on the left (West). Pin jumper selections are referenced to this orientation.

2.2.1. BAUD RATE

Select one baud rate by placing a jumper across J1, J2 or J3.

J1 baud 38400
J2 baud 19200
J3 baud 9600

2.2.2. XIO ADDRESSES

Select block of addresses in XIO space for peripherals. The 7 bit address (A1 to A7) along with the decode of A8 to A10 gives 8 banks of 32 words. Use jumper to select logical "1".

J7 msb XIO block decode
J8
J9
J10
J12
J14
J16 lsb

2.2.3. WAIT STATES

Select count for number of wait states required. Use a jumper to the East to select logical "1" and to the West to select logical "0".

Wait State	0	1	2	3	4	5	6	7	8
J11	x	1	0	1	0	1	0	1	0
J13	x	1	1	0	0	1	1	0	0
J15	x	1	1	1	1	0	0	0	0
J17	0	1	1	1	1	1	1	1	1

2.2.4. IMA31750 SELECTION

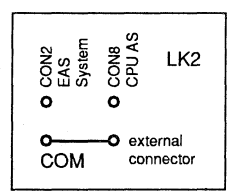
J4 1750A/B select (South for 1750A, North for 1750B)
LK1 Sysclk = CLK (North)
LK3 Configuration word = CPU pin, IC23, IC24 are not required (south), or decode for 1750B using IC23, IC24 (North)

2.2.5. NMA31750 SELECTION

J4 1750A/B select (South for 1750A, North for 1750B)
LK1 Sysclk = CLKOUT (South)
IC25, IC26 are not required with a NMA31750 and may be replaced with wire links.

2.2.6. NO MMU SELECTION

LK2	CON2-COM	AS drives system address strobe
AND	CON8-COM	AS to external 96-way connector
LK4	lsb	CPU addresses linked to Extended addresses
LK5		CPU addresses linked to Extended addresses
LK6		CPU addresses linked to Extended addresses
LK7	msb	CPU addresses linked to Extended addresses



2.2.7. MMU SELECTION

LK8		BMA31751 Mode
LK2	CON2-COM	EAS to external 96-way connector
OR	CON8-COM	AS to external 96-way connector

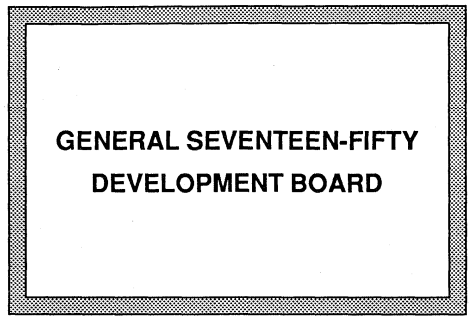
2.2.8. TO VIEW SECOND RS232 PORT ON MONITOR TERMINAL

J5 Port2 transmission to monitor
J6 Port2 receive to monitor

Note: Do not use with the command 'V'.

2.3. WELCOME MESSAGE

After pressing RESET, you should get a banner and prompt of the form:



Typing H at this point will give a menu of available commands.

3. SBC MONITOR COMMAND REFERENCE

Monitor functions are selected from a menu by a letter (case independent) and carriage return. Any subsequent information required is supplied by the user in response to the questions.

'H'	Help Page	Brings up menu to aid selection
'A'	Change Current Address Pointer	Allows an address to be selected so that its contents can be viewed or changed by the 'R' or 'W' options. Also see 'D','I'
'W'	Write Data at Current Address Pointer	Write data to the selected address .Use with 'A','D','I','R'
'R'	Read Data at Current Address Pointer	Reads the data at the current address pointer. Use with 'A','D','I',
'G'	Execute User Routine	This allows a program in the system (either put in manually or externally) to be run. If the program ends with URS R15 (i.e. return from subroutine) control will pass back to the monitor
'B'	Block Read	Reads block of data from memory and displays it on the screen. Block continues reading until any key is pressed
'P'	Program	A method to enter short programs manually. User enters start address and then the machine code (data), the module moves automatically onto the next address after 4 characters have been entered. Typing a 'Q' in place of a hexadecimal number will terminate input. Often used in conjunction with 'G'
'I'	Increment Current Address Pointer	Increments address pointer. Use in conjunction with 'W','R'
'D'	Decrements Address Pointer	Decrements address pointer. Use in connection with 'R','W'
'E'	Enable Interrupts with User Mask	Allows interrupt mask to be changed, and whether interrupts are to be enabled or disabled

'S'	Ram Editor	Displays a block of memory on the screen (HEX and ASCII). Arrow keys are used to move round the screen to edit specific addresses ***CONTROL A*** Select address ***CONTROL P*** Previous page ***CONTROL N*** Next page ***CONTROL C*** Exit ***TAB*** Switches between HEX and ASCII editing
'T'	RAM Tester	This checks RAM addresses from 1000 to FFFF
'M'	Change Monitor Routine Base Address	Option to move the monitor program to a safe area not used by the application.
'C'	Block Copy	Copies block of memory from one address to another area with a choice of the number of words.
'F'	Block Fill	Allows variable amounts of memory to be filled with a user selected value.
'L'	Download File	Download a program from a PC or VAX. Used when monitor is linked through to PC or VAX(see 'V' option.). Typing ***L*** causes the board to wait for the host system to send a .LDM file.
'V'	VAX Terminal Emulator	Allows the terminal to connect direct to a VAX .through the other port. 1750 Assembler Programs written on a VAX, and assembled using CASM (the 1750 assembler provided) to create a '.LDM' file can be downloaded to the board using the command ***GSDB /L < file name>*** . Control can be passed from the Vax to the board monitor by typing ***GSDB***

4. CASM SOFTWARE

4.1. USE OF THE SOFTWARE

CASM, the Mil-Std-1750 assembler, is run on the PC using the command syntax :-

CASM <filename> [-l, -d, -m, -h]

CASM requires the input file to be in ASCII format. The default file extension '.SFS' is assumed, but other extensions can be used if specified as part of the filename, thus :-

CASM ROM402 will assemble the source file ROM402.SFS'
CASM MYFILE.TXT will assemble the source file 'MYFILE.TXT'

During a normal assembly run CASM will generate the following files :-

CASM MYFILE generates MYFILE.HEX
MYFILE.LDM
[MYFILE.LST - optional]

The '.HEX' file is a simple output file used by PROMBLOW.EXE to download compiled code to an EPROM programmer. Data is held as an ASCII text file in ADDRESS : DATA format. The '.LDM' file is the output file used by DOWNLOAD.EXE. This file (also held as an ASCII text file) conforms roughly to INTEL LOADER format file specifications. This format includes addressing information which enables the downloader to automatically locate the file at the correct start address (usually specified by an ORG statement) and checksumming information in order to enable the detection of errors across the RS232 link used in the transfer.

CASM will generate suitable error messages on screen which will detail assembler errors along with the code fragment which generated that particular error. Should the '-l' option have been specified, these error messages will also form part of the '.LST' listing file and will be placed next to the suspect line of source code.

4.1.1. CASM COMMAND LINE OPTIONS
Four command line options are available for CASM :-

-l - this option produces a listing file with the same base name as the source file, and extension '.LST'. This file contains both the instruction address, its operand and data (both in hex format) and the original source line from which the assembled code was generated. '.LST' files are useful to check source code against assembly when errors have occurred.

-m - this option relates to the '-l' option, modifying the way in which MACRO's are printed in the listing file. By default CASM will simply print a 'Call to macro xxxx' whenever a macro is called. By using the '-m' option a full listing of the macro code is printed each time the macro is called.

-h - this option changes the default radix so that all numbers within the assembled program will be treated as hexadecimal rather than decimal.

-d - this option simply causes CASM to echo its date of compilation to the screen. This enables the user to check that the version being used is the most up to date. (At the time of writing the latest revision is V2.20).

4.1.2. CASM DIRECTIVES
CASM accepts the following standard assembler directives (case independent):-

Directive	Function
%INCLUDE "MYFILE.EXT"	Includes the named source file as part of the source to be assembled.
ORG <address (hex)>	Sets the current program counter to the value <address> in hex.
EVEN	Sets the program counter to be on an EVEN address
STORE <number>	Reserves <number> (decimal) words of space in memory. NOTE - these locations are not cleared to any particular value by the assembler.
DATA <val1 val2 val3 ....>	The following data values are stored into memory at the current and sequential program counter (PC) addresses.
TEXT <ascii text>	The following string of text is interpreted and placed in memory at the current address. TEXT also recognises the following sub-directives :-\r inserts a carriage return (0D h) into the string. \n inserts a linefeed (0A h) into the string. \0 places a NULL (00 h) in the current string.
LITERAL "string"	Places the string which is enclosed by quotes into memory in a similar manner to TEXT. This statement does not recognise the \r, \n, \0 directives.
CONS <numeric>	This directive converts the following numeric string into a number in either 1750 floating point format, extended floating point format or normal hex format. The result is then placed into memory. Numbers are preceded by X' or 0X for 16 bit hex; Y' or 0Y for 32 bit hex; E' or 0E' for floating point numbers.X,Y,E are case independent
PAGE	This directive inserts a page break into the 'LST' listing file.
<label> EQU <data>	This directive equates the label, <label> to the hex value <data>.
$	This directive always equates to the current value of the program counter and may be used in any numerical expressions within the assembly code.
MA31750	Enables the extra opcodes and XIO instructions to directly support the MA31750 processor and the MIL-STD-1750B extensions which it supports.
MACRO	This directive allows the definition of simple macro functions which may be called at any point in the user program. **See Section 4.1.3**
END_MACRO	A companion directive to 'MACRO' which ends the macro definition.

4.1.3. COMMAND MACROS

Macros allow repeated pieces of code to be written once and given a reference name. They are called into the main program whenever required and are replaced at assembly time with the full routine.

MACRO	this directive allows the definition of simple macro functions
END_MACRO	a companion directive to 'MACRO' which ends the macro definition.

Example:-

```
MACRO       fred                    /defines a macro named 'fred'
            lim   r12, fred_msg     /load r12 with pointer to message
            sjs   r15, tprint       /call the ROM print routine
END_MACRO                           /end of macro definition

      Start lim   r10, 0004         /Beginning of main program, r10:=4
            fred                    /call to macro 'fred'
            soj   r10, Start        /loop r10 times

            .....                   /rest of code

fred_msg    text  This message was printed by a macro call \r\n\0
```

4.1.4. RADIX SELECTION

CASM supports either decimal or hexadecimal numbering systems. The default numbering system is decimal. This default may be changed using either the '-h' command line switch to default to hexadecimal numbering. Alternatively, the assembler directive RADIX may be used as shown below. In 'RADIX hex' numbers are always treated as hexadecimal, however in 'RADIX dec' numbers can be entered in either hex or decimal but will be converted to decimal by default. (see examples)

Example:-

```
RADIX hex

    Stack equ 000f
        LIM   r12,   000f       /compiles to  85C0 000F
        LIM   stack, 0001       /             85F0 0001
        LIM   rf,    0010       /             85F0 0010

RADIX dec

        LIM  r15, 0010          /compiles to  85F0 000A
        LIM  r15, 0x0010        /             85F0 0010
        LIM  r15, 0022          /             85F0 0016
        LIM  r15, 00AA          /             85F0 00AA
```

4.1.5. LABELS

When writing code which will be assembled by CASM, it should be noted that labels which are also valid hex addresses, valid 1750 instructions (including named XIO's such as ESUR or RCFR) or valid assembler directives should be avoided. Use of such labels within assembly code will cause an error.

CASM differentiates between upper and lower case characters only for labels, thus 'LABEL1' will refer to a different object to 'label1'.

5. PROMBLOW SOFTWARE

As stated earlier PROMBLOW is designed to be used to download assembled code to an EPROM programmer. The software uses the assembler '.HEX' files which are expected to be broadcast to an EPROM programmer down an RS232 link in ASCII-HEX-SPACE format. The software defaults to 1200 baud communications, however command line switches are available which can be used to configure the software to run at other rates. The default file name is 'A.OUT', other filenames must be specified with the full name plus '.HEX' extension.

PROMBLOW uses the RS232 port COM1: as the standard output port.

5.1. COMMAND LINE SWITCHES

The command switches are as follows :-

-b <value> - changes the transmission rate to <value>.
-s <value> - defines the number of stop bits transmitted.
-w <value> - defines the word length transmitted.
-p <value> - defines the type (if any) of parity used.

EXAMPLE:

'PROMBLOW ROM500.HEX -b 9600' will transfer the file ROM500.HEX down the RS232 link at 9600 baud.

6. DOWNLOAD SOFTWARE

The downloader software package, comprising DOWNLOAD.EXE and DOWNLD.SFS, is used to download assembled files to the MA31750 board. DOWNLOAD.EXE is run on the PC and transfers the '.LDM' file specified via COM1: to the board. DOWNLOAD always assumes the file extension '.LDM' unless specified otherwise. Thus :-

DOWNLOAD MYFILE has the same effect as
DOWNLOAD MYFILE.LDM

DOWNLOAD.EXE on the PC allows the same command line options as PROMBLOW to configure baud rate, stop bits, word length and parity.

DOWNLD.SFS is the source code for the MA31750 board half of the software downloader, and is contained in the EPROM. This code receives the data through one of the USART ports, checks the line checksum for each line, and (assuming the checksum is correct) puts the incoming code into memory at the correct address. Should a checksum error occur the program will abort, with the download unfinished, at the line where the error occurred.

7. EDGE CONNECTOR PINOUT

96 WAY CONNECTOR DATA

Pin No.	ROW A	ROW B	ROW C
1	D0	A0	INT15N
2	D1	A1	INT13N
3	D2	A2	INT11N
4	D3	A3	INT10N
5	D4	A4	INT08N
6	D5	A5	INT02N
7	D6	A6	IOI2N
8	D7	A7	IOI1N
9	D8	A8	PWRDN
10	D9	A9	MPROEN
11	D10	A10	PEN
12	D11	A11	SYSFN
13	D12	A12	XEXADEN
14	D13	A13	BUSFLTN
15	D14	A14	INTAKN
16	D15	A15	LOCKN
17	D16	EA0	REQN
18	DSN	EA1	GRANTN
19	RDN	EA2	DMAKN
20	WRN	EA3	CONREQN
21	RDWN	EA4	GLPE
22	OIN	EA5	XRDYN
23	MION	EA6	TGON
24	RESETN	EA7	PS0
25	SUREN	EA8	PS1
26	SYSCLK	EA9	PS2
27	CSN0	EA10	PS3
28	CSN1	PB0	AS0
29	CSN2	PB1	AS1
30	CSN3	PB2	AS2
31	CSN4	PB3	AS3
32	Vcc	See LK2	Vcc

DS3563-3.3

MAS281

MIL-STD-1750A MICROPROCESSOR

The MAS281 Microprocessor is a MIL-STD-1750A (Notice 1), 16-bit Central Processing Unit (CPU). It consists of three CMOS/SOS large-scale integration (LSI) chips: the MA17501 Execution Unit (EU), the MA17502 Control Unit (CU), and the MA17503 Interrupt Unit (IU). These three units can be mounted on, and interconnected within a 64-pin ceramic substrate. The microprocessor is also available as a 3-chip set without the ceramic substrate (see ordering information on page 55).

The MAS281 is optimised for real-time I/O and arithmetic intensive operations. Key performance-enhancing features include a parallel multiplier/accumulator, 32-bit barrel shifter, instruction pre-fetch queue, and multiport register file. Additional features include a comprehensive Built-In-Test (BIT), interval timers A and B, trigger-go counter, and Start-Up ROM interface.

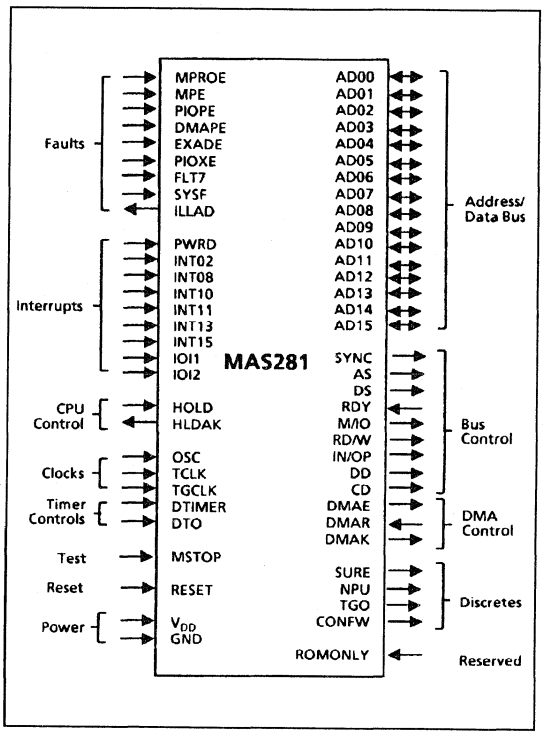
In accordance with MIL-STD-1750A, the MAS281 supports a 64K-word address space. An optional BMA31751 Memory Management Unit/Block Protect Unit (MMU(BPU)) chip may be added externally to expand this address space to 1M-words or add a 1K-word memory block protection capability,

The MAS281 is offered in several screening grades which are described in this document. For availability of speed grades, please contact GEC Plessey Semiconductors.

FEATURES

- MIL-STD-1750A 16-Bit Microprocessor
- Full Performance over Military Temperature Range (-55°C to + 125°C)
- Radiation Hard CMOS/SOS Technology
- Performance Optimised Architecture
  - Parallel Multiplier/Accumulator
  - 32-bit Barrel Shifter
  - Instruction Pre-Fetch
  - Multi-Port Register File
- Implements MIL-STD-1750AOptions
  - Timers A and B
  - Trigger-Go Counter
  - Start-Up ROM Interface
- 64 K-word Address Space Expandable to 1 M-word with Optional MMU

BLOCK DIAGRAM



1.0 ARCHITECTURE

The MAS281 Microprocessor is a high performance implementation of the MIL-STD-1750A (Notice 1) instruction set architecture. It consists of three custom CMOS/SOS Large Scale Integration chips referred to as the Execution Unit, Control Unit, and Interrupt Unit - mounted on, and interconnected within, a 64-pin, dual in-line ceramic substrate. Figure 1 depicts the interconnection of these chips via the substrate while Figure 2 depicts the architectural details within each chip.

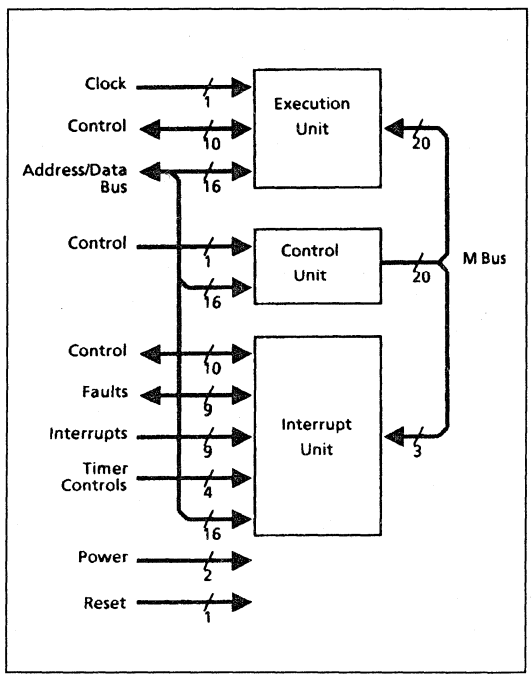


Figure 1: MAS281 Microprocessor Block Diagram

The MAS281 architecture has been optimised for both real time I/O and arithmetic intensive operations. Two key features of this architecture which contribute to the overall high performance of the MAS281 are; a barrel shifter and a parallel multiplier/accumulator. These subsystems allow the MAS281 to perform multi-bit shifts, multiplications, divisions, and normalisations in a fraction of the clock cycles required on machines not having such resources. This is especially true of floating-point operations, in which the MAS281 excels. Such operations constitute 16% of the Digital Avionics Instruction Set (DAIS) mix and a generally much higher percentage of many signal processing algorithms, therefore having a significant impact on system performance.

In accordance with MIL-STD-1750A, the MAS281 can access a 64K-word address space. With the addition of an external MA31751 chip configured as a Memory Management Unit (MMU), this address space may be expanded to a full 1Mword. Furthermore, this configuration provides write and access lock and key protection down to 4K-word blocks. By also configuring the MA31751 as a Block Protect Unit (BPU), write protection may be extended down to 1K-word blocks. For those applications not requiring adherence to the address space requirements of MIL-STD-1750A, the MAS281 may be optionally configured with up to 1Mword each of instruction and operand space.

In addition to implementing all of the required features of MIL-STD-1750A, the MAS281 also incorporates a number of optional features. Interval timers A and B as well as a trigger-go counter are provided. Most specified XIO commands are decoded directly on the module and an additional set of commands, associated with MMU and BPU operations, are directly decoded on the MA31751 chip. Those commands not directly decoded are output for decoding by external logic in accordance with the XIO and VIO protocols of MIL-STD-1750A.

1.1 EXECUTION UNIT (EU)

The EU provides the computational resources for the MAS281. Key features include: (1) a three-bus (R, S, and Y) data path consisting of an arithmetic/logic unit (ALU), three-port register file, barrel shifter, parallel multiplier/accumulator, and status register; (2) instruction fetch registers IC, IA, and IB; (3) operand transfer registers A, DI, and DO; (4) a state sequencer; and (5) microinstruction decode logic. A brief description of these features follows:

1.1.1 ARITHMETIC/LOGIC UNIT (ALU)

A full function 16-bit ALU is used to perform arithmetic and logic operations on one or two 16-bit operands in a single machine cycle. The ALU supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit floating-point extended precision data in two's complement form. The ALU generates several machine flags which reflect the outcome of its operations. These flags are stored in the condition status (CS) field of the status register.

1.1.2 THREE PORT REGISTER FILE

A 24-word by 16-bit wide register file is used to store operands, addresses, base pointers, stack pointers, indexes, and temporary values. Registers R0 through R15 are general purpose and user accessible in accordance with MIL-STD-1750A; remaining registers are accessible only by microcode. Wrap-around concatenation of R0 through R15 allows 32- and 48-bit operands to be stored. The three-port architecture allows two 16-bit operands to be read and a third 16-bit operand to be written simultaneously.

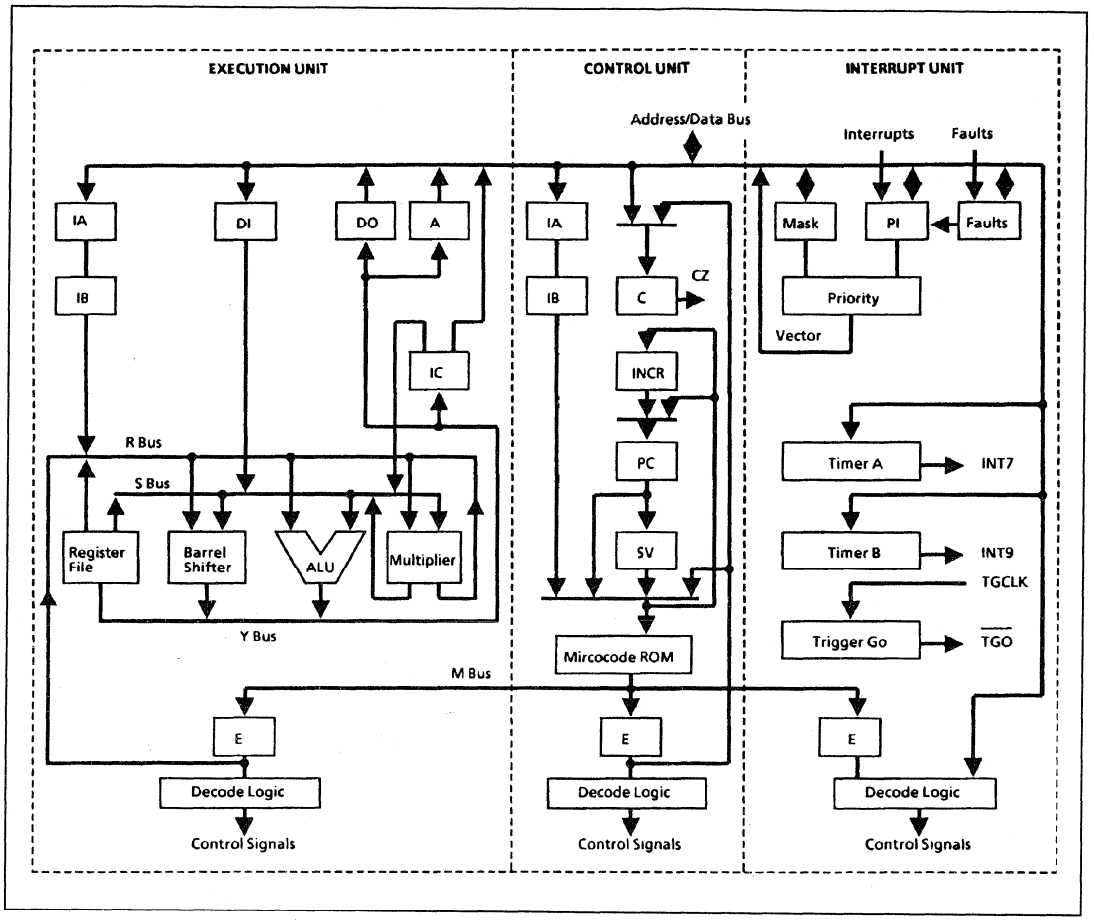


Figure 2: MAS281 Architecture

1.1.3 PARALLEL MULTIPLIER/ACCUMULATOR

This multiplies a 24-bit multiplicand by a 4-bit multiplier and accumulates the product in a single machine cycle. Only four iterations through the multiplier are required to complete a 16-bit by 16-bit multiply.

1.1.4 BARREL SHIFTER

This shifter is a 32-bit input, 16-bit output right-shift network. The barrel shifter allows multibit shifts to be accomplished in a single machine cycle and is used by the microcode for all shift, rotate, and normalise operations.

1.1.5 STATUS REGISTER

This 16-bit register holds the condition status (CS) bits C, P, Z, and N; the 4-bit address state (AS) field; and the 4bit processor state (PS) field. The CS bits are updated after each logical, shift, and arithmetic operation performed by the ALU.

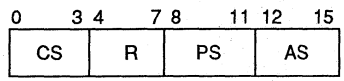
The CU interrogates these bits during conditional operations to determine which course of action to follow. The AS field is used during expanded memory access to define the page register set to be used for instruction and operand memory references. The PS field is used during memory protect operations to define the access key used for memory accesses. The PS field is also used during execution of privileged instructions. PS must be zero for such operations to be legal. Figure 3 depicts the status register format

1.1.6 STATE SEQUENCER

The EU utilises a state machine, clocked by the system oscillator, to generate processor timing and control signals. These signals constitute the lowest level of control available within the module, and provide the framework for basic operations, such as selecting the next microinstruction to be executed, sequencing bus control signals to effect a memory transfer, or performing an operation within the ALU. Each complete pass through the state machine corresponds to one such operation and constitutes a machine cycle.

A machine cycle requires five or more oscillator cycles with the exact number determined by the type of operation being performed. Internal processor operations, excluding internally decoded XIO commands, require either five or six oscillator cycles, the former associated with sequential microcode execution and the latter with microcode branches. Internally decoded XIO commands require a minimum of six oscillator cycles to complete. External processor operations require a minimum of five oscillator cycles to complete.

The internal ready signal is generated by the IU whenever an internally decoded XIO command is detected An external ready interface is provided which allows external machine cycles to be extended when interfacing with slow devices. The external ready signal is provided by external logic and must be asserted in order to conclude the machine cycle.



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result<0
R	4 - 7	RESERVED
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3: Status Word Format

1.1.7 OPERAND TRANSFER REGISTERS

The Address (A), Data In (DI), and Data Out (DO) registers serve to buffer transfers between the data path and the Address/Data (AD) bus. These registers are used under microcode control and are not directly accessible by software. A description of the use of these registers during memory and I/O operations is provided in section 3.0.

1.1.8 INSTRUCTION FETCH REGISTERS

The Instruction Counter (IC), Instruction A (IA), and Instruction B (IB) registers allow sequential instruction fetches to be performed without the assistance of the ALU. The IC register, which holds a 16-bit address and points to the next instruction to be fetched, is loaded indirectly via reset, jump, or branch operations. Once loaded, it uses a dedicated counter to sequence from one instruction to the next. IA and IB serve as an instruction pipeline with IA storing the next instruction to be executed. DI also plays a role by storing any immediate operands. Use of these registers during instruction fetches is described in section 3.0.

1.1.9 MICROCODE CONTROL LOGIC

All EU operations are performed under microcode control. As depicted in Figure 2, microinstructions are provided by the CU over the M bus, buffered by the Execution (E) register, and decoded to generate various control signals.

1.2 CONTROL UNIT (CU)

The CU provides microprogrammed control of all MAS281 operations. It features a microsequencer, a microcode storage ROM, and an instruction mapping ROM. A brief description of these features follows:

1.2.1 MICROSEQUENCER

This 12-bit wide microcode address generator controls all microcode ROM accesses. The microsequencer features a program counter (PC) which points to the next sequential microinstruction, a program counter save register (SV) to save return addresses for microsubroutines, address increment logic (INCR), instruction pipeline registers (IA and IB), a next address multiplexer, a loop counter (C), and various miscellaneous systems.

The microsequencer controls the execution of each MILSTD-1750A, or macro, instruction by stepping through its corresponding microcode sequence. If the macroinstruction is a conditional, the CS bits of the status word will be interrogated to determine the necessary course of action. At the completion of each macroinstruction, the microsequencer checks to see if a Hold request or an interrupt is pending. If so, the microsequencer will branch to the appropriate microinstruction sequence. If not, the microsequencer begins sequencing the next macroinstruction.

Note that the microsequencer is itself under the control of the EU state sequencer. Each processor machine cycle corresponds to the execution of a single microinstruction.

1.2.2 MICROCODE ROM

This is a 2k- (2048) word by 40-bits/word ROM which stores the microinstructions that implement the MIL-STD-1750A instruction set. The address of the next microinstruction to be accessed is generated by the microsequencer. The accessed microinstruction is output to the M-bus and broadcast to the EU and IU. In addition to the microinstruction sequences corresponding to the MIL-STD-1750A instructions, the microcode ROM also stores sequences for performing initialisation, interrupt response, Hold response, instruction prefetch, built-intest (BIT), and BIFs.

1.2.3 INSTRUCTION MAPPING ROM

This is a 512-word by 8-bits/word ROM which is used during microcode branches.

1.3 INTERRUPT UNIT (IU)

The IU incorporates a pending interrupt register, a mask register, a priority encoder, a fault register, two interval timers (A and B), a trigger-go counter, XIO command decode logic, and microcode control logic. A brief description of these features follows:

1.3.1 PENDING INTERRUPT REGISTER (PL)

This 16-bit register is used to capture and hold interrupts until they can be processed by software. PI supports three dedicated external, six user-definable external, and seven dedicated internal interrupts. Interrupts are captured at the beginning of each machine cycle and are stored using a logic 1 to represent a pending interrupt. Anti-repeat logic is provided to prevent multiple captures of the same interrupt.

1.3.2 MASK REGISTER (MK)

This 16-bit register is used to store the interrupt mask. Interrupts are masked by ANDing each mask bit with its corresponding PI register bit. Interrupts which are masked will be captured in the PI register but will not be acted on until unmasked. Interrupt level 0 can not be masked. A logic 0 in a given bit position indicates that the corresponding bit in the PI register will be masked.

1.3.3 PRIORITY ENCODER

This encoder generates an interrupt request to the CU whenever one or more unmasked interrupts are pending and enabled in the PI and encodes the highest priority unmasked pending interrupt as a 4-bit vector. This vector is read by the EU over the AD bus during interrupt servicing in order to create the interrupt Linkage and Service pointers.

1.3.4 FAULT REGISTER

This 16-bit register is used to capture and hold both internal and user implemented external faults. Faults are captured at the beginning of each machine cycle and are stored using positive logic, i e, a logic "1" represents a fault. Setting any one or more faults in FT will cause a level 1 (machine error) interrupt request. Once a fault is set in FT, it may only be cleared via an XIO command.

1.3.5 TIMERS A AND B

These are two 16-bit software controllable timers. Timer A is clocked by the TCLK input while Timer B is clocked by the internally generated TCLK/10. Timers A and B will generate interrupt levels 7 and 9, respectively, when their maximum counts of 65,536 are reached.

1.3.6 TRIGGER-GO COUNTER

This 16-bit counter is clocked by the TGCLK input, is enabled during system initialisation, and may be reset but not stopped by software action. It is stopped, however, upon overflow or by assertion of the DTIMERN input. Upon overflow, the TGON discrete output goes low and stays low until the counter is reset by software. This counter is typically used as a system "watchdog" timer.

1.3.7 XIO COMMAND DECODE LOGIC

This logic decodes all internally supported XIO commands and generates the control signals necessary to carry out the commanded action. An internal ready signal is generated upon command detection and is used by the EU state sequencer as previously discussed. Table 7b in Section 4.0 identifies the XIO commands which are internally supported by the MAS281.

1.3.8 MICROCODE CONTROL LOGIC

Decode logic, which translates microcode received from the CU into control signals, is used both by the MAS281 and by the external system.

2.0 INTERFACE SIGNALS

2.1 PIN ASSIGNMENTS

Figure 4 defines the pin assignment for the MAS281 module. See section 10.0 for full packaging and pin assignment information.

All signals - with the exception of power, ground and ROMONLYN - are TTL compatible. In addition, each function is provided with Electrostatic Discharge (ESD) protection circuitry. Figure 5 depicts a typical system implementation using many of these signals. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name, or by following the signal name with an "N" suffix, e.g., DDN. If a signal has a dual function, both function names will be used separated by a "/". The function name to the left of the "/" will be active high while the function to the right will be active low, again with an "N" suffix, e g., RD/WN.

2.2 PIN FUNCTIONS

A description of each pin function follows. The function name is presented first, followed by its acronym and description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Full timing characteristics of each of the functions are shown in section 6.0.

2.2.1 POWER AND GROUND (VDD & GND)

The MAS281 utilizes a single VDD power supply. A singlepoint ground is provided for the three chips on the substrate and is brought out on two module pins.

2.2.2 OSCILLATOR (OSC)

This input clocks the EU state sequencer which, in turn, generates timing and control signals for the rest of the module. To minimize skew between OSC edges and signals derived from OSC, and thereby optimize system performance, the OSC rise and fall times should be minimised. It is recommended that a clock driver with a high drive capability, such as a 54AS244, 54ALS244 or 54HST244, be used.

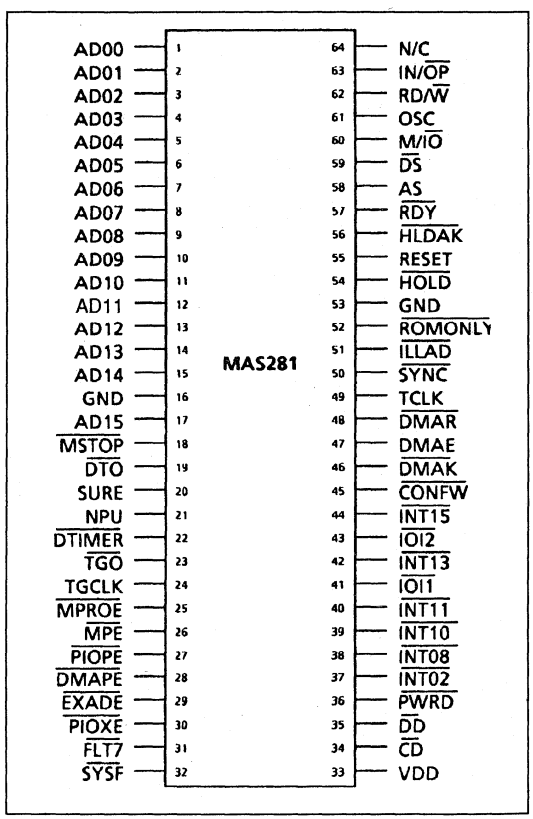


Figure 4: Pin Assignments

2.2.3 SYNCHRONIZATION CLOCK (SYNC)

This active low output transitions from high to low to signal the start of a new machine cycle. It should be used as a timing reference for those operations which must be synchronized to the basic machine cycle.

SYNCN cycles associated with external memory or I/O bus transactions are a minimum of five OSC periods in duration and may be extended by inserting wait states via the external ready interface, For such cycles, a SYNCN low indicates that either an address or XIO command is on the AD bus; a high indicates data is on the bus. Wait states extend the high state of SYNCN.

SYNCN cycles associated with internal CPU operations, are either five or six OSC periods in duration. Six OSC periods are required for machine cycles associated with microcode branches or with the execution of internally decoded XIO commands. Five OSC periods are required for all other internal operations.

[Note: For modules operating at high OSC frequencies, the internal ready logic provided on the IU may cause a wait state to be inserted during execution of internal XIO commands. This would result in a SYNCN cycle of seven OSC periods duration. Though unlikely, this condition must be taken into account in implementing an external ready interface. Refer to the description of the Ready (RDYN) signal below for further details.]

SYNCN continues to cycle during DMA and HOLD states. Such cycles are five OSC periods in duration.

2.2.4 ADDRESS STROBE (AS)

Output/Hi-Z. This active high signal indicates that an address has been placed on the AD bus. This address is guaranteed valid at the high to low transition of AS. AS should be used to strobe an address latch during AD bus demultiplexing. This latch should be a transparent type for optimum performance. AS is placed in the high impedance state during DMA and Hold cycles and is held low during internal (non-XIO) operations.

2.2.5 DATA STROBE (DS)

Output/Hi-Z. This active low signal indicates that the AD bus is being used for data transfers. During read operations, DSN should be used by the selected external device to enable data onto the AD bus. This data is guaranteed valid on the low to high transition of DSN. The selected external device should use the low to high edge of DSN to perform the write. DSN is placed in the high impedance state during DMA and Hold cycles and is held high during internal (nonXIO) operations.

2.2.6 READ/WRITE (RD/W)

Output/Hi-Z, This dual function signal indicates the direction of data flow on the AD bus. A high level indicates a read operation with data being input to the module. A low level indicates a write operation with data being output by the module. RD/WN may be combined with DSN to generate separate read and write strobes. This signal goes valid shortly

after SYNCN goes low to indicate the start of a new machine cycle and remains valid until a new SYNCN cycle is begun, RD/WN is placed in the high impedance state during DMA and Hold cycles.

2.2.7 MEMORY/INPUT-OUTPUT (M/IO)

Output/Hi-Z, This dual function signal indicates the type of transfer of the AD bus that is occurring. A high state identifies memory transfers. A low state identifies I/O transfers. M/ION goes valid shortly after SYNCN goes low to indicate the start of a new machine cycle and remains valid until a new SYNCN cycle is begun. M/ION is placed in the high impedance state during DMA and Hold cycles and is held high during internal (non-XIO) operations.

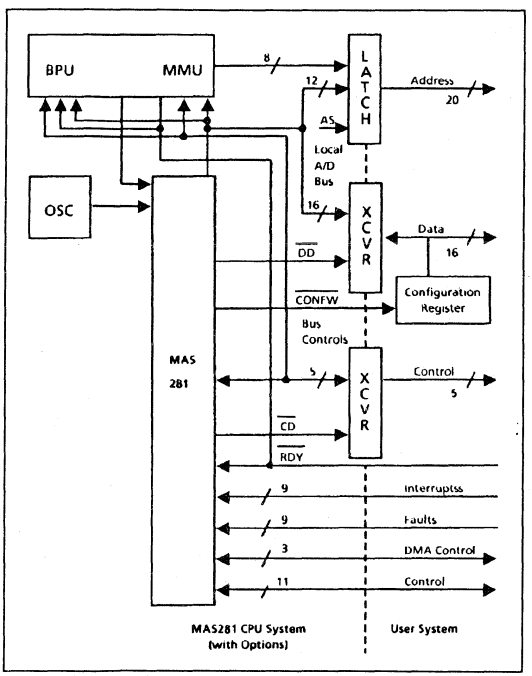


Figure 5: Typical MAS281/MA31751 System Interface

2.2.8 INSTRUCTION/OPERAND (IN/OP)

Output/Hi-Z. This dual function signal indicates the type of data on the AD bus during the data portion of a SYNCN cycle. A high state identifies an instruction while a low state identifies an operand. IN/OPN goes valid shortly after SYNCN goes low to indicate the start of a new SYNCN cycle and remains valid until a new SYNCN cycle is begun. This signal is required during expanded memory accesses. IN/OPN is placed in the high impedance state during DMA and Hold cycles.

2.2.9 ADDRESS/DATA BUS (AD00 - AD15)

Input/Output/Hi-Z. AD00 through AD15 comprise a bidirectional multiplexed address and data bus which serves both as the communication path between the external system and module as well as the communication path among the three chips on the module. It is important to note that the AD bus is shared between the external system and internal module resources. To avoid bus contention during internal operations, the AD bus must be isolated from the external system through the use of a bus transceiver. A data direction signal (DDN) is provided for transceiver control .

Addresses, data and commands appearing on the AD bus are represented in positive logic. A high level indicates a logic 1 and a low level indicates a logic 0. AD00 is the most significant bit position whilst AD15 is the least significant bit position. The AD bus is placed in the high impedance state during the data portion of a read SYNCN cycle as well as during DMA and Hold cycles.

2.2.10 READY (RDY)

This asynchronous active low input is used by the EU state sequencer, in conjunction with the internal ready signal, to determine when the current machine cycle may be completed. By holding RDYN high, wait states may be inserted, stretching out the current machine cycle and allowing slower devices sufficient time to complete their operations.

[Note: If RDYN is held high during two consecutive TCLK high-to-low transitions (with DSN low), a bus timeout fault will occur and will be indicated in the appropriate bit in the fault register. The occurrence of this fault will cause the EU state sequencer to terminate the current machine cycle, drop SYNCN low, and begin a new machine cycle. Also, the presently executing macroinstruction will be aborted and execution will branch, unless masked, to the machine error interrupt (level 1) software routine. The DTON signal may be used to override this feature.]

2.2.11 CONTROL DIRECTION (CD)

This active low output goes high to indicate the module is driving the AS, DSN, M/ION, RD/WN and IN/OPN signals. During DMA and Hold cycles, this signal goes low to indicate the module has relinquished control of these signals and has placed them in the high impedance state. The DMA or Console controller, respectively, may then drive these signals. This signal should be used to control the transfer direction of the control signal transceiver.

2.2.12 DATA DIRECTION (DD)

This active low signal indicates the direction of data transfer on the AD bus. This signal goes high to indicate a write transfer from the module to the external system. It also goes high during all internal module operations. DDN goes low to indicate a read transfer from the external system to the module. It also goes low during DMA and Hold cycles as well as during configuration register reads.

[Note: In addition to going high during the execution of internally implemented XIO commands, DDN also goes high

during execution of XIO commands which are implemented in the MA31751 MMU(BPU) chip.

If an MA31751 is used with the MAS281, it must reside on the MAS281 local AD bus rather than the system buses (see Figure 5). Table 7b in Section 4.0 identifies those XIO commands which are implemented in the MA31751].

2.2.13 DIRECT MEMORY ACCESS ENABLE (DMAE)

This active high output goes high in response to the DMAE XIO command. A high state indicates DMA requests will be acknowledged; a low state indicates a DMA request will be ignored.

2.2.14 DIRECT MEMORY ACCESS REQUEST (DMAR)

A low on this asynchronous active low input will cause the processor to suspend internal operations at the end of the current machine cycle. This request will only be acknowledged by the module when DMAE is high.

2.2.15 DIRECT MEMORY ACCESS ACKNOWLEDGE (DMAK)

This active low signal goes low in response to a DMA request if DMAE is high. A low state grants use of the system busses to the requesting DMA device by placing the module's AD bus, AS, DSN,RD/WN, M/ION and IN/OPN drivers into the high impedance state and by pulling CDN and DDN low. The high-to-low transition is synchronized to the falling edge of SYNCN to ensure that the current machine cycle is completed before the DMA device is granted the bus. DMAKN will remain low until the requesting device raises DMARN.

2.2.16 HOLD REQUEST (HOLD)

A low on this asynchronous active low input will cause the module to suspend internal processor functions at the end of the currently executing MIL-STD-1750A instruction. A Hold state is also entered if the processor encounters a breakpoint (BPT) instruction and the configuration word indicates the presence of a Console (bit 15 = 0).

[Note: Hold should be syncronised to the AS signal.]

2.2.17 HOLD ACKNOWLEDGE (HLDAK)

This active low output goes low either upon completion of the MIL-STD-1750A instruction during which HOLDN went low or if the processor encounters a breakpoint (BPT) instruction with Console present indicated in the configuration word register. A low on this signal indicates to the requesting device that that the module AD bus, AS, DSN, M/ION, RD/WN, and IN/OPN drivers have been placed in the high impedance state. The Hold state is terminated either by raising HOLDN high or, in the case of a BPT caused Hold, by pulsing HOLDN low and high again (see Section 6.0).

2.2.18 SYSTEM RESET (RESET)

This asynchronous active high input should be raised high to reset the module. The high-to-low transition of this input will start the module's initialization.

2.2.19 START-UP ROM ENABLE (SURE)

This active high output goes high during initialization and may also be asserted by software with the ESUR XIO command. This signal remains high until removed by software via the DSUR XIO command. When a Start-Up ROM is present, this signal should be used to qualify its chip select or output enable input such that the ROM may be accessed only when SURE is high.

[NOTE: Instruction pipelining must be considered in transitioning from Start-Up ROM to RAM when using the DSUR XIO command. If a system overlays RAM with the Start-Up ROM and transitions to execution from RAM by simply executing DSUR from the ROM, then IA will contain the value stored in the ROM location immediately following DSUR. This value will be treated as an instruction and the module will attempt to execute it. In such cases, it is recommended that DSUR be followed by an unconditional branch instruction with offset, i e, the BR instruction. An alternative approach is simply to jump to a portion of RAM not overlaid by the Start-Up ROM and execute DSUR from RAM.]

2.2.20 CONFIGURATION WORD (CONFW)

This active low output goes low when the module reads the external configuration register and should be used as that register's output enable strobe (see Section 6.0). Table 1 defines the required format of the configuration register. A zero in a given bit position indicates the specified device is present. Bits 0 through 11 are not used by the module.

The configuration register is read during initialization to determine the system configuration. It is also read whenever a (BPT) instruction is executed to determine the presence of a Console. If a console is not present, a BPT will be interpreted as a NOP. DDN goes low during a configuration register read. Thus, the configuration register must reside on the system AD bus rather than the local AD bus (see Figure 5).

2.2.21 NORMAL POWER UP (NPU)

This active high output is dropped low during module initialization as the first step of BIT. If BIT is successful, NPU goes high and remains high until reset by software via the RNS XIO command. NPU cannot be set high by software.

2.2.22 TIMER CLOCK (TCLK)

This clock input is used by interval timers A and B as well as the interface fault timer. Timer A is clocked at the TCLK frequency while timer B is clocked at a frequency of TCLK/10. MIL-STD-1750A requires that this input be a 100kHz pulse train.

Bit	Device
15	Console
14	MMU
13	BPU
12	Output Discrete Register
11-0	Unused

Table 1: Configuration Register Bit Assignment

2.2.23 TRIGGER-GO CLOCK (TGCLK)

This clock input is used by the internal 16-bit trigger-go counter. The trigger-go counter counts at the same frequency as TGCLK.

2.2.24 TRIGGER-GO DISCRETE (TGO)

This active low output goes low whenever the trigger-go counter overflows, i e., the counter rolls over to 0000. It returns to the high state when the trigger-go counter is reset by software via the GO XIO command.

2.2.25 DISABLE TIMER (DTIMER)

A low on this active low input disables timers A and B as well as the trigger-go counter. A low also disables DMA access by forcing DMAE low and DMAKN high. Raising DTIMERN allows timers A and B and the trigger-go counter to resume counting from the value at which they were stopped. A high also allows normal DMA operation.

2.2.26 DISABLE TIMEOUT (DTO)

A low on this active low input will reset and disable the bus fault timeout circuitry.

2.2.27 POWER DOWN INTERRUPT (PWRD)

A low on this active low input is captured in the PI register by a SYNCN high-to-low transition. This sets pending interrupt 0. This is the highest priority interrupt and cannot be masked or disabled.

2.2.28 USER INTERRUPTS (INT02,08,10,11,13 AND 15)

A low on any of these active low inputs will be captured in the PI register by a SYNCN high-to-low transition and will set pending interrupt levels 2, 8, 10, 11, 13, and 15, respectively. Level 2 is the highest priority user level while level 15 is the lowest priority. These interrupts are maskable and can be disabled. Unused inputs should be pulled up to VDD.

[NOTE: The INTO2 service routine should clear the PI Register using the RPI 0002 instruction.]

2.2.29 I/0 DEDICATED INTERRUPTS (IOI1 & IOI2)

A low on either IOI1N or IOI2N will be captured in the PI register by a SYNCN high-to-low transition and will set pending interrupt levels 12 and 14, respectively. Unused inputs should be pulled up to VDD.

[NOTE: Interrupt levels 1, 3, 4, 5, 6, 7, and 9 are dedicated to internal machine interrupts.]

2.2.30 MEMORY PROTECT ERROR (MPROE)

A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that an access fault, execute protect, or write protect violation has been detected. Bit O of the module Fault Register (FT) is set if this signal goes low during a memory cycle; bit 1 is set if it goes low during a DMA cycle. Either condition immediately sets pending interrupt level 1 and in the case of a memory cycle error, causes the currently executing MIL-STD-1750A instruction to be aborted.

Although the MAS281 aborts the macroinstruction, system memory management, and / or block protect hardware is responsible for preventing the erroneous bus cycle from accessing memory. To effectively use this feature, MPROEN should be pulled low prior to the high-to-low SYNCN transition of the next machine cycle. This can easily be accomplished by injecting wait states to hold off the DSN rising edge (write cycle) and the SYNCN falling edge (read cycle) until the system protection circuitry can decide whether or not to allow the transaction.

2.2.31 MEMORY PARITY ERROR (MPE)

A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a parity error has been detected during a memory transfer. Bit 2 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.32 PROGRAMMED I/O PARITY ERROR (PIOPE)

A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a parity error has been detected during an external I/O transfer. Bit 3 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.33 DMA PARITY ERROR (DMAPE)

A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a parity error has been detected during a DMA data transfer. Bit 4 of the module Fault Register (FT) is set when this signal goes low This, in turn, causes pending interrupt level 1 to be set.

2.2.34 EXTERNAL ADDRESS ERROR (EXADE)

A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a system address error has been detected. Bit 8 of the module Fault Register (FT) is set when this signal goes low during a

memory fault; bit 5 is set if it goes low during an I/O fault. As with MPROEN, either condition immediately sets pending interrupt level 1 and causes the currently executing MIL-STD-1750A instruction to be aborted .

2.2.35 PROGRAMMED I/O TRANSFER ERROR (PIOXE)

A low on this active low input, captured by the SYNCN high-to-low transition, is used to inform the module that a programmed I/O data transfer error has been detected. Bit 6 of the module Fault Register (FT) is set when this signal goes low. This, in turn, causes pending interrupt level 1 to be set.

2.2.36 FAULT #7 (FLT7)

A low on this active low input, captured by the SYNCN high-to-low transition, sets bit 7 of the Fault Register (FT). This is a user definable fault.

2.2.37 SYSTEM FAULT (SYSF)

A low on this active low input, captured by the SYNCN high-to-low transition, sets bits 13 and 15 of the Fault Register (FT). This is a user definable fault.

2.2.38 ILLEGAL ADDRESS (ILLAD)

This active low output drops low if the EXADEN input drops low or if the bus fault timeout circuit causes an interface timeout.

2.2.39 MICROCODE STOP (MSTOP)

MSTOPN allows microcode to be single-stepped and is reserved for use by GEC Plessey Semiconductors. MSTOPN must be pulled up to VDD in customer applications.

2.2.40 ROM ONLY (ROMONLY)

ROMONLYN is used for testing by GEC Plessey Semiconductors and must be pulled up to VDD in customer applications.

3.0 OPERATING MODES

MAS281 operating modes include: (1) initialisation, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) DMA support, (6) Hold support, and (7) timer operations.

3.1 INITIALISATION

The module executes a microcoded initialisation routine in response to a hardware reset. This routine clears module registers, disables and masks interrupts, reads the configuration register, resets the output discrete register (if implemented), initialises the MMU and BPU (if implemented), performs Built-In-Test (BIT), raises the Start-Up ROM enable discrete, clears and starts timers A and B, resets the trigger-go counter, and loads the instruction pipeline. Table 2 summarises the resulting initialisation state, and Table 3 provides a detailed breakdown of the initialisation sequence.

BIT consists of five subroutines, as outlined in table 4, and begins by pulling NPU low. This is the first time after reset that NPU is guaranteed low. If all five subroutines execute successfully, NPU is raised high. If any part of BIT fails, an error code identifying the failed subroutine is loaded into the Fault Register (FT), BIT is aborted, and NPU is left in the low state. Table 4 defines the coding of BIT results in FT. In the event of such a failure, the resulting module reset state will be dependent on where in BIT the error occurred and may not be the same as that shown in Table 2. A BIT failure indication in FT will set the level 1 interrupt request bit of the Pending Interrupt (PI) register. Since initialisation disables and masks interrupts, this interrupt request will not be asserted .

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero and will be from the Start-Up ROM if implemented. Whether BIT passes or not, the processor will begin instruction execution at this point.The system start-up code may include a routine to enable and unmask interrupts in order to detect and respond to a BIT failure.

[NOTE: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, timers A and B must be clocked during this interval, i.e., TCLK must be applied.]

MAS281	
Instruction Counter (IC)	Zeroed
Status Word (EU and MMU) (SW)	Zeroed
Fault (FT)	Zeroed
Pending Interrupt (PI)	Zeroed
Mask (MK)	Zeroed
Interrupts	Disabled
DMA Access	Disabled
Timer A	Reset and Started
Timer B	Reset and Started
Trigger-Go Timer	Reset and Started
MMU	
Page Registers	Group 0 Enabled
AL, W, E Fields	Zeroed
PPA Field	Logical to Physical Map
BPU	
Write Protect	Zeroed
Global Memory Protect	Enabled

Table 2: Initialisation State

Label	Cycle	
MAIN	B 1	1. Enable Control of DMAE Output signal
	P	2. -
	B1	3. Clear MAS281 Execution Unit Status Word (SW) Clear Interrupt Mask (MK) (Internal I/O command, SKM 2000H)
	B1	4. Clear Pending Interrupt Register (PI) and Fault Register (FT) (Internal I/O Command, CLIR,2001 H) Clear Instruction Counter (IC)
	P	5. -
	B1	6. Disable Interrupts (Internal I/O Command, DSBL,2003H)
	P	7. -
	B1	8. Clear MMU Status Word (Internal I/O Command, WSW, 200EH) (Note 1)
	P	9. -
	B1	10. Disable DMA Access (Internal I/O Command, DMAD, 4007H)
	P	11. -
	B1	12. Read Configuration Register (Internal I/O Command, RCW, 8400H, CONFWN Drops low per Figure 25, Section 5.0)
	P	13. -
	P	14. -
	B2	15. - (If Output Discrete Register Present, then Continue; Else, Skip to 18.)
	P	(16). -
	I/O	(17). Clear Output Discrete Register (External I/O Command)
	P	18. -
	B2	19. - (If BPU present, then Branch to BPU; else, continue)
	P	20. -
	B2	21. - (If MMU present, then Branch to MMU, Else, Continue)
	P	22. - (Setup Temporary Register to indicate No MMU Present)
	B2	23. - (Branch to MAS281 BIT)
	P	24. -
	B1	25 Enable Start-Up ROM (Internal I/O Command, ESUR,4004H; SURE Raises High per Figure 25, Section 5.0)
	P	26. -
	B1	27. Clear and Start Timer A (Internal I/O Command, OTA,400AH)
	B1	28. Reset the Trigger-Go timer (mternal I/O Command, GO,400BH)
	P	29. -
	B1	30. Clear and Start Timer B (Internal I/O Command, OTB,400EH)
	B2	31. - (Branch to Load Instruction Pipeline Routine)
	M	32. Load data-In register (DI) and instruction Register A (IA) from [IC] Increment IC
	M	33. Load Data-In Register (DI) and Instruction Register a (IA) from [IC] ([IA] Moves to IB), Increment IC, Map Instruction Register B (IB) into MIcrocode Routine
BPU	P	(1). -
	P	(2). - (Set Loop to Clear Memory Protect RAM)
	I/O	(3). Clear a Location in MPRAM (Internal I/O Command, LMP,50XXH), Increment Address, Do 128 Times
		(4). - (Branch Back to 20)
MMU	P	(1). -
	P	(2). -
	P	(3). - (Setup Loop to Load Instructlon Page Registers (IPR) and Operand Page Registers (OPR) with Sequential Values of 0 to 255)
	P	(4). -
	P	(5). -
	I/O	(6). Load a Location in the IPR wlth the value of the Location Address (Internal I/O Command, WIPR, 51 XYH)
	I/O	(7). Load a Location in the OPR Increment Loaded Value with the Value of the Location Address (Internal I/O Command. WOPR,52XYH)
	P	(8). - (Increment IPR Address)
	P	(9). - (Increment OPR Address- Repeat Loop 14 - 9 1256 Times)
	B2	(10). - (Setup Temporary Register to Indlcate MMU Present; Branch back to 23)

Notes:

1. This operation is performed whether or not an MMU is present.
2. "-" indicates internal CPU operation
3. Sequence numbers in "( )" are performed only under the stated conditions.
4. Each step enumerated above represents a single machine (SYNC) cycle of the type shown in the "Cycle" column.
   "P" indicates a 5 OSC cycle,60% duty cycle, machine cycle.
   "I/O" and "M" Indicate a 5 OSC cycle,50% duty cycle, machine cycle.
   "B1" indicates a 6 OSC cycle 50% duty cycle machine cycle.
   "B2" indicates a 6 OSC cycle 66% duty cycle machine cycle

Table 3: MAS281 Initialisation Sequence

3.2 INSTRUCTION EXECUTION

Once initialisation has been completed, the module will begin instruction execution. Instruction execution is characterised by a variety of operations, each one or more machine cycles in duration. Depending on the instruction being executed at the time, these operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by DMA operations and at the conclusion of any given instruction by an interrupt or Hold request.

3.2.1 INTERNAL CPU CYCLES

Internal CPU cycles are used to perform all CPU data manipulation and housekeeping operations. Internal CPU cycles are either five or six oscillator periods in duration and are characterised by AS low and DSN, DDN and M/ION high. Section 6.0 provides timing characteristics for internal CPU cycles. Tables 7a and 7b in Section 4.0 provide machine cycle counts (both the five and the six OSC cycle variety) associated with each MIL-STD-1750A instruction.

3.2.2 INSTRUCTION FETCHES

Instruction Fetches are used to keep the instruction pipeline full. This ensures that the next instruction is always ready for execution when the preceding instruction is completed. During jump and branch instruction execution, the pipeline is flushed, and then it is refilled via two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of interrupt and hold request processing.

Instruction fetches are characterised by IN/OPN high but are otherwise identical to an operand read transfer. For a detailed explanation of the function of various bus control signals during instruction fetches, refer to the discussion of operand transfers below. Section 6.0 provides timing characteristics for instruction fetches. Machine cycles associated with instruction fetches are a minimum of five oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts included in Table 7a of Section 4.0 include instruction fetches.

Instruction fetches use instruction pipeline registers IA and IB, the instruction counter (IC), and the data input register (DI) and proceed as follows: assuming an empty instruction pipeline (occurring as a result of a reset, jump, or branch), the contents of IC are placed on the AD bus as an address. The returned value, which will be an instruction, is stored in the IA register.

The value in IC is incremented (via its dedicated counter) and the next fetch is performed. This second returned value, which may be either an instruction or an immediate operand, is stored in both the IA and DI registers. The instruction previously stored in IA is advanced to IB to be executed.

The instruction in IB is checked to determine if an immediate operand is required. If so, that operand has already been pre-fetched and resides in both IA and DI. If not, then the value currently in IA is an instruction. If IA contains an operand, another instruction fetch is performed and the returned value is stored only in IA (the contents of IB and DI are preserved). If IA contains an instruction, however, the next fetch is deferred until the contents of IB are no longer needed. At that time, the deferred fetch is performed, IA is advanced to IB for execution, and the newly returned value is stored in both IA and DI.

This sequence repeats until the instruction pipeline is again emptied at which time the whole process is repeated .

3.2.3 OPERAND TRANSFERS

Operand transfers are used to obtain (read in) operands to be used by an instruction and to save (write out) any results of an instruction's execution. Section 6.0 provides timing characteristics for operand transfers. Machine cycles associated with operand transfers are a minimum of five oscillator periods in duration. The RDYN signal may be used to insert wait states to accommodate slow memory. Machine cycle counts in Table 7a of Section 4.0 include operand transfers.

Operand transfers use the address register (A), the data input register (DI), and data output register (DO). Before the operand transfer begins, the processor calculates the effective operand address and stores this value in A. For write transfers, the processor loads the operand into the DO register.

All operand transfers between the module and memory are referenced to the AS and DSN bus control signals and are characterised by IN/OPN low and, by M/ION and CDN high. The transfer begins by placing the contents of A (the address register) on the AD bus immediately following the SYNCN high-to-low transition. The AS strobe then goes high to enable the system's transparent address latch. The address is assured valid on the high-to-low transition of AS. The DDN signal is high during the address portion of the transfer; its subsequent action depends on whether the transfer is a read or write.The RDWN signal indicates the direction of the transfer. If the operand is a write, the address from A is replaced by the operand in DO when SYNCN transitions from low-to-high. Next, the DSN signal goes low and can be used by the memory system to generate a write enable. Data is guaranteed valid at the low-to-high transition of DSN. DDN stays high for the duration of a write transfer. The memory system must pull RDYN low to conclude the transfer.

If the operand transfer is a read, the AD bus drivers are placed in a high impedance state at the low-to-high transition of SYNCN to give the memory system access to the bus. Next, the DSN signal goes low and can be used by the memory system to generate an output enable. Shortly after DSN goes low, DDN also goes low. This should be used by the system to reverse the direction of the system's AD bus transceivers. The memory system must pull RDYN low to conclude the transfer. Data will be read into the DI register on the SYNCN high-to-low transition 3.2.4 Input/Output Transfers

Input/Output transfers utilize the MIL-STD-1750A XIO and VIO protocols and are characterized by M/ION and IN/OPN low and CDN high. RD/WN defines the direction of the transfer. AS and DSN cycle as with operand transfer operations. The procedure followed depends on whether the transfer is associated with one of the internally implemented XIO commands or an externally implemented capability. An exception is the Read Configuration Word (RCW) command

which is decoded by the MAS281 but is treated, in some ways, like an externally implemented XIO command. This exception is discussed below.

Internal I/O transfers involve all XIO commands which are decoded internally either by the MAS281 or by the MA31751 MMU/BPU chip (with the exception noted above). Table 7b identifies these commands. The A, DI and DO registers are used as in operand transfers. Internal I/O transfers are characterised by DDN staying high for the duration of the transfer in order to prevent bus contention between the module AD bus and the system bus. Machine cycle associated with internal I/O commands are normally six oscillator cycles in duration but might be extended to seven OSC cycles by the internal ready interface if the module is run at high frequencies. Internal I/O transfers may be subdivided into writes, reads and commands as follows:

I/O writes consist of a command phase followed by the value to be written. The command is placed on the AD bus from the A register at the SYNCN high-to-low transition and is assured valid on the high-to-low transition of AS. The value to be written is placed on the AD bus from the DO register at the SYNCN low-to-high transition and is written to the internal I/O device by the subsequent SYNCN high-to-low transition. An example of an internal I/O write is loading timer A.

I/O reads consist of a command phase followed by the value returned by the internal device. The command is placed on the AD bus from the A register at the SYNCN high-to-low transition and is assured valid on the highto-low transition of AS. The internal I/O device places the value to be read on the AD bus at the SYNCN low-tohigh transition. This value is captured by the DI register on the subsequent SYNCN high-to-low transition. An example of such an operation is reading the interrupt mask register.

I/O commands consist of a command phase alone. The command is placed on the AD bus from the A register at the SYNCN high-to-low transition and is executed at the following SYNCN high-to-low transition. An example of an I/O command is raising the DMAE discrete.

External I/O transfers are similar to internal I/O transfers with the following exceptions: (1) DDN goes low, as with operand transfers, during an I/O read; and (2) external I/O machine cycles are normally five OSC cycles in duration and may be extended via the RDYN signal as with operand transfers.

As discussed earlier, the Read Configuration Word command is a special case. It is decoded internally to generate a read strobe (CONFWN) and therefore uses both the standard internal I/O six OSC period machine cycle as well as the internal ready interface to extend its cycle. It relies on an externally implemented configuration register, however, and therefore cycles DDN as with external I/O cycles. Therefore, the configuration word register must reside on the system side of the data bus transceivers as opposed to residing directly on the local AD bus (as shown in Figure 5).

Nine user interrupt request inputs are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the high-to-low transition of SYNCN and latched into the Pending Interrupt (PI)

BIT	Test Coverage	BIT Fail Codes (FT 13,14,15)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	220
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	165
3	Interrupt Unit- MK, PI, FT Enable/Disable Interrupts	111	216
4	Status Word Control User Flags General Registers (R0 - R15)	110	155
5	Timer A Timer B	111	775
-	BIT Pass/Fail Overhead	-	25

Note: BIT pass is indicated by all zeros in FT bits 13,14, and 15.

Table 4: Built-in Test Coverage and Tuning

register on the following SYNC high-to-low transition (with the exception of INT02N which is latched into PI when INT02N is first detected). This sequence occurs whether interrupts are enabled or disabled or whether the specific interrupt is masked or unmasked.

Each external PI register input is buffered by a falling edge detector to prevent repeat latching of requests held low beyond the first SYNCN high-to-low transition. An interrupt request input must transition to the high state before a subsequent request on that input will be detected.

When an interrupt request is latched into PI, it is ANDed with its corresponding mask bit in the mask register (MK). Interrupt level 0 is not maskable. Any unmasked pending interrupts are output to the priority encoder where the highest priority is encoded as a 4-bit vector. If interrupts are enabled, and an unmasked interrupt is pending, the priority encoder will assert an interrupt request to the CU.

Upon completing execution of a given MIL-STD-1750A instruction, the CU's microsequencer checks the state of the priority encoder's interrupt request. If an interrupt request is asserted, the microsequencer branches to the microcode interrupt service routine. This routine performs a read of the priority encoder's 4-bit pending interrupt vector, stores the value in the EU DI register, and then uses this value to calculate the appropriate interrupt linkage and service pointers. The pointers serve as addresses to data structures used in servicing interrupts. Figure 6 depicts this relationship. Table 5 defines pointer values.

Using the linkage and service pointers, the microcode interrupt service routine performs the following: (1) the current contents of the status word, mask register, and instruction counter are saved; (2) a write status word I/O command is executed with an all zero data word; (3) the new mask is loaded into MK and interrupts are disabled; (4) the new status word is read and checked for a valid AS field - If AS is non-zero and an MMU is not present, AS is set to zero and fault 11 (address state error) is set in the fault register FT; (5) a write status word command using the new status word is performed; and (6) the new IC value is loaded into IC, the instruction pipeline is filled starting at the new address, and instruction execution begins.

[NOTE: The steps listed above represent a summary of actions performed during interrupt servicing and do not necessarily reflect the actual order in which these events take place.]

If an interrupt is latched during the interrupt service routine, it will not be processed until interrupts are re-enabled. If an AS fault occurs during the service routine, interrupt level 1 will be set. This interrupt will be serviced when interrupts are re-enabled unless it is masked by the new value in MK.

3.4 FAULT SERVICING

Eight user fault inputs are provided. A low on any of these inputs will be latched into the Fault Register (FT) at the high-to-low transition of SYNCN.

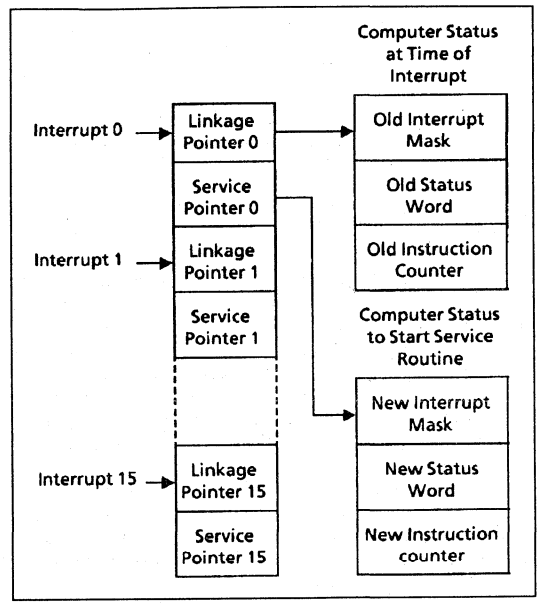


Figure 6: Interrupt Vectoring

	Interrupt	LP Address	SP Address
PWRD	0	20	21
	1	22	23
INT02	2	24	25
	3	26	27
	4	28	29
	5	2A	2B
	6	2C	2D
	7	2E	2 F
INT08	8	30	31
	9	32	33
INT10	10	34	35
INT11	11	36	37
IOI1	12	38	39
INT13	13	3A	3B
IOI2	14	3C	3D
INT15	15	3E	3F

Table 5: Interrupt Pointer Definitions

No falling edge detectors are provided to prevent repeat latching of faults held low beyond the first SYNCN high-to-low transition. However, all FT bits are ORed together and input to the PI bit 1 through an edge detector to prevent the fault register from causing multiple level 1 interrupts.

The sequence of events following a fault capture depends on the type of fault as follows:

3.4.1 MPEN, PIOPEN, DMAPEN, PIOXEN, FLT7N, AND SYSFN

The capture of one or more of these faults immediately sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT. The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the service interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit.

When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting bit(s). Therefore, a level 1 interrupt would be latched again if there was no anti-repeat logic to prevent a never-ending loop of interrupts.

During the SYNCN cycles between fault capture and the beginning of the microcode interrupt handling routine, AS and DSN are forced to their inactive states. In the case of MPROEN, which may reflect an attempted write violation, it is required that system hardware provide the additional protection necessary to inhibit memory write strobe.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the RCFR internal I/O command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the internal I/O command RFR, but this command should be used carefully.

3.4.2 MPROEN, EXADEN, AND BUS FAULT TIME-OUT

The capture of one or more of these faults immediately sets pending interrupt level 1 (machine error) of the Pending Interrupt (PI) register. Furthermore, the instruction currently executing is aborted at the SYNCN high-to-low transition following the SYNCN high-to-low transition that latched the fault. The IC value saved in the interrupt linkage table for the level 1 interrupt always points to the instruction which was in instruction pipeline register IA at the time of the abort. Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT.

The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit. When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting fault bit(s). Therefore, a level 1 interrupt would be latched again if there were no anti-repeat logic to prevent a never-ending loop of interrupts from occurring .

3.5 DMASUPPORT

DMA data transfers are performed under the control of a system DMA controller over the system AD bus. The user signals that DMA requests will be honored by setting the DMAE output high via the DMAE internal XIO command. The DMA controller may request use of the AD bus by pulling the module's DMARN input low.

Unless the DMAE output is high, all such requests will be ignored. If DMAE is high, DMARN will be acknowledged by DMAKN dropping low. This occurs at the first SYNCN high-to-low transition after DMARN goes low.

DMAKN low indicates that the module has relinquished control of the AD bus by placing its AD bus, AS, DSN, M/ION, RD/WN and IN/OPN drivers in their high impedance state. DDN is dropped low to direct the system data bus transceivers to drive the local AD bus and CDN is dropped low to disable the control signal buffers. The DMA controller relinquishes control of the AD bus by raising DMARN high. The module responds by raising DMAKN high at the next SYNCN high-to-low transition and continuing with program execution.

3.6 HOLD SUPPORT

The Hold state is provided to facilitate debugging of user software by allowing the user to disable the MAS281 and access system resources. Hold state timings is defined in Section 6.0. The Hold state can be entered either by pulling HOLDN low or by executing a BPT instruction with the Console present and indicated in the Configuration Word. These two approaches, as well as methods for using the Hold state to single step through software, are discussed below:

3.6.1 USING HOLDN

At the completion of the currently executing instruction, the microsequencer checks the state of the HOLDN input. If low, the microsequencer branches to the microcode Hold service routine. This routine decrements IC twice, enables the Hold termination sequence, drops HLDAKN low, and enters the Hold state. HLDAKN drops low three SYNCN cycles after the final SYNCN cycle of the currently executing instruction. A low on HLDAKN indicates that the module has relinquished the AD bus by placing its AD bus, AS, DSN, M/ION, RD/WN and IN/OPN drivers into the high impedance state and, DDN and CDN drop low.

When HOLDN is returned high, the Hold state will end on the subsequent high-to-low transition of SYNCN. This is signified by raising HLDAKN, at which point thc module resumes control of the AD bus, AS, DSN, M/ION, RD/WN and IN/OPN signals. CDN and DDN raise high.Thc instruction pipeline is then refilled and instruction execution resumes with the first instruction loaded into the pipeline

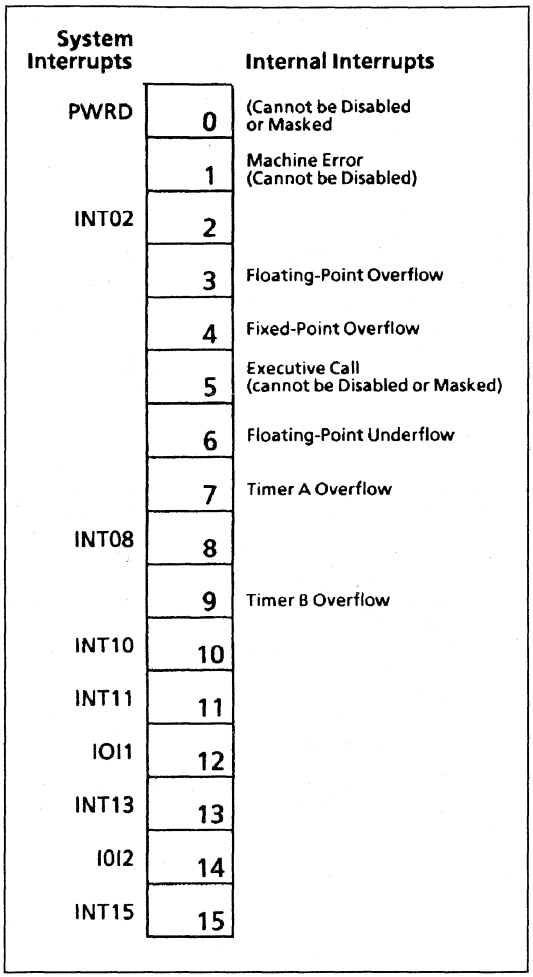


Figure 7: Pending Interrupt Register Bit Assignments

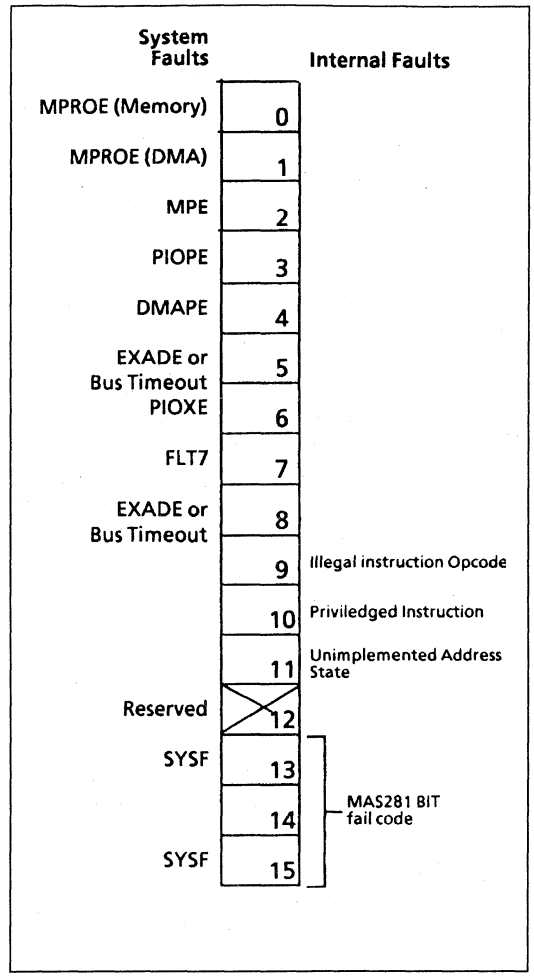


Figure 8: Fault Register Bit Assignments

3.6.2 USING BPT

The Hold state may also be entered by executing a BPT instruction with Console present indicated in the Configuration Word. On encountering a BPT instruction, the processor reads the Configuration Word to check for the presence of a Console. If a Console is indicated, the microsequencer branches to the microcode BPT Hold service routine. This routine decrements IC once, drops HLDAKN low, and enters the Hold state.

To release the MAS281 from a BPT initiated Hold state, the HOLDN input must be pulsed low in accordance with the timing diagrams in Section 6.0. When HOLDN returns high, the Hold state will be released on the following SYNCN high-to-low transition. The instruction pipeline is then refilled and instruction execution resumes with the first instruction loaded into the pipeline.

3.6.3 SINGLE-STEPPING

Software can be single-stepped through the proper use of the HOLDN input and the BPT instruction. Use the BPT instruction to mark the beginning of the section of code which will be stepped through. Pulse HOLDN low to release the BPT initiated Hold state and then pull HOLDN low again during the two subsequent SYNCN cycles that refill the instruction pipeline. When the first instruction following Hold release completes execution, the module will once again enter the

Hold state. Again pulling HOLDN will cause the next instruction to execute. This process may be repeated as long as required. Raising HOLDN high will resume normal operation.

3.7 TIMER OPERATIONS

The MAS281 implements interval timers A and B, a trigger-go counter, and a bus fault timer. A discussion of each follows:

3.7.1 TIMERS A AND B

Timer A is clocked by the TCLK input; timer B is clocked by an internally generated TCLK/10. MIL-STD-1750A requires TCLK to be a 100-kHz pulse train. If allowed to overflow, timers A and B will set level 7 and level 9 interrupt requests, respectively. Timing characteristics of each timer are defined in Section 5.0. Either timer can be read, loaded, started, and stopped through the use of internally decoded XIO commands.

These commands are identified in Table 7b in Section 4.0. By asserting the DTIMERN input, both timers will halt and all internally decoded XIO commands which would change their state are disabled (asserting DTIMERN also disables DMA accesses by driving DMAE low and DMAKN high). Raising DTIMERN allows the timers to resume counting from their suspended state and allows timer commands to function normally (DMA control lines are again allowed to change).

A feature of the MAS281 timers is the choice of disabling, or not disabling, the interval timers A and B upon execution of a BPT software instruction when a Console is connected. If full compliance with MIL-STD-1750 (Notice 1) is desired, the halting of timers A and B can be accomplished by pulling DTIMERN low upon execution of a BPT instruction with a Console connected. Two suggested ways to do this are: (1) connect HLDAKN to DTIMERN through an AND gate; or (2) allow the system Console to pull DTIMERN low upon receiving HLDAKN low. The first option provides a faster response and is a less complicated method, whereas the second choice allows the option of halting timers A and B, or not halting them.

[NOTE: As described in Section 2.2, DTIMERN low suspends the trigger-go timer and disables DMA access (forces DMAE low and DMAKN high) in addition to halting timers A and B].

3.7.2 TRIGGER-GO COUNTER

The trigger-go counter is clocked by the TGCLK input. Timing characteristics for trigger-go counter operation are defined in Section 6 0. DTIMERN disables and enables operation in the same manner as with timers A and B. Whenever the trigger-go counter overflows, TGON drops low and remains low until the counter is reset via the GO internal XIO command.

3.7.3 BUS FAULT TIMER

All bus operations are monitored to ensure timely completion. A hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition) and is reset upon receipt of the external ready (RDYN) signal.

If this circuit fails to reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 8 (if the transaction is with memory) or bit 5 (if the transaction is with I/O) of the Fault Register (FT) is set. This sets pending interrupt level 1 and causes the current bus cycle to be terminated by forcing SYNCN low. The MIL-STD-1750A instruction is aborted, and control passes to the level 1 interrupt service routine (if the level 1 interrupt is unmasked). This feature is disabled by pulling DTON low.

4. SOFTWARE CONSIDERATIONS

The MAS281 implements the full MIL-STD-1750A instruction set. Table 7a lists the instruction set and provides performance data for each instruction. Table 7b provides a summary of the XIO commands which are internally decoded on the module. Resources available to the software programmer are depicted in Figure 9. A discussion of data types, addressing modes and benchmarking considerations follows.

4.1 DATA TYPES

The MAS281 fully supports 16-bit fixed-point single precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended precision floating point data types. Figure 10 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. All floating-point operands are expected to be normalized. If not normalized, the results from an instruction are not defined.

4.2 ADDRESSING MODES

The MAS281 supports the eight addressing modes specified in MIL-STD-1750A. These addressing modes are depicted in Figure 11 and are defined below.

4.2.1 REGISTER DIRECT (R)

The register specified by the instruction contains the required operand.

4.2.2 MEMORY DIRECT (D,DX)

Memory Direct (without indexing) is an addressing mode in which the instruction contains the memory address of the required operand. In Memory Direct-Indexed (DX), the memory address of the required operand is specified by the sum of the contents of an index register (RX) and the instruction address field (A). Register R1 through R15 may be specified for indexing.

4.2.3 MEMORY INDIRECT (I, IX)

Memory Indirect (without indexing) is an addressing mode in which the memory address specified by the instruction contains the address of the required operand. In Memory Indirect with Pre-Indexing (IX), the sum of the contents of a specified index register and the instruction address field in the address that contains the address of the required operand. Registers R1 through R15 may be specified for pre-indexing.

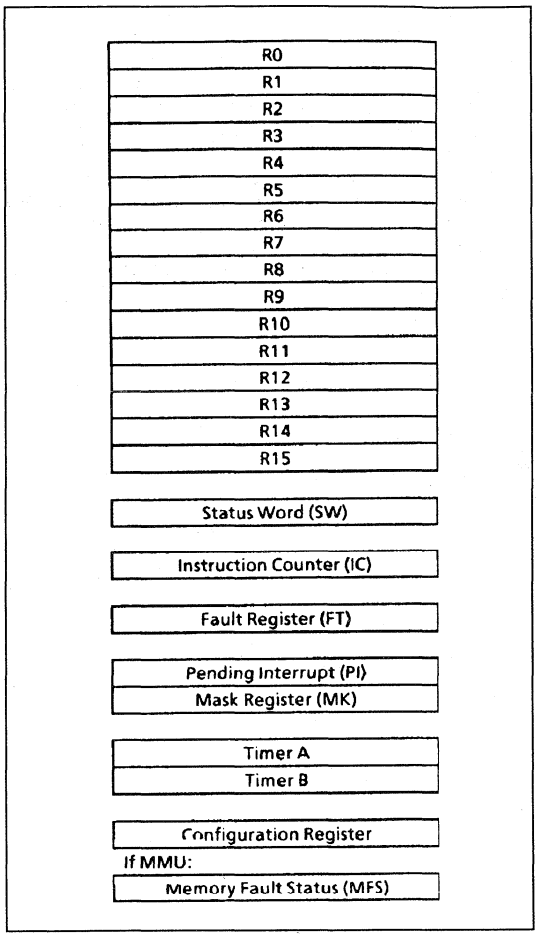


Figure 9: Register Set Model

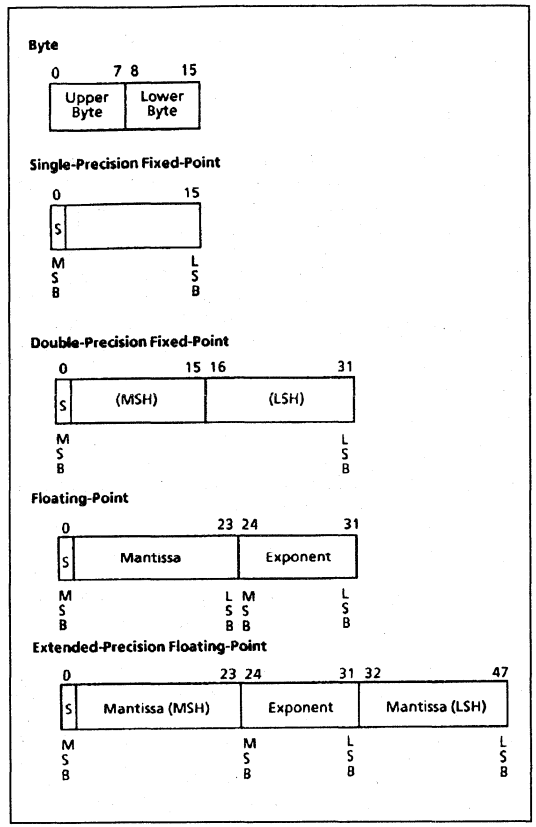


Figure 10: Data Formats

4.2.4 IMMEDIATE LONG (IM, IMX)

There are two formats which implement Immediate Long Addressing; one allows indexing and one does not. For the indexable form, if the specified index register, RX, is not equal to zero, the contents of RX are added to the immediate field to form the required operand; otherwise, the immediate field contains the required operand.

4.2.5 IMMEDIATE SHORT (IS)

In this mode the required 4-bit operand is contained within the 16-bit instruction. The Immediate Short addressing mode accommodates two formats; one which interprets the contents of the immediate field as positive data and the other which interprets the contents of the immediate field as a negative data.

4.2.5.1 IMMEDIATE SHORT POSITIVE (ISP)

The immediate operand is treated as a positive integer between 1 and 16.

4.2.5.2 IMMEDIATE SHORT NEGATIVE (ISN)

The immediate operand is treated as a negative integer between -1 and -16. Its internal form is a two's complement, sign-extended 16-bit number.

4.2.6 INSTRUCTION COUNTER RELATIVE (ICR)

This addressing mode is used for 16-bit branch instructions. The contents of the instruction counter minus two (the address of the current instruction) is added to the sign-

extended 8-bit displacement field within the instruction. This sum then points to the memory address to which control will be transferred if the branch is taken.

4.2.7 BASE RELATIVE (B)

There are two formats which implement Base Relative Addressing; one allows indexing and one does not. For the non-indexable form, the contents of the instruction specified base register (BR = BR' + 12) is added to the 8-bit displacement field (DU) of the 16-bit instruction. For the indexable form, the sum of the contents of a specified index register and a specified base register is the address of the required operand. Registers R1 through R15 may be specified for indexing. Registers R12 through R15 may be specified as the base register.

4.2.8 SPECIAL

This addressing mode is applicable to instructions that do not follow the above formats. The instructions that use this special mode are indicated in Table 7a.

4.3 BENCHMARKING

Table 7a defines the number and type of machine cycles associated with each MIL-STD-1750A instruction. This information may be used when benchmarking MAS281 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix, however, is that it does not reflect the impact of data dependencies on system performance. For example, a multiplication in which an operand is zero may be performed much faster than one with two non-zero operands. Also, the DAIS mix does not specify such time consuming operations as normalization and alignment.

Realistic benchmarks must therefore take both the instruction mix and data dependencies into account. To this end, machine cycle counts in Table 7a which have data dependencies, are annotated with either an "a" or "wa"suffix.

An "a" suffix reflects an average number of machine cycles (where each of several possibilities is equally likely) and a ""wa" suffix reflects a weighted average number of machine cycles (where some data possibilities are more likely than others).

Weighted averages are only applicable to floating-point operations. Weighted averages provided in Table 7a are based on the Sweeney (IBM) guidelines. These guidelines take a wide range of data dependencies into consideration. Normalization and alignment operations are also represented. Table 6 defines MAS281 throughput, at various frequencies and wait states, for the DAIS mix using Sweeney data dependencies.

It should be noted that using the Sweeney guidelines is a conservative approach to benchmarking. If best case assumptions are made and such operations as normalization and alignment are not considered, MAS281 performance figures are approximately 50% higher than those indicated in Table 6.

f_{osc} MHz	0	1	2	3
25	743.4	698.3	658.4	622.8
20	594.7	558.7	526.7	498.2
15	446.0	419.0	395.0	373.7
10	297.4	279.3	263.4	249.1

Number of Wait States in Memory Access Cycle

Table 6: Throughput (KIPS)

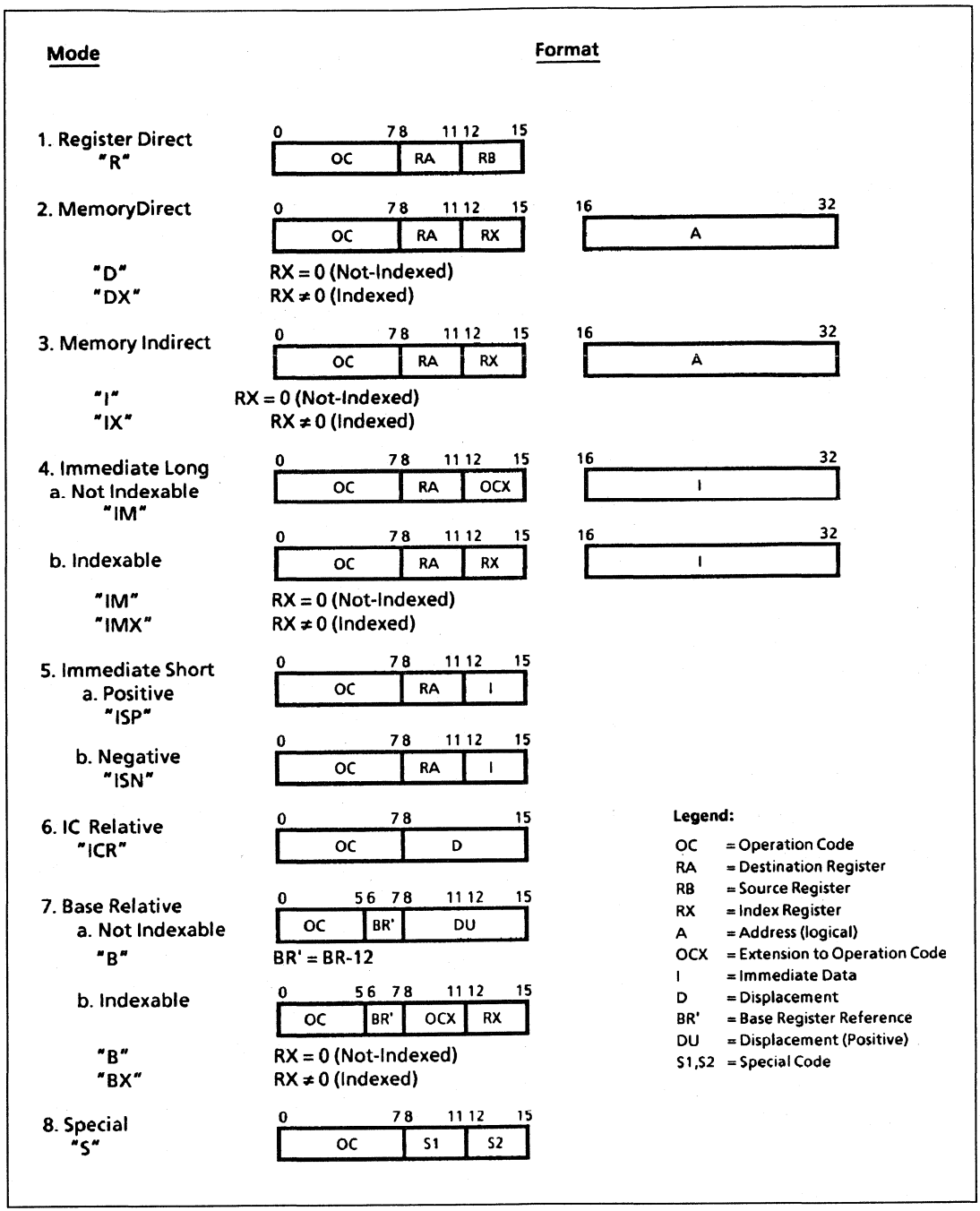


Figure 11: Addressing Modes

4.4 INSTRUCTION SUMMARY

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
LOAD/STORE						
Single Precision Load	81	LR	R	1	0	0
	0X	LB	B	2	1	0
	4X 0	LBX	BX	2	1	0
	82	LISP	ISP	1	0	0
	83	LISN	ISN	1	0	0
	80	L	D, DX	3	0	0
	85	LIM	IM,IMX	2	0	0
	84	LI	I,IX	4	1	0
Double-Precision Load	87	DLR	R	1	2	0
	0X	DLB	B	3	1	0
	4X 1	DLBX	BX	3	2	0
	86	DL	D, DX	4	0	0
	88	DLI	I,IX	5	1	0
Single-Precision Store	0X	STB	B	2	2	0
	4X 2	STBX	BX	2	2	0
	90	ST	D, DX	3	1	0
	94	STI	I, IX	4	1	0
Store a Non-Negative Constant	91	STC	D,DX	3	1	0
	92	STCI	I, IX	4	1	0
Double-Precision Store	0X	DSTB	B	3	2	0
	4X 3	DSTX	BX	3	2	0
	96	DST	D DX	4	0	0
	98	DSTI	I, IX	5	1	0
Load Multiple Registers	89	LM	D,DX	3+n	1	1
Store Multiple Registers	99	STM	D,DX	3+n	1	1
INTEGER ARITHMETIC						
Single-Precision Integer Add	A1	AR	R	1	1	0
	1 X	AB	B	2	2	0
	4X 4	ABX	BX	2	2	0
	A2	AISP	ISP	1	1	0
	A0	A	D, DX	3	1	0
	4A 1	AIM	IM	2	1	0
Increment Memory by a Positive Integer	A3	INCM	D,DX	4	1	0
Single-Precision Absolute Value of Register	A4	ABS	R	1	1.5	1a
Double-Precision Absolute Value of Register	A5	DABS	R	1	2.5	1a

* M = memory, P = processor (5 OSC cycles) B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 7a: Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
Double-Precision Integer Add	A7	DAR	R	1	3	0
	A6	DA	D, DX	4	1	0
Single Precision Integer Subtract	B1	SR	R	1	1	0
	1 X	SBB	B	2	2	0
	4X 5	SBBX	BX	2	2	0
	B2	SISP	ISP	1	1	0
	B0	S	D, DX	3	1	0
	4A 2	SIM	IM	2	1	0
Decrement Memory by a Positive Integer	B3	DECM	D,DX	4	1	0
Single Precision Negate Register	B4	NEG	R	1	1	0
Double-Precision Negate Register	B5	DNEG	R	1	3	0
Double-Precision Integer Subtract	B7	DSR	R	1	3	0
	B6	DS	D,DX	4	1	0
Single Precision Integer Multiply with 16-Bit Product	C1	MSR	R	1	6.5	4a
	C2	MISP	ISP	1	7.5	4a
	C3	MISN	ISN	1	7.5	4a
	C0	MS	D,DX	3	6 5	4a
	4A 4	MSIM	IM	2	6.5	4a
Single Precision Integer Multiply with 32-Bit Product	C5	MR	R	1	5	3
	1X	MB	B	2	7	3
	4X 6	MBX	BX	2	7	3
	C4	M	D, DX	3	5	3
	4A 3	MIM	IM	2	5	3
Double-Precision Integer Multiply	C7	DMR	R	1	41	4.5a
	C6	DM	D,DX	4	40	4.5a
Single Precision Integer Divide with 16-Bit Dividend	D1	DVR	R	1	20.25	5.5a
	D2	DISP	ISP	1	20	5.5a
	D3	DISN	ISN	1	20.5	5.5a
	D0	DV	D,DX	3	20.25	5.5a
	4A 6	DVIM	IM	2	20.25	5.5a
Single Precision Integer Dividewith 32-Bit Dividend	D5	DR	R	1	21.75	6.5a
	1X	DB	R	2	22.75	6.5a
	4X 7	DBX	BX	2	22.75	6.5a
	D4	D	D,DX	3	21.75	6.5a
	4A 5	DIM	IM	2	22.75	6.5a
Double-Precision Integer Divide	D7	DDR	R	1	79.5	5.5a
	D6	DD	D,DX	4	77.5	5.5a

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

Table 7a: Insttruction Summary (continued)

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
LOGICAL						
Inclusive Logical OR	E1	ORR	R	1	0	0
	3X	ORB	B	2	1	0
	4X F	ORBX	BX	2	1	0
	E0	OR	D, DX	3	0	0
	4A 8	ORIM	IM	2	0	0
Logical AND	E3	ANDR	R	1	0	0
	3X	ANDB	B	2	1	0
	4X E	ANDX	BX	2	1	0
	E2	AND	D, DX	3	0	0
	4A 7	ANDM	IM	2	0	0
Exclusive Logical OR	E5	XORR	R	1	0	0
	E4	XOR	D, DX	3	0	0
	4A 9	XORM	IM	2	0	0
Logical NAND	E7	NR	R	1	1	0
	E6	N	D, DX	3	1	0
	4A B	NIM	IM	2	1	0
Set Bit	51	SBR	R	1	0	0
	50	SB	D, DX	4	1	0
	52	SBI	I, IX	5	2	0
Reset Bit	54	RBR	R	1	1	0
	53	RB	D, DX	4	1	0
	55	RBI	I ,IX	5	2	0
Test Bit	57	TBR	R	1	0	0
	56	TB	D, DX	3	0	0
	58	TBI	I, IX	4	1	0
Test and Set Bit	59	TSB	D,DX	4	0	2
Set Variable Bit in Register	5A	SVBR	R	1	0	1
Reset Variable Bit in Register	5C	RVBR	R	1	1	1
Test Variable Bit in Register	5E	TVBR	R	1	0	1
Store Register Through Mask	97	SRM	D,DX	4	3	0
BYTE						
Load From Upper Byte	8B	LUB	D,DX	3	0	0
	8D	LUBI	I,IX	4	1	0
Load From Lower Byte	8C	LLB	D DX	3	1	0
	8E	LLBI	I, IX	4	2	0
Store Into Upper Byte	9B	STUB	D,DX	4	1	0
	9D	SUB I	I, IX	5	3	0
Store Into Lower Byte	9C	STLB	D,DX	4	1	0
	9E	SLBI	I,IX	5	2	0
Exchange Bytes in Register	EC	XBR	S	1	0	1

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles).

Table 7a: Instruction Summary (continued)

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
COMPARE						
Single-Precision Compare	F1	CR	R	1	0	0
	3X	CB	B	2	1	0
	4X C	CBX	BX	2	1	0
	F2	CISP	ISP	1	0	0
	F3	CISN	ISN	1	0	0
	F0	C	D, DX	3	0	0
	4A A	CIM	IM	2	0	0
Compare Between Limits	F4	CBL	D,DX	4	2.75	1.75a
Double-Precision Compare	F7	DCR	R	1	2	0
	F6	DC	D, DX	4	0	0
JUMP/BRANCH						
Jump on Condition	70	JC	D, DX	2	0.5	1a
	71	JCI	I,IX	3	0 5	1a
Jump to Subroutine	72	JS	D, DX	2	2	0
Subtract One and Jump	73	SOJ	D, DX	2	2.5	1a
Branch Unconditionally	74	BR	ICR	2	2	0
Branch if Equal to (Zero)	75	BEZ	ICR	1 5	1	1a
Branch if Less than (Zero)	76	BLT	ICR	1.5	1	1a
Branch to Executive	77	B EX	S	16	12	3a
Branch if Less than or Equal to (Zero)	78	BLE	ICR	1.5	1	1a
Branch if Greater than (Zero)	79	BGT	ICR	1.5	1	1a
Branch if Not Equal to (Zero)	7A	BNZ	ICR	1.5	1	1 a
Branch if Greater than or Equal to (Zero)	7B	BGE	ICR	1.5	1	1a
SHIFT						
Shift Left Logical	60	SLL	R	1	1	0
Shift Right Logical	61	SRL	R	1	1	0
Shift Right Arithmetic	62	SRA	R	1	1	0
Shift Left Cyclic	63	SLC	R	1	1	0
Double Shift Left Logical	65	DSLL	R	1	3	0
Douible Shift Right Logical	66	DSRL	R	1	2	0
Double Shift Right Arithmetic	67	DSRA	R	1	2	0
Double Shift Left Cyclic	68	DSLC	R	1	3	0
Shift Logical, Count in Register	6A	SLR	R	1	1	3
Shift Arithmetic, Count in Register	6B	SAR	R	1	1.5	3.50a
Shift Cyclic, Count in Register	6C	SCR	R	1	1	3.25a
Double Shift Logical, Count in Register	6D	DSLR	R	1	2.25	4a
Double Shift Arithmetic, Count in Register	6E	DSAR	R	1	3.19	4.94a
Double Shift Cyclic, Count in Register	6F	DSCR	R	1	3.5	3a

* M = memory, P = processorr (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists.

Table 7a: Instruction Summary (continued)

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
CONVERT						
Convert Floating-Point to 16-Bit Integer	E8	FIX	R	1	4.25	4.5a
Convert 16-Bit Integer to Floating-Point	E9	FLT	R	1	3	2a
Convert Extended-Precision Floating-Point to 32-Bit Integer	EA	EFIX	R	1	12.25	6.25a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EB	EFLT	R	1	7.5	3.5a
STACK						
Stack IC and Jump to Subroutine	7E	SJS	D, DX	4	3	0
Unstack IC and return from Subroutine	7F	URS	S	3	1	1
Pop Multiple registers off the Stack	8F	POPM	S	2.5+n (n=O to 15)	2.25+n (n=O to 15)	4.25a
Push Multiple Registers on to the Stack	9F	PSHM	S	1 + n (n=O to 15)	4.5 + n (n=O to 15)	2a
I/O (See I/O Command Summary)						
Execute I/O	48	XIO**	IM,IMX	3	3.583	6.277a
Vectored I/O	49	VIO**	D,DX	-	-	-
SPECIAL						
Built-In Function Call	4F	BIF	S			
Move Multiple Words, Memory-to-Memory	93	MOV	S	1+4n	1+3n	1+2na
Exchange Words in Registers	ED	XWR	R	1	2	0
Load Status	7D	LST**	D, DX	8	2	3
	7C	LSTI**	I, IX	9	2	4
No Operation	FF	NOP	S	1	2	2
Break Point	FF	BPT	S	3	4	4

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists
** Priveleged instruction

Table 7a: Instruction Summary (continued)

Operation	Op Code/Ext	Mnemonic	Format	Cycles *		
				M	P	B
FLOATING-POINT						
Extended-Precision Floating-Point Load	8A	EFL	D, DX	5	0	1
Extended-Precision Floating-Point Store	9A	EFST	D, DX	5	0	1
Floating-Point Absolute Value of Register	AC	FABS	R	1	1.75	3.25a
Floating-Point Negate Register	BC	FNEG	R	1	3.25	3.75a
Floating-Point Compare	F9	FCR	R	1	2.75	2.875wa
	3X	FCB	B	2	2.75	2.875wa
	4X D	FCBX	BX	2	2.75	2.875wa
	F8	FC	D, DX	3	1.75	2.875wa
Extended-Precision Floating-Point Compare	FB	EFCR	R	1	3.25	2.875wa
	FA	EFC	D,DX	4.25a	2.75	2.875wa
Floating-Point Add	A9	FAR	R	1	7.625	8.25wa
	2X	FAB	B	3	6.625	8.25wa
	4X 8	FABX	BX	3	6.625	8.25wa
	A8	FA	D, DX	4	5.625	8.25wa
Extended-Precision Floating-Point Add	AB	EFAR	R	1	21.3125	10.5625wa
	AA	EFA	D, DX	5	19.3125	10.5625wa
Floating-Point Subtract	B9	FSR	R	1	8.625	8.625wa
	2X	FSB	B	3	7.625	8.625wa
	4X 9	FSBX	BX	3	7.625	8.625wa
	B8	FS	D, DX	4	6.625	8.625wa
Extended-Precision Floating-Point Subtract	BB	EFSR	R	1	23.0625	11.8125wa
	BA	EFS	D, DX	5	21.0625	11.8125wa
Floating-Point Multiply	C9	FMR	R	1	12.75a	6.25wa
	2X	FMB	B	3	12.75a	6.25wa
	4X A	FMBX	BX	3	12.75a	6.25wa
	C8	FM	D, DX	4	11.75a	6.25wa
Extended-Precision Floating-point Multiply	CB	EFMR	R	1	59.75	6.25wa
	CA	EFM	D, DX	5	57.75	6.25wa
Floating-Point Divide	D9	FDR	R	1	31.5	32.75wa
	2X	FDB	B	3	30 5	32.75wa
	4X B	FDBX	BX	3	30 5	32.75wa
	D8	FD	D, DX	4	29.5	32.75wa
Extended-Precision Floating-Point Divide	DB	EFDR	R	1	102.625	47.875wa
	DA	EFD	D, DX	5	100.625	47 875wa

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists
wa = weighted average favouring one or more possible alternatives

Table 7a: Instruction Summary (continued)

4.5 INTERNAL I/O COMMAND SUMMARY

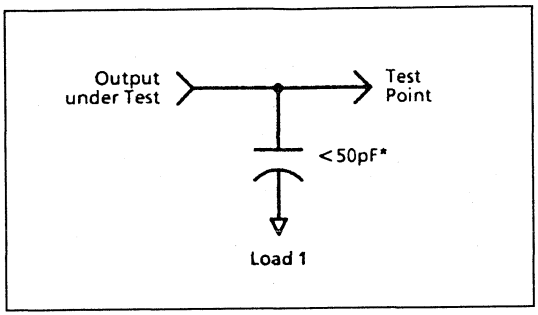
Operation	Command	Mnemonic	Cycles *		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-Up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct Memory Access Disable	4007	DMAD	2	3	9
Timer A Start	4008	TAS	2	3	9
Ti mer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register Without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	50XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	51XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	DIXY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

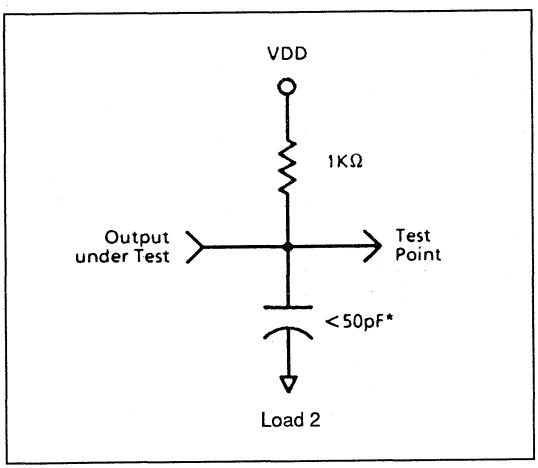
* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles),
a = average if more than one alternative exists

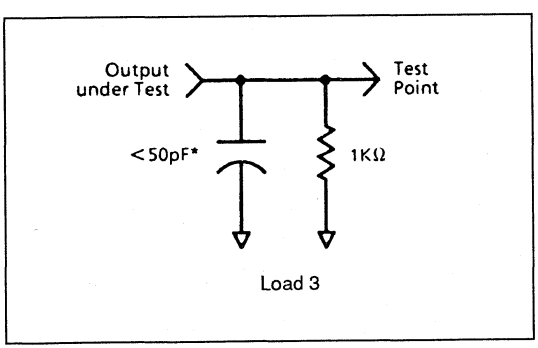
Table 7b: Internal I/O Command Summary

5.0 TIMING CHARACTERISTICS & DIAGRAMS

This section provides detailed timing specifications for the MAS281, under the test loads detailed below. Cross hatching in all figures indicates either a "don't care" or undeterminate state.







*Includes all jig and parasitic capacitance

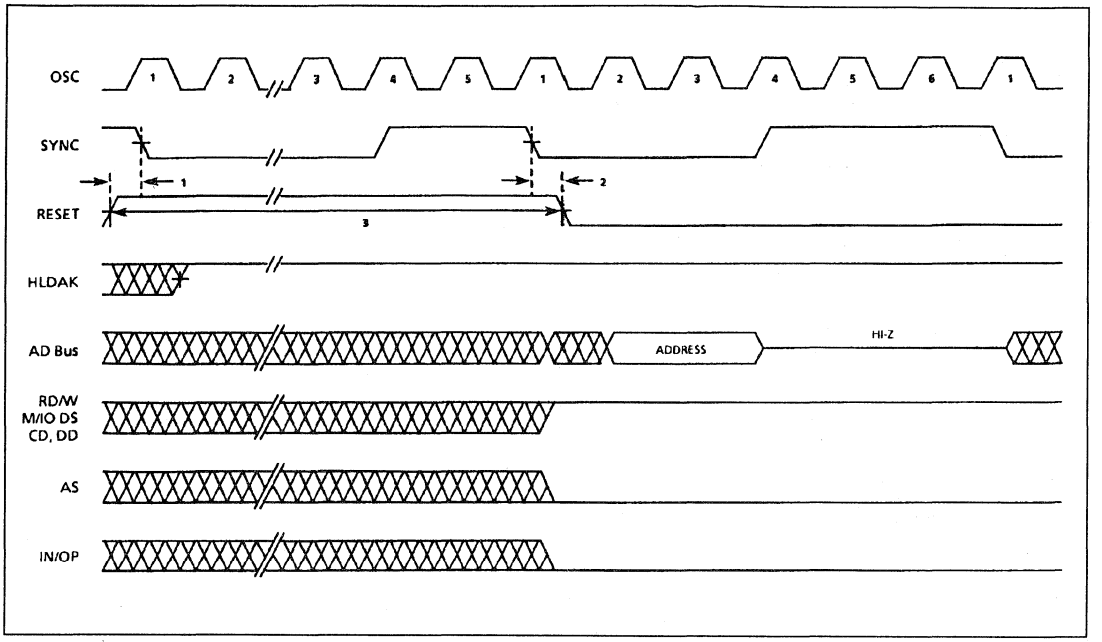


Figure 12: Reset Timing

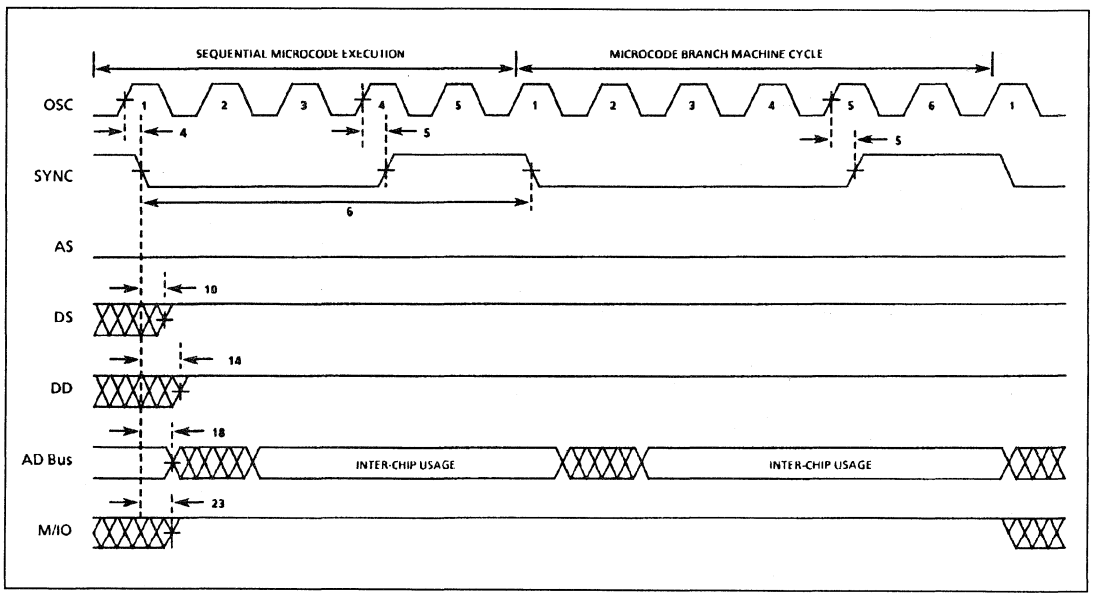
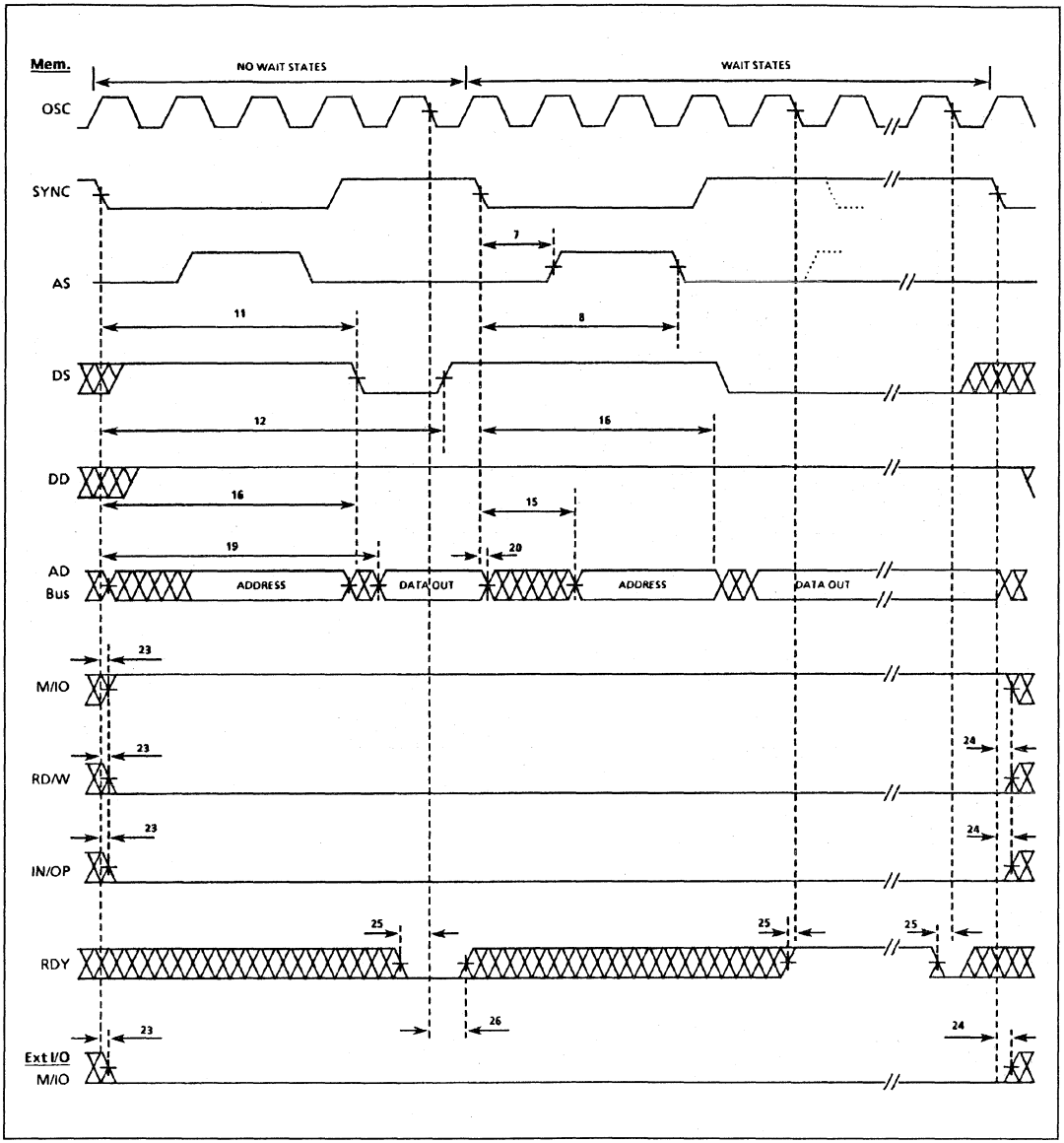


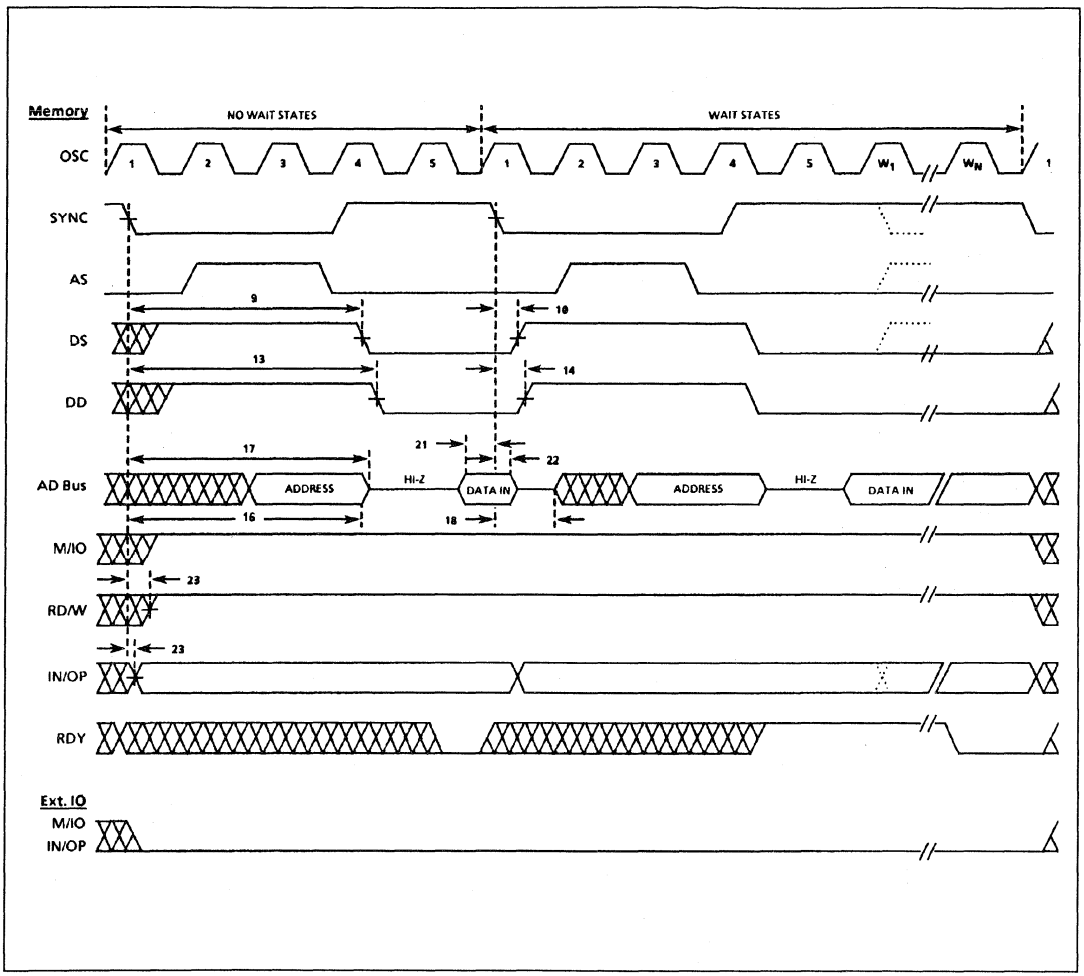
Figure 13: Internal CPU Operations



NOTES:

1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states: CD = HIGH and DMAK = HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW.

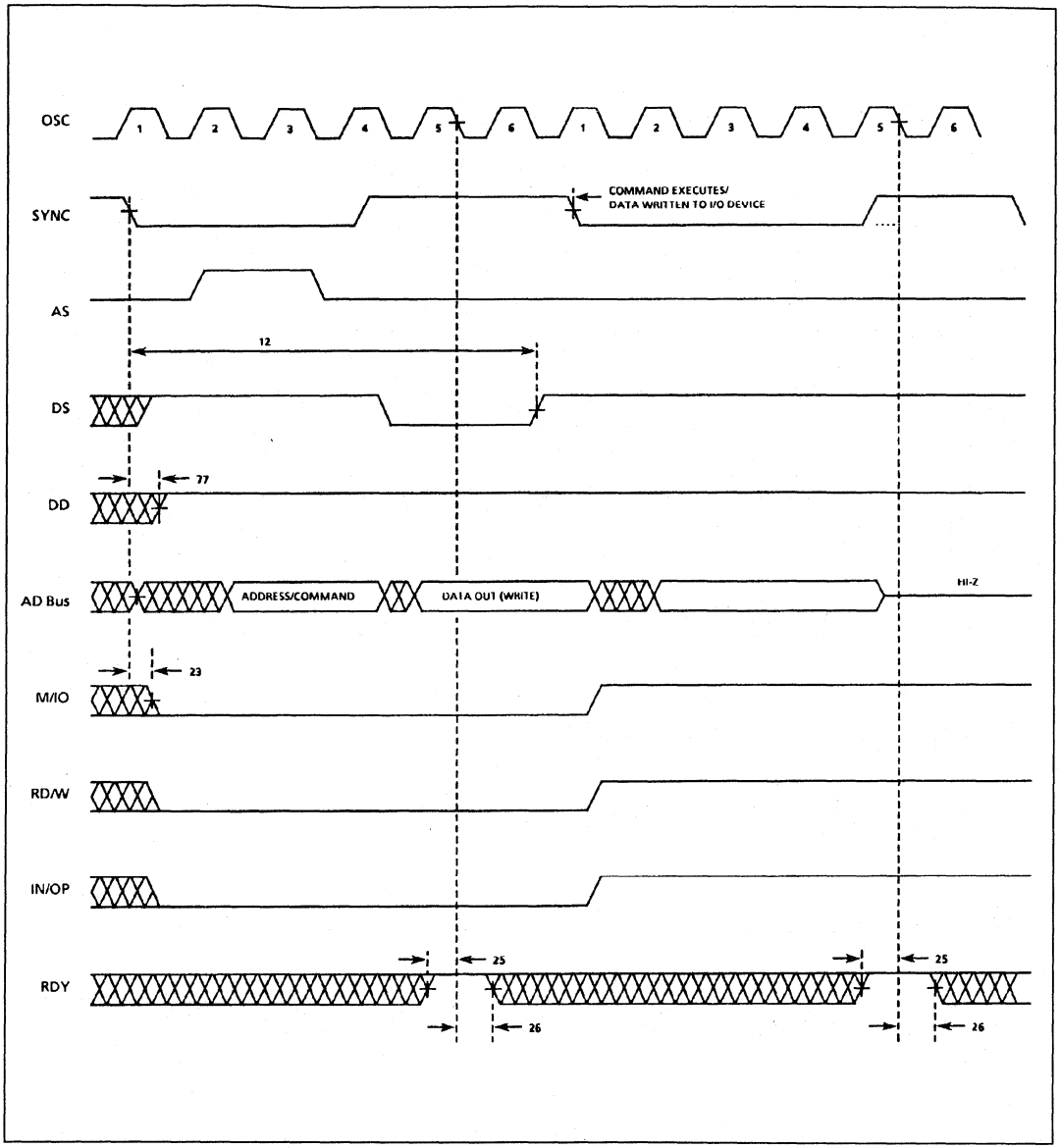
Figure 14: Write Transfer Timing



NOTES:

1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states: CD = HIGH, HLDAK = HIGH and DMAK = HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW.

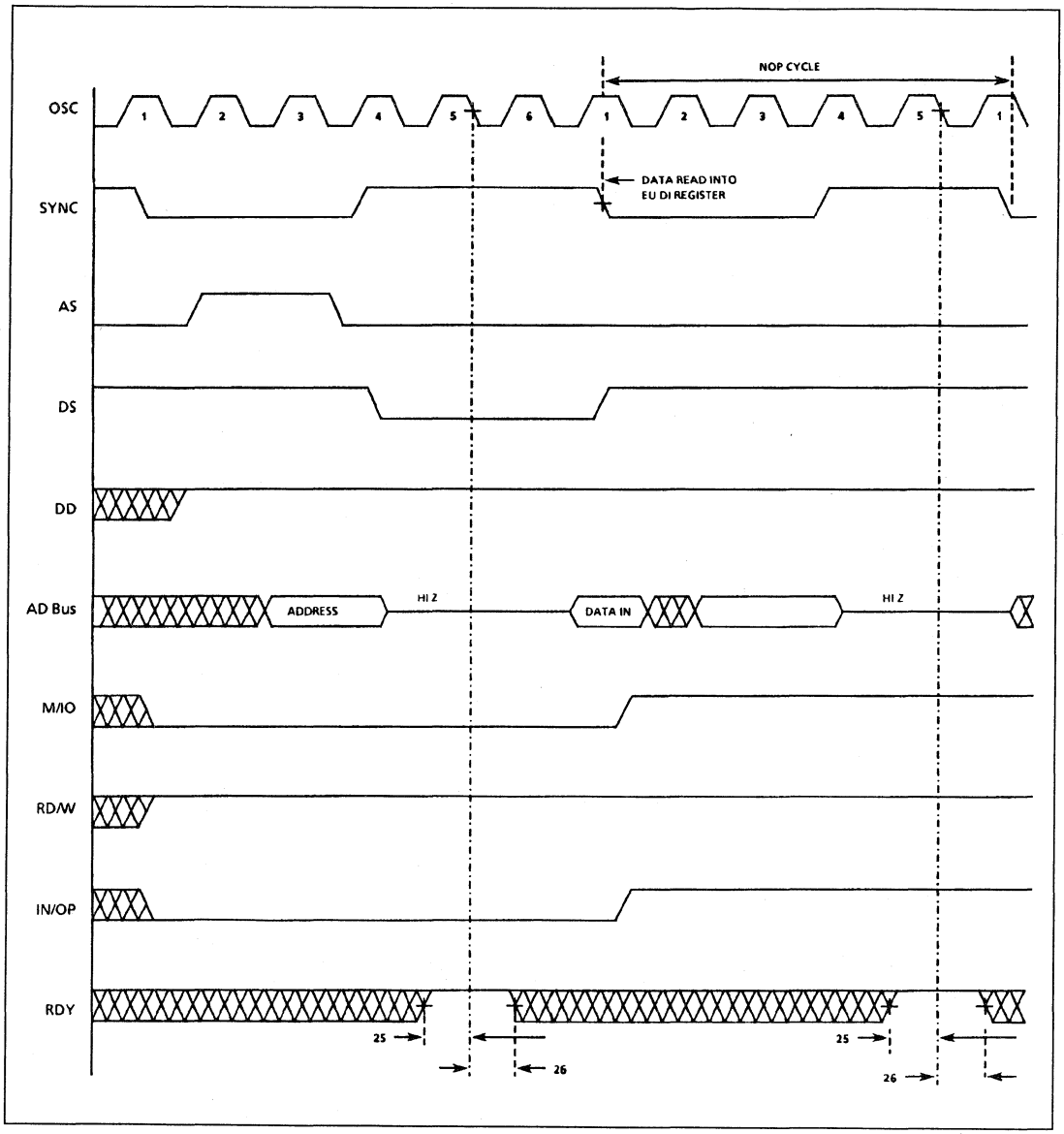
Figure 15: Read Transfer Timing.



NOTES:

1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states: CD = HIGH, HLDAK = HIGH and DMAK HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW.

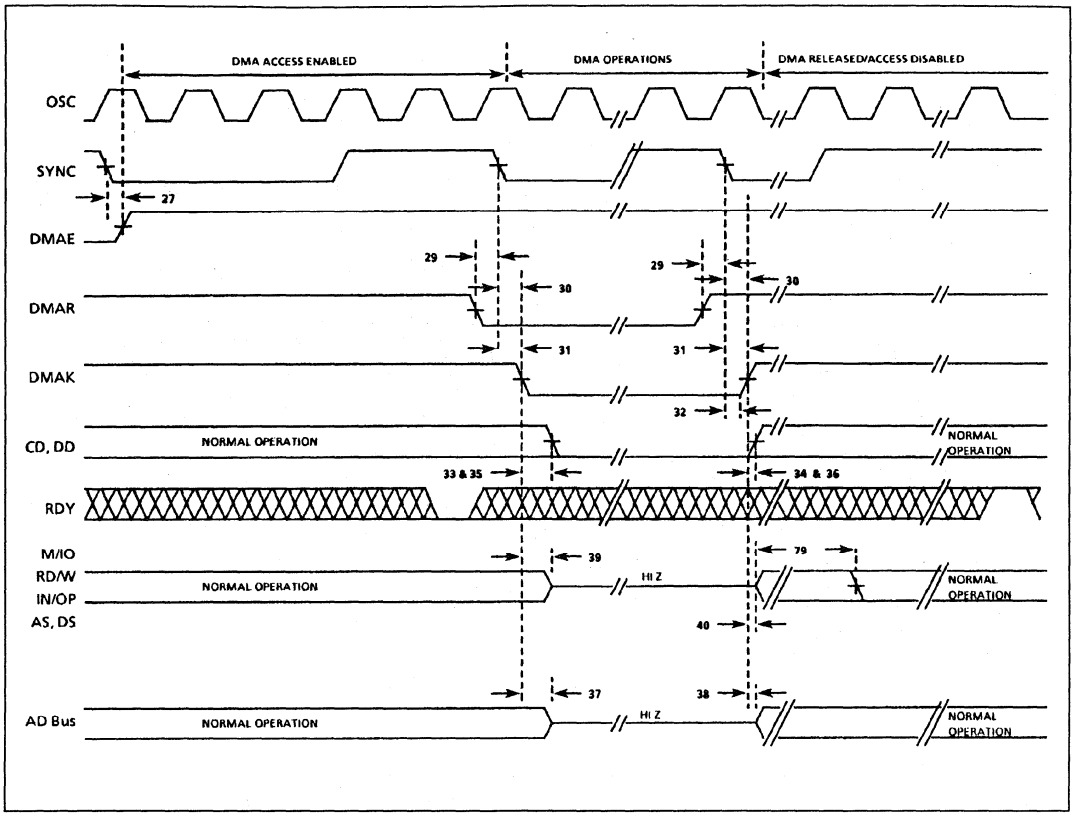
Figure 16: Internal I/O Write/Command



NOTES:

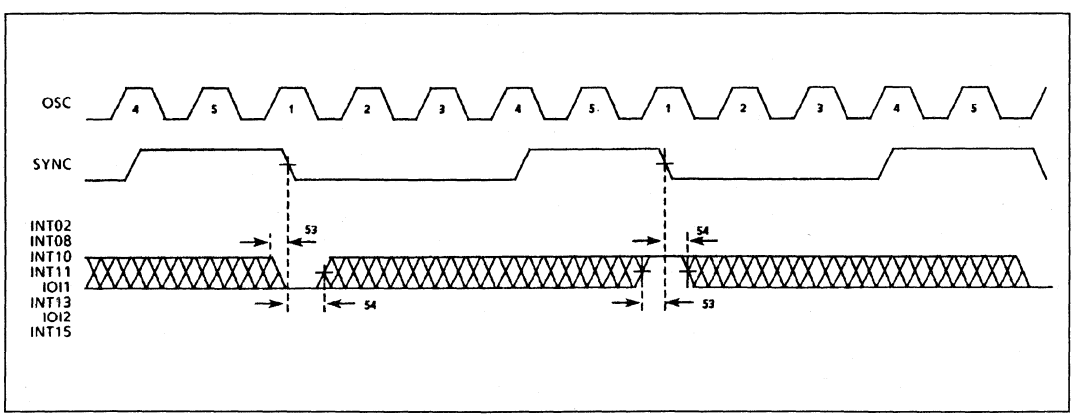
1. Dashed timing lines indicate no-wait cycle timing.
2. Other output states: CD = HIGH, HLDAK = HIGH and DMAK HIGH
3. Other required input states: HOLD = HIGH, DMAR = HIGH and RESET = LOW.

Figure 17: Internal I/O Read Timing



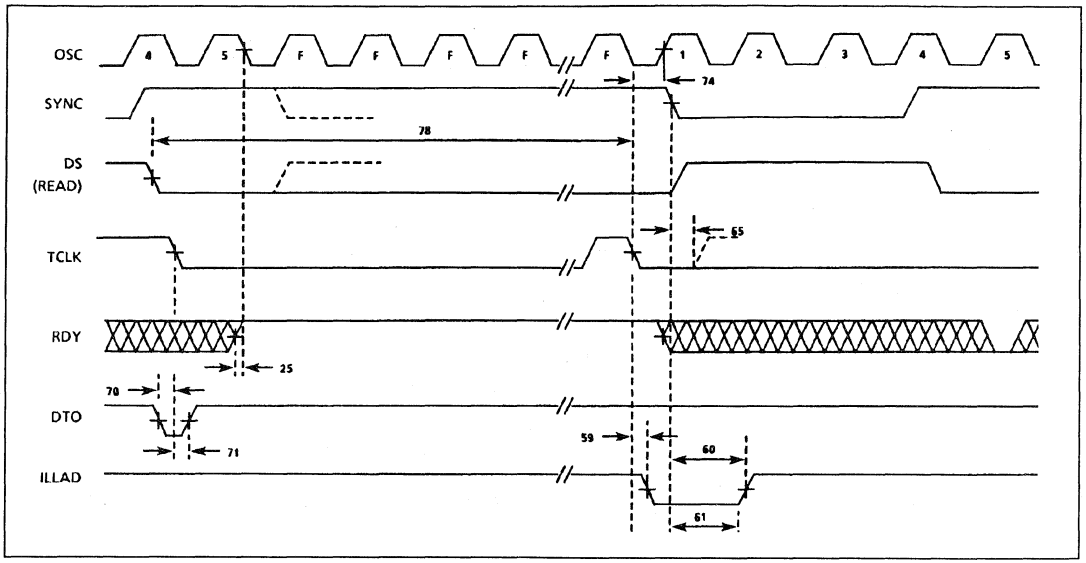
NOTE:
Other required input states: DTIMER = HIGH and RESET = LOW

Figure 18: DMA Access/Release Timing



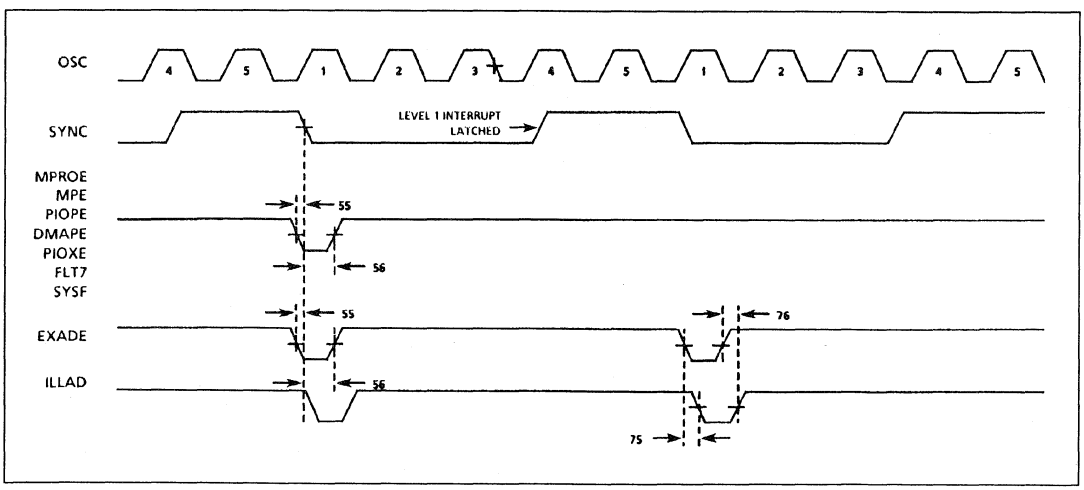
NOTE:
Other required input: RESET = LOW

Figure 19: Interrupt Request Timing



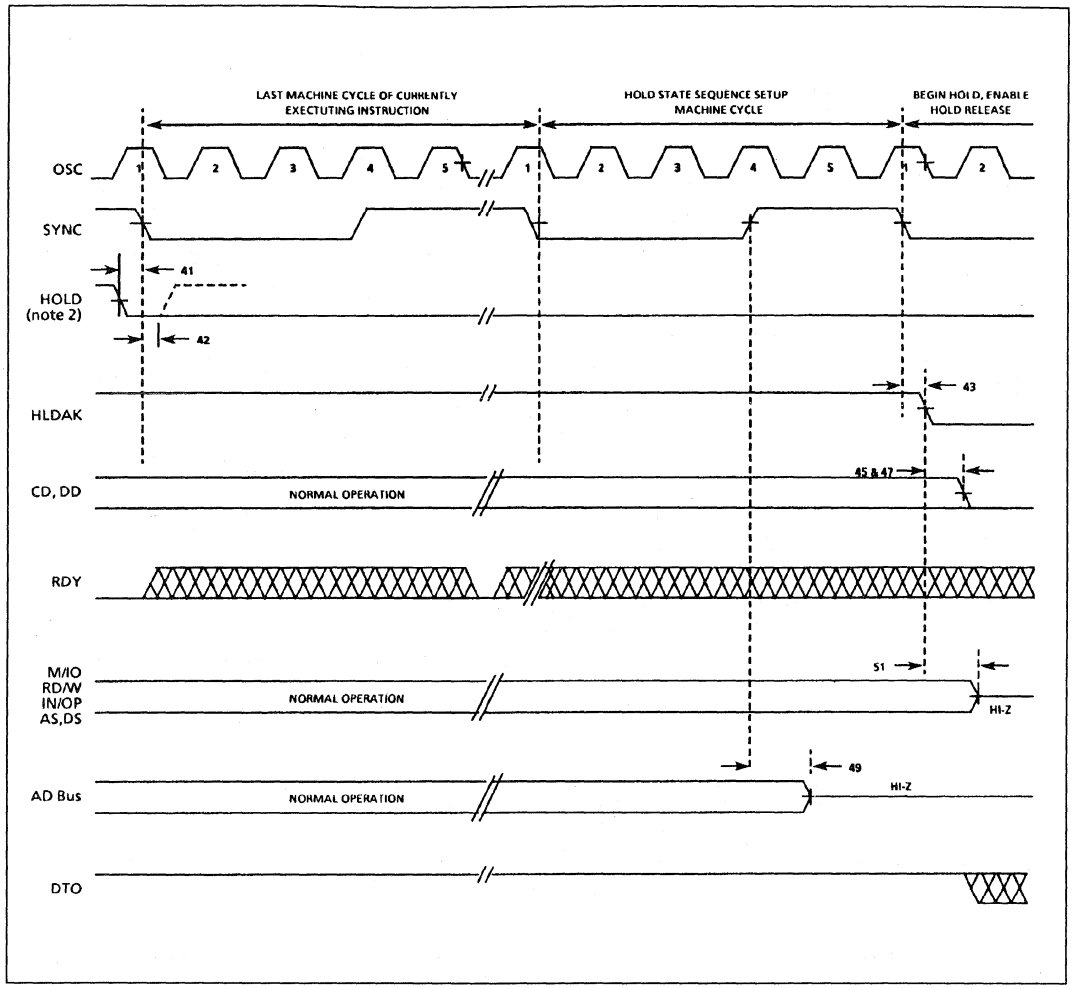
NOTES:
1. 2 TCLK falling edges during a continuous DS = low are necessary to cause a bus fault timeout.
2. Other output states: HLDAK = HIGH.
3. Other required input states: DTO = HIGH and RESET = LOW.

Figure 20: Bus Fault Timeout Timing



NOTES:
1. Assumes only one fault active at a time.
2. Buffered EXADE.
3. Other required input state: RESET = LOW.

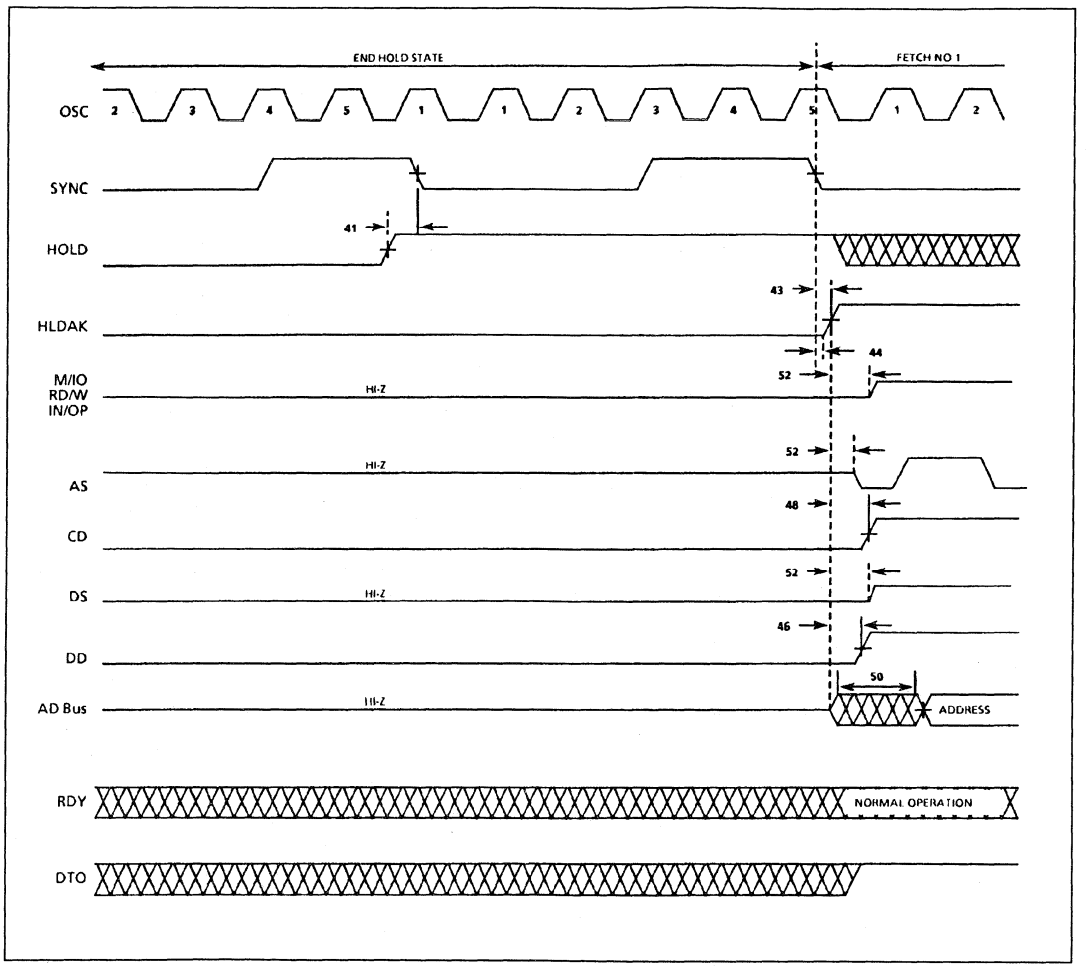
Figure 21: Fault Capture Timing



NOTES:

1. The "don't care" state will continue to exist until HLDAK = HIGH, RDY will then resume normal operation.
2. HOLD falling may occur at any time during software execution. The diagram shows the last possible time it can occur and be assured of entering the HOLD state after the current instruction completes execution.
3. Other required input states: RESET = LOW.

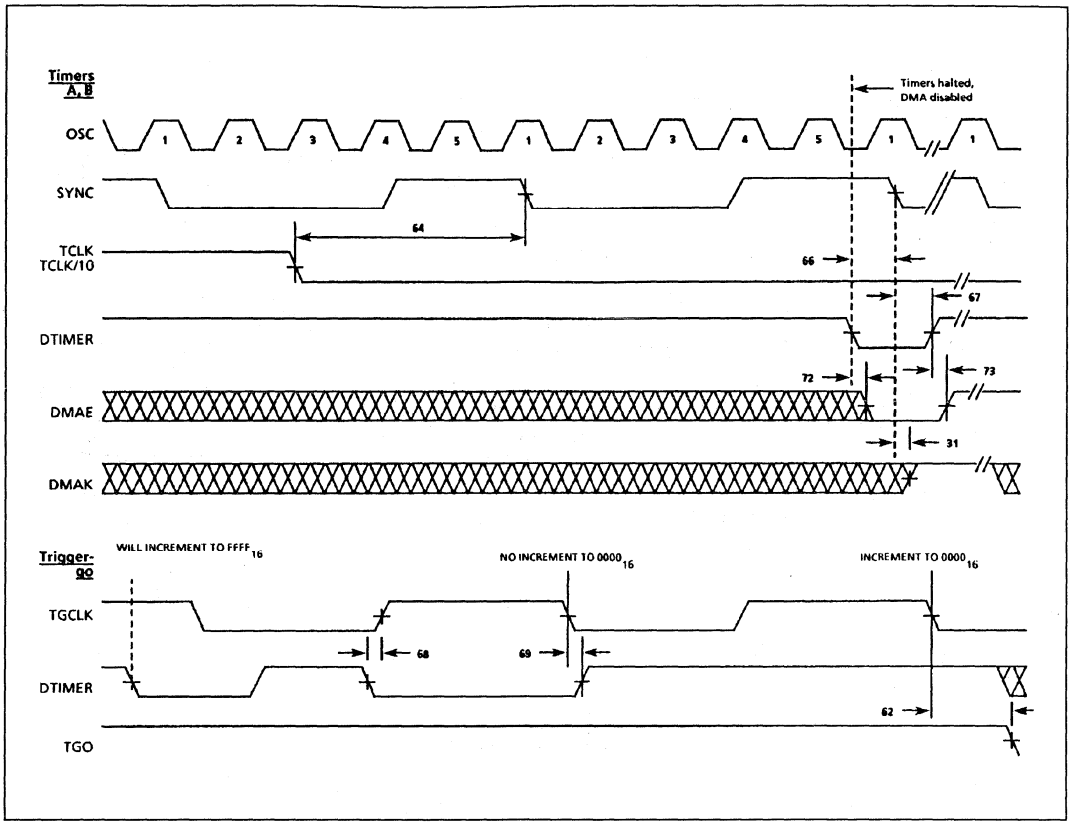
Figure 22: Hold State Generation Timing



NOTES:

1. ADDRESS = IC(BPT) initiated the Hold state.
   ADDRESS = IC(Hold) - 2, if HOLD = LOW initiated the Hold state (unless changed by the monitor system).
2. Other output states: DMAK HIGH.
3. Other required input states: DMAR = HIGH and RESET = LOW.

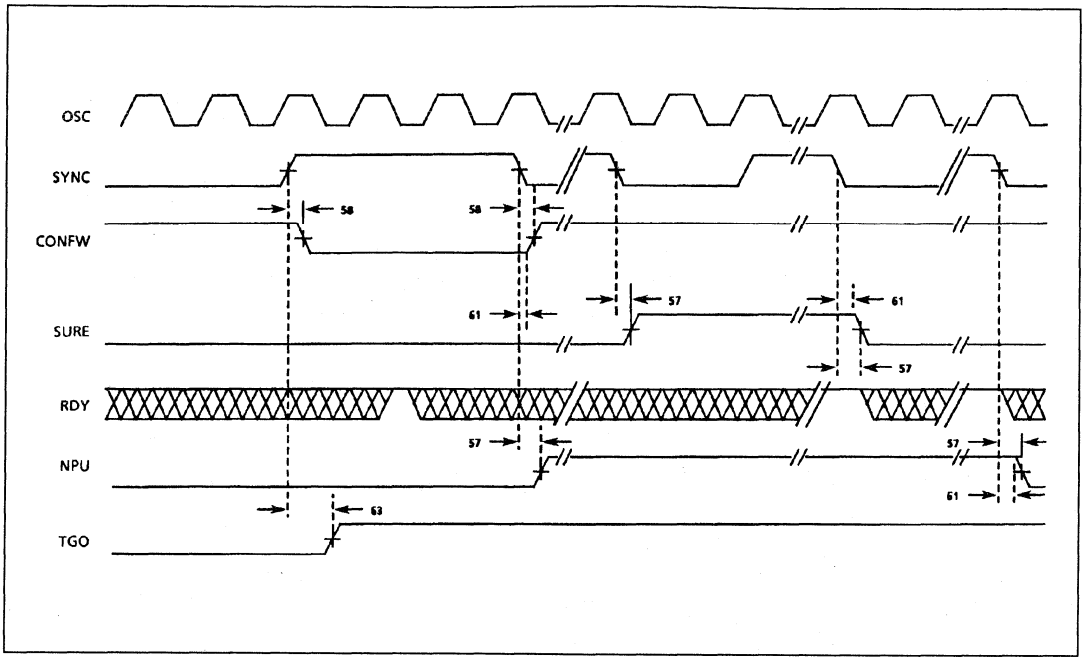
Figure 23: Hold State Termination Timing



NOTES:

1. Other required input: RESET = LOW.
2. TCLK/10 is the internally derived Timer B clock.
3. Timers A and B are clocked on the second SYNC falling edge after TCLK set-up time is satisfied.

Figure 24: Timer Operations



NOTES:

1. Other required input states: RESET = LOW.

Figure 25: Discrete Outputs Timing

6.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	V_{DD}+0-3	V
Current through any pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Table 8: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliabillty.

DEFINITION OF SUBGROUPS

Subgroup	Definition
1	Static characteristics specified in Table 9 at +25°C
2	Static characteristics specified in Table 9 at +125°C
3	Static characteristics specified in Table 9 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Table 10 at +25°C
10	Switching characteristics specified in Table 10 at +125°C
11	Switching characteristics specified in Table 10 at -55°C

7.0 DC ELECTRICAL CHARACTERISTICS

			Total Dose Radiation Not Exceeding $3x10^5$ Rad (Si)			
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	TTL Input High Voltage		2.0			V
V_{IL}	TTL Input Low Voltage				0.8	V
V_{CH}	OSC Input High Voltage		4.0			V
V_{CL}	OSC Input Low Voltage				1.0	V
V_{OH}	TTL Output High Voltage	I_{OH} = -1.4mA V_{DD} = 4.5V	3.5			V
V_{OL}	TTL Output low Voltage	I_{OL} = 2.0mA V_{DD} = 5.5V			0.4	V
I_{IZ}	Input Leakage Current (Note 1)	V_{DD} = 5.5V			±10	µA
I_{OZ}	Output Leakage Current (Note 1)	V_{DD} = 5.5V			±150	µA
I_{DD}	Power Supply Current	f = 20MHz		70	133	mA

Mil-Std-883, method 5005, subgroups 1, 2, 3
V_{DD} = 5V±10%, over full operating temperature range
Note 1: Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C

Table 9: Operating DC Electrical Characteristics

8.0 TIMING PARAMETERS

NO.	Parameter	Test Condition (notes 1 & 9)	Min. (note 2)	Max. (note 2)	Units
1	RESET setup to SYNC lo (note 3)		-	30	ns
2	RESET hold after SYNC lo (note 3)		-	15	ns
3	RESET hi to RESET lo (note 3)		2	-	SYNC
4	OSC hi to SYNC lo	Load 1	10	40	ns
5	OSC hi to SYNC hi	Load 1	10	40	ns
6	SYNC lo to SYNC lo (notes 4 & 5)	Load 1	5_T - 2	5_T + 2	ns
7	SYNC lo to AS hi (note 6)	Load 1	1_T - 10	1_T + 5	ns
8	SYNC lo to AS lo	Load 1	2.5_T - 10	2.5_T + 15	ns
9	SYNC lo to DS lo (read)	Load 1	3_T - 5	3_T + 20	ns
10	SYNC lo to DS hi (read)	Load 1	10	30	ns
11	SYNC lo to DS lo (write)	Load 1	3_T - 5	3_T + 22	ns
12	SYNC lo to DS hi (write) (note 5)	Load 1	4.5_T -5	4.5_T + 10	ns
13	SYNC lo to DD lo	Load 1	3_T + 20	3_T + 60	ns
14	SYNC lo to DD hi	Load 1	20	60	ns
15	SYNC lo to Address valid	Load 2	-	68	ns
16	Address valid after SYNC lo	Load 2	3_T + 15	-	ns
17	SYNC lo to AD Bus Hi-Z (read) (notes 7 & 10)	Load 2	-	3_T + 50	ns
18	SYNC lo to AD Bus active(read) (note 10)	Load 2	15	-	ns
19	SYNC lo to Data valid (write)	Load 2	-	3_T + 45	ns
20	Data valid after SYNC lo (write)	Load 2	12	-	ns
21	Data set up to SYNC lo (read)		20	-	ns
22	Data hold after SYNC lo (read) (note 8)	Load 2	0	-	ns
23	SYNC lo to M/IO, RD/VV, IN/OP valid	Load 1	-	70	ns
24	M/IO, RD/WN, IN/OP valid after SYNC lo	Load 1	5	-	ns
25	RDY setup to OSC lo		15	-	ns
26	RDY hold after OSC lo		5	-	ns
27	SYNC lo to DMAE valid	Load 1	-	75	ns
28	DMAE valid after SYNC lo	Load 1	5	-	ns
29	DMAR setup to SYNC lo		20	-	ns
30	DMAR hold after SYNC lo		10	-	ns

NOTES:

Mil-Std-883, method 5005, subgroups 9, 10, 11

1. Unless otherwise noted, test condltions are as follows: OSC duty cycle = 50%, input rise and fall time < 5ns, timing measured from 50% of VDD points.
2. t = 1 OSC period. 0.5t implies a 50% OSC duty cycle; fractional t's may be adjusted to reflect actual OSC duty cycle.
3. Data obtained by characterisation or analysis, is not routinely measured.
4. Add 1t for potential branch cycle.
5. Add 1t for internal XIO cycle; nt for n memory wait states.
6. Excluding DMA or HOLD conditions.
7. Measured to pre-Hi-Z steady state ± 10% of VDD.
8. Measurement minus $1x10^{-7}$ in [1-(VIL-0 5/VDD-0.5)] nsecs.
9. Output references SYNC, DMAK, and HLDAK drive into load 1.
10. Guaranteed by component LSI testing: not measured on microprocessor module.

Table 10. Timing Parameters

NO.	Parameter	Test Condition (notes 1 & 9)	Min. (note 2)	Max. (note 2)	Units
31	SYNC lo to DMAK valid	Load 1	-	50	ns
32	DMAK valid after SYNC lo	Load 1	5	-	ns
33	DMAK lo to DD lo	Load 1	-	30	ns
34	DMAK hi to DD hi	Load 1	-	30	ns
35	DMAK lo to CD lo	Load 1	-	30	ns
36	DMAK hi to CD hi	Load 1	-	30	ns
37	DMAK lo to AD Bus Hi-Z (note 7)	Load 2	-	70	ns
38	DMAK hi to AD Bus valid (note 10)	Load 2	-	60	ns
39	DMAK lo to AS, DS, M/IO, RD/W, IN/OP Hi-Z (note 7)	Load 2	-	50	ns
40	DMAK hi to AS, DS, M/IO, RD/W, IN/OP valid (note 10)	Load 2	-	59	ns
41	HOLD set up to SYNC lo		40	-	ns
42	HOLD hold after SYNC lo		15	-	SYNC
43	SYNC lo to HLDAK valid	Load 1	-	20	ns
44	HLDAK valid after SYNC lo	Load 1	-7	-	ns
45	HLDAK lo to DD lo	Load 1	-	50	ns
46	HLDAK hi to DD hi	Load 1	-	50	ns
47	HLDAK lo to CD lo	Load 1	-	50	ns
48	HLDAK hi to CD hi	Load 1	-	50	ns
49	HLDAK lo to AD Bus Hi-Z (Hold) (notes 7 & 10))	Load 2	-	60	ns
50	HLDAK hi to AD bus valid (note 10)	Load 2	-	50	ns
51	HLDAK to AS, DS, M/IO, RD/W, IN/OP Hi-Z (notes 7 & 10)	Load 2	-	30	ns
52	HLDAK to AS, DS, M/IO, RD/W, IN/OP valid (note 10)	Load 1	-	30	ns
53	Interrupts set up to SYNC lo		20	-	ns
54	Interrupts hold after SYNC lo		10	-	ns
55	Faults setup to SYNC lo		20	-	ns
56	Faults hold after SYNC lo		15	-	ns
57	SYNC lo to SURE, NPU valid	Load 1	-	50	ns
58	SYNC hi to CONFW valid	Load 1	-	75	ns
59	TCLK lo to ILLAD lo (Bus timeout) (note 10)	Load 1	-	75	ns
60	SYNC lo to ILLAD hi (Bus timeout) (note 10)	Load 1	-	75	ns

Notes:

1. Unless otherwise noted, test conditions are as follows: OSC duty cycle = 50%, input rise and fall time < 5ns, timing measured from 50% of VDD points.
2. t = 1 OSC period. O 5t implies a 50% OSC duty cycle; fractional t's may be adjusted to reflect actual OSC duty cycle.
7. Measured to pre-Hi-Z steady state ±10% of VDD.
9. Output references SYNC, DMAK, and HLDAK drive into load 1.
10. Guaranteed by component LSI testing: not measured on microprocessor module.

Table 10: Timing Parameters (continued)

NO.	Parameter	Test Condition (notes 1 & 9)	Min. (note 2)	Max. (note 2)	Units
61	SURE, NPU, ILLAD, CONFW valid after SYNC lo (note 10)	Load 1	5	-	ns
62	TGCLK lo to TGO lo (Timer clocking) (note 10)	Load 1	-	150	ns
63	SYNC hi to TGO hi (Reset Trigger-Go XIO) (note 10)	Load 1	-	75	ns
64	TCLK setup to SYNC lo (note 10)		30	-	ns
65	TCLK hold after SYNC lo (note 10)		10	-	ns
66	DTIMER setup to SYNC lo (note 10)		50	-	ns
67	DTIMER hold after SYNC lo (note 10)		10	-	ns
68	DTIMER setup to TGCLK hi (note 10)		30	-	ns
69	DTIMER hold after TGCLK lo (note 10)		12	-	ns
70	DTO setup to TCLK lo (note 10)		30	-	ns
71	DTO hold after TCLK lo (note 10)		10	-	ns
72	DTIMER lo to DMAE lo (note 10)	Load 1	-	60	ns
73	DTIMER hi to DMAE normal operation (note 10)	Load 1	-	60	ns
74	TCLK lo to Normal operation after bus timeout (note 10)		-	100	ns
75	EXADE lo to ILLAD lo (note 10)	Load 1	-	60	ns
76	EXADE hi to ILLAD hi (note 10)	Load 1	-	60	ns
77	SYNC lo to DD hi (Internal to XIO) (note 3, 10)	Load 1	-	60	ns
78	Bus fault timeout interval (note 3, 10)		1	2	TCLK
79	DD hi to AS lo (DMA) (note 3, 10)	Load 1	20	-	ns
80	DS hi to Data valid (note 10)	Load 1 (DS), Load 2 (Data)	15	-	ns

Notes:

1. Unless otherwise noted, test conditions are as follows: OSC duty cycle = 50%, input rise and fall time < 5ns, timing measured from 50% of VDD points.
2. t = 1 OSC period 0.5t implies a 50% OSC duty cycle; fractional t's may be adjusted to reflect actual OSC duty cycle
3. Data obtained by characterisation or analysis, is not routinely measured.
9. Output references SYNC, DMAK, and HLDAK drive into load 1.
10. Guaranteed by component LSI testing: not measured on microprocessor module.

Table 10: Timing Parameters (continued)

9.0 CHIP SET INTERCONNECTION

To form the MAS281 processor from the individual chips MA17501, MA17502 and MA17503, connects should be made as shown below.

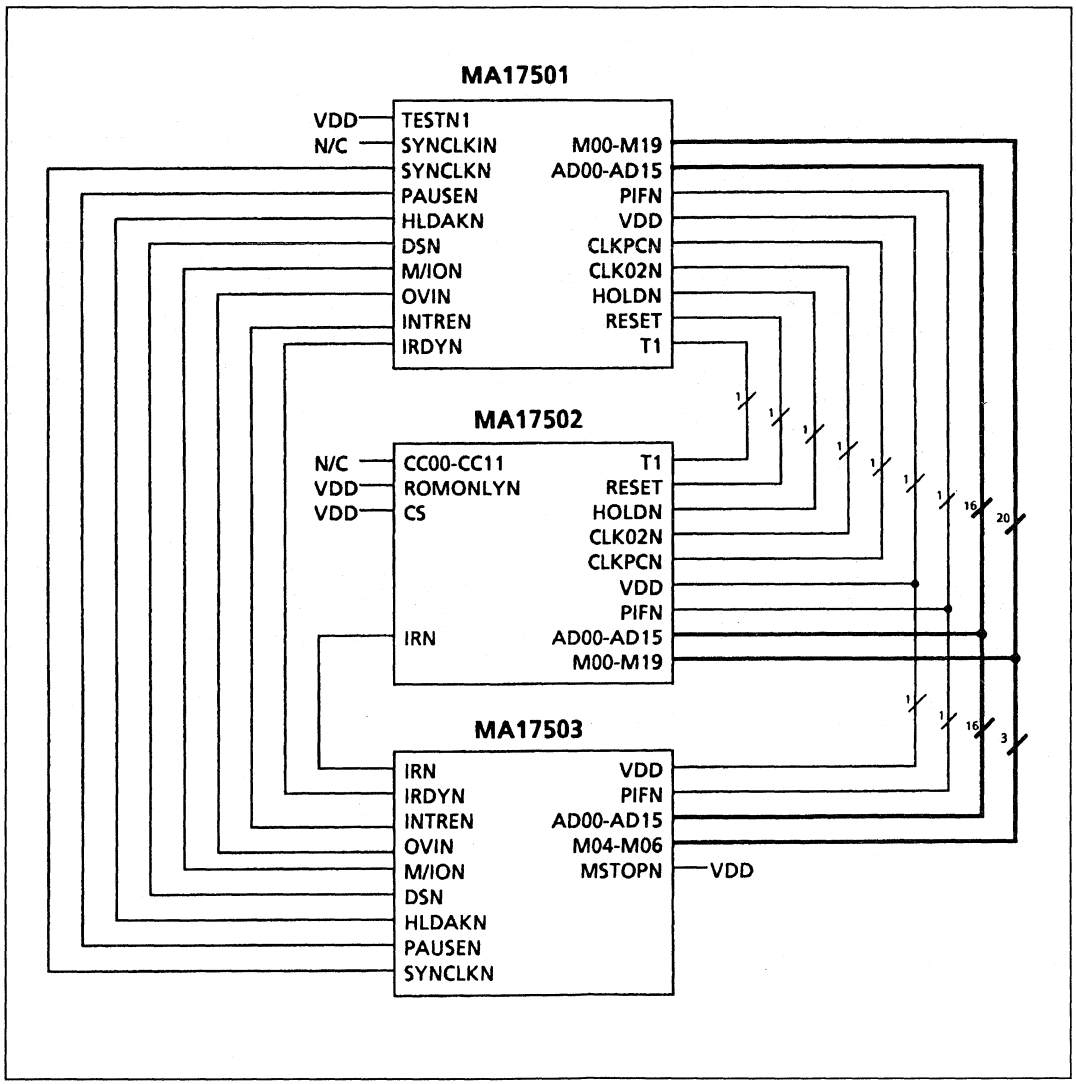


Figure 26: Chip Set Interconnection Diagram

10.0 PACKAGING INFORMATION

DUAL-IN-LINE CERAMIC MODULE
(MAS281 - PACKAGE TYPE C)

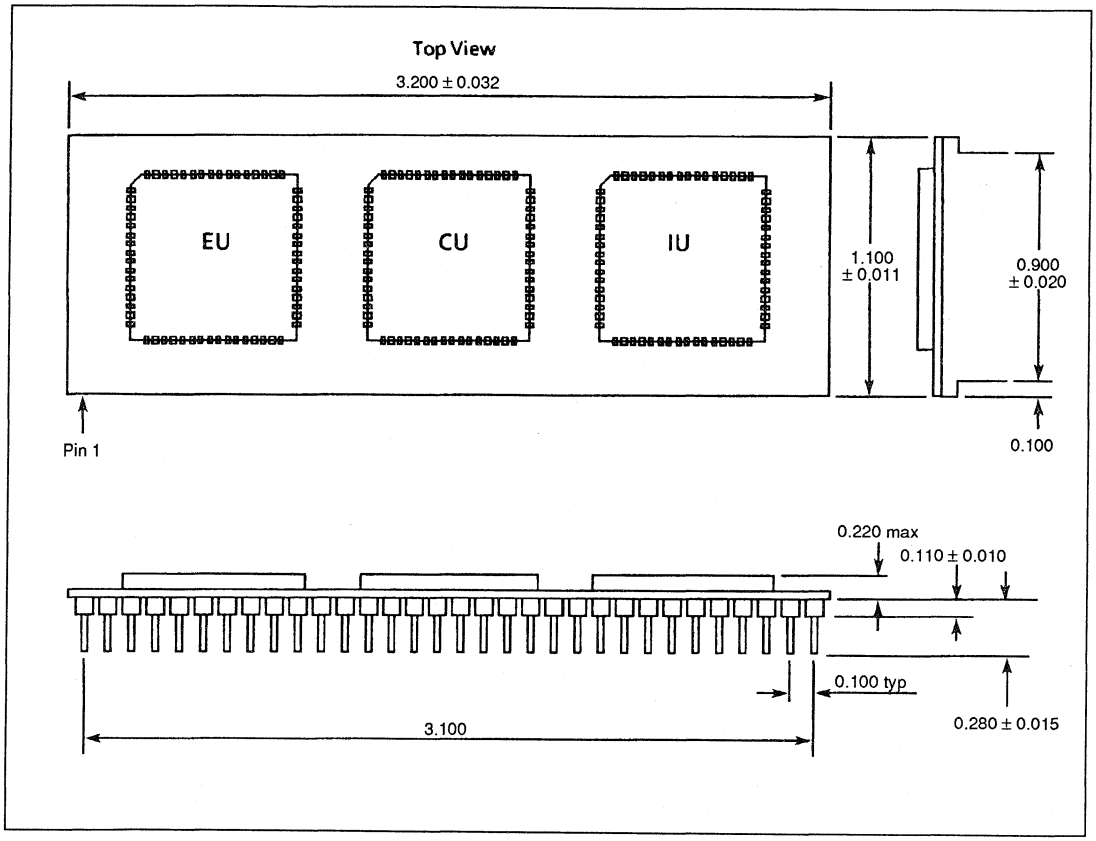


Figure 27: Dimensioned Drawing

FLATPACK CERAMIC MODULE
(MAS281 - PACKAGE TYPE F)

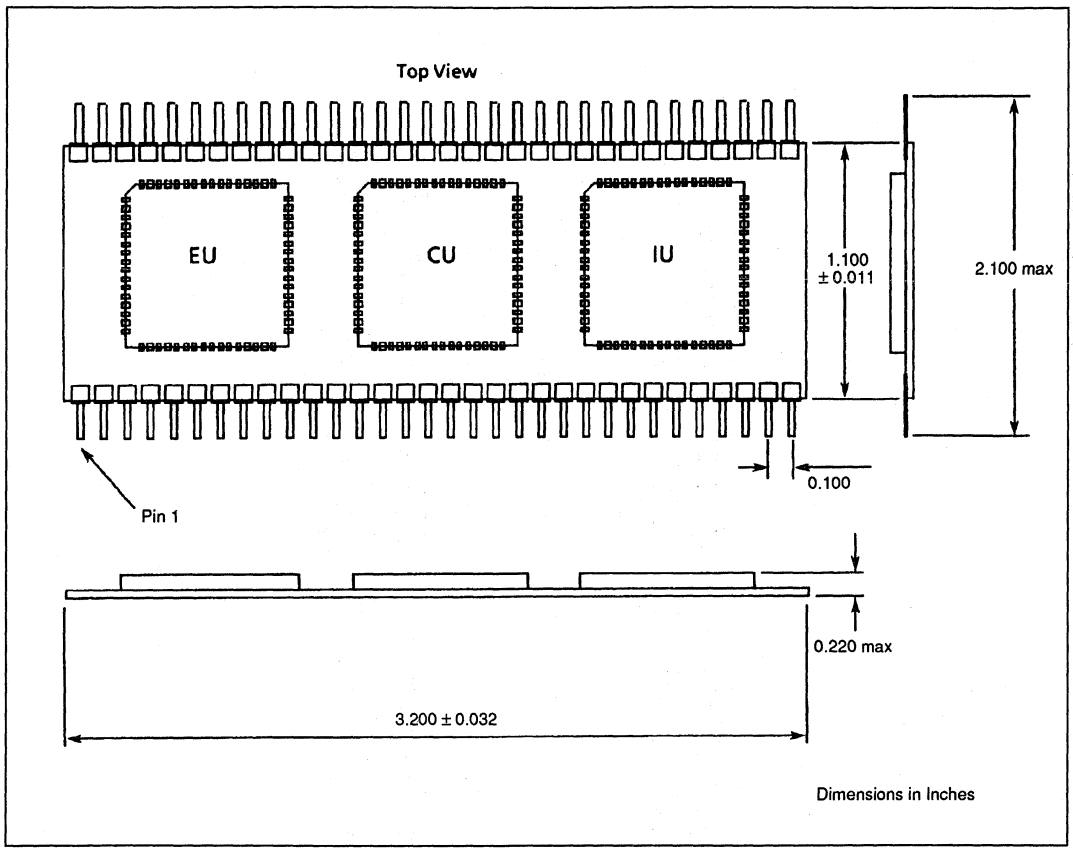


Figure 28a: Dimensioned Drawing

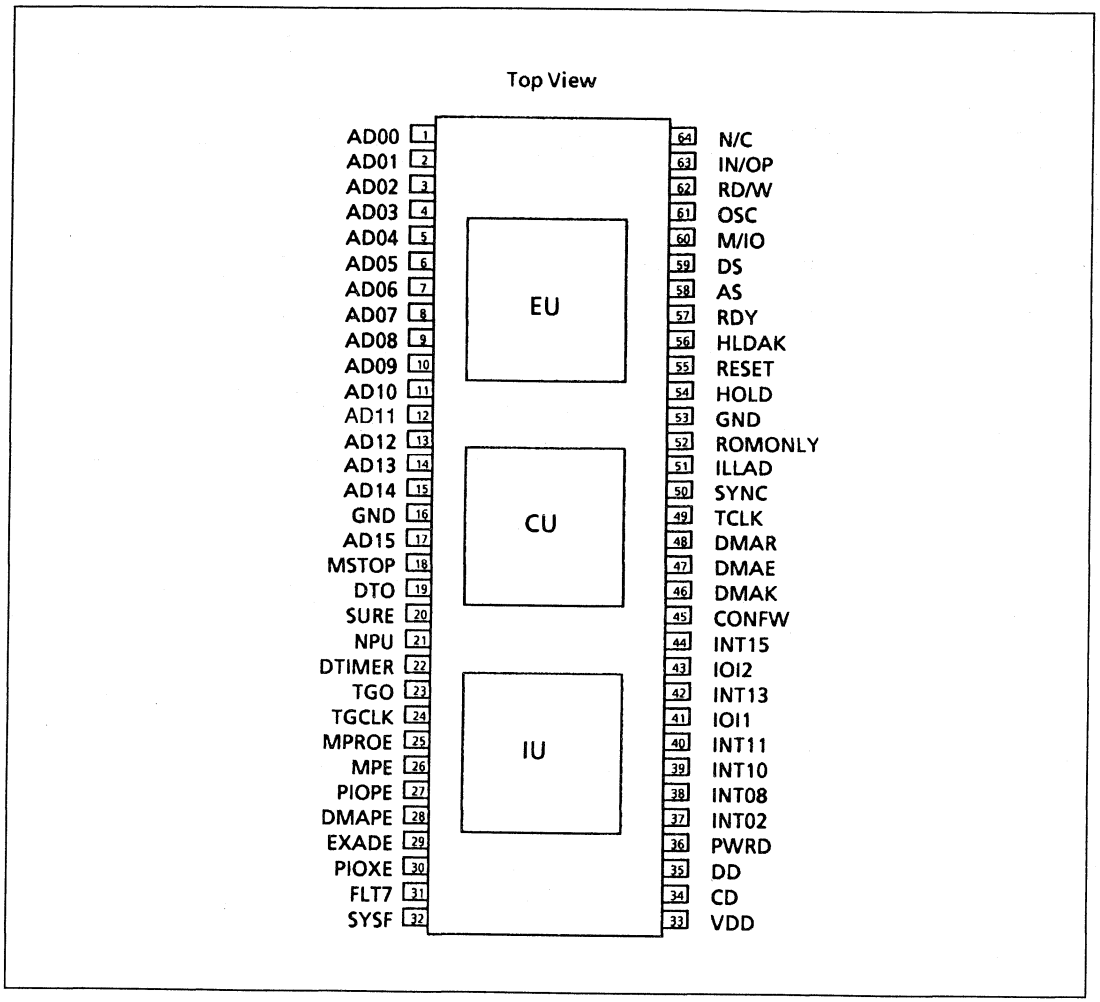
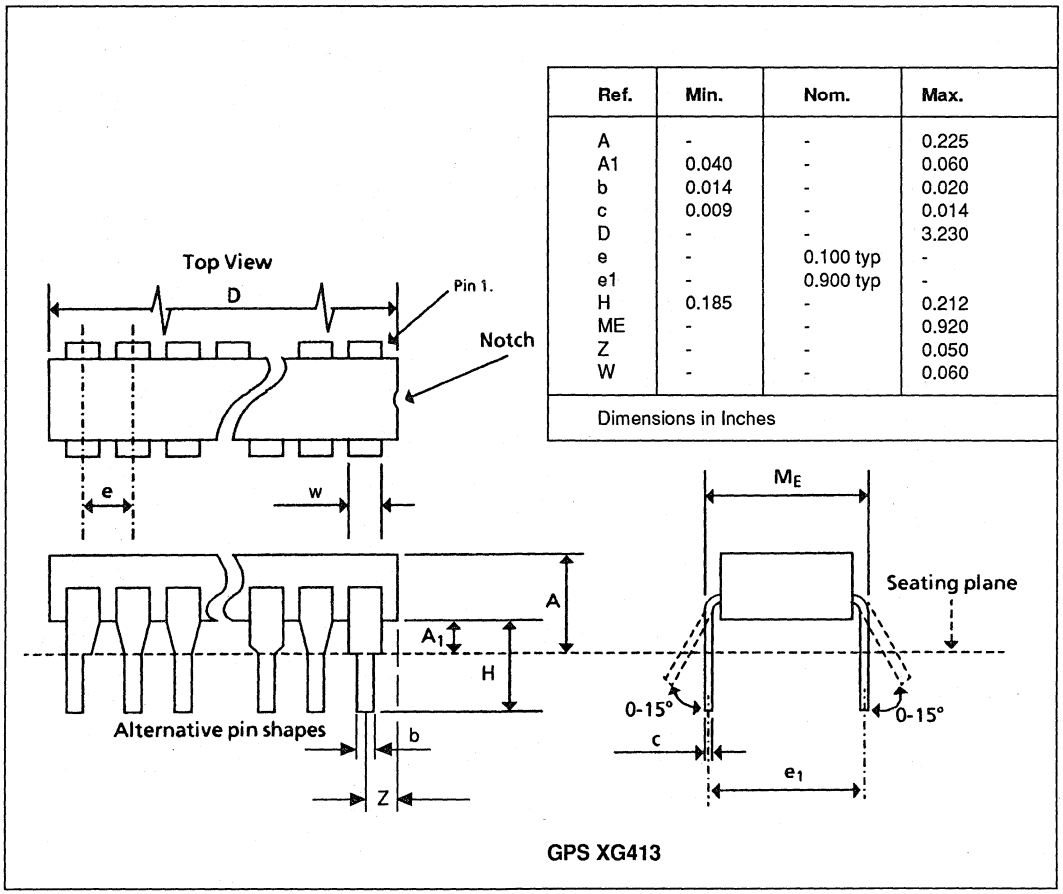


Figure 28b: Pin Assignment for Dual-In-Line (Type C) and Flatpack (Type F) Ceramic Modules

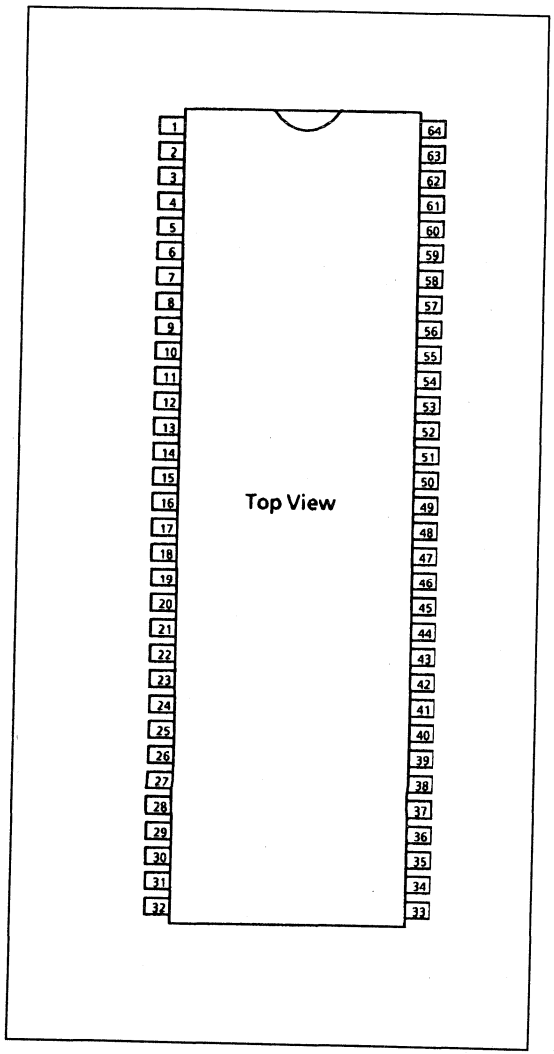
CERAMIC DUAL-IN-LINE
(MA17501 TO MA17503 - PACKAGE TYPE C)



Ref.	Min.	Nom.	Max.
A	-	-	0.225
A1	0.040	-	0.060
b	0.014	-	0.020
c	0.009	-	0.014
D	-	-	3.230
e	-	0.100 typ	-
e1	-	0.900 typ	-
H	0.185	-	0.212
ME	-	-	0.920
Z	-	-	0.050
W	-	-	0.060

Dimensions in Inches

Figure 29a: Dimensioned Drawing



Pin No.	17501	17502	17503
1	OSC	IRN	ILLADN
2	NC	VDD	DTON
3	SYSCLK1N	PIFN	SYNCLKN
4	SYNCLKN	AD00	DSN
5	CLKPCN	AD01	INTREN
6	CLK02N	AD02	CONFWN
7	AS	AD03	IRDYN
8	DSN	AD04	M/ION
9	GND	AD05	DMAKN
10	M/ION	AD06	DMAE
11	RD/WN	AD07	DMARN
12	GND	AD08	M04
13	IN/OPN	AD09	M05
14	INTREN	AD10	M06
15	PIFN	AD11	TCLK
16	M19	AD12	AD00
17	M18	AD13	AD01
18	M17	AD14	AD02
19	M16	AD15	AD03
20	M15	CLK02N	AD04
21	M14	CLKPCN	AD05
22	M13	M19	AD06
23	M12	M18	AD07
24	M11	M17	AD08
25	M10	M16	AD09
26	M09	M15	AD10
27	M08	M14	AD11
28	M07	M13	AD12
29	M06	M12	AD13
30	M05	M11	AD14
31	M04	M10	AD15
32	M03	M09	GND
33	M02	M08	MSTOPN
34	M01	NC	SURE
35	M00	M07	NPU
36	TESTN	M06	DDN
37	AD15	M05	DTIMERN
38	AD14	M04	TGON
39	AD13	M03	TGCLK
40	AD12	M02	CDN
41	NC	M01	PIFN
42	VDD	GND	MPROEN
43	AD11	CS	MPEN
44	AD10	M00	PIOPEN
45	AD09	CC00	DMAPEN
46	AD08	CC01	EXADEN
47	AD07	CC02	PIOXEN
48	AD06	CC03	FLT7N
49	AD05	CC04	SYSFN
S0	AD04	CC05	VDD
S I	AD03	CC06	IRN
52	GND	CC07	PAUSEN
53	AD02	CC08	OVI
S4	AD01	CC09	PWRDN
55	AD00	CC10	INT02N
56	HOLDN	CC11	INT08N
57	RESET	ROMONLYN	INT10N
58	HLDAKN	NC	INT11N
S9	PAUSEN	GND	IOI1N
60	T1	NC	INT13N
61	OVIN	NC	I0I2N
62	IRDYN	T1	INTI5N
63	RDYN	RESET	HLDAKN
64	SYNCN	HOLDN	NC

Figures 29b: Pin Assignments

LEADLESS CHIP CARRIER
(MA17501 TO 3 - PACKAGE TYPE L)

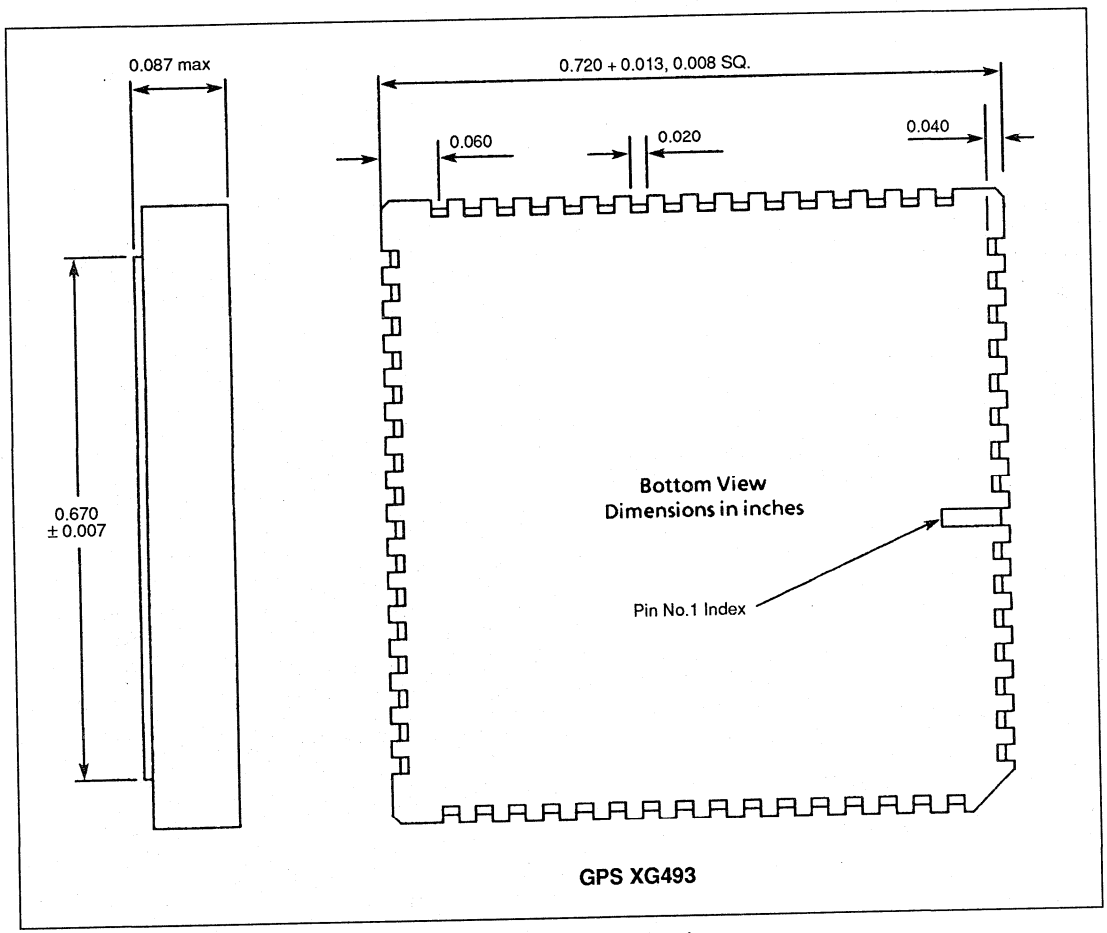
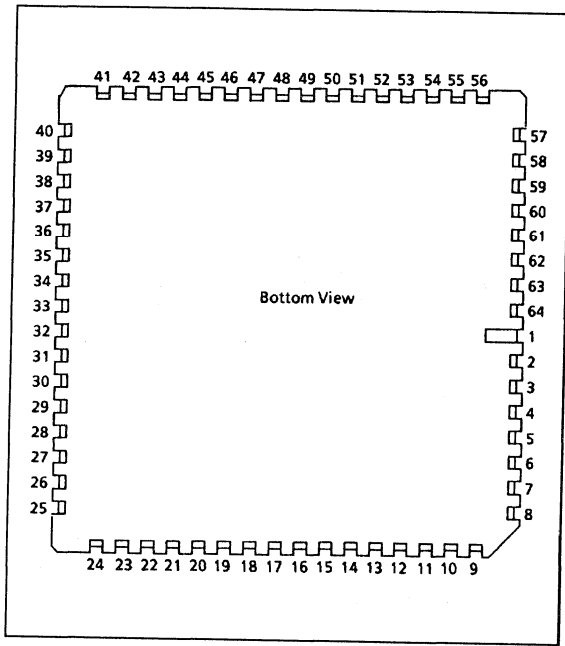


Figure 30a: Dimensioned Drawing



Pin No.	17501	17502	17503
1	OSC	IRN	ILLADN
2	NC	VDD	DTON
3	SYSCLK1N	PIFN	SYNCLKN
4	SYNCLKN	AD00	DSN
S	CLKPCN	AD01	INTREN
6	CL K02N	AD02	CONFWN
7	AS	AD03	IRDYN
8	D5N	AD04	M/ION
9	GND	AD05	DMAKN
10	M/ION	AD06	DMAE
11	RD/WN	AD07	DMARN
12	GND	AD08	M04
13	IN/OPN	AD09	M05
14	INTREN	AD10	M06
1S	PIFN	AD11	TCLK
16	M19	AD12	AD00
17	M18	AD13	AD01
18	M17	AD14	AD02
19	M16	AD15	AD03
20	M15	CLK02N	AD04
21	M14	CLKPCN	AD05
22	M13	M19	AD06
23	M12	M18	AD07
24	M11	M17	AD08
25	M10	M16	AD09
26	M09	M15	AD10
27	M08	M14	AD11
28	M07	M13	AD12
29	M06	M12	AD13
30	M05	M11	AD14
31	M04	M10	AD15
32	M03	M09	GND
33	M02	M08	MSTOPN
34	M01	NC	SURE
35	M00	M07	NPU
36	TESTN	M06	DDN
37	AD15	M05	DTIMERN
38	AD14	M04	TGON
39	AD13	M03	TGCLK
40	AD12	M02	CDN
41	NC	M01	PIFN
42	VDD	GND	MPROEN
43	AD11	CS	MPEN
44	AD10	M00	PIOPEN
45	AD09	CC00	DMAPEN
46	AD08	CC01	EXADEN
47	AD07	CC02	PIOXEN
48	AD06	CC03	FLT7N
49	AD05	CC04	SYSFN
50	AD04	CC0S	VDD
51	AD03	CC06	IRN
52	GND	CC07	PAUSEN
53	AD02	CC08	OVI
54	AD01	CC09	PWRDN
55	AD00	CC10	INT02N
56	HOLDN	CC11	INT08N
57	RESET	ROMONLYN	INT10N
58	HLDAKN	NC	INT11N
59	PAUSEN	GND	IOI1N
60	T1	NC	INT13N
61	OVIN	NC	IOI2N
62	IRDYN	T1	INT15N
63	RDYN	RESET	HLDAKN
64	SYNCN	HOLDN	NC

Figures 30b: Pin Assignments

TOPBRAZE FLATPACK
(MA17501 TO 3 - PACKAGE TYPE F)

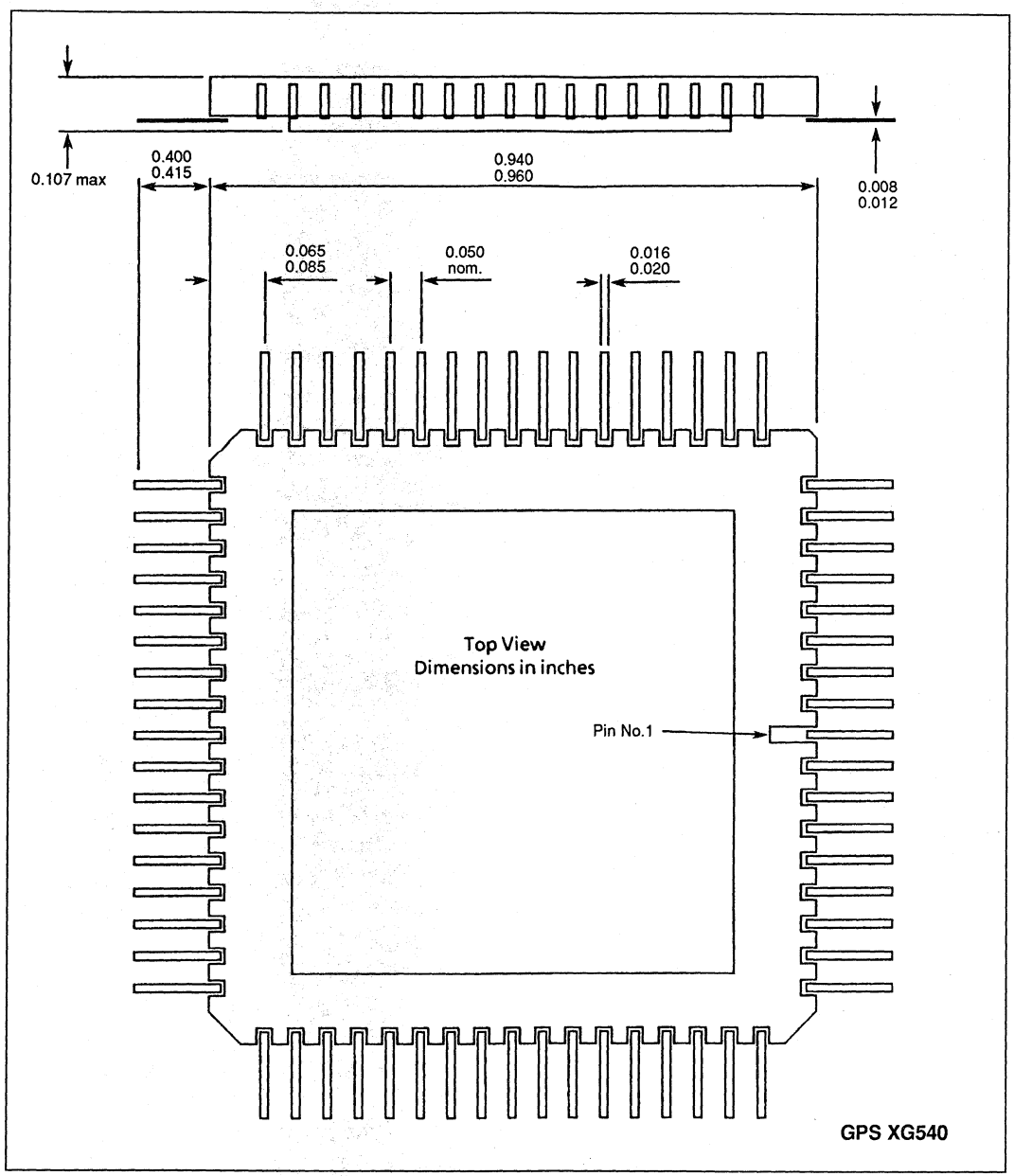
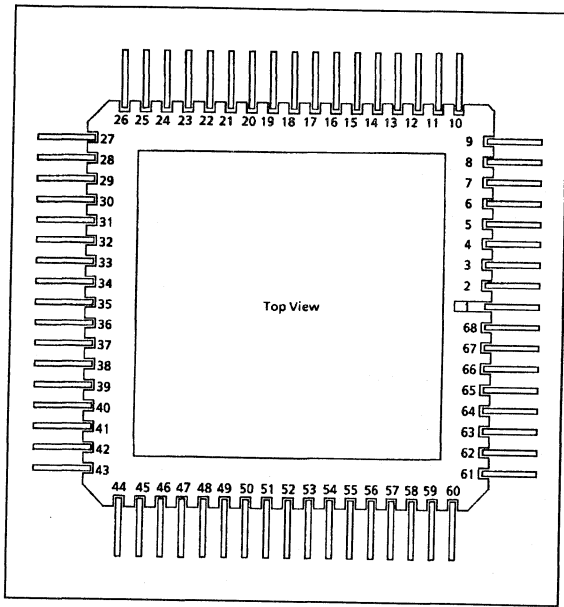


Figure 31a: Dimensioned Drawing



Pin No	17501	17502	17503
1	OSC	IRN	NC
2	NC	NC	ILLADN
3	NC	VDD	DTON
4	SYSCLKIN	PIFN	SYNCLKN
5	SYNCLKN	AD00	DSN
6	CLKPCN	AD01	INTREN
7	CLK02N	AD02	CONFWN
8	AS	AD03	IRDYN
9	DSN	AD04	M/ION
10	NC	AD05	DMAKN
11	GND	AD06	DMAE
12	M/ION	AD07	DMARN
13	RD/WN	AD08	M04
14	GND	AD09	M05
15	NC	AD10	M06
16	IN/OPN	AD11	TCLK
17	INTREN	AD12	AD00
18	PIFN	AD13	AD01
19	M19	AD14	AD02
20	M18	AD15	AD03
21	M17	CLK02N	AD04
22	M16	CLKPCN	AD05
23	M15	M19	AD06
24	M14	M18	AD07
25	M13	M17	AD08
26	M12	M16	NC
27	M11	M15	AD09
28	M10	M14	AD10
29	M09	M13	AD11
30	M08	M12	AD12
31	M07	M11	AD13
32	M06	M10	AD14
33	M05	M09	AD15
34	M04	M08	NC
35	M03	NC	GND
36	M02	NC	MSTOPN
37	M01	M07	SURE
38	M00	M06	NPU
39	TESTN	M05	DDN
40	AD15	M04	DTIMERN
41	AD14	M03	TGON
42	AD13	M02	TGCLK
43	AD12	M01	CDN
44	NC	NC	PIFN
45	NC	GND	MPROEN
46	VDD	CS	MPEN
47	AD11	M00	PIOPEN
48	AD10	CC00	DMAPEN
49	AD09	CC01	EXADEN
50	AD08	CC02	PIOXEN
51	AD07	CC03	FLT7N
52	AD06	CC04	SYSFN
53	AD05	CC05	VDD
54	AD04	CC06	NC
55	AD03	CC07	IRN
56	GND	CC08	PAUSEN
57	AD02	CC09	OVI
58	AD01	CC10	PWRDN
59	AD00	CC11	INT02N
60	HOLDN	ROMONLYN	INT08N
61	RESET	NC	INT10N
62	HLDAKN	GND	INT11N
63	PAUSEN	NC	IOI1N
64	T1	NC	INT13N
65	OVIN	NC	IOI2N
66	IRDYN	T1	INT15N
67	RDYN	RESET	HLDAKN
68	SYNCN	HOLDN	NC

Figure 31b: Pin Assignments

11.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019 Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 32: Radiation Hardness Parameters

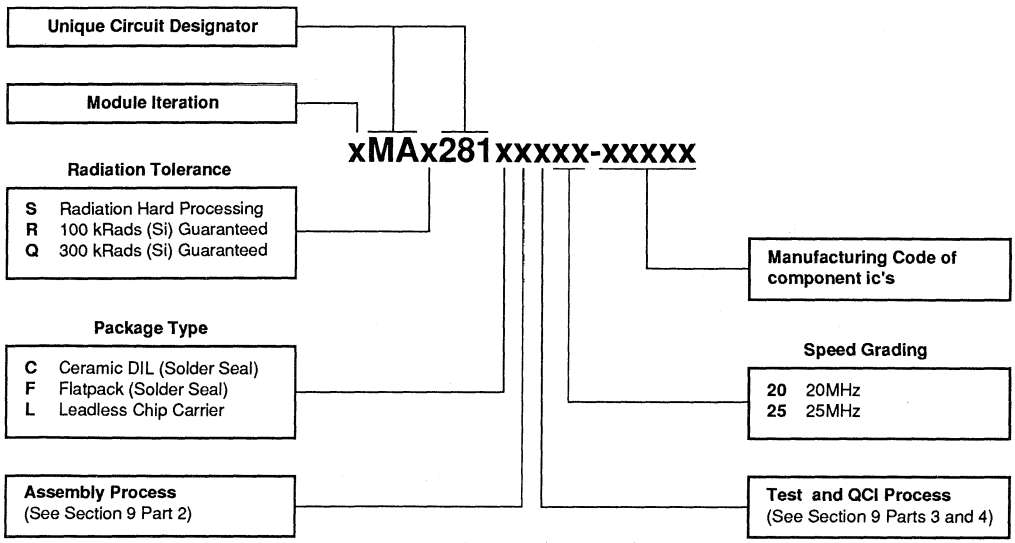
12.0 ORDERING INFORMATION

The processor can be ordered in the form of a module, consisting of three chips in leadless chip carriers, mounted on a ceramic tile. The module can be supplied with dual-in-line (C) or flatpack (F) lead configurations.

The three chips which form the processor can be packaged as separate devices. They are available in leadless chip carrier (L), flatpack (F), or ceramic dual-in-line packages (C).

Module - MAx281xxx

Chip Set - MAx17501xxx
MAx17502xxx
MAx17503xxx



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3564-3.4

MA17501

RADIATION HARD MIL-STD-1750A EXECUTION UNIT

The MA17501 Execution Unit is a component of the GEC Plessey Semiconductors MAS281 chip set. Other chips in the set include the MA17502 Control Unit and the MA17503 Interrupt Unit. Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit. These chips in conjunction implement the full MIL-STD-1750A Instruction Set.

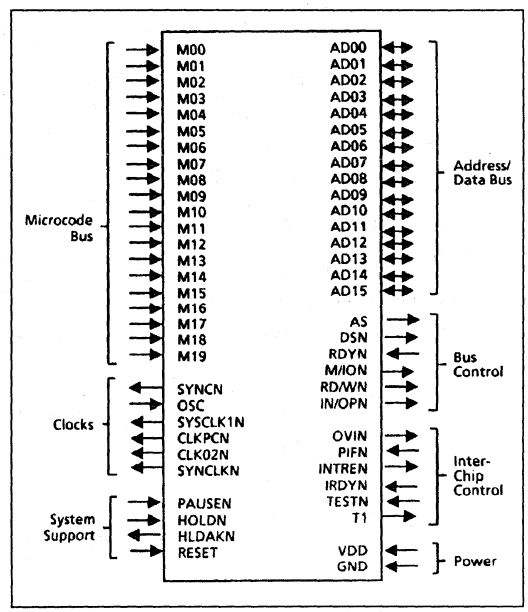
The MA17501 - consisting of a full function 16-bit ALU, 24 x 16-bit dual-port RAM register file, 32-bit barrel shifter, 4 x 24-bit parallel multiplier, synchronisation clock generation logic, and microcode decode logic - provides all computational, logical, and synchronisation functions for the chip set. Table 1 provides brief signal definitions.

The MA17501 is offered in several package styles including; dual-in-line, flatpack and leadless chip carrier. Full packaging information is given at the end of the document.

FEATURES

- MIL-STD-1750A Instruction Set Architecture
- Full Performance over Military Temperature Range (-55°C to +125°C)
- Radiation Hard CMOS/SOS Technology
- 16-Bit Bidirectional Address/Data Bus
- 16-Bit Full Function Registered ALU
- 32-Bit Barrel Shifter
- 24 x 16-Bit Dual-Port RAM File
  - 16 User Accessible General Purpose Registers
  - 8 Microcode Accessible Registers
- 4 x 24-Bit Parallel Multiplier
  - 48-Bit Accumulator
  - 16-Bit x 16-Bit Multiply in 4 Machine Cycles
- Instruction Pre-Fetch
- MAS281 Integrated Built-in Self Test
- TTL Compatible System Interface

BLOCK DIAGRAM



1.0 SYSTEM CONSIDERATIONS

The MA17501 Execution Unit (EU) is a component of the GEC Plessey Semiconductors MAS281 chip set. This chip set implements the full MIL-STD-1750A instruction set architecture. The other chips in the set are the MA17502 Control Unit (CU) and the MA17503 Interrupt Unit (IU). Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit (MMU(BPU)).

Figure 1 depicts the relationship between the chip set components. The EU provides the arithmetic and logical computation resources for the chip set. The EU also provides program sequencing logic in support of branching and subroutine functions. The IU provides interrupt and fault handling resources, DMA interface control signals, and the three MIL-STD-1750A timers. The EU and IU are each controlled by microcode from the CU. The MMU(BPU) may be configured to provide 1M-word memory management (MMU) and/or 1K-word memory block write protection (BPU) functions.

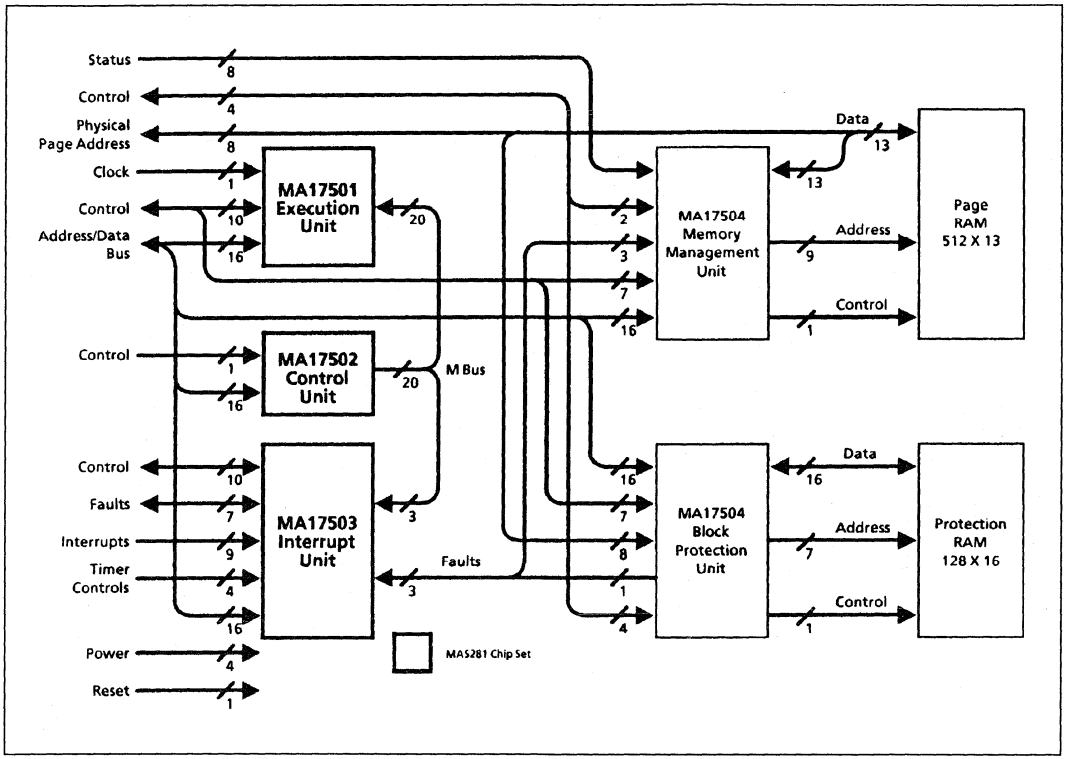


Figure 1: MAS281 Chip Set with Optional MA17504 and Support RAMs

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of a MA31751 allows access to a 1M-word address space and/or provides hardware support for 1K-word memory block write protection.

The EU, as with all components of the MAS281 chip set, is fabricated with GEC Plessey Semiconductors CMOS/SOS process technology. Input and output buffers associated with signals external to the MAS281 are TTL compatible.

Detailed descriptions of the EU's companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and DAIS mix benchmarking analysis are provided in separate applications notes.

The Execution Unit consists of a full function 16-bit ALU, 32-bit barrel shifter, 4 x 24-bit parallel multiplier, 24 x 16bit dual-port RAM register file, processor status word register, three operand transfer registers, three instruction fetch registers, various interconnect buses, synchronization clock generation logic, and microcode decode logic. Details of these components are depicted in Figure 2 and are discussed below:

2.0 ARCHITECTURE

2.1 ALU

The ALU is a full function 16-bit arithmetic/logic unit capable of performing arithmetic and logic operations on either one or two 16-bit operands in a single machine cycle. In addition to operand manipulation, the ALU is used to compute memory addresses.

The ALU supports 16-bit fixed-point single-precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit floating-point extended-precision data in two's complement representation. Double-precision and extended-precision operands are passed through the ALU 16 bits at a time on consecutive machine cycles. Machine flags provide an indication of ALU results and are used to set condition status (CS) bits C, P, Z, and N in the Status Word Register. Condition status bits and the Status Word register are discussed below.

Signal	I/O	Definition
AD00 - AD15	I/O	External 16-Bit Address/Data Bus
AS	O/Z	Address Strobe Indicates Address Information on A/D Bus
$\overline{\text{CLKPC}}$	O	Precharge Clock
$\overline{\text{CLK02}}$	O	Phase 2 Clock
$\overline{\text{PAUSE}}$	I	DMA Acknowledge (A/D Bus to be used for DMA)
$\overline{\text{DS}}$	O/Z	Data Strobe Indicates Data Information on A/D Bus
$\overline{\text{HLDAK}}$	O	Hold Acknowledge
$\overline{\text{HOLD}}$	I	Hold Request Suspends Internal Processor Functions
IN/$\overline{\text{OP}}$	O/Z	Instruction/Operand Indicates Type of Memory Access
$\overline{\text{INTRE}}$	O	Interrupt Enable
$\overline{\text{IRDY}}$	I	Interrupt Unit Ready Signal
M/$\overline{\text{IO}}$	O/Z	Memory or Input/Output Indicates Transaction on A/D Bus
M00 - M19	I	20-Bit Microcode Bus
OSC	I	External Oscillator Clock
$\overline{\text{OVI}}$	O	Overflow Indicator
$\overline{\text{PIF}}$	I	Privileged Instruction Fault
RD/$\overline{\text{W}}$	O/Z	Read/Write IndicatesData Direction on A/D Bus
$\overline{\text{RDY}}$	I	Ready Informs CPU of the Conclusion of External Bus Cycle
$\overline{\text{RESET}}$	I	Reset Indicates Device Initialization
$\overline{\text{SYNCLK}}$	O	Interrupt Unit's Sync Clock
$\overline{\text{SYNC}}$	O	System Clock - CPU Sync Clock (External)
$\overline{\text{SYSCLK1}}$	O	System Clock (Internal)
$\overline{\text{TEST}}$	I	Test Enable
T1	O	Branch or Jump Control
VDD		Power (External), 5 Volts
GND		Ground

Table 1: Signal Definitions

2.2 BARREL SHIFTER

The Barrel Shifter is a 32-bit input, 16-bit output right shift network. A 32-bit operand may be shifted right arithmetically, logically, or cyclically up to 31 bit positions in a single machine cycle. While not directly accessible or visible to user programs, the Barrel Shifter is utilized by microcode to effect all shift, rotate, and normalize instructions with minimum execution time.

2.3 PARALLEL MULTIPLIER

The Parallel Multiplier performs a 4-bit multiplier by 24-bit multiplicand multiplication plus accumulation in a single machine cycle. Only four machine cycles are required to complete a 16-bit by 16-bit multiplication. Contained within the multiplier is a 48-bit product accumulation register with the lower 24 bits serving as a source operand register.

On each multiply machine cycle, the lower four bits of the accumulator are multiplied by 24 bits from the two ALU operand source buses (R and S). The lower 24 bits of this 28-bit product are then added to the upper 24 bits of the accumulator and the whole accumulator is shifted right four bits. This right shift makes room for the upper four bits of the product. The four bits shifted out are used in the next multiply iteration.

2.4 DUAL-PORT REGISTER FILE

The Register File is a dual port RAM structure containing 24, 16-bit registers. Sixteen of these registers are general purpose and user accessible. These user accessible registers - referred to as R0 through R15 - may be used as accumulators, index registers, base registers temporary operand registers, or stack pointers. The remaining eight registers are only accessible by microcode.

Adjacent registers are concatenated to effectively form 32-bit and 48-bit registers for storage of double precision and extended-precision operands, respectively. Instructions access these operands by specifying the register containing the most significant part of the operand, and the register set wraps around automatically under microcode control, e.g., R15 concatenates with R0 for 32-bit operands and R15 concatenates with R0 and R1 for 48-bit operands.

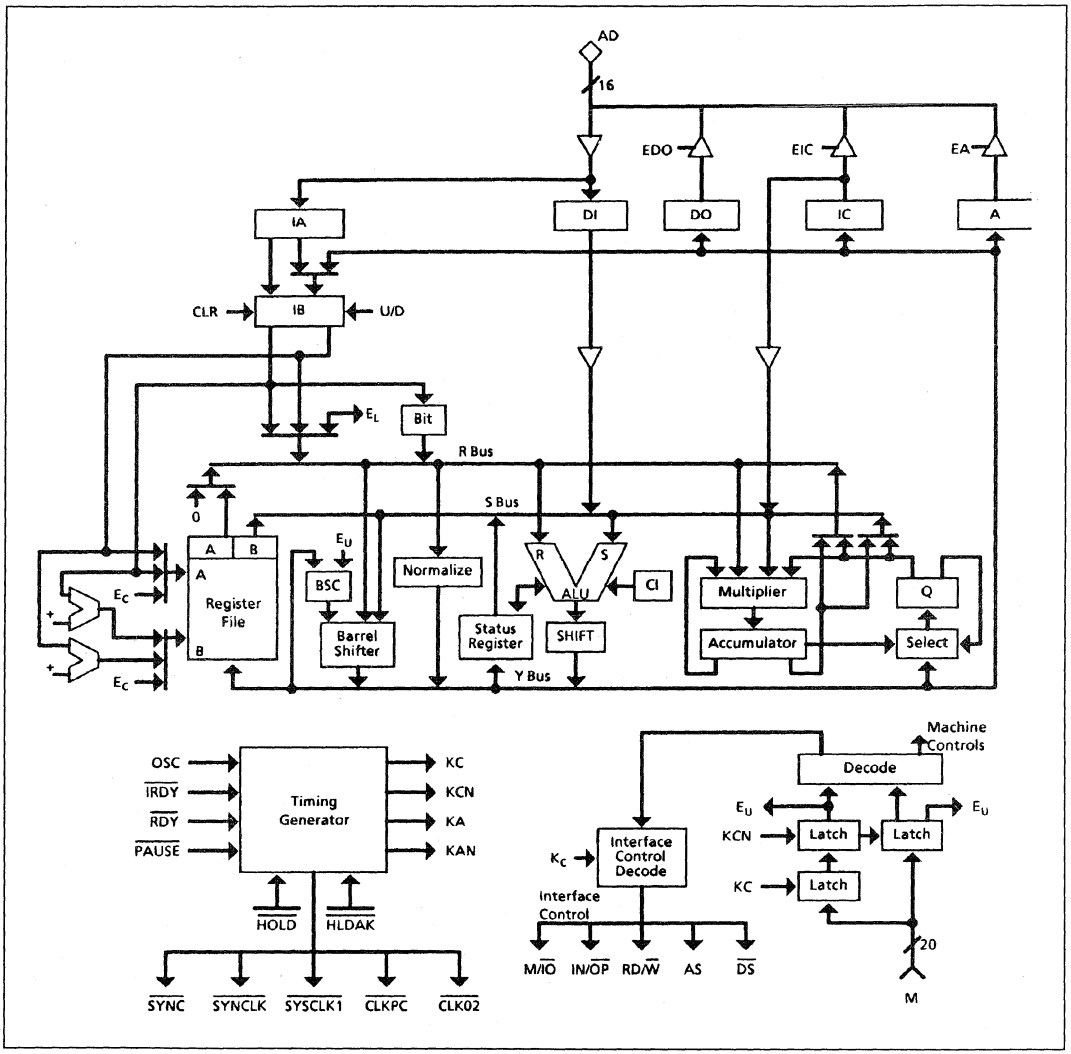


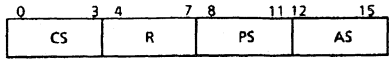
Figure 2: MA17501 Execution Unit Architecture

2.5 STATUS WORD REGISTER

The Status Word Register (SW) holds the condition status (CS) bits C, P, Z, and N generated by ALU operations. The SW also stores the address state (AS) and processor state (PS) fields. Figure 3 defines the Status Word Register storage format. The CS bits are stored with each logical, shift, and arithmetic operation performed by the ALU as required by MIL-STD-1750A and remain valid until changed by subsequent operations. The CS bits are interrogated during "jump on condition" and "instruction counter relative" MIL-STD-1750A branch instructions.

2.6 OPERAND TRANSFER REGISTERS

The Address (A), Data Output (DO), and Data Input (DI) registers are referred to as Operand Transfer Registers. These registers serve as storage buffers between internal EU buses and the EU's externally accessible address/data (AD) Bus. The DO register buffers data transferred from the EU to the AD Bus. The A register buffers operand addresses and XIO commands onto the AD Bus. The DI register buffers data transferred from the AD Bus to the EU .



Field	Bits	Description
CS		CONDITION STATUS:
	0	C- Carry from an addition or no borrow from a subtraction
	1	P- Result >0
	2	Z- Result = 0
	3	N- Result < 0
R	4 - 7	RESERVED
PS	8 - 11	PROCESSOR STATE: (a)- Memory access key code (b)- Privileged instruction enable
AS	12 - 15	ADDRESS STATE: Page register sets for expanded memory addressing

Figure 3: Status Word Format

2.7 INSTRUCTION FETCH REGISTERS

The Instruction Counter (IC), Instruction A (IA), and Instruction B (IB) registers allow sequential instruction fetches to be performed without assistance from the ALU. The IC register, which holds the 16-bit address of the next instruction to be fetched from memory, is loaded automatically by reset, jump, or branch operations. Once loaded, it functions as a dedicated counter to sequence from one instruction to the next. The current IC contents may be stored in registers R0 through R15 or in memory (pushed onto a stack) to provide return linkages for subroutine calls. As part of the microcoded interrupt handling routine the IC is saved in memory via the interrupt linkage pointer.

Registers IA and IB provide an instruction look-ahead capability. In the case of 16-bit instructions, IB holds the instruction currently executing while IA holds the next instruction to be executed. In the case of 32-bit instructions, IB and IA each hold half of the instruction. IA and DI (DI stores the immediate operands) are loaded as the instruction in IA is transferred to IB for execution; if the instruction in IB uses an immediate operand, IA is reloaded with the next instruction while DI maintains the immediate data. This overlapping of operations allows higher performance levels to be achieved.

2.8 BUSES

Three 16-bit wide buses (R, S, and Y) interconnect the EU data storage and computational elements. The R and S buses accept operands from selected EU data storage elements and route them to inputs of selected EU computational elements. The Y, or destination, bus serves to route computational results either back to EU data storage and computational elements or to the various operand transfer registers.

A 16-bit multiplexed Address/Data (AD) Bus provides a communications path between the EU, other components of the MAS281 chip set, and any other devices mapped into the chip set's address space. Data transfers between the AD Bus and the R, S, and Y buses are buffered by the operand transfer registers.

A 20-bit multiplexed microcode (M) bus provides a pathway between the Control Unit (CU) and the Execution Register (E) buffered microcode decode logic on the EU chip. Microcode placed on this bus by the CU controls all actions of the EU.

2.9 SYNCHRONISATION CLOCK GENERATION LOGIC

The Execution Unit generates all of the synchronisation clocks required by the chip set and CPU system. The EU converts an externally supplied oscillator signal into five synchronisation signals: SYNCN, SYSCLK1N,SYNCLKN, CLKPCN, CLK02N. The EU generates SYNCN for elements external to the chip set whereas SYNCLKN and SYSCLK1N are generated for the Interrupt Unit and internal EU synchronisation, respectively. SYSCLK1N is also brought out on a pin for use by external monitoring systems. The EU generates CLKPCN and CLK02N for use in the Control Unit. The CU uses CLKPCN to precharge the M Bus and transmit the first microword while CLK02N is used to transmit microword two.

The EU also contains the wait state generation interface. Failure of memory or I/O subsystems to drive RDYN low at the proper time during the DSN pulse causes the EU to hold SYNCLKN, SYNCN, SYSCLK1N, and CLKPCN in the high state; CLK02N, AS and DSN, in the low state; and RD/WN, IN/OPN and M/ION in their current states for one or more oscillator cycles beyond the end of the normal five OSC cycle machine cycle. When RDYN is asserted low, the EU allows the machine cycle to conclude at the high-to-low transition of the current oscillator cycle. This will allow all the synchronisation and control signals to resume normal operation.

Additionally, IRDYN is used to signal completion of internal I/O command control of the Interrupt Unit (IU). The IU thus can extend the duration of the above mentioned bus signals. Failure of the IU to drive IRDYN low at the proper time during the DSN low pulse causes the EU to hold SYNCLKN, SYNCN, SYSCLK1N, and CLKPCN in the high state; CLK02N, AS, and DSN in the low state; and IN/OPN, M/ION, and RD/WN in the state for the normal five OSC cycle machine cycle. When the IU asserts IRDYN low, the EU allows the machine cycle to conclude at the high-to-low transition of the current oscillator cycle. This will allow all the synchronisation and control signals to resume normal operation.

[NOTE: Whenever the EU is executing a machine cycle which requires IRDYN to drop low for completion, the machine cycle will be a minimum of six OSC cycles long. The maximum duration of this machine cycle depends on the length of time that the IU holds IRDYN high.]

3.0 INTERFACE SIGNALS

All signals comply with the voltage levels of Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND. A 500-ohm pull-up at the OSC input pin is recommended to damp line reflections.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix, e.g., HOLDN. Referenced signals that are not found on the MA17501 are preceded by the originating chip's functional acronym in parentheses, e.g., (IU)DMARN.

A description of each pin function, grouped according to functional interface, follows. The function acronym is presented first, followed by its definition, its type, and its detailed description. Function type is either input, output, high impedance (Hi-z), or a combination thereof. Timing characteristics of each of the functions described is provided in Section 5.0.

3.1 POWER INTERFACE

The power interface consists of one 5V VDD connection and three common GND pins.

3.2 CLOCKS

The Execution Unit provides the synchronisation clocks for the MAS281 chip set. Together these clocks form the basic operation cycle.

3.2.1 Oscillator (OSC)

Input. The MA17501 requires a single external oscillator input for operation. The EU converts the oscillator into the five other clocks listed in this section. To minimise skew between OSC edges and signals derived from OSC, the OSC rise and fall times should be minimised. It is recommended that a clock driver with high drive capability, such as a 54AS244, 54ALS244 or 54HST240, be used to drive the OSC input.

In order to avoid double clocking due to line reflections, a 500-ohm pull-up resistor, placed close to the EU, is recommended.

3.2.2 Synchronisation Clock (SYNCN)

Output. The MA17501 provides the MAS281 Synchronisation Clock output to synchronise external circuitry to the MAS281 machine cycle. The high-to-low transition of this signal indicates the start of a new machine cycle.

SYNCN cycles associated with external memory or I/O bus transactions are a minimum of five OSC cycles in duration and may be extended by inserting wait states via the RDYN input. SYNCN low indicates that either an address or XIO command is on the AD Bus; a high indicates data is on the bus. Wait states extend the high state of SYNCN.

SYNCN cycles associated with internal CPU operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[NOTE: For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a SYNCN cycle of seven OSC cycles duration. Though unlikely, this condition must be taken into account in implementing a RDYN generation circuit. Refer to the description of the RDYN signal for further details].

3.2.3 IU Synchronisation Clock (SYNCLKN)

Output. The SYNCLKN signal is a logical equivalent of the SYNCN signal provided for Interrupt Unit synchronisation.

3.2.4 System Clock (SYSCLK1N)

Output. SYSCLK1N is the MA17501's synchronization clock. It is the logical equivalent of SYNCN and SYNCLKN with the exception that during PAUSEN low or during HLDAKN low, SYSCLK1N is held in its low state. SYSCLK1N, like SYNCLKN, has a VSS to VDD logic level swing.

3.2.5 Precharge Clock (CLKPCN)

Output. CLKPCN is used by the MA17502 Control Unit (CU) to synchronize the precharging of the internal M Bus and most other CU operations to the MAS281 machine cycle.

CLKPCN cycles associated with MAS281 external memory or I/O bus transactions are a minimum of five OSC cycles in duration and are extended when wait states are inserted via the RDYN input. CLKPCN low indicates that the internal CU M Bus is being precharged to the high state; the low-to-high transition places the lower 20 bits of a microinstruction on the external M Bus. Wait states extend the high state of CLKPCN. When PAUSEN or HLDAKN is low, CLKPCN is held low.

CLKPCN cycles associated with internal MAS281 operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[NOTE: For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a CLKPCN cycle of seven OSC cycles duration.]

3.2.6 Phase 2 Clock (CLK02N)

Output. CLK02N is used by the MA17502 Control Unit (CU) in conjunction with CLKPCN to synchronize microinstruction transmission on the M Bus to the MAS281 machine cycle.

CLK02N cycles associated with MAS281 external memory or I/O bus transactions are a minimum of five OSC cycles in duration and are extended when wait states are inserted via the RDYN input.

The high-to-low transition of CLK02N places the upper 20 bits of a microinstruction on the external M Bus. Wait states extend the trailing (based on SYNCN high-to-low beginning the machine cycle) low state of CLK02N. When PAUSEN or HLDAKN is low, CLK02N is held high.

CLK02N cycles associated with internal MAS281 operations are either five or six OSC cycles in duration. Six OSC cycles are required for machine cycles associated with microcode branches or with the execution of internally (Interrupt Unit) decoded XIO commands. Five OSC cycles are used for all other internal operations, e.g., register to register transfers, ALU functions, etc.

[NOTE: For MAS281s operating at high OSC frequencies, the Interrupt Unit logic that creates IRDYN may cause a wait state to be inserted during execution of internal XIO commands. This would result in a CLK02N cycle of seven OSC cycles duration.]

3.3 BUS CONTROL

This group of signals is provided to control Address/Data (AD) bus transmissions (See Figure 4). The signals indicate when address or data information is on the AD Bus and what type of transaction is taking place during a particular machine cycle.

3.3.1 Address Strobe (AS)

Output/Hi-z. AS high indicates that the Address/Data (AD) Bus contains address information. The address information is assured stable at the high-to-low transition of this signal. In this way, AS provides the necessary control for a system Address Bus transparent latch system interface.

The Interrupt Unit uses AS to extract the XIO command information off the AD Bus for internally decoded XIO commands, and the Memory Management Unit/Block Protection Unit (MMU(BPU)) uses AS to extract address information for memory management and block protection functions, and to extract XIO command information for MMU(BPU) decoded XIO commands.

AS is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. During internal non-AD Bus related CPU operations, AS is held low for the entire machine cycle via microcode control.

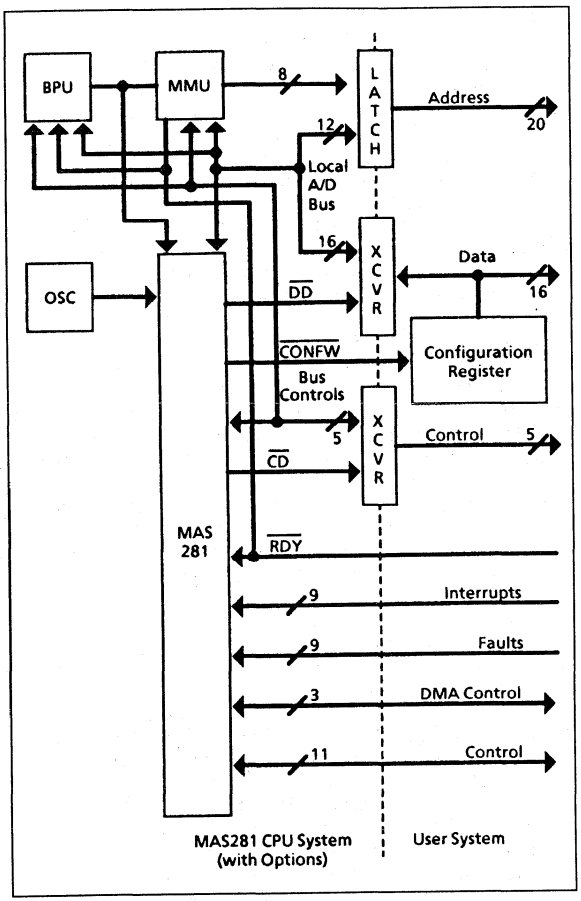


Figure 4: Typical MAS281/MA17504 System Interface

3.3.2 Data Strobe (DSN)

Output/Hi-z. DSN low indicates that data is on the AD Bus (write/output cycles) or that the MAS281 AD Bus drivers are in the high-impedance state (read/input cycles). For write/output cycles, the data is guaranteed stable at the low-to-high transition of DSN. For read/input cycles, the DSN low-to-high transition indicates the acceptance of data by the MAS281 (SYSCLK1N high-to-low transition latches AD Bus data into the IA and DI registers).

DSN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. DSN is held high, for the entire machine cycle, during internal non-AD Bus operations via microcode.

3.3.3 Read/Write (RD/WN)

Output/Hi-z. RD/WN defines the direction of data flow on the bidirectional AD Bus and provides read/write cycle information to the MMU(BPU) for write protection control. RD/WN high indicates a read/input bus cycle and data transfer to the MAS281. RD/WN low indicates a write/output bus cycle and data transfer from the MAS281.

This signal is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. RD/WN is placed in the high impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low.

3.3.4 Memory/Input-Output (M/ION)

Output/Hi-z. M/ION defines the type of device involved in the data transfer occurring on the AD Bus and provides functional control for the Interrupt Unit (IU) and the Memory Management Unit/Block Protection Unit (MMU(BPU)). The IU ignores memory transfer AD Bus activity and the MMU(BPU) uses M/ION to decide whether to decode the address information on the AD Bus as an MMU(BPU) XIO command or a memory address. M/ION high indicates a memory access, and M/ION low indicates an input-output operation.

This signal is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. M/ION is placed in the high impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low. M/ION is raised high, for the entire machine cycle, during internal non AD Bus operations via microcode.

3.3.5 Instruction/Operand (IN/OPN)

Output/Hi-z. IN/OPN high indicates an instruction is to be read from memory during the current AD Bus cycle. IN/OPN is low for all other MAS281 directed AD Bus transfers. The Memory Management Unit/Block Protection Unit (MMU(BPU)), when configured as a MMU, uses IN/OPN to select the proper page register set within the specified page register group.

IN/OPN is asserted at the SYNCN high-to-low transition and remains valid for the duration of the current SYNCN period. IN/OPN is placed in the high-impedance state during DMA cycles by PAUSEN low and during the Hold state by HLDAKN low.

3.3.6 Ready (RDYN)

Input. During external AD Bus transfers (those dealing with devices external to the MAS281 chip set), a low is required on this input to allow the MAS281 machine cycle to complete (high-to-low transition of SYNCN). RDYN high is used to prolong the data portion of the machine cycle (SYNCN high) to accommodate slow memory and I/O devices. The MAS281 assumes memory or I/O devices are NOT ready to provide (accept) data to (from) the AD Bus, and requires these devices to signal their readiness via the RDYN input.

A low on RDYN, enveloping the current machine cycle's fifth (or later) OSC cycle high-to-low transition, allows the current machine cycle to complete (SYNCN high-to-low transition) at the following low-to-high transition of the OSC input.

3.4 BUSES

The following is a discussion of the communication buses connecting the MA17501 to the other chips of the MAS281 set. The AD Bus transfers all data and instructions and the M Bus provides the microcode instructions from the MA17502.

3.4.1 Address/Data Bus (AD Bus)

Input/Output/Hi-z. These signals comprise a 16-bit bidirectional multiplexed address and data bus. During external bus transfers, the AD Bus accommodates the transfer of address and data information between the MA17501 and memory, or I/O ports. During internal bus operations, the AD Bus provides additional communication among the Execution, Control, Interrupt and Memory Management/Block Protection Units. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit address. A high on this bus corresponds to a logic one and a low corresponds to a logic zero.

Address information is valid on the bus at the AS high to-low transition. The RD/WN signal indicates the MA17501 AD Bus drivers state during the data portion of the bus cycle (DSN low) and the M/ION function defines the type of device the transfer is with. The AD Bus drivers are placed in the high impedance state during Read operations (DSN low), during DMA cycles by PAUSEN low, and during the Hold state by HLDAKN low.

3.4.2 Microcontrol Bus (M Bus)

Input. The M Bus is a 20-bit multiplexed microcontrol bus which provides microcoded control to the EU. The Control Unit multiplexes the 40-bit microcode instructions into two 20-bit words. The upper 20 bits are placed on the M Bus by the CLKPCN low-to-high transition and the lower 20 bits are placed on the M Bus by the trailing high-to-low transition of CLK02N. The microinstruction is reassembled in the EU's Execution (E) register and used to control EU functions during the next machine cycle. M19 is the most significant bit position and M00 is the least significant bit position for both microwords. The high order 20 bits are transmitted first, followed by the low order 20 bits of the microinstruction. A high on this bus corresponds to a logic one and low corresponds to a logic zero.

3.5 SYSTEM SUPPORT INTERFACE

The system support interface signals have control over functions that affect the chip set as a whole.

3.5.1 Processor Pause (PAUSEN)

Input. PAUSEN is driven low by the Interrupt Unit upon acknowledgement of a DMA transfer request. A low on PAUSEN causes the EU to place all the bus control signals (AS, DSN, M/ION, RD/WN, IN/OPN) and the AD Bus in the high impedance state, and to disable all clock outputs, except for SYNCLKN and SYNCN. The requesting device maintains control of the AD Bus and bus control lines until (IU)DMARN is raised high, thus causing PAUSEN to raise high.

It is recommended that the MAS281 chip set be buffered to the memory/input-output system. If an MMU(BPU) peripheral chip is used for memory expansion/protection it must reside on the MAS281 side of these buffer transceivers (see Figure 4). Thus, for a DMA device to access the MMU(BPU), the MAS281 AD Bus and bus control signal drivers must be in the high impedance state to allow the DMA device to drive these signals. The interrupt Unit also provides the CDN signal for the directional control of the bus control transceivers.

3.5.2 Processor Hold Request (HOLDN)

Input. A low on this input suspends all chip set functions (except SYNCN and SYNCLKN) at the end of the current MIL-STD-1750A instruction. The AD Bus and bus control functions (AS, DSN, M/ION, IN/OPN, RD/WN) are placed in the high impedance state permitting a monitor system to take control of the memory/input-output system. The internal synchronisation clocks are placed in an inactive state, which halts further instruction sequencing until HOLDN is released. As with DMA cycles, the reason for this is to allow access to the MMU(BPU) if an expanded memory system is used. The (IU)CDN output is provided for control bus transceiver directional control during the Hold state. This input should be synchronised to AS falling.

3.5.3 Processor Hold Acknowledge (HLDAKN)

Output. HLDAKN drops low after reaching the end of the MIL-STD-1750A instruction during which HOLDN was pulled low, or after encountering a BPT software instruction. The Hold state is terminated by raising HOLDN high (if HOLDN low initiated the Hold state), or by pulsing HOLDN low (if the Hold state was initiated by a BPT instruction). During the Hold state, software execution is suspended and the MAS281 interface functions are placed in the high impedance state to allow a monitor system to take control of the memory/input-output system.

3.6 INTER-CHIP CONTROL

The following signals perform control functions internal to the MAS281 chip set. These functions include microcode execution branching control and arithmetic error indication.

3.6.1 Internal Ready (IRDYN)

Input. The IRDYN signal is the means by which Interrupt Unit (IU) command cycles, involving the AD Bus, are completed. The IU drops IRDYN low when the XIO command has been decoded and allows the six OSC period machine cycle to complete. The IRDYN and RDYN signals are effectively ORed together to control the EU clock generation circuitry; therefore, RDYN should be high during IU decoded XIO commands.

3.6.2 Interrupt Unit Microinstruction Enable (INTREN)

Output. The Execution Unit controls the Interrupt Unit (IU) 3-bit microcode interface through the use of the INTREN signal. INTREN low enables the IU microcode decoding logic. IU functions handled through microcode are; enable/disable DMA interface XIO command control, set Normal Power-Up discrete, load fault register, and read encoded 4-bit vector identifying the highest priority pending interrupt.

Machine cycles during INTREN low are a special case of internal non-AD Bus operations. These cycles are denoted by a six OSC period machine cycle.

3.6.3 Overflow Indicator (OVIN)

Output. OVIN is an indication that a fixed-point overflow condition, as specified in MIL-STD-1750A, has occurred during an operation. The Interrupt Unit accepts this as an input to the pending interrupt register level four interrupt bit.

3.6.4 Privileged Instruction Fault (PIFN)

Input. PIFN low is an indication to the Execution Unit that a fault, requiring the current MIL-STD-1750A instruction to be aborted, has occurred. The faults that cause the instruction abort are 0, 5, and 8 which are, respectively, memory protect error ((IU)MPROEN low), an out-of-bounds memory/input-output address ((IU)EXADE low), or a bus fault timeout. In response to PIFN low, the EU maintains AS low, DSN high, and forces the M/ION signal high for two machine cycles. In addition, the EU will internally complete the current SYNCN cycle and resume operation. This allows the Control Unit to sequence to the interrupt handling routine without affecting the bus status.

3.6.5 Branch or Jump Control (T1)

Output. The Execution Unit raises the T1 signal high to indicate a microcode conditional branch condition is true. The Control Unit accepts T1 and feeds it into the microcode address multiplexer where microinstruction branches are effected.

3.6.6 Test Microword (TESTN)

Input. The TESTN signal is used during chip test to load 40-bit microinstructions into the EU execution register. TESTN low loads E39 (MSB) to E20, and TESTN high loads E19 to E00 (LSB). TESTN should be pulled-up to VDD in customer applications.

4.0 OPERATING MODES

The following discussions detail the MAS281 chip set operating modes from the perspective of the Execution Unit. MAS281 operating modes involving the MA17501 include: (1) Initialisation, (2) Instruction Execution, (3) Interrupt Servicing, (4) Fault Servicing, (5) DMA Support, and (6) Software Development Support.

4.1 INITIALISATION

RESET starts the chip set microcoded initialisation sequence, but also affects the Execution Unit Circuitry directly. When RESET is raised high, the Hold state acknowledge signal (HLDAKN) is forced high thus releasing the MAS281 from the Hold state (if changing HOLDN is unable to release the Hold state). RESET also forces the clock generation circuitry to create a five OSC period machine cycle by disabling state machine inputs that vary the machine cycle length.

Upon releasing RESET, the EU Hold State circuitry is enabled and the clock generation circuitry is allowed to function normally. HOLDN will not have an effect on chip set operation until the initialisation routine has completed because the microcode branch to the Hold routine is disabled.

The microcoded initialisation routine clears the Instruction Counter (IC), Status Word Register (SW), and Register File (R00-R15) and performs the BIT. The successful completion of the BIT is necessary to guarantee the register file is cleared at the end of the initialisation routine.

The microcoded BIT exercises all legal microinstruction bit combinations and tests all internally accessible structures of the MAS281. For the Execution Unit this includes the full Register Set, ALU, Multiplier, Barrel Shifter, and Macroflag logic. Table 2 details the tests performed by each of the five BIT subroutines.

If any part of BIT fails, an error code identifying the failed subroutine is loaded into the Interrupt Unit Fault Register (via the AD Bus), BIT is aborted, and NPU is left in the low state. Table 2 defines the coding of the BIT results. (INTREN enables microcode control of the Interrupt Unit (IU) to raise NPU high (if BIT passes) and load BIT error codes (if BIT fails) into the IU Fault Register).

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero (page zero) from the Start-Up ROM (if implemented). Whether or not BIT passes, the processor will begin instruction execution at this point.

[NOTE: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, the Timers A and B must be clocked for BIT success.]

BIT	Test Coverage	BIT Fail Codes ($FT_{13,14,15}$)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	166
3	Interrupt Unit - MK, PI, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15	110	154
5	Timer A Timer B	111	763
-	BIT Pass/Fail Overhead	-	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15.

Table 2: MAS281 BIT Summary

4.2 INSTRUCTION EXECUTION

Instruction execution is characterised by a variety of operations composed of various types of machine cycles. The Execution Unit contains the clock generation circuitry that creates the different machine cycles depending on the particular operation being performed at the time. These operations include: (1) internal CPU cycles, (2) instruction fetches, (3) operand transfers, and (4) input/output transfers. Instruction execution may be interrupted at the end of any individual machine cycle by the PAUSEN (denoting DMA operations) clock generation circuitry input, and at the beginning of any given MIL-STD-1750A instruction by an (IU)IRN or HOLDN low input to the Control Unit.

4.2.1 Internal CPU Cycles

All CPU data manipulation and housekeeping operations are performed using internal CPU cycles. Internal CPU cycles are either five or six OSC periods long and are characterised by AS low and DSN, (IU)DDN, and M/ION high. Section 5.0 provides timing characteristics for internal CPU cycles.

The majority of Internal CPU Cycles are five OSC period machine cycles. Six OSC period machine cycles occur when executing conditional jump or branch microinstructions; the EU is calculating the branch condition to determine the state of the T1 output signal.

4.2.2 Instruction Fetches

Instruction fetches are used to keep the instruction pipeline full. This ensures that the next instruction is ready for execution when the preceding instruction is completed.

During jump and branch instruction execution the pipeline is flushed, then refilled via two consecutive instruction fetches starting at the new instruction location. The pipeline is also refilled as part of the interrupt and Hold processing.

Instruction fetches are five (minimum) OSC period machine cycles characterised by IN/OPN, M/ION, and RD/WN high. Instruction fetches use pipeline registers IA and IB, the instruction counter (IC), and the data input register (DI). Assuming an empty instruction pipeline (as a result of a reset, jump or branch), the contents of IC are placed on the AD Bus as an address. The returned value (the instruction) is stored in the IA register. The IC register is incremented (dedicated counter mode) and the next fetch is performed.

This second returned value, which may be an instruction or an immediate operand, is stored in both the IA and DI registers as the previous contents of IA advance to the IB register to be decoded into their microcoded routine. If the second returned value is an immediate operand, a third instruction fetch will occur with the instruction being loaded into IA only; DI retains the immediate operand.

The data portion (SYNCN high) of instruction fetch cycles can be extended beyond their minimum five OSC periods by use of the RDYN signal. RDYN held high during the high-to-low transition of the machine cycles fifth OSC cycle will extend the data portion of the machine cycle. The machine cycle can be completed at any succeeding OSC cycle high-to-low transition by enveloping this OSC edge with RDYN low.

4.2.3 Operand Transfers

Operand transfers are used to obtain operands to be used by an instruction and to save any results of an instructions execution. Machine cycles associated with operand transfers are a minimum of five OSC periods in duration. The RDYN signal can be used to insert wait states into the data portion of the machine cycle (SYNCN high) to accommodate slow memory.

Operand transfers use the address register (A), data input register (DI), and data output register (DO). Before the operand transfer begins, the Execution Unit calculates the effective operand address and stores this value in A.

For write transfers the EU loads the operand into DO. For operand ready cycles the EU latches the operand from the AD Bus into DI at the SYSCLK1N high-to-low transition.

All operand transfers between the MAS281 and memory are referenced to the AS and DSN bus control signals and are characterised by IN/OPN low, M/ION and CDN high, and RD/WN (high, read; low, write).

The EU first places the contents of A on the AD Bus at the SYSCLK1N high-to-low transition. Shortly following, AS is raised high to enable the system address bus transparent latch. This address is assured valid at the high-to-low transition of AS. At the SYSCLK1N low-to high transition, DSN drops low to indicate the contents of DO have been placed on the AD Bus (write) or the EU AD Bus drivers have been placed in the high impedance state (read).

DSN subsequently raises high when the output data is stable, prior to SYSCLK1N dropping low, or raises high in response to SYSCLK1N dropping low to indicate the EU's acceptance of the input data.

All operand transfer cycles are allowed to complete via the RDYN input. During the data portion of the cycle the EU assumes memory is NOT READY, and requires RDYN low to signal the memory's readiness to complete the cycle. If RDYN is high at the high-to-low transition of the fifth OSC cycle within the operand transfer cycle, a wait state will be injected (one OSC period at a time) for each OSC high-to-low transition that RDYN remains high. Memory readiness, thus cycle completion, is signalled by RDYN low enveloping a subsequent OSC high-to-low transition.

4.2.4 Input/Output Transfers

Input/Output transfers are characterised by M/ION and IN/OPN low, and RD/WN (high, input; low, output). AS and DSN operate as during operand transfers. Two different types of input/output transfers are controlled by the Execution Unit: internal and external.

Internal I/O transfers involve all XIO commands that are decoded by the Interrupt Unit (IU) and use the local AD Bus to transfer response data. These commands are listed in Table 3 (the only exception is RCW; it is an IU decoded, IRDYN completed, External I/O command). Internal XIO commands implemented in the IU (per Table 3) use a six OSC period machine cycle and the IRDYN cycle completion input. Internal XIO commands implemented in the MA31751 MMU/BPU use a minimum five OSC period machine cycle. The system RDYN generator provides the RDYN cycle completion input to the EU.

The term "local AD Bus" in this context refers to the AD Bus on the processor side of the system data bus demultiplexing transceivers. The three chips of the MAS281 and the MA17504 (in either configuration) reside on the local AD Bus and communicate to the user system through the required address and data bus buffers, as depicted in Figure 4.

External I/O transfers involve all XIO and VIO instructions not included under Internal I/O transfers. They execute during a minimum five OSC period machine cycle that is extendible via RDYN, as previously described.

4.3 INTERRUPT SERVICING

Interrupts are latched into the Interrupt Unit (IU) pending interrupt register by the SYNCLKN high-to-low transition. The IU signals the Control Unit (CU) that an interrupt is pending and the CU branches to the microcoded interrupt handling routine at the completion of the currently executing MIL-STD-1750A instruction.

The EU supports the interrupt handling routine by enabling microcode control of the IU at the proper time via the INTREN signal and by calculating the memory addresses of the service and linkage pointers based on the 4-bit interrupt priority code transmitted by the IU. Machine cycles during which INTREN is low are six OSC periods in length. During these INTREN cycles, DSN and M/ION are high, and AS is low.

The EU also provides a hardwired interrupt to the IU. the OVIN interrupt signals a fixed-point arithmetic overflow.

4.4 FAULT SERVICING

The Interrupt Unit (IU) latches fault inputs into the fault register on the high-to-low transition of SYNCLKN. Faults other than 0, 5, and 8 latch a level one pending interrupt in the IU and the interrupt sequencing proceeds as previously explained. Faults 0, 5, and 8 caused during non-DMA AD Bus transactions demand more immediate attention; the MIL-STD-1750A instruction during which the fault occurred must be aborted.

PIFN indicates to the Control Unit that one of these faults has occurred and forces a branch to the "next instruction fetch" microinstruction so that the interrupt caused by the PIFN fault can be serviced immediately. Under normal instruction execution circumstances, the bus control signals would operate during the machine cycle between the fault and the instruction fetch machine cycle. PIFN causes the bus control signals AS and DSN to stay in their inactive state during this transitional machine cycle to allow the branch to the microcoded interrupt routine without performing any AD Bus transactions.

4.5 DIRECT MEMORY ACCESS

The Interrupt Unit DMA interface logic signals the Execution Unit (EU) that it has acknowledged a DMA request (PAUSEN low). PAUSEN low causes the EU to halt the synchronisation clocks CLK02N (high), CLKPCN (low), and SYSCLK1N (low); disables clock generation circuitry input that could vary the machine cycle length; and places all bus control signals and the AD Bus in the high impedance state. The SYNCN and SYNCLKN clocks continue to operate with a five OSC cycle period. Upon removal of PAUSEN by the Interrupt Unit, the MAS281 resumes microinstruction execution where it was interrupted.

4.6 SOFTWARE DEVELOPMENT SUPPORT

The Execution Unit responds to a HOLDN signal by suspending all internal operations upon completion of the currently executing instruction. Microcode, from the Control Unit, directs HLDAKN low during the third SYNCN cycle after HOLDN has been pulled low and the previous instruction has been completed. M/ION, RD/WN, IN/OPN, AS, DSN, and the AD Bus are placed in the high impedance state permitting a monitor system to take control of the memory/input-output system. Raising HOLDN releases the MAS281 from the Hold state and instruction execution begins by refilling the pipeline.

The execution of a BPT instruction also causes HLDAKN to drop low and the bus control signals and AD Bus to be placed in the high impedance state. A low pulse on HOLDN releases the MAS281 from the BPT initiated Hold state.

Operation	Command Code(Hex)	Mnemonic	Cycles*		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt Request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct Memory Access Disable	4007	DMAD	2	3	9
Timer A Start	4008	TAS	2	3	9
Timer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
Input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	S0XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	S1XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	D1XY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 3: Internal I/O Command Summary

5.0 TIMING CHARACTERISTICS

This section provides the detailed timing specifications for the MA17501. Figure 5 depicts the test loads used to obtain timing data. Figures 6 through 20 depict the timing waveforms associated with various MA17501 signals. Table 5 provides values for parameters specified in the timing waveforms. All timing values provided in Table 5 are valid over the full military temperature range (-55°C to +125°C), and are measured from 50% point to 50% point (50% VDD supply voltage, unless otherwise specified). Crosshatching in Figures 6 through 20 indicates either a "don't care" or indeterminate state.

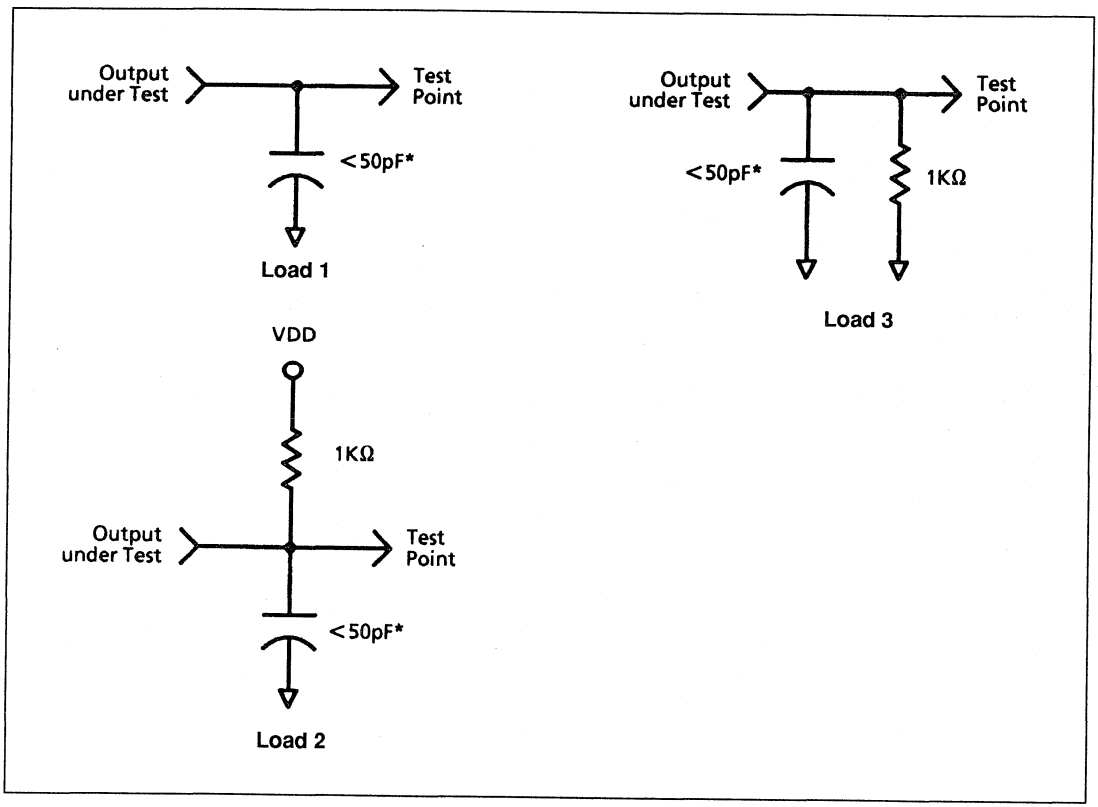


Figure 5: Test Loads

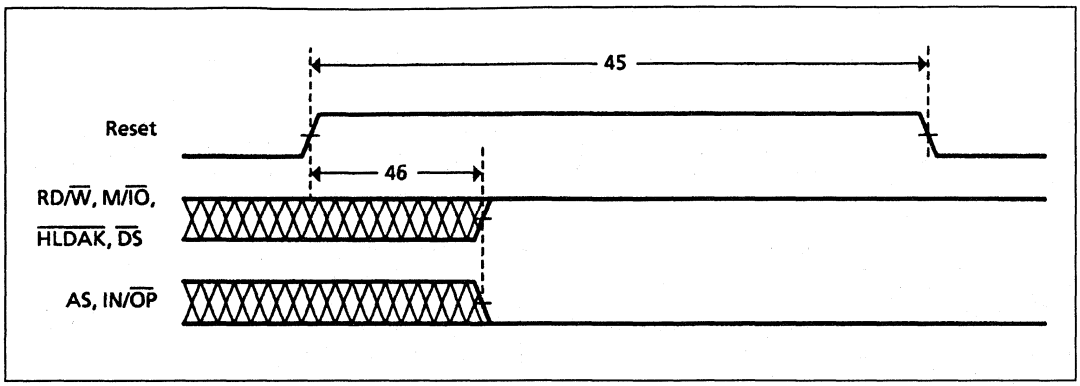


Figure 6: Reset Timing

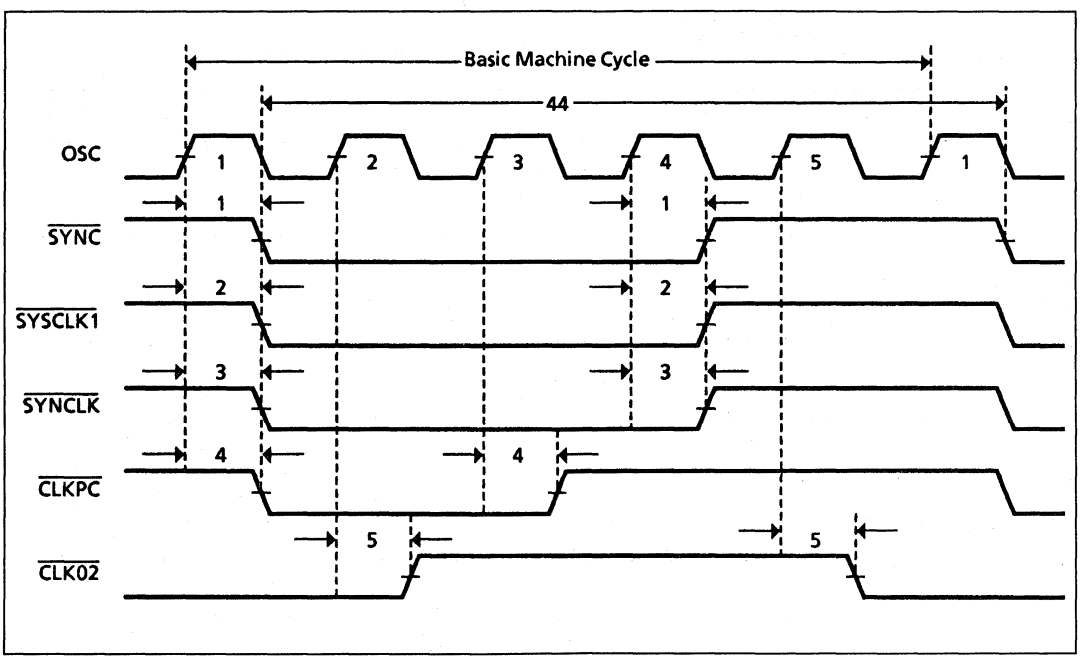


Figure 7: Basic Clock Timing

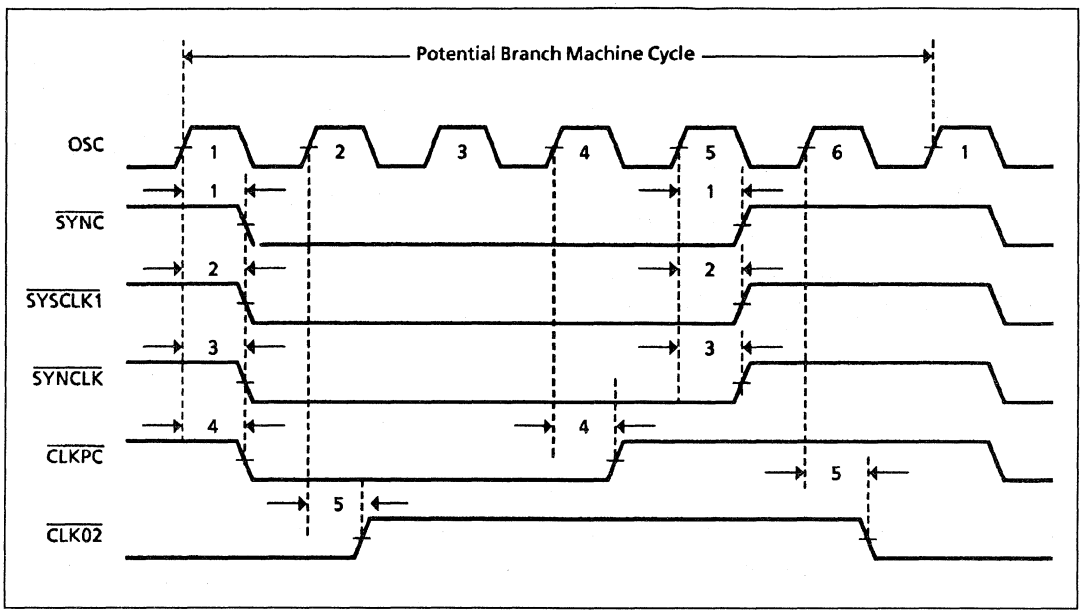


Figure 8: Potential Branch Clock Timing

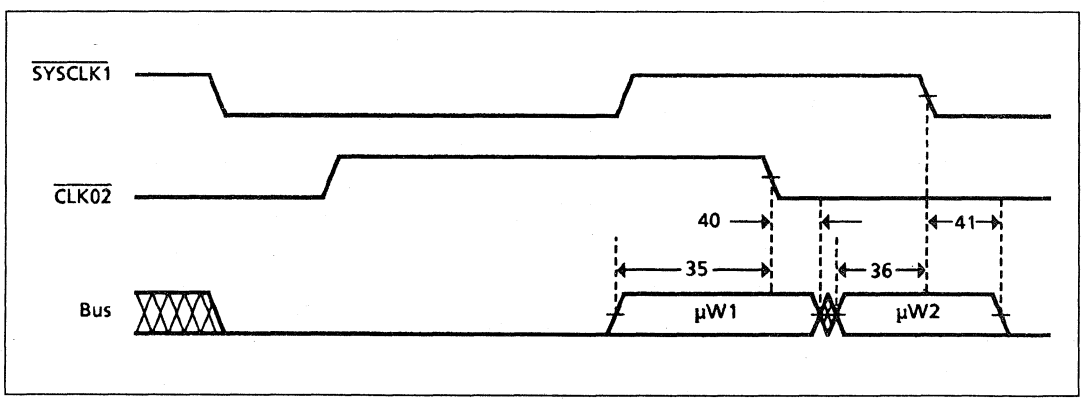


Figure 9: Microcode Bus Timing

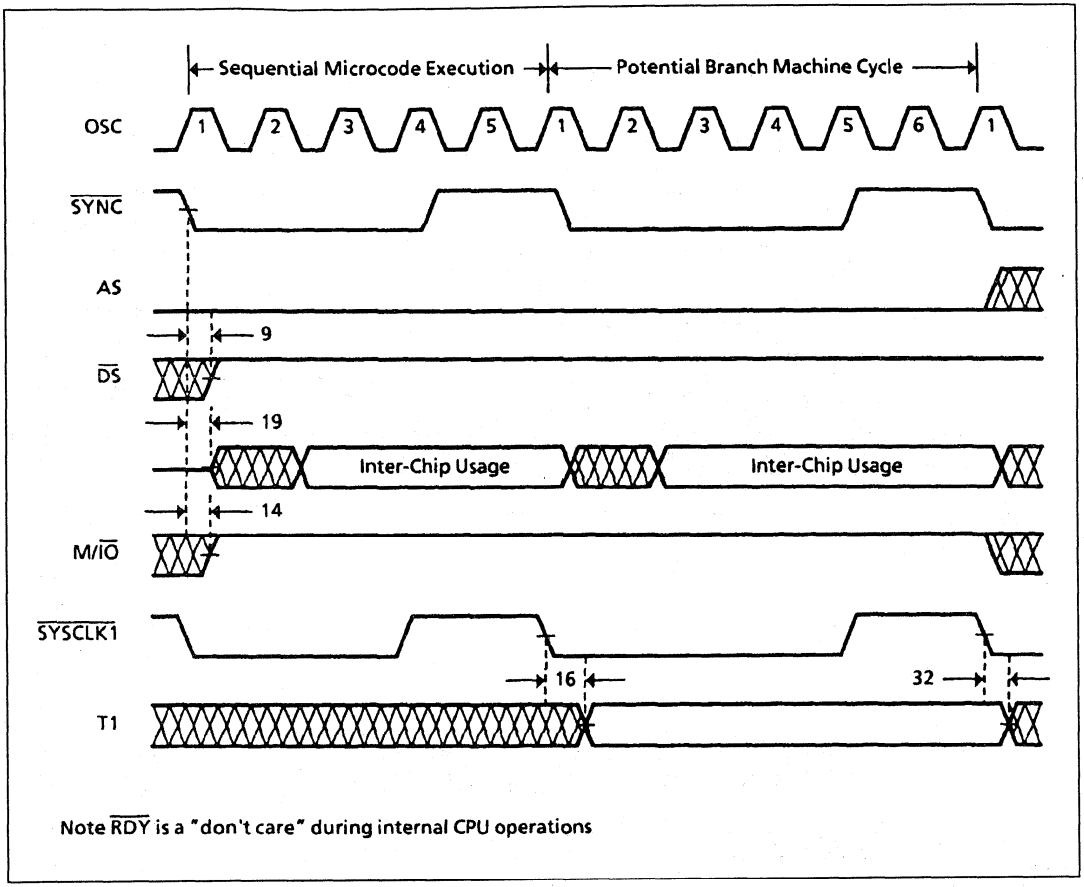


Figure 10: Internal Processor Cycle

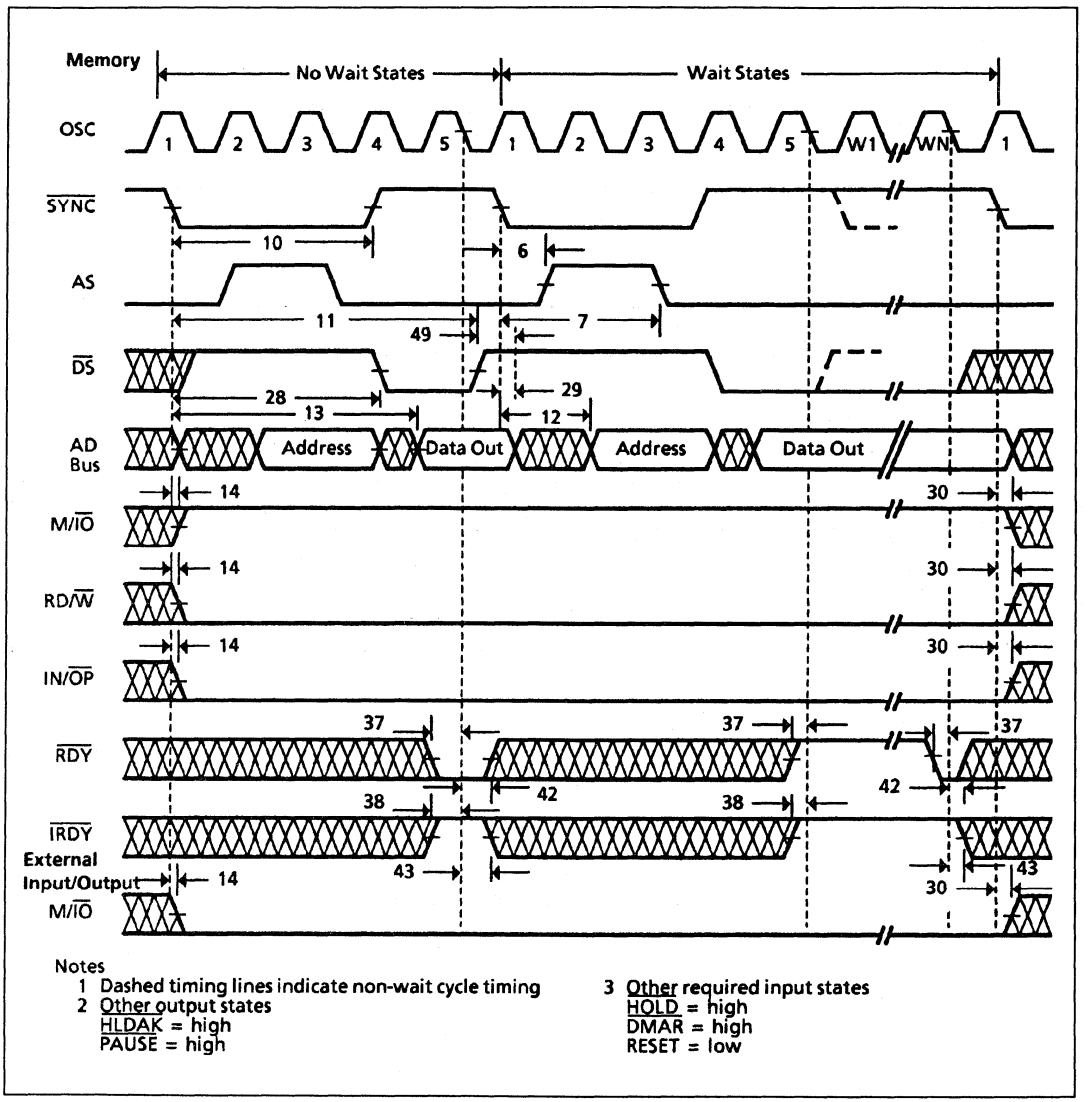


Figure 11: Write Transfer Timing

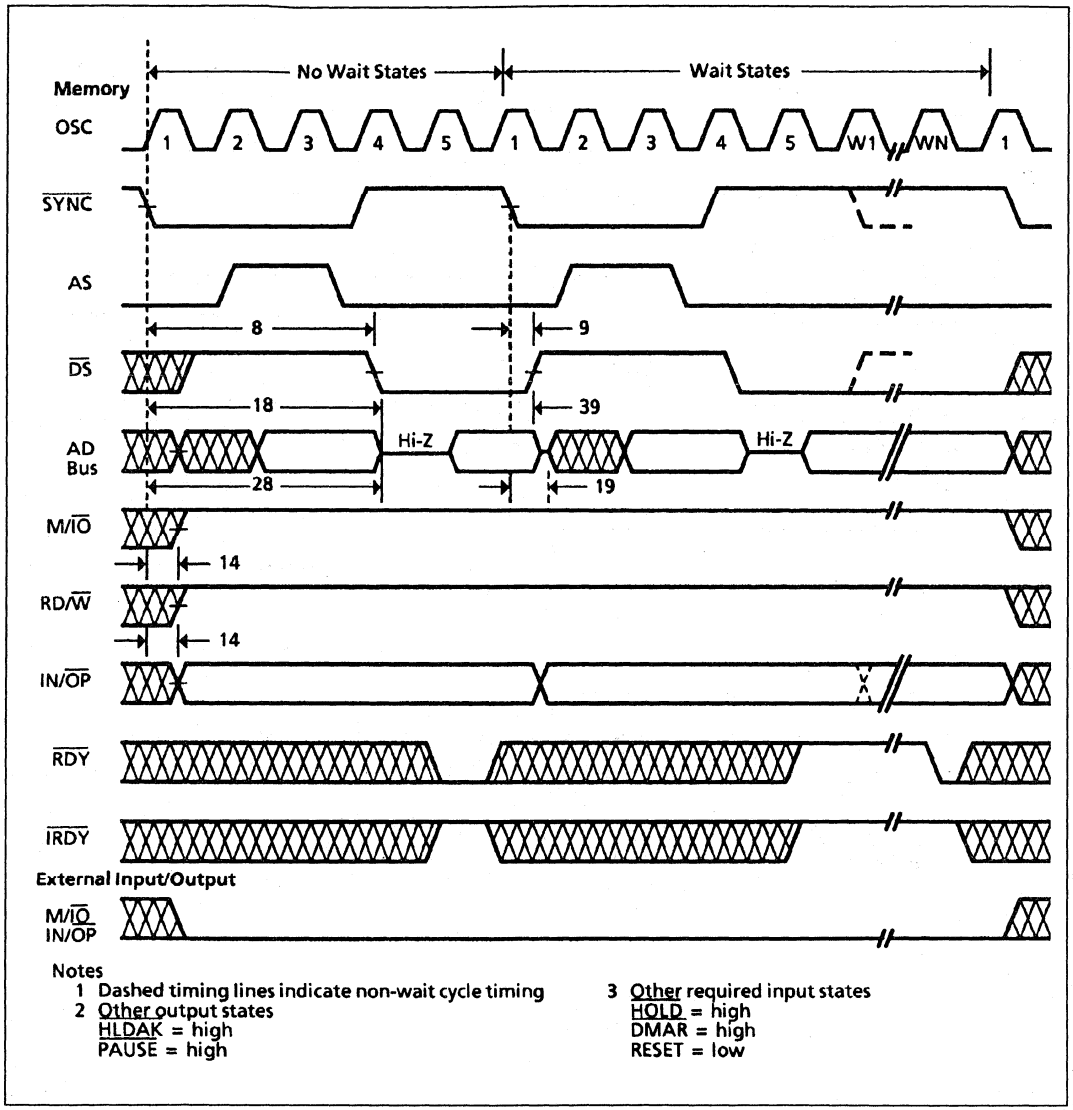


Figure 12: Read Transfer Timing

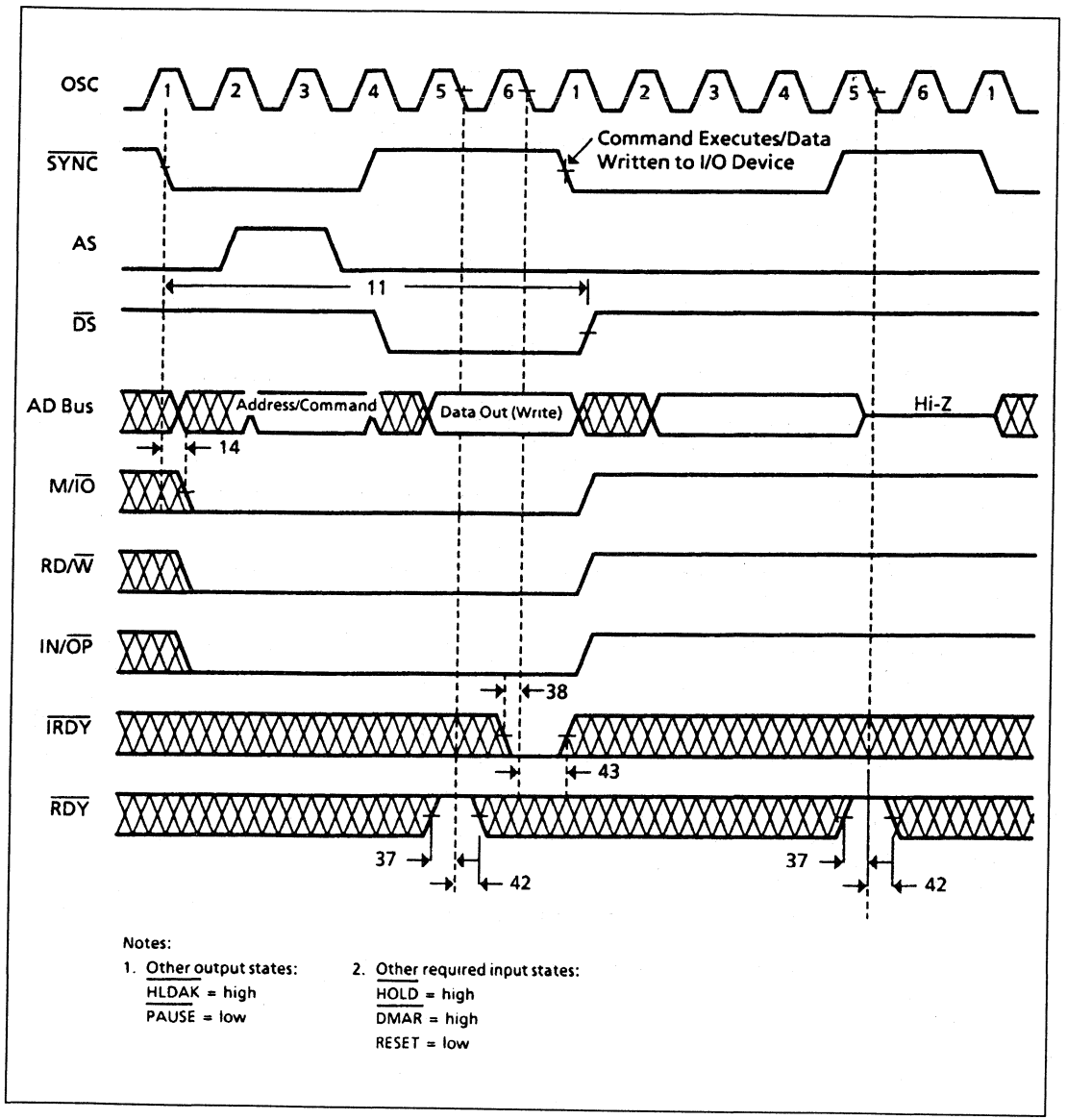
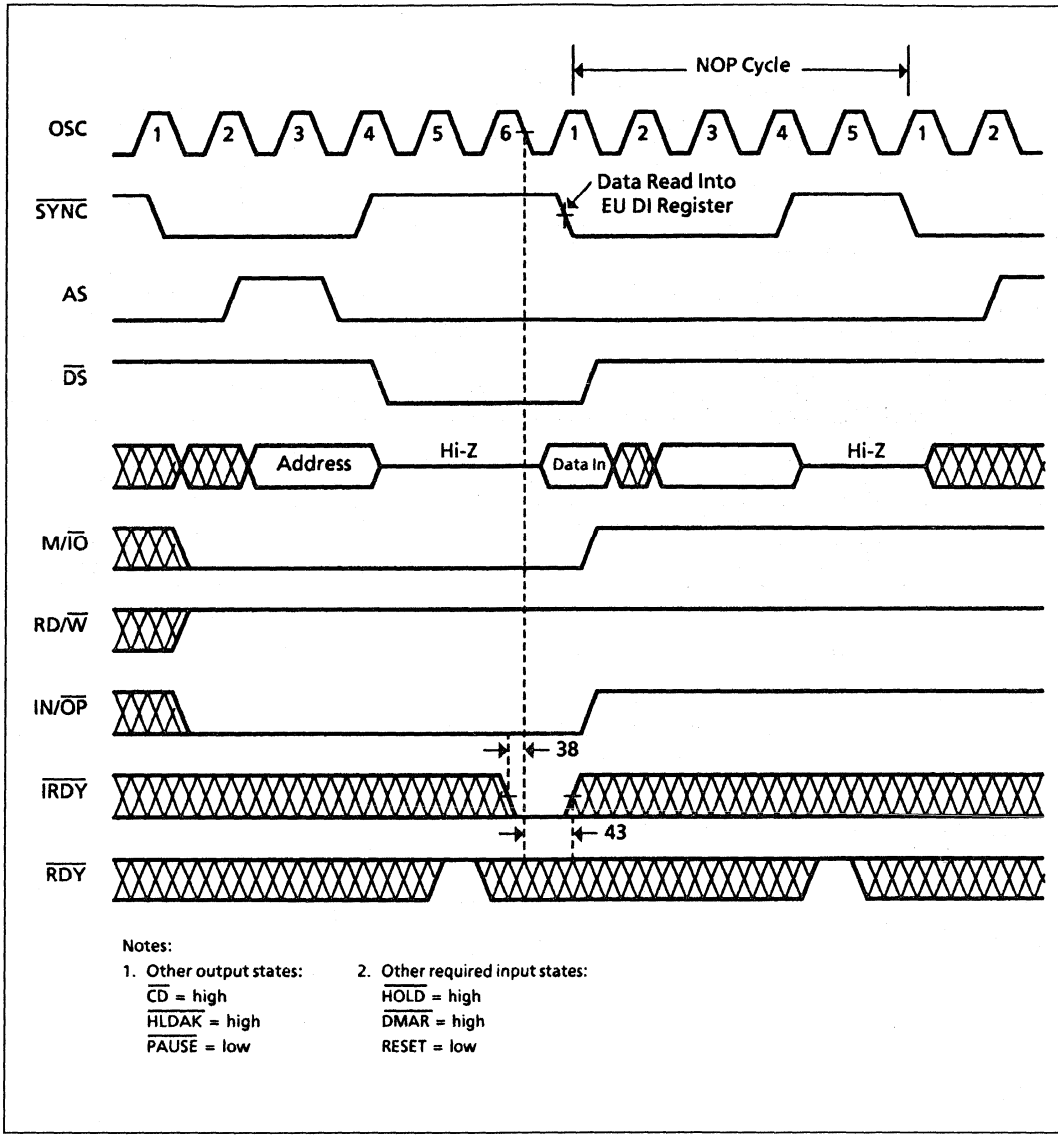


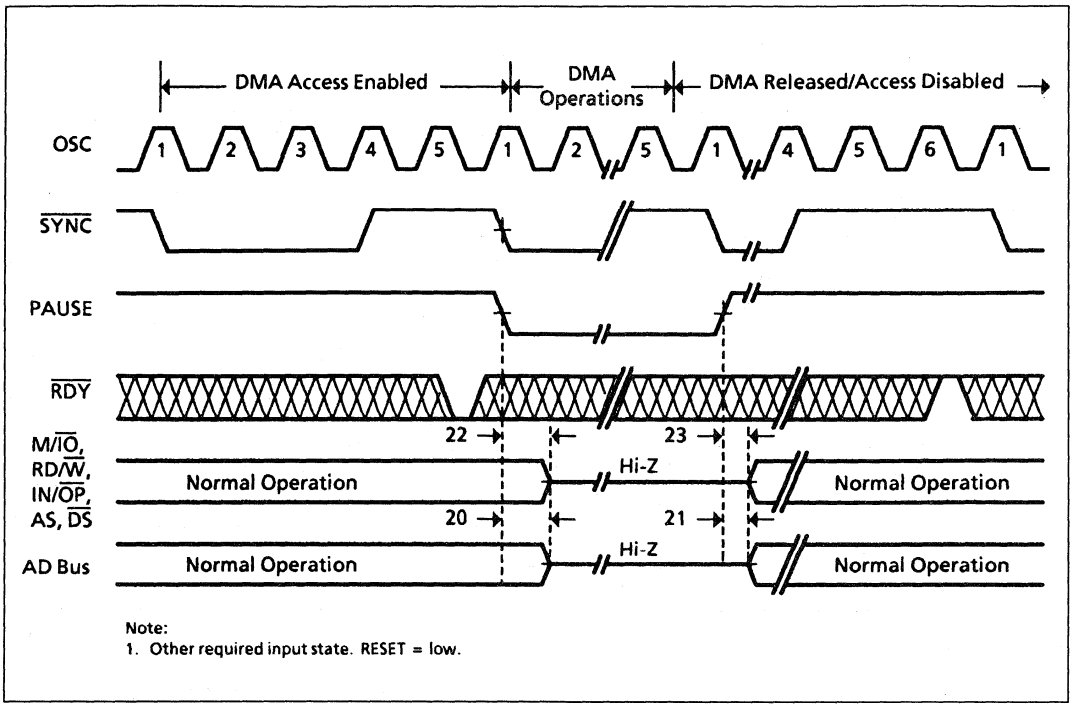
Figure 13: Internal I/O Timing - Write/Command



Notes:

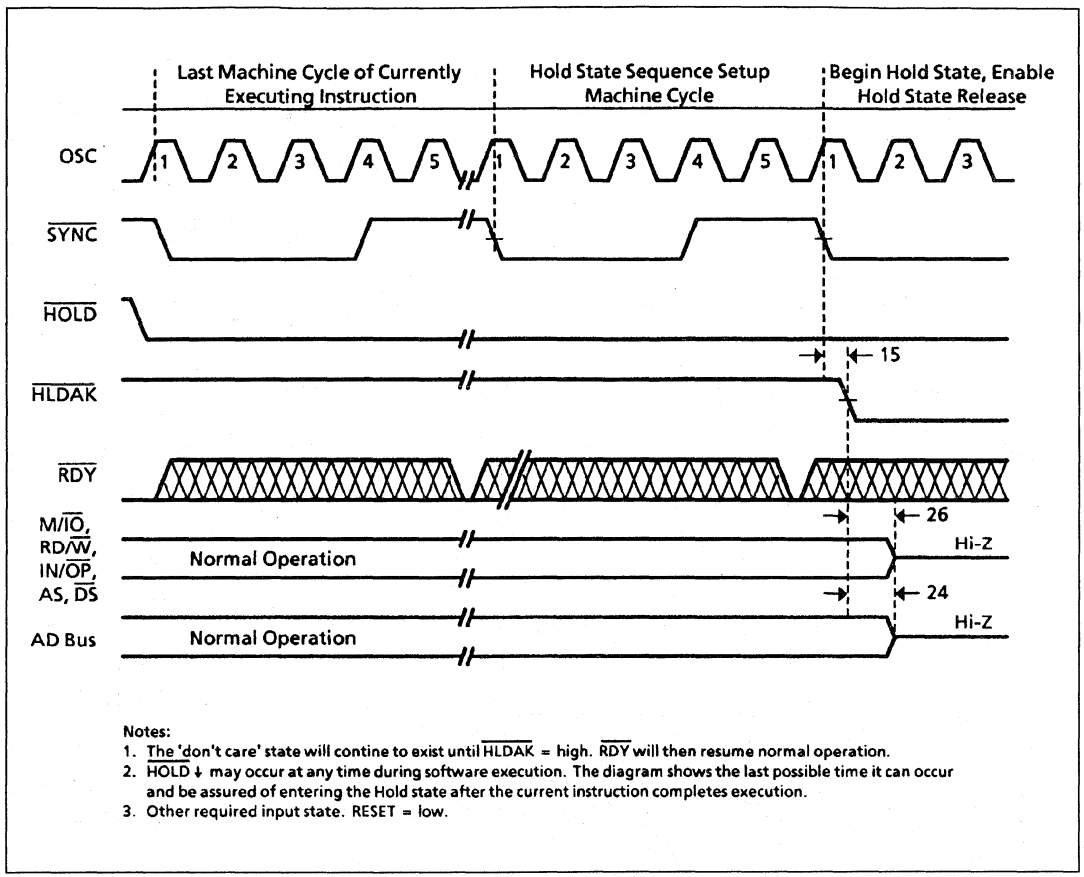
1. Other output states:
   - CD = high
   - HLDAK = high
   - PAUSE = low
2. Other required input states:
   - HOLD = high
   - DMAR = high
   - RESET = low

Figure 14: Internal I/O Timing - Read



Note:
1. Other required input state. RESET = low.

Figure 15: DMA Access/Release Timing



Notes:
1. The 'don't care' state will contine to exist until HLDAK = high. RDY will then resume normal operation.
2. HOLD ↓ may occur at any time during software execution. The diagram shows the last possible time it can occur and be assured of entering the Hold state after the current instruction completes execution.
3. Other required input state. RESET = low.

Figure 16: Hold State Generation Timing

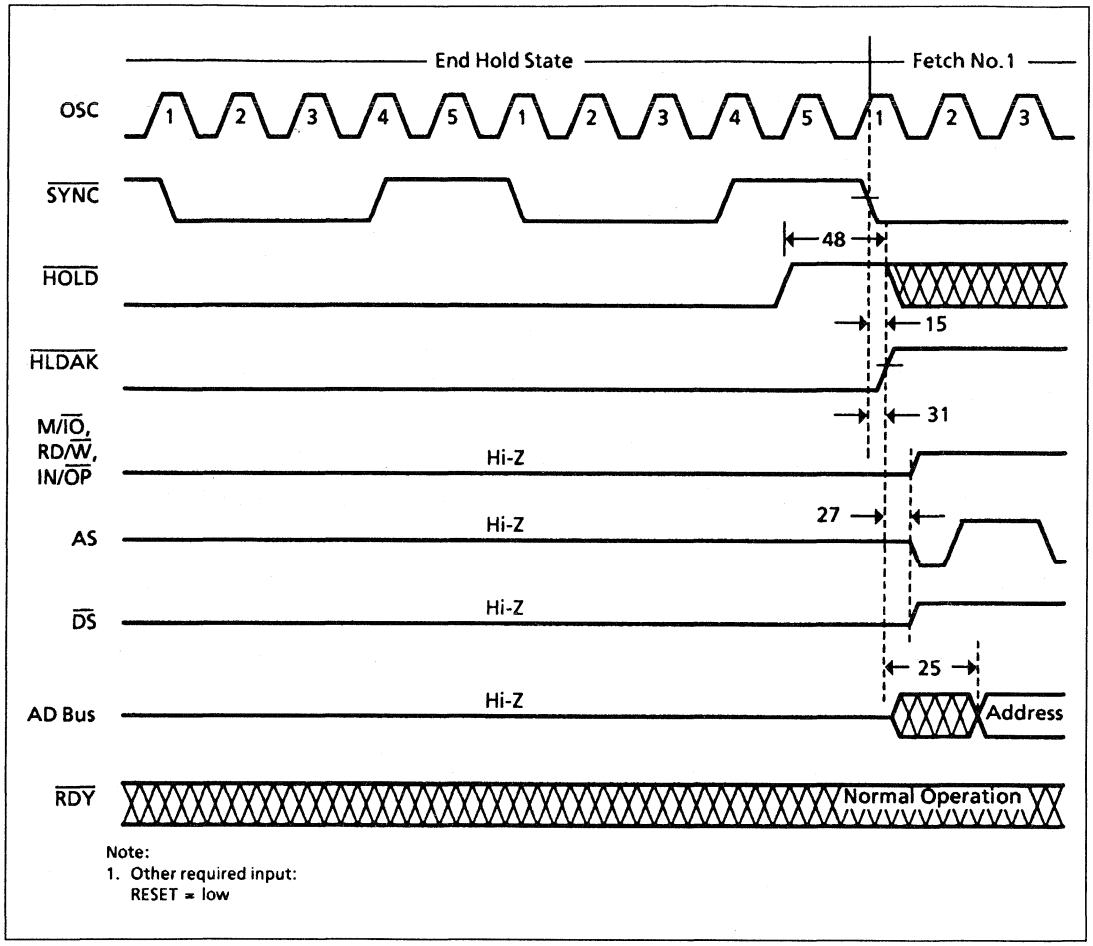


Figure 17: Hold State Termination Timing

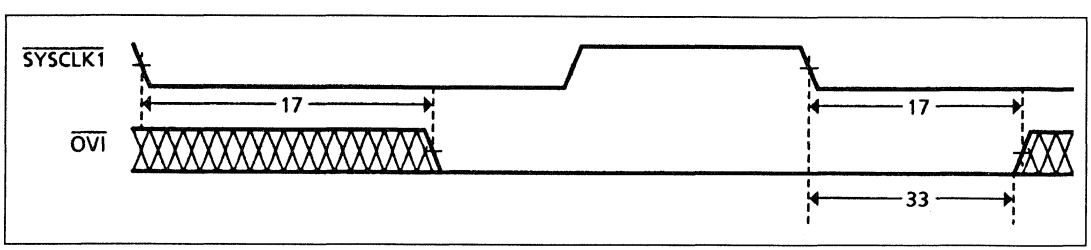


Figure 18: Fixed Point Overflow Timing

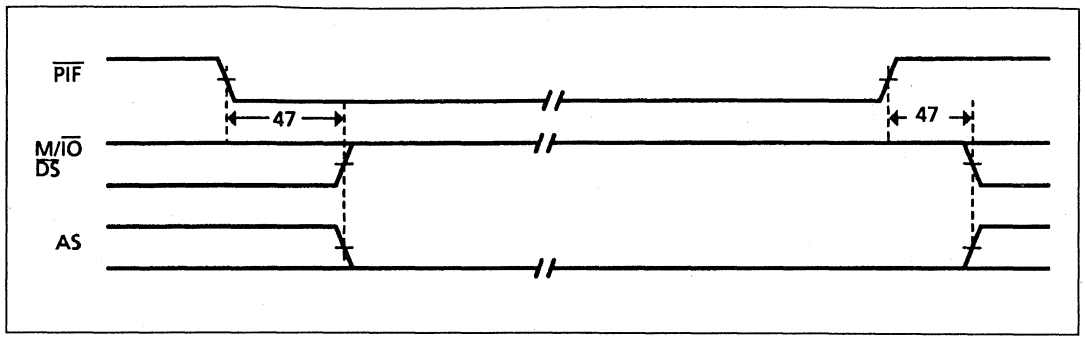


Figure 19: Instruction Abort Fault Timing

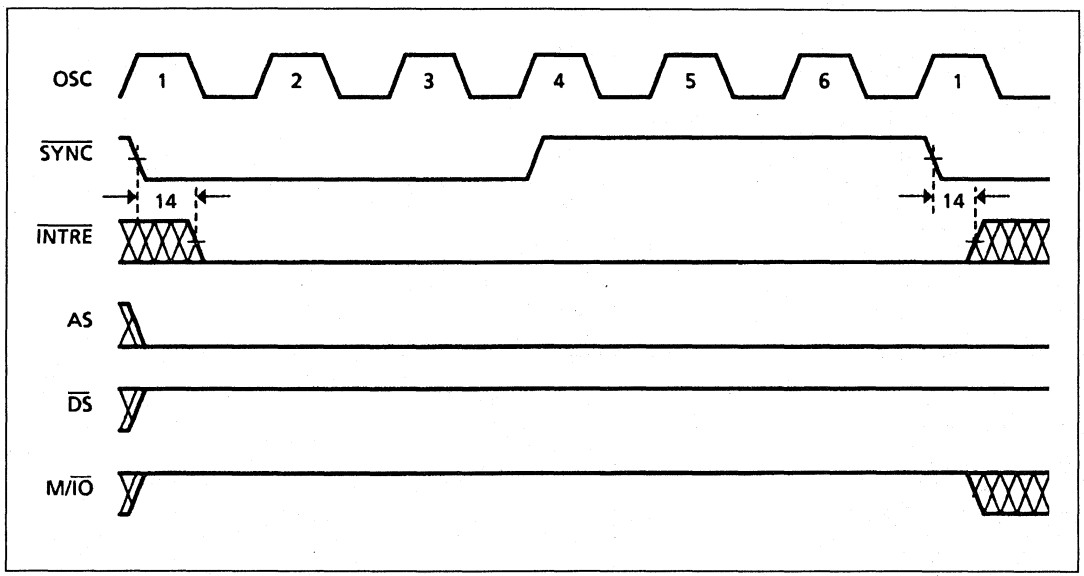


Figure 20: Interrupt Unit Microcode Enable Timing

Subgroup	Definition
1	Static characteristics specified in Table 6 at +25°C
2	Static characteristics specified in Table 6 at +125°C
3	Static characteristics specified in Table 6 at -55°C
7	Functional tests at +25°C
8a	Functional tests at +125°C
8b	Functional tests at -55°C
9	Switching characteristics specified in Table 4b at +25°C
10	Switching characteristics specified in Table 4b at +125°C
11	Switching characteristics specified in Table 4b at -55°C

Table 4a: Definition of Subgroups

No.	Parameter	Test Conditions (1) (2)	Min (2)	Typ (2)	Max (2)	Units
1	OSC ↑ to SYNCN	Load 1	10		40	ns
2	OSC ↑ to SYSCLK1N	Load 1			40	ns
3	OSC ↑ to SYNCLKN	Load 1			40	ns
4	OSC ↑ to CLKPCN	Load 1			40	ns
5	OSC ↑ to CLK02N	Load 1			40	ns
6	SYNCN ↓ to AS ↑	Load 1	1τ-10		1τ+5	ns
7	SYNCN ↓ to AS ↓ (4)	Load 1	2.5τ-10		2.5τ+15	ns
8	SYNCN ↓ to DSN (Read)	Load 1	3τ-5		3τ+20	ns
9	SYNCN ↓ to DSN ↓ (Read) (3)	Load 1	10		30	ns
10	SYNCN ↓ to DSN ↓ (Write)	Load 1	3τ-5		3τ+22	ns
11	SYNCN ↓ to DSN ↑ (Write) (3)	Load 1	4.5τ-5		4.5τ+10	ns
12	SYNCN ↓ to Address Valid	Load 1			68	ns
13	SYNCN ↓ to Data Valid	Load 1			3τ+45	ns
14	SYNCN ↓ to M/ION, RD/WN, IN/OPN, INTREN Valid	Load 1			70	ns
15	SYNCN ↓ to HLDAKN Valid	Load 1			20	ns
16	SYSCLKN1 ↓ to T1 Valid	Load 1			75	ns
17	SYSCLKN1 ↓ to OVIN Valid	Load 1			100	ns
18	SYNCN ↓ to AD Bus Hi-Z (Read) (6)	Load 2			3τ+50	ns
19	SYNCN ↓ to AD Bus Active (Read)	Load 2	15			ns
20	PAUSEN ↓ to AD Bus Hi-Z (Read) (6)	Load 2			70	ns
21	PAUSEN ↑ to AD Bus Valid	Load 2			60	ns
22	PAUSEN ↓ to AS, DSN, M/ION, RD/WN, IN/IOPN Hi-Z (6)	Load 2, 3			50	ns
23	PAUSEN ↑ to AS, DSN, M/ION, RD/WN, IN/IOPN Valid	Load 2, 3			59	ns
24	HLDAKN ↓ to AD Bus Hi-Z (Read) (6)	Load 2			60	ns
25	HLDAKN ↑ to AD Bus Valid	Load 2			50	ns
26	HLDAKN ↓ to AS, DSN, M/ION, RD/WN, IN/IOPN Hi-Z (6)	Load 2, 3			30	ns
27	HLDAKN↑ to AS, DSN, M/ION, RD/WN, IN/IOPN Valid	Load 2, 3			30	ns
28	Address after SYNCN ↓	Load 1	3τ+15			ns
29	Data after SYNCN ↓	Load 1	12			ns
30	M/ION, RD/WN, IN/OPN, INTREN after SYNCN	Load 1	5			ns
31	HLDAKN after SYNCN ↓	Load 1	-7			ns
32	T1N after SYSCLK1N ↓	Load 1	15			ns
33	OVIN after SYSCLK1N ↓	Load 1	20			ns
34	Data to SYNCN ↓		20			ns
35	Microcode to CLK02N ↓		10			ns
36	Microcode to SYSCLK1N ↓		10			ns
37	RDYN to OSC ↓		15			ns
38	IRDYN to OSC ↓		15			ns
39	Data after SYNCN ↓		0			ns
40	Microcode after CLK02N ↓		5			ns
41	Microcode after SYSCLK1N ↓		15			ns
42	RDYN after OSC ↓		5			ns
43	IRDYN after OSC ↓		10			ns
44	SYNCN to SYNCN ↓ (7)		5τ-2		5τ+2	ns
45	RESET ↑ to RESET ↓ (7)		2			ns
46	RESET ↑ to Related Outputs Valid (7)				50	ns
47	PIFN to Related Outputs Valid				50	ns
48	HOLDN to Related Outputs Valid (7)				50	ns
49	DSN to Data Valid (Write) (7)	Load 3 (DSN) Load 2 (Data)	15			ns
50	SYNCN to SYNCLKN (No.1 - No.3)		-5		8	ns
51	CLKPCN to SYNCLKN (No.4 - No.3)		-5		5	ns
52	SYSCLK1 to CLKPC (No.2 - No.4)		-5		10	ns

MIL-STD-883, Method 5005, Subgroup 9, 10, 11

Notes:
1. T_A = +25°C, -55°C and +125°C tested at VDD = 4.5V and 5.5V
2. r = 1OSC period 0.5r implies 50% OSC duty cycle
3. Add 1r for internal XIO; nr for memory wait
4. Excluding DMA and Hold conditions
5. Unless otherwise noted: $V_{IL} = \geq 0.0V$, $V_{IHTTL} \leq 4.0V$, VIHOSC = 4.0V timing measured from 50% to 50% points
6. High impedance measured by 20% (of VDD) voltage change using 1K-ohm pullup resistor
7. Data obtained by characterisation or analysis, not routinely measured
8. Load 2 applies to bus interface signals AS, RD/W and IN/OP; Load 3 applies to bus interface signals M/ION and DSN

Table 4b: Timing Parameter Values

6.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.0 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Total Dose Radiation Not Exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS}+1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{CH}	OSC Input High Voltage (Note 6)	-	4.0	-	-	V
V_{CL}	OSC Input Low Voltage (Note 6)	-	-	-	1.0	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2mA, V_{DD} = 5.5V	-	-	0.5	V
V_{OHT}	TTL Output High Voltage (Note 2)	I_{OH} = -1.4mA, V_{DD} = 4.5V	3.5	-	-	V
V_{OLT}	TTL Output Low Voltage (Note 2)	I_{OH} = -1.4mA, V_{DD} = 4.5V	-	-	0.4	V
V_{OHCLK}	Clock Output High Voltage (Note 3)	I_{OH} = -12mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLCLK}	Clock Output Low Voltage (Note 3)	I_{OL} = 12mA, V_{DD} = 5.5V	-	-	0.5	V
I_I	Input Leakage Current (Note 4)	V_{DD} = 5.5V, V_{IN} = 0V or 5.5V	-	-	±10	µA
I_{OZ}	Output Leakage Current (Note 4)	V_{DD} = 5.5V, V_O = 0V or 5.5V	-	-	±50	µA
I_{IPU}	TESTN Input Pullup Current (Note 5)	V_{DD} = 5.5V, TESTN = 0V	-	-150	-300	µA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V, OSC = 20MHz	-	25	35	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V, OSC = 0MHz	-	5	10	mA

Mil-Std-883, Method 5005, Subgroup 1, 2, 3.

Notes: 1. The following signals are CMOS compatible:
   a) CMOS inputs: Microcode Bus, (M00-M19), TESTN, IRDYN and PIFN.
   b) CMOS outputs: T1, OVIN, INTREN, SYSCLK1N, CLKPCN and CLK02N.
2. The following signals are TTL compatible:
   a) TTL inputs: HOLDN, RESET, PAUSEN, RDYN and OSC.
   b) TTL outputs: HOLDAKN and SYNCN.
   c) TTL 3 state outputs: AS, DSN, M/ION, RD/WN and IN/OPN.
   d) TTL 3 state I/O signals: Address/Data Bus (AD00-AD15).
3. The clock output pins, SYSCLK1N, SYNCLK, CLKPCN and CLK02N have a higher drive capability than the standard outputs.
4. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
5. The TESTN input signal is used during chip test and has an integral pullup reistor. In normal operation TESTN is at V_{DD}.
6. Guaranteed but not tested.

Table 6: Operating DC Electrical Characteristics

8.0 PACKAGING INFORMATION

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.508	0.014	-	0.020
c	0.229	-	0.36	0.009	-	0.014
D	-	-	82.04	-	-	3.230
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	22.86 Typ.	-	-	0.900 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	23.4	-	-	0.920
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG413

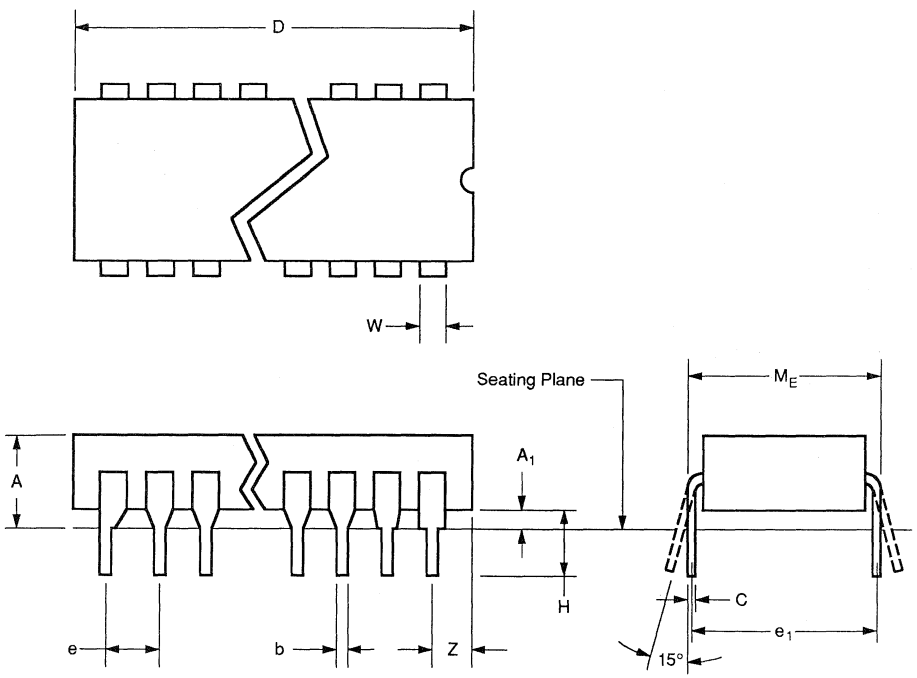


Figure 21a: 64-Lead Ceramic DIL - Package Style C

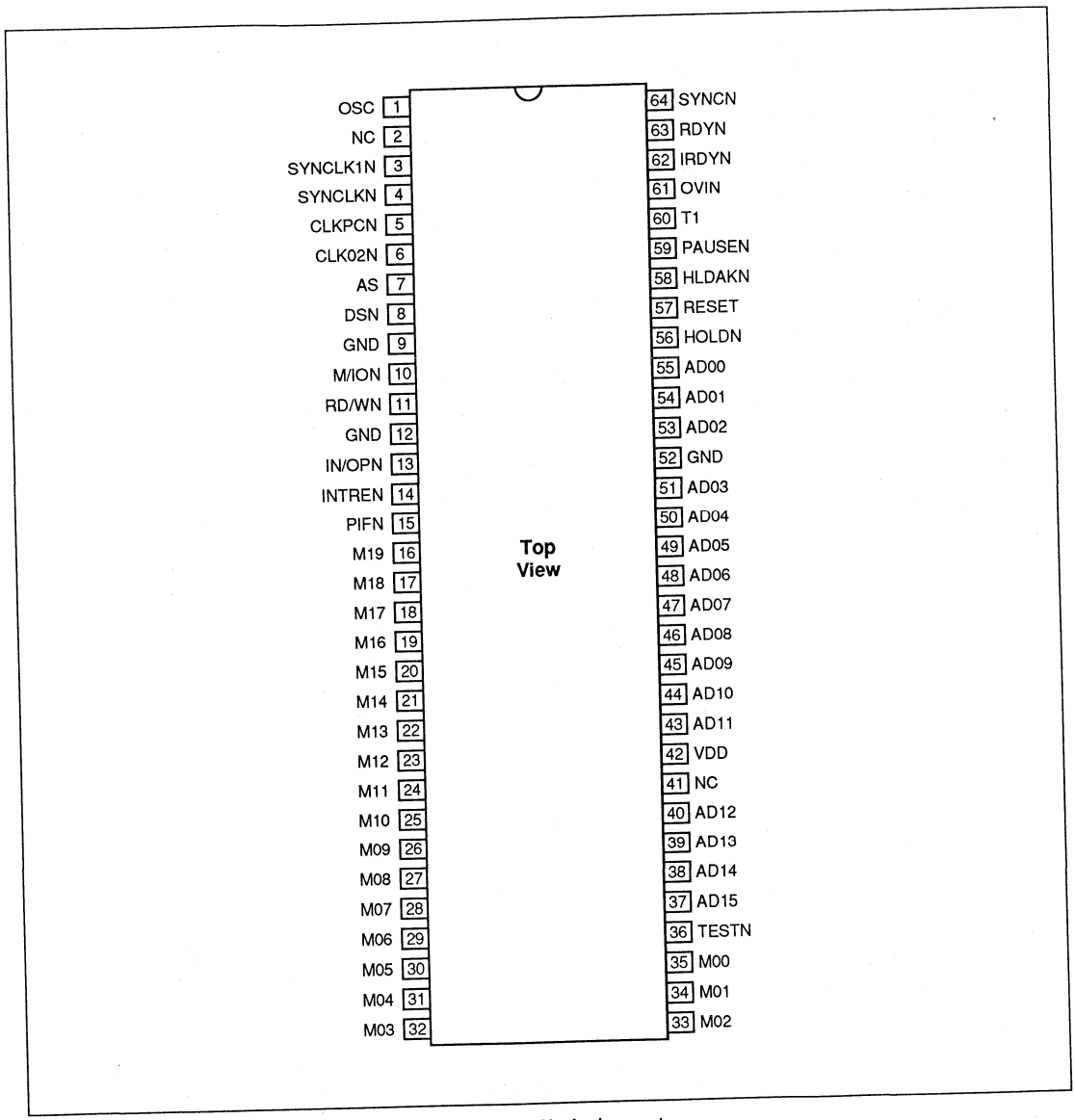


Figure 21b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.905	-	2.21	0.075	-	0.087
b1	-	0.51	-	-	0.020	-
D	18.08	-	18.62	0.712	-	0.733
E	18.08	-	18.62	0.712	-	0.733
e	-	1.02	-	-	0.040	-
Z	1.40	-	1.78	0.055	-	0.070

XG493

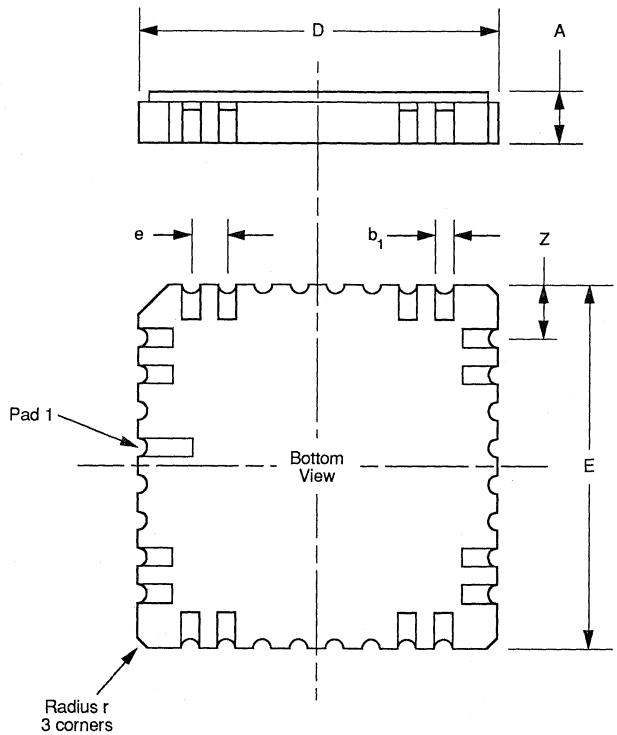


Figure 22a: 64-Lead Leadless Chip Carrier - Package Style L

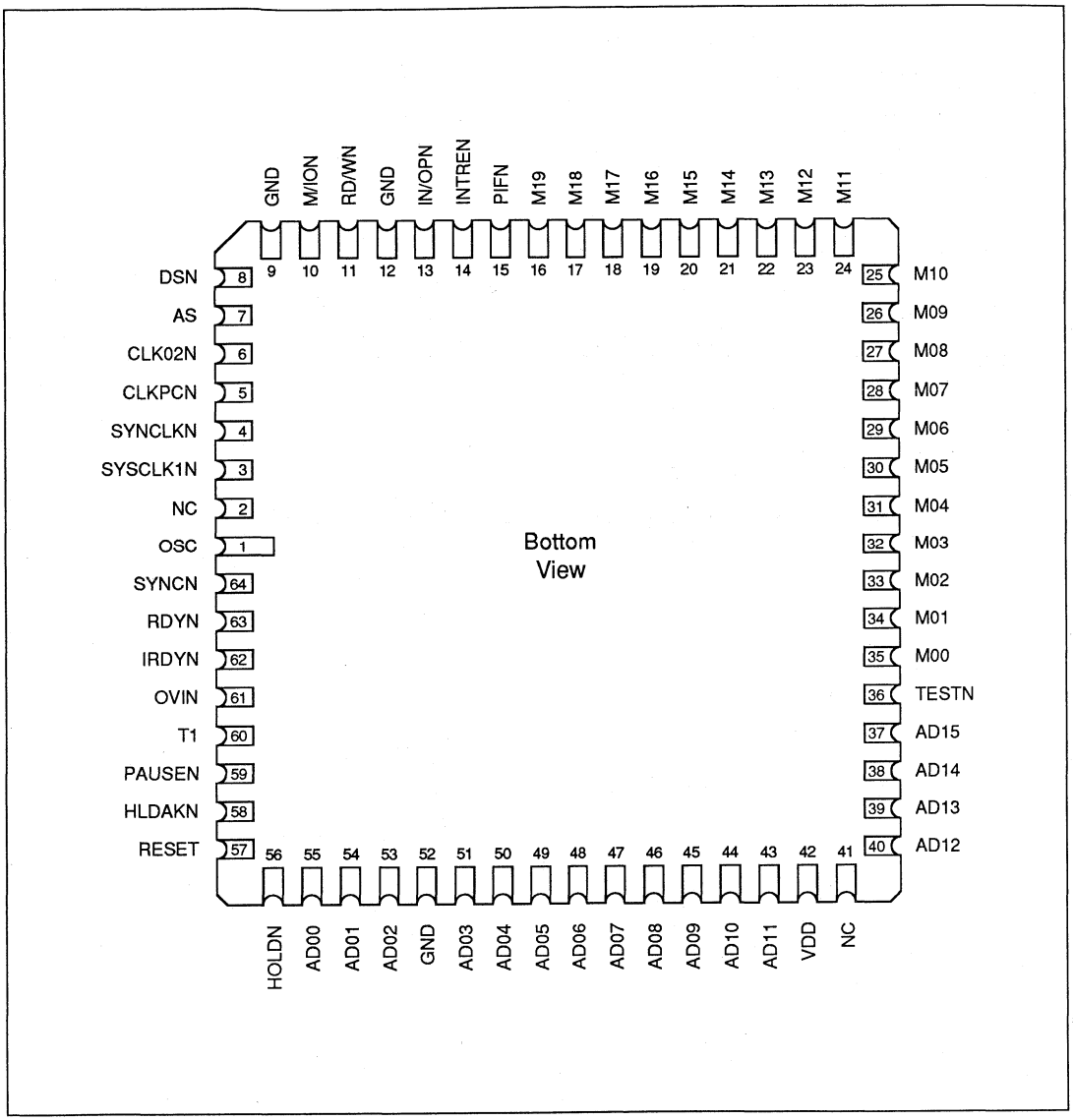


Figure 22b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

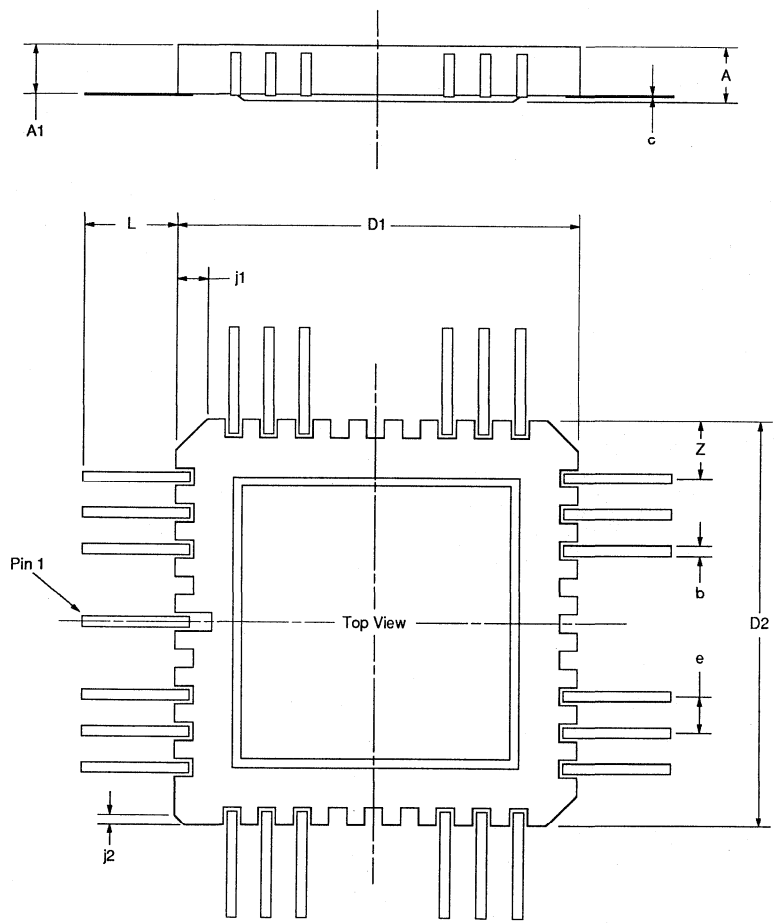


Figure 23a: 68-Lead Topbraze Flatpack - Package Style F

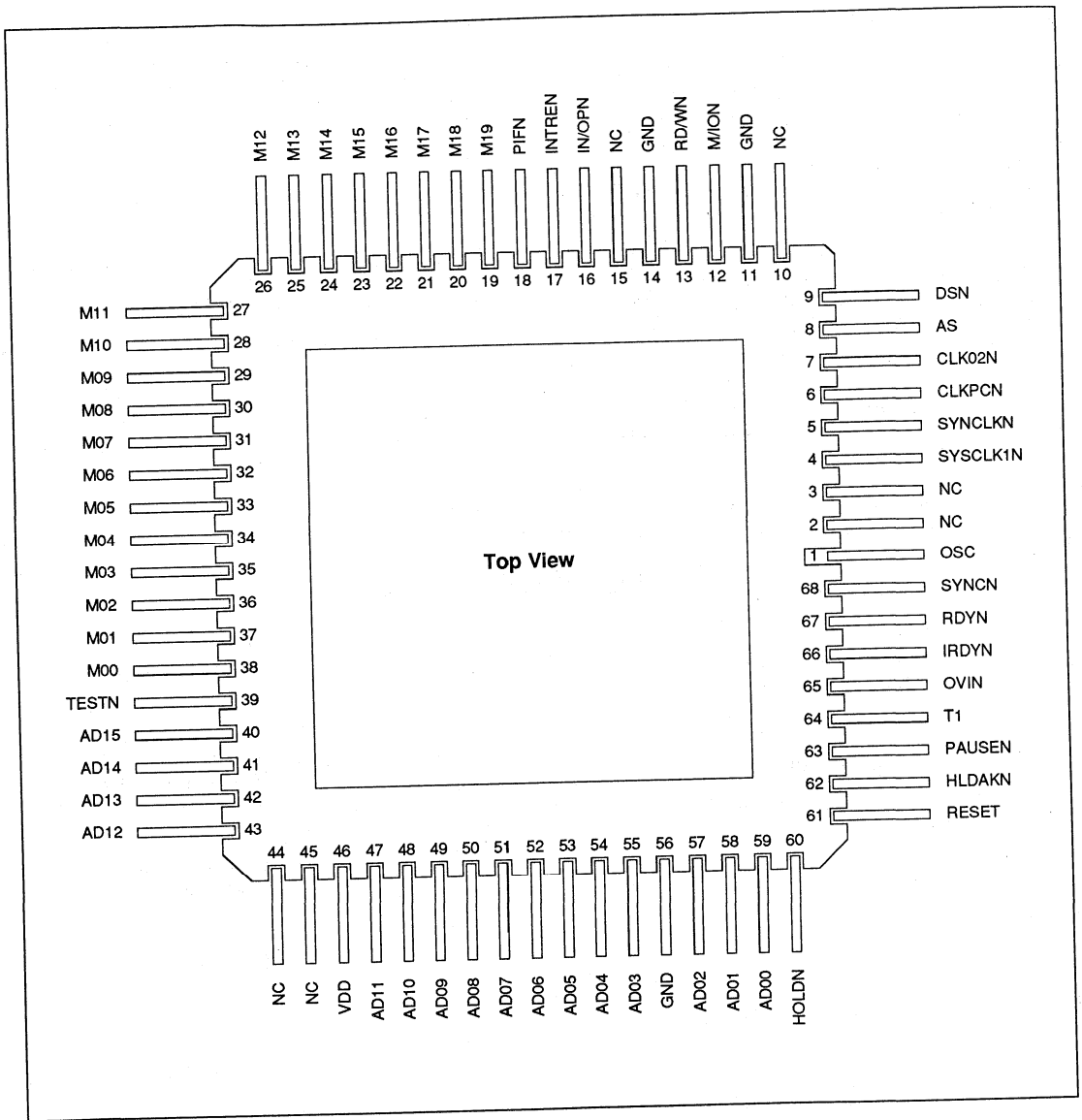


Figure 23b: Pin Assignments

9.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

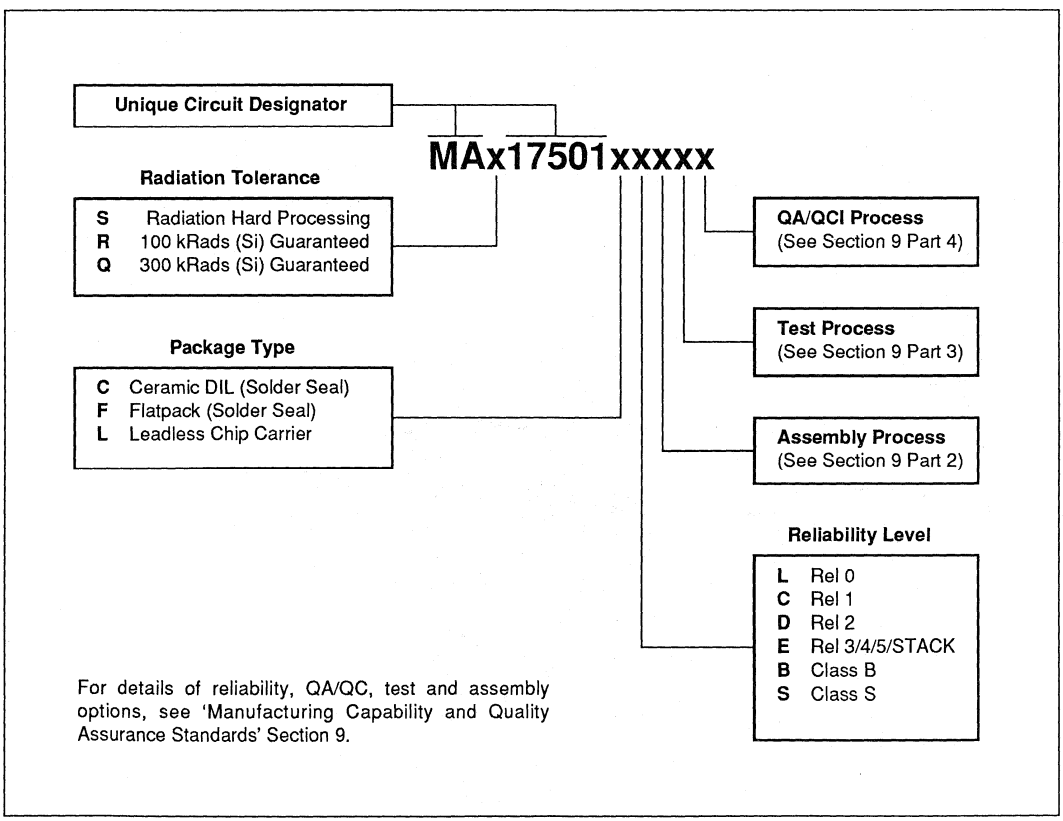
GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request
** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 10: Radiation Hardness Parameters

10.0 ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3565-3.4

MA17502

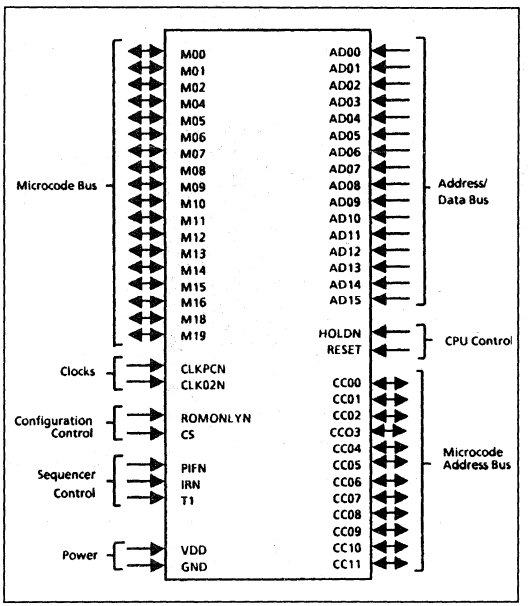
RADIATION HARD MIL-STD-1750A CONTROL UNIT

The MA17502 Control Unit is a component of the MAS281 chip set. Other chips in the set include the MA17501 Execution Unit and the MA17503 Interrupt Unit. Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit. In conjunction these chips implement the full MIL-STD-1750A Instruction Set Architecture.

The MA17502 consisting of a microsequencer, a microcode storage ROM, and an instruction mapping ROM - controls all chip set operations. Table 1 provides brief signal definitions.

The MA17502 is offered in several speed and screening grades, and in dual in-line, flatpack or leadless chip carrier packaging. Screening options are described in this document. For availability of speed grades, please contact GPS.

BLOCK DIAGRAM



FEATURES

- MIL-STD-1750A Instruction Set Architecture
- Full Performance Over Military Temperature Range
- 12-Bit Microsequencer
  - Instruction Prefetch
  - Pipelined Operation
  - Subroutine Capability
- On-Chip ROM
  - 2K x 40-Bit Microcode Store
  - 512 x 8-Bit Instruction Map
- MAS281 Integrated Built-In Self Test
- TTL Compatible System Interface
- Low Power CMOS/SOS Technology

1.0 SYSTEM CONSIDERATIONS

The MA17502 Control Unit (CU) is a component of the GPS MAS281 chip set. The other chips in the set are the MA17501 Execution Unit (EU) and the MA17503 Interrupt Unit (IU). Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit (MMU(BPU)). The Control Unit, in conjunction with these chips, implements the full MIL-STD-1750A Instruction Set Architecture. Figure 1 depicts the relationship between the chip set components.

The CU provides the microprogram storage and sequencing resources for the chip set. The EU provides the MAS281's system synchronizing and arithmetic/logic computational resources. The IU provides interrupt and fault handling resources, DMA interface control signals, and the three MIL-STD-1750A timers. The MMU/BPU may be configured to provide 1M-word memory management (MMU) and/or 1K-word memory block write protection (BPU) functions.

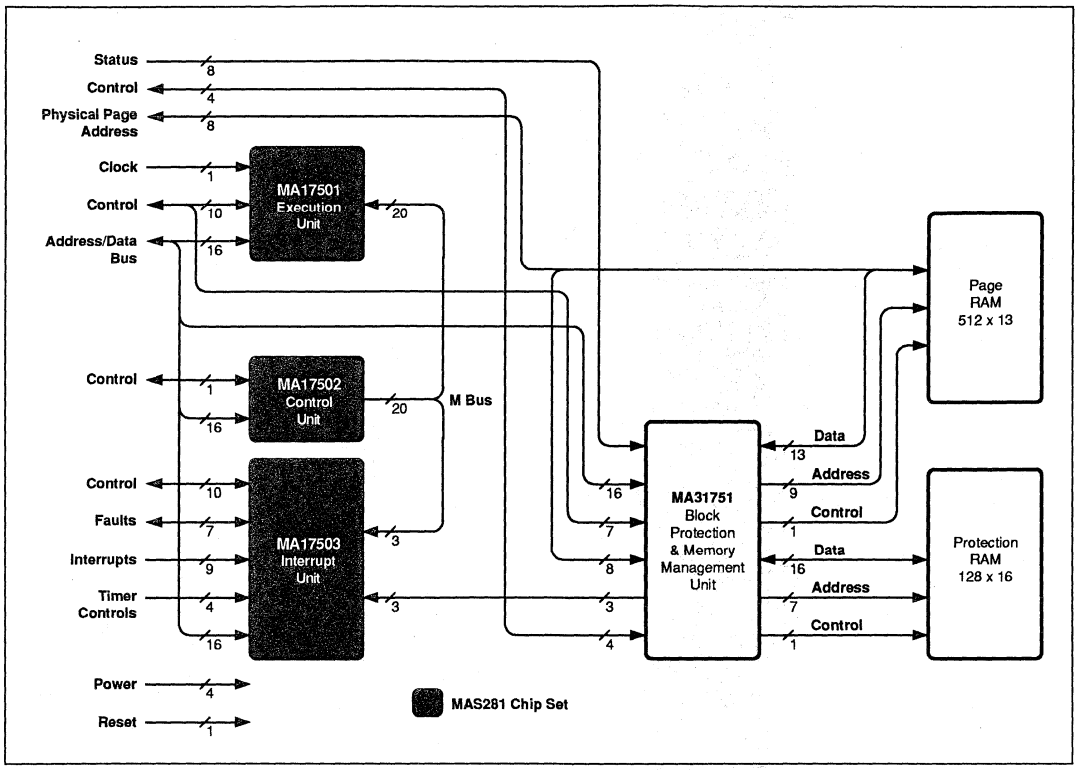


Figure 1: MAS281 Chip Set With Optional MA17504 and Support RAMs

Signature	I/O	Definition
AD00 - AD15	I	External 16-Bit Address/Data Bus
CC00 - CC11	I/O	12-Bit Microcode Address Bus
$\overline{\text{CLKPC}}$	I	Precharge Clock
$\overline{\text{CLK02}}$	I	Phase 2 Clock
$\overline{\text{CS}}$	I	Chip Select
$\overline{\text{HOLD}}$	I	Hold Request Suspends Internal Processor Functions
$\overline{\text{IR}}$	I	Interrupt Request
M00 - M19	I/O/Z	20-Bit Microcode Bus
NC	-	No Connection
$\overline{\text{PIF}}$	I	Privileged Instruction Fault
$\overline{\text{RESET}}$	I	Rest Indicates Device Initialization
$\overline{\text{ROMONLY}}$	I	Indicates if Control Unit to be Used as ROM Only
T1	I	Branch or Jump Control
VDD		Power (External), 5 Volts
GND		Ground

Table 1: Signal Definitions

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of an MMU configured MA31751 allows access to a 1M-word address space. This can also be configured as a BPU to provide hardware support for 1K-word memory block write protection.

The CU, as with all components of the MAS281 chip set, is fabricated with CMOS/SOS process technology. Input and output buffers associated with signals external to the MAS281 are TTL compatible.

Detailed descriptions of the CU's companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and the Digital Avionics Instruction Set (DAIS) mix benchmarking analysis are provided in separate applications notes.

2.0 ARCHITECTURE

The Control Unit consists of a microsequencer, an instruction mapping ROM, a microcode storage ROM, and various buses. Details of these components are shown in Figure 2 and are discussed below:

2.1 MICROSEQUENCER

The CU microsequencer is a 12-bit wide microcode address generator. Major features of the microsequencer include a microprogram counter (PC), a microprogram counter save register (PC Save), microcode address increment logic, instruction pipeline registers IA and IB, an iteration of loop counter, a next microcode address source multiplexer, and various pipelining latches. These features are represented in Figure 2.

The 12-bit microcode address width allows the microsequencer to access up to 4096 words of microcode. The MIL-STD-1750A instructions are implemented as sequences of microinstructions stored within the lower 2048 locations of this address space. The address for each microinstruction in a sequence is provided by the next microcode address source multiplexer. This multiplexer, under control of the CU control logic, select from one of six next address sources. Sequential, direct jump, conditional jump, and subroutine address generation modes are supported.

Sequential addressing is accomplished by providing a path from the output of the next microcode address multiplexer to an incrementer and back to the PC register input. Direct jumps are supported by routing a portion of the microinstruction to one of the next microcode address source multiplexer inputs. Conditional jumps are determined in the ALU of the Execution Unit which communicates the decision to the CU via the T1 signal. The T1 signal enables a portion of the microcode word to create the new address. Subroutine jumps are accomplished by loading the contents of the incremented PC register into the PC Save register and then performing a direct jump. Upon completion of the subroutine, the contents of the PC Save register are used as the next microcode address.

A new microinstruction sequence begins when an opcode residing in the IA or IB register is selected by the next microcode address source multiplexer and used as an address to simultaneously access both the CU's Instruction Mapping ROM and the Microcode Storage ROM. The instruction Mapping ROM access provides a pointer which is then used to update the microprogram counter (PC); the Microcode Storage ROM access provides the first microinstruction of the sequence. Remaining microinstructions in a sequence are accessed through the use of the four address generation modes discussed above.

Iterative microprogram operations are achieved through the use of the loop counter. The loop counter may be selectively loaded from either the AD bus or directly from microcode. This counter tracks the number of iterations remaining and, when appropriate, issues a completion signal (CZ). When an iterative operation is called for, the loop counter is loaded and the CU control logic repeats a particular microinstruction sequence, using the four address generation modes discussed above, until the CZ signal is received.

2.2 INSTRUCTION MAPPING ROM

The CU instruction mapping ROM provides 512 8-bit words of microcode instruction vector storage. The address space of this ROM is mapped into a portion of the microcode storage ROM's address space. Hence, both ROMs are accessed whenever the microcode address falls within this range. The eight bits from the instruction mapping ROM serve as-the lower eight bits of a 12-bit microcode address; the upper four bits are a hardwired constant. The 12-bit microcode address formed from the 4-bit constant and the mapping ROM's eight bits are loaded into the PC register of the microsequencer and serve as a means to access nonsequential microcode addresses within the address space allocated to both the instruction mapping and microcode storage ROMs.

2.3 MICROCODE ROM

The CU microcode ROM provides 2K (2048) 40-bit words of storage capacity. All of the microcode required to implement the full MIL-STD-1750A Instruction Set Architecture (ISA) fits in one such ROM.

2.4 BUSES

A 16-bit multiplexed Address/Data (AD) bus provides a communications path between the CU, the other components of the MAS281 chip set, the MA31751 MMU/BPU, and any other devices mapped into the chip set's address space. The CU receives MIL-STD-1750A instructions, accessed from system memory, over this bus and loads them into its instruction pipeline registers.

A 20-bit multiplexed Microcode (M) bus provides a pathway between the CU chip and the microcode decode logic on all other chips which are under CU microcode control. The 40-bit wide microinstructions from the CU's microcode ROM are multiplexed on chip as two 20-bit words and presented on the interchip M bus during alternate phases of CLK02N. Microcode bits 39 through 20 are placed on the M bus during the CLK02N low phase and bits 19 through 0 during the high phase of CLK02N. The M bus is bidirectional to permit microcode memory expansion.

A 12-bit microcode address (CC) bus is used to route microcode addresses from the next microcode address source multiplexer to the microcode and instruction mapping ROMs as shown in Figure 2.

3.0 INTERFACE SIGNALS

All signal definitions are shown in Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix. e.g. HOLDN. Referenced signals that are not found on the MA17502 are preceded by the originating chip's functional acronym in parentheses, e.g. (IU)DMAKN.

A description of each pin function, grouped according to functional interface, follows. The function acronym is presented first, followed by its definition, its type, and its detailed description. Function type is either input, output, high impedance (Hi-Z), or a combination thereof. Timing characteristics of each of the functions described are provided in Section 6.0.

3.1 POWER INTERFACE

The power interface consists of a single 5V VDD connection and two common GND connections.

3.2 CLOCKS

The clock interface, discussed below, is the means by which the synchronous, microcoded operation of the MAS281 is driven.

3.2.1 Precharge Clock (CLKPCN)

Input. The MA17501 Execution Unit (EU), generates the CLKPCN signal for the Control Unit. The Control Unit uses this signal for most of its internal sequencing. During the low phase of CLKPCN, the internal M Bus is precharged to the high state to accelerate its response.

The normal CLKPCN period is defined by five OSC cycles (two cycles low and three cycles high). When a microcode branch is indicated by the EU, the low state of CLKPCN is extended to three OSC cycles. During execution of Interrupt Unit decoded XIO and microcode commands, the high state of CLKPCN is extended to four OSC cycles. Also, during external bus cycles, RDYN may be used to cause the EU to prolong the high state of CLKPCN to greater than three OSC cycles; this allows the MAS281 chip set to interface with slower external memory or input/output devices.

During DMA ((IU)DMAKN is low) or Hold ((EU)HLDAKN is low), CLKPCN will remain low until the CPU takes control again.

3.2.2 Phase 2 Clock (CLK02N)

Input. The MA17501 generates the CLK02N signal for the Control Unit. The CU then uses this signal, in conjunction with CLKPCN, to control the distribution of microcode on the M Bus. CLK02N is used to multiplex the 40-bit microcode instruction into two 20-bit words (μW1 and μW2). The high-to-low edge of CLK02N switches μW1 (bits 39 through 20) off the M Bus while switching μW2 (bits 19 through 0) onto the M Bus.

The normal CLK02N period is defined by five OSC cycles (one cycle low, three cycles high, one cycle low). When a microcode branch is indicated by the EU, the high state of CLK02N is extended to four cycles. During execution of Interrupt Unit decoded XIO and microcode commands, the trailing low state of CLK02N is extended to two OSC cycles. Also, during external bus cycles, RDYN may be used to cause the EU to prolong the CLK02N trailing low state to greater than one OSC cycle; this allows the MAS281 chip set to interface with slower external memory or inpuVoutput devices.

During DMA ((IU)DMAKN is low) or Hold ((EU)HLDAKN is low), CLKPCN will remain low until the CPU takes control again.

3.3 BUSES

The following is a discussion of the communication buses connecting the three-chip set. The AD Bus and M Bus are mainly operand transfer buses, while the CC Bus is strictly for providing microcode addresses to auxiliary CUs.

3.3.1 Address/Data Bus (AD Bus)

Input. These signals comprise the multiplexed address and data bus. During external bus operations, the AD bus accommodates the transfer of instructions, from memory and I/O ports, to the MA17502. During internal bus operations, the AD bus provides additional data to the Control Unit from the Execution Unit. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit address. A high on this bus corresponds to a logic 1 and a low corresponds to a logic 0. Information on the AD Bus is clocked into the CU by the high-to-low transition of CLKPCN.

3.3.2 Microcode Bus (M Bus)

Input/Output/Hi-z. The M Bus is the 20-bit multiplexed microcode bus. The 40-bit microcode instruction is multiplexed onto the M Bus as two 20-bit words (μW1 and μW2). The first half of the microcode word, μW1 (bits 39 through 20), is assured valid on the high-to-low transition of CLK02N and μW2 (bits 19 through 0) is assured valid on the high-to-low transition of CLKPCN. M00 corresponds to microcode bit 0 (μW1) or 20 (μW2) while M19 corresponds to microcode bit 19 (μW1) or 39 (μW2). A high level indicates a logic 1 and a low level indicates a logic 0. A high level on CS allows the Control Unit to distribute microcode over this bus, a low level places the bus in the high impedance state.

During DMA or Hold states, CLKPCN is held low, thus holding the internal M bus in the precharged state. Precharging the internal M Bus forces the 20 bits of the external M Bus low.

3.3.3 Microcode Address Bus (CC Bus)

Input/Output/Hi-Z. The CC bus is provided for future expansion and is left unconnected.

3.4 SEQUENCER CONTROL

The following is a discussion of the microsequencer control input signals. These signals support chip set functions that require microcode branching based on the results of operations performed in the Execution or Interrupt Units.

3.4.1 Interrupt Request (IRN)

Input. A low on this input directs the CU to service pending interrupt requests latched by the Interrupt Unit (IU). Upon completion of the currently executing MIL-STD-1750A instruction, the CU checks the IRN input. If IRN is low, then the CU sequencer will branch to the microcoded interrupt service routine; else the next MIL-STD-1750A instruction is mapped to its microcode routine. The microcoded interrupt service routine

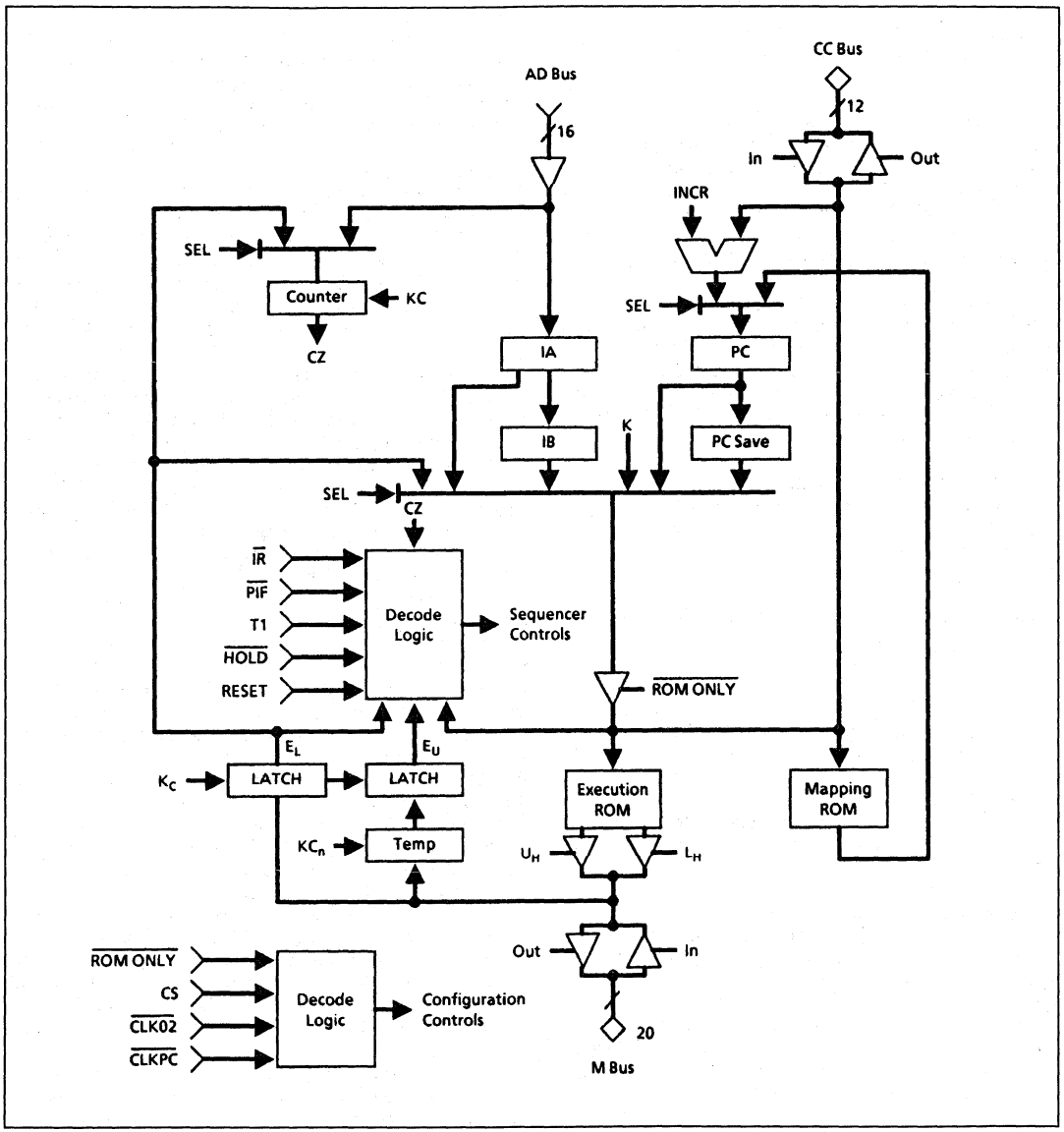


Figure 2: MA17502 Control Unit Architecture

stores the processor state, retrieves the highest priority pending interrupt's service routine processor state, and vectors software execution to the user's interrupt service routine. IRN originates in the IU.

3.4.2 Privileged Instruction Fault (PIFN)

A low on this signal causes the CU to enable control of the DMA interface (located in the Interrupt Unit), abort the currently executing MIL-STD-1750A instruction and check the IRN input for a pending level 1 interrupt caused by the IU latching a memory protect (MPROEN), memory address (EXADEN), or Bus Time-out fault. PIFN originates in the IU.

3.4.3 Branch or Jump Control (T1)

Input. A high on this input directs the CU microcode address sequencer to branch execution to a nonsequential microcode address. This signal is under the control of the Execution Unit's ALU and its level is dependent on the outcome of the presently executing microcode instruction, e.g. conditional branch. T1 originates in the EU.

3.5 CONFIGURATION CONTROL

The following inputs are provided for control of multiple CU systems. They allow for expansion of the microcode store to 4K 40-bit words.

3.5.1 ROM-Only (ROMONLYN)

Input. This signal is provided for future microcode expansion and must be pulled up to VDD.

3.5.2 Chip Select (CS)

Input. A high on this signal enables the CU to drive the 20-bit external M Bus. This signal is provided for future microcode expansion and must be pulled up to VDD.

3.6 CPU CONTROL

Grouped under this heading are signals that have CPU-wide control of normal operation. Each of these has the ability to "freeze" the processor.

3.6.1 Hold Request (HOLDN)

Input. A low on this input will suspend internal processor functions at the end of the currently executing MIL-STD1750A instruction. When this signal becomes active, the CU completes the currently executing MIL-STD-1750A instruction, then branches to the Hold microcode routine and enters the Hold state. The CU will resume normal operation by refilling the instruction pipeline registers (IA and IB) upon release of HOLDN.

3.6.2 System Reset (RESET)

Input. A high on this input for a duration of at least one CLKPCN period will reset the MAS281 chip set by forcing the Control Unit to microcode address zero. The high-to-low transition of this input will cause the CU to begin executing the MAS281 initialisation sequence starting with the first instruction in microcode. Built-in Test (BIT) is performed as part of the initialisation sequence. At the conclusion of initialisation and successful execution of BIT, the MAS281 will be initialised as shown in Table 3.

4.0 OPERATING MODES

The following discussions detail the MAS281 chip set operating modes from the perspective of the Control Unit. MAS281 operating modes involving the MA17502 include: (1) Initialisation, (2) Instruction Execution, (3) Interrupt Servicing, (4) DMA Support, and (5) HOLD Support.

4.1 INITIALISATION

The MA17502 sequences the MAS281 chip set through the microcoded initialisation routine in response to a high pulse on the RESET input. This routine clears the chip set registers, disables and masks interrupts' reads the configuration register, resets the output discrete register (if applicable), initialises the MMU and BPU (if applicable), performs Built-in Test (BIT), raises the StartUp ROM Enable discrete, clears and starts timers A and B, resets the Trigger-Go counter, and loads the instruction pipeline. The initialisation sequence is contained in the first 33 locations of microcode ROM (an additional 14 locations contain the optional MMU and BPU initialisation code). Because the initialisation sequence clears the Execution Unit's Instruction Counter and Status Word (also the address and processor state copies stored in the MMU(BPU), if applicable), program execution begins with the instruction located at address zero (page zero). Table 2 provides a detailed breakdown of the initialisation sequence and Table 3 summarises the resulting initialised state.

BIT occupies 332 words of microcode storage ROM, and consists of five subroutines that exercise the internal circuitry of the MAS281, as outlined in Table 4. BIT begins by pulling the Normal Power-UP ((IU)NPU) output low; this is the first time after power-up that the state of NPU is guaranteed. If all five BIT subroutines execute successfully, NPU is raised high.

If any part of BIT fails, an error code identifying the failed subroutine is loaded into the Interrupt Unit Fault Register (via the AD Bus), BIT is aborted, and NPU is left in the low state. Table 4 defines the coding of the BIT results. (NPU is raised high through microcode control of the IU in conjunction with the (EU)INTREN signal. The BIT error codes are loaded in the IU Fault Register via the AD Bus under microcode control of the IU in conjunction with the (EU)INTREN signal.)

In the event of such a failure, the resulting chip set reset state is dependent on where in BIT the error occurred and may not be the same as that shown in Table 3. A BIT failure indication in the fault register sets the level 1 pending interrupt. Since initialisation disables and masks interrupts, the IRN input will remain high; thus the interrupt will not be serviced immediately.

The last action performed by the initialisation routine is to load the instruction pipeline. Instruction fetches start at memory location zero (page zero) from the Start-Up ROM (if implemented). Whether BIT passes or not, the processor will begin instruction execution at this point.

Note: To complete initialisation and pass BIT, interrupt and fault inputs must be high for the duration of the initialisation routine. Also, the Timers A and B must be clocked for BIT success.

Label	Cycle		
MAIN	B1	1.	Enable Control of DMAE Output signal
	P	2.	-
	B1	3.	Clear MAS281 Execution Unit Status Word (SW) Clear Interrupt Mask (MK) (Internal I/O command, SKM, 2000H)
	B1	4.	Clear Pending Interrupt Register (PI) and Fault Register (FT) (Internal I/O Command, CLIR, 2001H) Clear Instruction Counter (IC)
	P	5.	-
	B1	6.	Disable Interrupts (Internal I/O Command, DSBL, 2003H)
	P	7.	-
	B1	8.	Clear MMU Status Word (Internal I/O Command, WSW, 200EH) (Note 1)
	P	9.	-
	B1	10.	Disable DMA Access (Internal I/O Command, DMAD, 4007H)
	P	11.	-
	B1	12.	Read Configuration Register (Internal I/O Command, RCW, 8400H, CONFWN Drops low per Figure 25, Section 5.0)
	P	13.	-
	P	14.	-
	B2	15.	- (If Output Discrete Register Present, then Continue; Else, Skip to 18)
	P	(16).	-
	I/O	(17).	Clear Output Discrete Register (External I/O Command)
	B2	19.	- (If BPU present, then Branch to BPU; else, continue)
	P	20.	-
	B2	21.	- (If MMU present, then Branch to MMU; Else, Continue)
	P	22.	- (Setup Temporary Register to indicate No MMU Present)
	B2	23.	- (Branch to MAS281 BIT)
	P	24.	-
	B1	25.	Enable Start-Up ROM (Internal I/O Command, ESUR, 4004H; SURE Raises High per Figure 25, Section 5.0)
	P	26.	-
	B1	27.	Clear and Start Timer A (Internal I/O Command, OTA, 400AH)
	B1	28.	Reset the Trigger-Go timer (Internal I/O Command, GO, 400BH)
	P	29.	-
	B1	30.	Clear and Start Tlmer B (Internal I/O Command, OTB, 400EH)
	B2	31.	- (Branch to Load Instruction Pipeline Routine)
	M	32.	Load data-In register (DI) and instruction Register A (IA) from [IC], Increment IC
	M	33.	Load Data-In Register (DI) and Instruction Register a (IA) from [IC] ([IA] Moves to IB), Increment IC Map Instruction Register B (IB) into Microcode Routine
BPU	P	(1).	-
	P	(2).	- (Set Loop to Clear Memory Protect RAM)
	I/O	(3).	Clear a Location in MPRAM (Internal I/O Command, LMP, 50XXH), Increment Address; Do 128 Times
		(4).	- (Branch Back to 20.)
MMU	P	(1).	-
	P	(2).	-
	P	(3).	- (Setup Loop to Load Instruction Page Registers (IPR) and Operand Page Registers (OPR) wlth Sequential Values of 0 to 255)
	P	(4).	-
	P	(5).	-
	I/O	(6).	Load a Location in the IPR with the value of the Locatron Address (Internal I/O Command, WIPR, 51XYH)
	I/O	(7).	Load a Location in the OPR Increment Loaded Value with the Value of the Location Address (Internal I/O Command, WOPR, 52XYH)
	P	(8).	- (Increment IPR Address)
	P	(9).	- (Increment OPR Address - Repeat Loop [4. - 9.] 256 Times)
	B2	(10).	- (Setup Temporary Register to Indicate MMU Present; Branch back to 23)

Notes: 1. This operation Is performed whether or not an MMU is present.
2. "-" indicates internal CPU operation.
3. Sequence numbers in "( )" are performed only under the stated conditions.
4. Each step enumerated above represents a single machine (SYNC) cycle of the type shown in the "Cycle" column.
"P" indicates a 5 OSC cycle, 60% duty cycle, machine cycle.
"I/O" and "M" indicate a 5 OSC cycle, 50% duty cycle, machine cycle.
"B1" indicates a 6 OSC cycle 50% duty cycle machine cycle.
"B2" indicates a 6 OSC cycle 66% duty cycle machlne cycle.

Table 2: MAS281 Initialisation Sequence

MAS281	
Instruction Counter (IC)	Zeroed
Status Word (EU and MMU) (SW)	Zeroed
Fault (FT)	Zeroed
Pending Interrupt (PI)	Zeroed
Mask (MK)	Zeroed
General Register File (RO R15)	Zeroed
Interrupts	Disabled
DMA Access	Disabled
TimerA	Reset and Started
Timer B	Reset and Started
Trigger-Go Timer	Reset and Started
MMU	
Page Registers	Group Zero Enabled
AL, W, E, Fields	Zeroed
PPA Field	Logical to Physical Map
BPU	
Write Protect	Zeroed
Global Memory Protect	Enabled

Table 3: Initialisation State

BIT	Test Coverage	BIT Fail Codes ($FT_{13, 14,15}$)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Microcode Flags Multiply Divide	101	166
3	Interrupt Unit MK, PI, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15)	110	154
5	Timer A Timer B	111	763
	BIT Pass/Fail Overhead	-	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14 and 15

Table 4: Built In Test (BIT) Summary

4.2 INSTRUCTION EXECUTION

The MIL-STD-1750A microcoded instruction subroutines are stored in 1255 locations of microcode storage ROM. The Control Unit receives instructions from memory, via the AD Bus, through the instruction pipeline registers IA and IB. When the previous instruction or special process (Interrupts or Hold) has been completed, the new instruction residing in register IB is selected by the next microcode address source multiplexer. A 4-bit hardwired constant, appended by the instruction opcode, is then used as the first address of a microcode sequence which distributes the required control to execute the instruction. The microsequencer generates the remaining microcode addresses necessary to complete the sequence as described in Section 2.0 of this data sheet entitled, "Architecture".

Upon completion of the current instruction, the CU will accept the next instruction in the program unless an interrupt, DMA, or Hold request is received. The interrupt and Hold request share a common branch point in microcode. If an interrupt and Hold request are both pending at the conclusion of the MIL-STD-1750A instruction microcode routine, the Hold request has priority and is serviced first. Upon release of the Hold state, the first instruction will execute even if the interrupt is still pending; when this instruction is complete the interrupt will be serviced (assuming the HOLDN input has not been driven low during execution of this instruction). Interrupt, DMA, and Hold support are explained in more detail in following sections.

4.3 DIRECT MEMORY ACCESS

Direct Memory Access (DMA) is controlled by the Execution Unit (EU) in concert with the Interrupt Unit DMA interface. The CU supports DMA by suspending processor control upon completion of the current machine cycle. If DMA is enabled ((UI)DMAE signal, high) a DMA request ((IU)DMARN input, low) to the MAS281 causes the IU to acknowledge with DMAKN, low. When the EU receives the DMAKN (DMA Acknowledge) signal from the IU, the CU clocks are suspended (CLKPCN, low; CLK02N, high) halting the MAS281's microcode sequencing. Microinstruction execution remains suspended until DMARN is removed. When DMARN is removed, microcode execution resumes where DMARN had interrupted it.

4.4 INTERRUPT HANDLING

Interrupts are handled by the interrupt Unit (IU) and communicated to the CU via the IRN input. The CU checks the status of the IRN (Interrupt Request) signal after the completion of each MIL-STD-1750A microcode instruction sequence. If the IRN signal is low, the CU initiates interrupt handling, otherwise the CU processes a new instruction.

IU interrupt handling is controlled by the CU through three microcode bits - M04, M05, and M06. Upon receipt of the IRN signal and after completion of the currently executing instruction, the CU branches to a microcoded interrupt handling routine. The microprogram sequence supplies microcoded control to the IU for reading the highest priority pending interrupt vector code, which also clears this pending interrupt.

Due to the similarity of interrupt and hold request handling by the CU, if a Hold and interrupt request are pending at the end of an instruction sequence the Hold has priority and will be serviced.

4.5 HOLD SUPPORT

The CU accepts a Hold request in much the same way as an interrupt request. After the completion of each MIL-STD-1750A microcode instruction sequence, the CU checks the status of the HOLDN signal. If the HOLDN signal is low, a microcoded sequence suspends further internal processing functions; otherwise, the CU processes a new instruction or services interrupt requests (Hold requests have priority over interrupt requests).

The Control Unit responds to an active HOLDN signal, upon completion of the currently executing instruction, but branching to a microprogrammed sequence of instructions that suspends all internal operations. This sequence of microinstructions allows the processor to resume instruction execution at the point HOLDN was accepted when the CU regains control of the processor. The MAS281 remains in the Hold state until HOLDN is pulled high (if the Hold state was reached through the hardware interface, HOLDN) or HOLDN is pulsed low (if the Hold state was reached through software, BPT instruction). HOLDN should be synchronised to AS falling.

5.0 SOFTWARE CONSIDERATIONS

The MAS281 chip set implements the full MIL-STD-1750A instruction set. Table 6a gives a brief listing of this instruction set and provides performance data for each instruction. Table 6b provides a summary of the I/O commands implemented in MAS281 and MA31751 MMU/BPU hardware. A complete description of this instruction set is provided in MIL-STD-1705A (Notice 1). The register set available to the software programmer is depicted in Figure 3. A discussion of data types, addressing modes, and benchmarking considerations fol lows.

5.1 DATA TYPES

The MAS281 chip set supports 16-bit fixed-point single precision, 32-bit fixed-point double-precision, 32-bit floating-point, and 48-bit extended-precision floatingpoint data types. Figure 4 depicts the formats of these data types.

All numerical data is represented in two's complement form. Floating-point numbers are represented by a fractional two's complement mantissa with an 8-bit two's complement exponent. The MAS281 expects all floating point operands to be normalised. If they are not normalised, the results from an instruction are not defined.

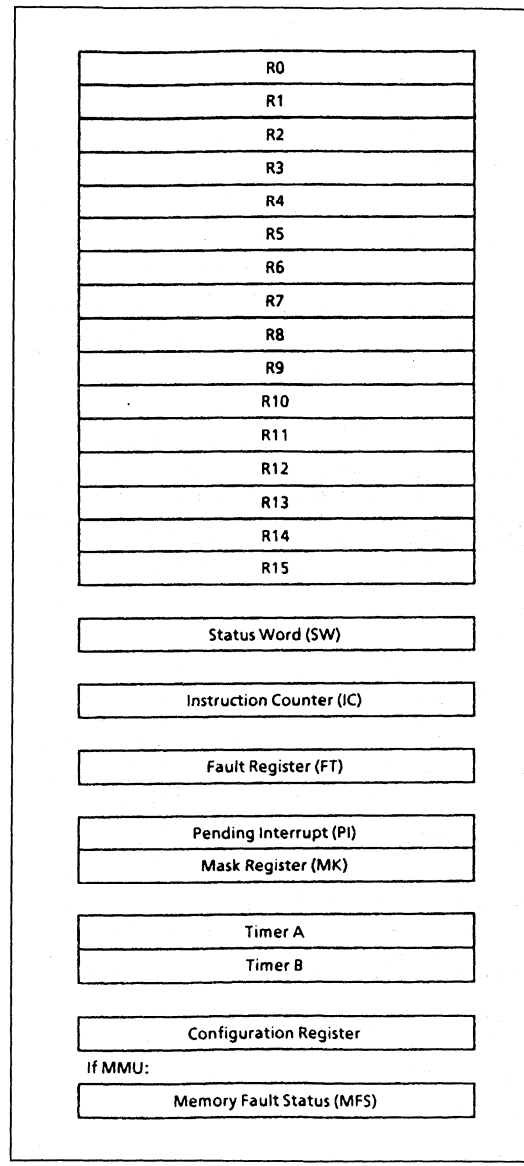


Figure 3: Register Set Model

5.2 ADDRESSING MODES

The MAS281 chip set supports the eight addressing modes specified in MIL-STD-1750A. These addressing modes are shown in Figure 5 and are defined below.

5.2.1 Register Direct (R)

The register specified by the instruction (RB) contains the required operand.

5.2.2 Memory Direct (D,DX)

Memory Direct (without indexing) is an addressing mode in which the instruction contains the memory address (A) of the required operand. In Memory Direct (indexed), the memory address of the required operand is specified by the sum of the contents of an index register (RX) and the instruction address field (A). Registers R1 through R15 may be specified for indexing.

5.2.3 Memory Indirect (I,IX)

Memory Indirect (without indexing) is an addressing mode in which the memory address (A) specified by the instruction contains the address of the required operand. In Memory Indirect (pre-indexed), the sum of the contents of a specified index register (RX) and the instruction address field (A) is the address of the address of the required operand. Registers R1 through R15 may be specified for indexing.

5.2.4 Immediate Long (IM)

There are two formats that implement Immediate Long Addressing; one allows indexing and one does not. For the indexable format, if the specified index register (RX) is not equal to zero, the contents of RX are added to the immediate field to form the required operand, otherwise, the immediate field contains the required operand .

5.2.5 Immediate Short (IS)

In this mode the required 4-bit operand is contained within the 16-bit instruction. The Immediate Short addressing mode accommodates two formats; one which interprets the contents of the immediate field as positive data and the other which interprets the contents of the immediate field as negative data.

5.2.6 Immediate Short Positive (ISP)

The immediate operand is treated as a positive integer between 1 and 16.

5.2.7 Immediate Short Negative (ISN)

The immediate operand is treated as a negative integer between 1 and 16. Its internal form is a two's complement, sign-extended 16-bit number.

5.2.8 Instruction Counter Relative (ICR)

This addressing mode is used for 16-bit branch instructions. The contents of the instruction counter minus two (the address of the current instruction) is added to the sign-extended 8-bit displacement field (D) within the instruction. This sum then points to the memory address to which control may be transferred if a branch is to be taken.

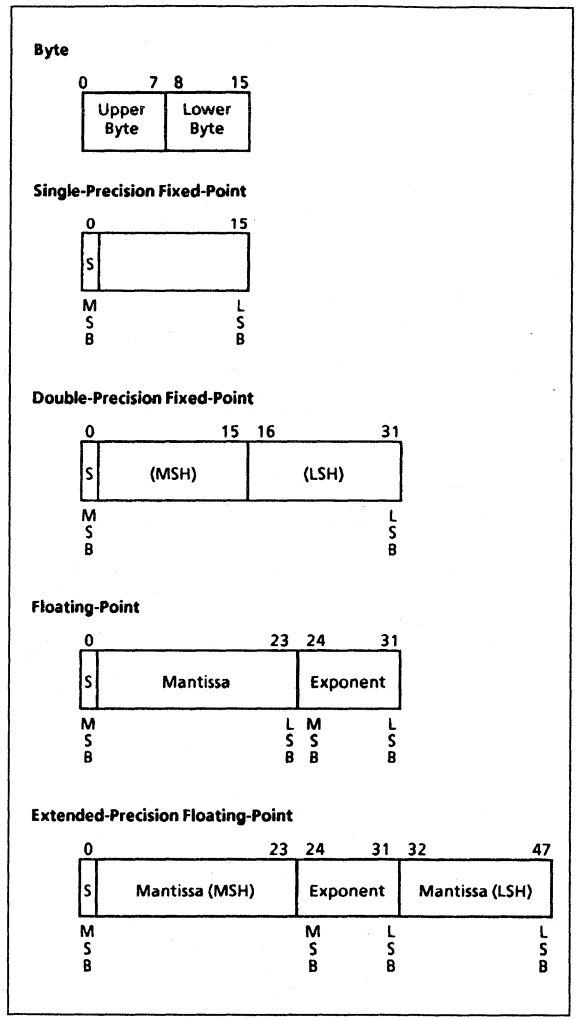


Figure 4: Data Formats

5.2.9 Base Relative (B)

There are two formats which implement Base Relative Addressing; one allows indexing and one does not. For the non-indexable form the contents of the instruction specified base register (BR = BR' + 12) is added to the 8-bit displacement field (DU) of the 16-bit instruction. For the indexable form, the sum of the contents of a specified index register (RX) and a specified base register (BR = BR' + 12) is the address of the required operand. Registers R1 through R15 may be specified for indexing and the base register may be R12 through R15.

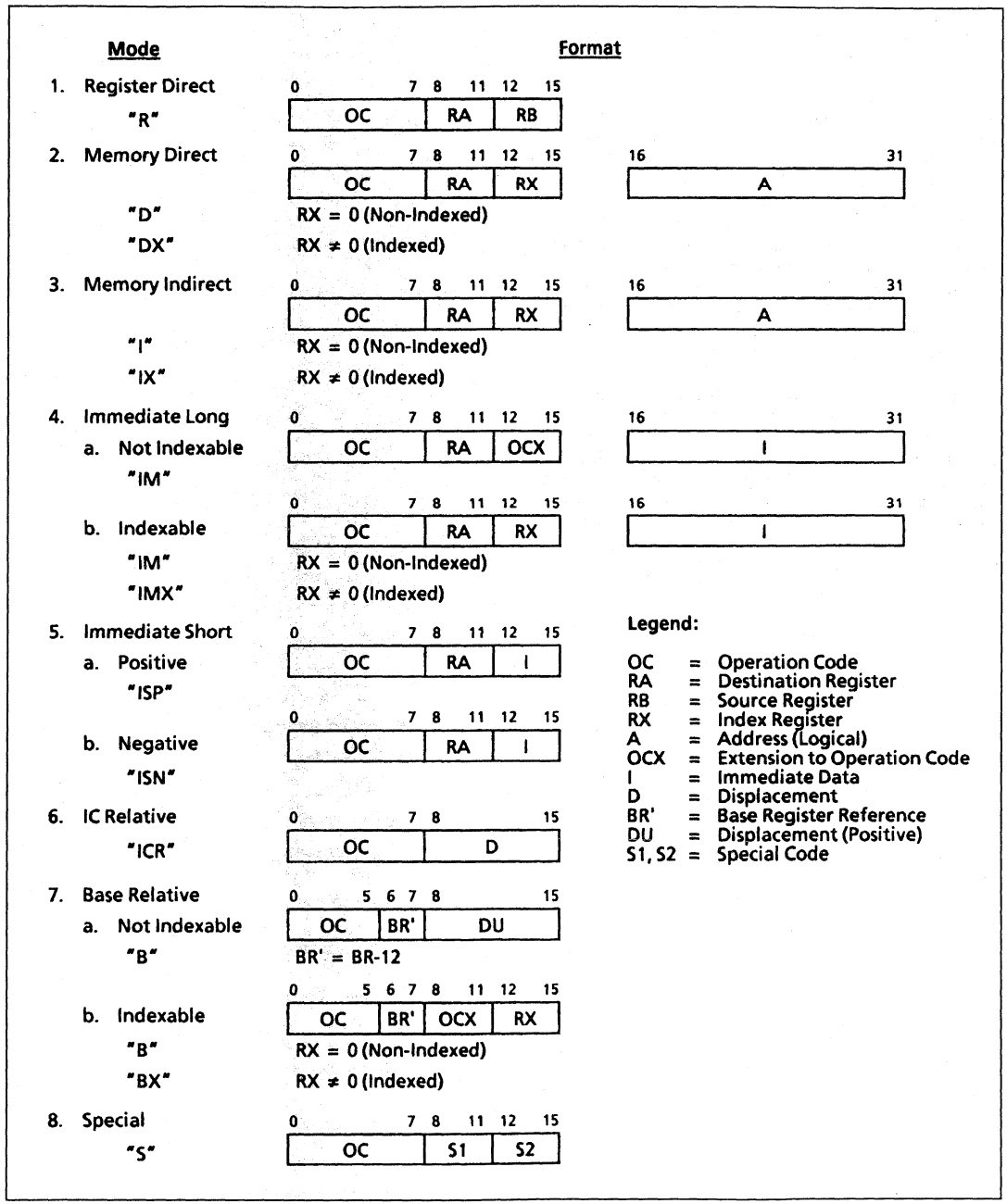


Figure 5: Addressing Modes

5.2.10 Special (S)

This addressing mode is applicable to instructions that do not follow the above formats.

5.3 BENCHMARKING

Table 6a defines the number and type of machine cycles associated with each MIL-STD-1750A instruction. This information may be used when benchmarking MAS281 performance. The Digital Avionics Instruction Set (DAIS) mix, which defines a typical frequency of occurrence for MIL-STD-1750A instructions, is used here for this purpose.

One problem with the DAIS mix, however, is that it does not reflect the impact of data dependencies on system performance. For example, a multiplication in which one operand is zero may be performed much faster than one with two non-zero operands. Also, the DAIS mix does not specify such time consuming operations as normalization and alignment.

Realistic benchmarks must therefore take both an instruction mix and data dependencies into account. To this end, machine cycle counts in Table 6a which have data dependencies are annotated with either an "a" suffix to reflect an average number of machine cycles (where each of several possibilities is equally likely) or with a "wa" suffix to reflect a weighted average number of machine cycles (where some data possibilities are more likely than others). Weighted averages are only applicable to floating-point operations.

Weighted averages provided in Table 6a, based on the Sweeney (IBM Systems Journal, Vol. 4, No. 1, 1965) guidelines, take a wide range of data dependencies into consideration. Normalization and alignment operations are also represented. Table 5 defines MAS281 throughput, at various frequencies and wait states, for the DAIS mix using Sweeney data dependencies.

It should be noted that using the Sweeney guidelines is a conservative approach to benchmarking. If best case assumptions are made and such operations as normalization and alignment are not considered, MAS281 performance figures are approximately 50% higher than those indicated in Table 5.

f_{OSC} MHz	0	1	2	3
25	743.4	698.3	658.4	622.8
20	594.7	558.7	526.7	498.2
15	446.0	419.0	395.0	373.7
10	297.4	279.3	263.4	249.1

Number of Wait States in Memory Access Cycle

Table 5: Throughput (KIPS)

5.4 INSTRUCTION SUMMARY

Operation	Op Code/Ext	Mnemonic	Format	Cycles*		
				M	P	B
LOAD/STORE						
Single Precision Load	81	LR	R	1	0	0
	0X	LB	B	2	1	0
	4X 0	LBX	BX	2	1	0
	82	LISP	ISP	1	0	0
	83	LISN	ISN	1	0	0
	80	L	D,DX	3	0	0
	85	LI M	IM,IMX	2	0	0
	84	LI	I,IX	4	1	0
Double-Precision Load	87	DLR	R	1	2	0
	0X	DLB	B	3	1	0
	4X 1	DLBX	BX	3	2	0
	86	D L	D,DX	4	0	0
	88	DLI	I,IX	5	1	0
Single-Precision Store	0X	STB	B	2	2	0
	4X 2	STBX	BX	2	2	0
	90	ST	D,DX	3	1	0
	94	STI	I,IX	4	1	0
Store a Non-Negative Constant	91	STC	D,DX	3	1	0
	92	STCI	I,IX	4	1	0
Double-Precision Store	0X	DSTB	B	3	2	0
	4X 3	DSTX	BX	3	2	0
	96	DST	D,DX	4	0	0
	98	DSTI	I,IX	5	1	0
Load Multiple Registers	89	LM	D,DX	3 + n	1	1
Store Multiple Registers	99	STM	D,DX	3 + n	1	1
INTEGER ARITHMETIC						
Single-Precision IntegerAdd	A1	AR	R	1	1	0
	1X	AB	B	2	2	0
	4X 4	ABX	BX	2	2	0
	A2	AISP	ISP	1	1	0
	A0	A	D,DX	3	1	0
	4A 1	AIM	IM	2	1	0
Increment Memory by a Positive Integer	A3	INCM	D,DX	4	1	0
Single-Precision Absolute Value of Register	A4	ABS	R	1	1.5	1a
Double-Precision Absolute Value of Register	A5	DABS	R	1	2.5	1a

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 6a: Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles*		
				M	P	B
Double-Precision Integer Add	A7	DAR	R	1	3	0
	A6	DA	D,DX	4	1	0
Single Precision Integer Subtract	B1	SR	R	1	1	0
	1X	SBB	B	2	2	0
	4X 5	SBBX	BX	2	2	0
	B2	SISP	ISP	1	1	0
	B0	S	D,DX	3	1	0
	4A 2	SIM	IM	2	1	0
Decrement Memory by a Positive Integer	B3	DECM	D,DX	4	1	0
Single Precision Negate Register	B4	NEG	R	1	1	0
Double-Precision Negate Register	B5	DNEG	R	1	3	0
Double-Precision Integer Subtract	B7	DSR	R	1	3	0
	B6	DS	D,DX	4	1	0
Single Precision Integer Multiply with 16-Bit Product	C1	MSR	R	1	6.5	4a
	C2	MISP	ISP	1	7.5	4a
	C3	MISN	ISN	1	7.5	4a
	C0	MS	D,DX	3	6.5	4a
	4A 4	MSIM	IM	2	6.5	4a
Single Precision Integer Multiply with 32-Bit Product	C5	MR	R	1	5	3
	1X	MB	B	2	7	3
	4X 6	MBX	BX	2	7	3
	C4	M	D, DX	3	5	3
	4A 3	MIM	IM	2	5	3
Double-Precision Integer Multiply	C7	DMR	R	1	41	4.5a
	C6	DM	D,DX	4	40	4.5a
Single Precision Integer Divide with 16-Bit Dividend	D1	DVR	R	1	20.25	5.5a
	D2	DISP	ISP	1	20	5.5a
	D3	DISN	ISN	1	20.5	5.5a
	D0	DV	D,DX	3	20.25	5.5a
	4A 6	DVIM	IM	2	20.25	5.5a
Single Precision Integer Divide with 32-Bit Dividend	D5	DR	R	1	21.75	6.5a
	1 X	DB	R	2	22.75	6.5a
	4X 7	DBX	BX	2	22.75	6.5a
	D4	D	D,DX	3	21.75	6.5a
	4A 5	DIM	IM	2	22.75	6.5a
Double-Precision Integer Divide	D7	DDR	R	1	79.5	5.5a
	D6	DD	D,DX	4	77.5	5.5a

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 6a (continued): Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles*		
				M	P	B
LOGICAL						
Inclusive Logical OR	E1	ORR	R	1	0	0
	3X	ORB	B	2	1	0
	4X F	ORBX	BX	2	1	0
	E0	OR	D,DX	3	0	0
	4A 8	ORIM	IM	2	0	0
Logical AND	E3	ANDR	R	1	0	0
	3X	ANDB	B	2	1	0
	4X E	ANDX	BX	2	1	0
	E2	AND	D,DX	3	0	0
	4A 7	ANDM	IM	2	0	0
Exclusive Logical OR	E5	XORR	R	1	0	0
	E4	XOR	D,DX	3	0	0
	4A 9	XORM	IM	2	0	0
Logical NAND	E7	NR	R	1	1	0
	E6	N	D,DX	3	1	0
	4A B	NIM	IM	2	1	0
Set Bit	51	SBR	R	1	0	0
	50	SB	D,DX	4	1	0
	52	SBI	I,IX	5	2	0
Reset Bit	54	RBR	R	1	1	0
	53	RB	D,DX	4	1	0
	55	RBI	I,IX	5	2	0
Test Bit	57	TBR	R	1	0	0
	56	TB	D, DX	3	0	0
	58	TBI	I,IX	4	1	0
Test and Set Bit	59	TSB	D,DX	4	0	2
Set Variable Bit in Register	5A	SVBR	R	1	0	1
Reset Variable Bit in Register	5C	RVBR	R	1	1	1
Test Variable Bit in Register	5E	TVBR	R	1	0	1
Store Register Through Mask	97	SRM	D,DX	4	3	0
BYTE						
Load From Upper Byte	8B	LUB	D,DX	3	0	0
	8D	LUBI	I,IX	4	1	0
Load From Lower Byte	8C	LLB	D,DX	3	1	0
	8E	LLBI	I,IX	4	2	0
Store Into Upper Byte	9B	STUB	D,DX	4	1	0
	9D	SUBI	I, IX	5	3	0
Store Into Lower Byte	9C	STLB	D,DX	4	1	0
	9E	SLBI	I,IX	5	2	0
Exchange Bytes in Register	EC	XBR	S	1	0	1

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 6a (continued): Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles*		
				M	P	B
COMPARE						
Single-Precision Compare	F1	CR	R	1	0	0
	3X	CB	B	2	1	0
	4X C	CBX	BX	2	1	0
	F2	CISP	ISP	1	0	0
	F3	CISN	ISN	1	0	0
	F0	C	D,DX	3	0	0
	4A A	CIM	IM	2	0	0
Compare Between Limits	F4	CBL	D,DX	4	2.75	1.75a
Double-Precision Compare	F7	DCR	R	1	2	0
	F6	DC	D,DX	4	0	0
JUMP/BRANCH						
Jump on Condition	70	JC	D,DX	2	0.5	1a
	71	JCI	I,IX	3	0.5	1a
Jump to Subroutine	72	JS	D,DX	2	2	0
Subtract One and Jump	73	SOJ	D,DX	2	2.5	1a
Branch Unconditionally	74	BR	ICR	2	2	0
Branch if Equal to (zero)	75	BEz	ICR	1.5	1	1a
Branch if Less than (zero)	76	BLT	ICR	1.5	1	1a
Branch to Executive	77	BEX	S	16	12	3a
Branch if Less than or Equal to (Zero)	78	BLE	ICR	1.5	1	1a
Branch if Greater than (Zero)	79	BGT	ICR	1.5	1	1a
Branch if Not Equal to (Zero)	7A	BNZ	ICR	1.5	1	1a
Branch if Greater than or Equal to (Zero)	7B	BGE	ICR	1.5	1	1a
SHIFT						
Shift Left Logical	60	SLL	R	1	1	0
Shift Right Logical	61	SRL	R	1	1	0
Shift Right Arithmetic	62	SRA	R	1	1	0
Shift Left Cyclic	63	SLC	R	1	1	0
Double Shift Left Logical	65	DSLL	R	1	3	0
Double Shift Right Logical	66	DSRL	R	1	2	0
Double Shift Right Arithmetic	67	DSRA	R	1	2	0
Double Shift Left Cyclic	68	DSLC	R	1	3	0
Shift Logical, Count in Register	6A	SLR	R	1	1	3
Shift Arithmetic, Count in Register	6B	SAR	R	1	1.5	3.50a
Shift Cyclic, Count in Register	6C	SCR	R	1	1	3.25a
Double Shift Logical, Count in Register	6D	DSLR	R	1	2.25	4a
Double Shift Arithmetic, Count in Register	6E	DSAR	R	1	3.19	4.94a
Double Shift Cyclic, Count in Register	6F	DSCR	R	1	3.5	3a

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 6a (continued): Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles*		
				M	P	B
CONVERT						
Convert Floating-Point to 16-Bit Integer	E8	FIX	R	1	4.25	4.5a
Convert 16-Bit Integer to Floating-Point	E9	FLT	R	1	3	2a
Convert Extended-Precision Floating-Point to 32-Bit Integer	EA	EFIX	R	1	12.25	6.25a
Convert 32-Bit Integer to Extended-Precision Floating-Point	EB	EFLT	R	1	7.5	3.5a
STACK						
Stack IC and Jump to Subroutine	7E	SJS	D,DX	4	3	0
Unstack IC and return from Subroutine	7F	URS	S	3	1	
Pop Multiple registers off the Stack	8F	POPM	S	2.5 + n (n=0-15)	2.25 + n (n=0-15)	4.25a
Push Multiple Registers onto the Stack	9F	PSHM	S	1 + n (n=0-15)	4.5 + n (n=0-15)	2a
I/O (See I/O Command Summary)						
Execute I/O	48	XIO**	IM,IMX	3	3.583	6.277a
Vectored I/O	49	VIO**	D,DX	-	-	-
SPECIAL						
Built-In Function Call	4F	BIF	S			
Move Multiple Words, Memory-to-Memory	93	MOV	S	1 + 4n	1 + 3n	1 + 2na
Exchange Words in Registers	ED	XWR	R	1	2	0
Load Status	7D	LST**	D,DX	8	2	3
	7C	LSTI**	I,IX	9	2	4
No Operation	FF	NOP	S	1	2	2
Break Point	FF	BPT	S	3	4	4

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles). ** Privileged instruction.
a = average if more than one alternative exists.

Table 6a (continued): Instruction Summary

Operation	Op Code/Ext	Mnemonic	Format	Cycles*		
				M	P	B
FLOATING-POINT						
Extended-Precision Floating-Point Load	8A	EFL	D,DX	5	0	1
Extended-Precision Floating-Point Store	9A	EFST	D,DX	5	0	1
Floating-Point Absolute Value of Register	AC	FABS	R	1	1 .75	3.25a
Floating-Point Negate Register	BC	FNEG	R	1	3.25	3.75a
Floating-Point Compare	F9	FCR	R	1	2.75	2.875wa
	3X	FCB	B	2	2.75	2.875wa
	4X D	FCBX	BX	2	2.75	2.875wa
	F8	FC	D,DX	3	1.75	2 875wa
Extended-Precision Floating-Point Compare	FB	EFCR	R	1	3.25	2.875wa
	FA	EFC	D,DX	4.25a	2.75	2.875wa
Floating-Point Add	A9	FAR	R	1	7.625	8.25wa
	2X	FAB	B	3	6.625	8.25wa
	4X 8	FABX	BX	3	6.625	8.25wa
	A8	FA	D,DX	4	5.625	8.25wa
Extended-Precision Floating-Point Add	AB	EFAR	R	1	21.3125	10.5625wa
	AA	EFA	D,DX	5	19.3125	10.5625wa
Floating-Point Subtract	B9	FSR	R	1	8.625	8.625wa
	2X	FSB	B	3	7.625	8.625wa
	4X 9	FSBX	BX	3	7.625	8.625wa
	B8	FS	D,DX	4	6.625	8.625wa
Extended-Precision Floating-Point Subtract	BB	EFSR	R	1	23.0625	11.8125wa
	BA	EFS	D,DX	5	21.0625	11.8125wa
Floating-Point Multiply	C9	FMR	R	1	12.75a	6.25wa
	2X	FMB	B	3	12.75a	6.25wa
	4X A	FMBX	BX	3	12.75a	6.25wa
	C8	FM	D,DX	4	11.75a	6.25wa
Extended-Precision Floating-point Multiply	CB	EFMR	R	1	59.75	6.25wa
	CA	EFM	D,DX	5	57.75	6.25wa
Floating-Point Divide	D9	FDR	R	1	31.5	32.75wa
	2X	FDB	B	3	30. 5	32.75wa
	4X B	FDBX	BX	3	30.5	32.75wa
	D8	FD	D,DX	4	29.5	32.75wa
Extended-Precision Floating-Point Divide	DB	EFDR	R	1	102.625	47.875wa
	DA	EFD	D,DX	5	100.625	47.875wa

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists, wa = weighted average favouring one or more possible alternatives.

Table 6a (continued): Instruction Summary

5.5 INTERNAL I/O COMMAND SUMMARY

Operation	Command Code (Hex)	Mnemonic	Cycles*		
			M	P	B
Implemented in MAS281					
Set Fault Register	0401	SFR	2	3	9
Set Interrupt Mask	2000	SMK	2	3	9
Clear Interrupt request	2001	CLIR	2	3	9
Enable Interrupts	2002	ENBL	2	3	9
Disable Interrupts	2003	DSBL	2	3	9
Reset Pending Interrupt	2004	RPI	2	3	9
Set Pending Interrupt Register	2005	SPI	2	3	9
Reset Normal Power Up Discrete	200A	RNS	2	3	9
Write Status Word	200E	WSW	2	3a	8.5a
Enable Start-Up ROM	4004	ESUR	2	3	9
Disable Start-Up ROM	4005	DSUR	2	3	9
Direct Memory Access Enable	4006	DMAE	2	3	9
Direct MemoryAccess Disable	4007	DMAD	2	3	9
Ti mer A Start	4008	TAS	2	3	9
Ti mer A Halt	4009	TAH	2	3	9
Output Timer A	400A	OTA	2	3	9
Reset Trigger-Go	400B	GO	2	3	9
Timer B Start	400C	TBS	2	3	9
Timer B Halt	400D	TBH	2	3	9
Output Timer B	400E	OTB	2	3	9
Read Configuration Word	8400	RCW	2	2	4
Read Fault Register Without Clear	8401	RFR	2	2	4
Read Interrupt Mask	A000	RMK	2	2	4
Read Pending Interrupt Register	A004	RPIR	2	2	4
Read Status Word	A00E	RSW	2	1	4
Read and Clear Fault Register	A00F	RCFR	2	2	4
Input Timer A	C00A	ITA	2	2	4
Input Timer B	C00E	ITB	2	2	4
Implemented in BPU					
Memory Protect Enable	4003	MPEN	2	4	8
Load Memory Protect RAM	50XX	LMP	2	4	8
Read Memory Protect RAM	D0XX	RMP	2	3	3
Implemented in MMU					
Write Instruction Page Register	51XY	WIPR	2	4	8
Write Operand Page Register	52XY	WOPR	2	4	8
Read Memory Fault Status	A00D	RMFS	2	3	3
Read Instruction Page Register	D1XY	RIPR	2	3	3
Read Operand Page Register	D2XY	ROPR	2	3	3

* M = memory, P = processor (5 OSC cycles), B = processor (6 OSC cycles), a = average if more than one alternative exists.

Table 6b: Internal I/O Command Summary

6.0 TIMING CHARACTERISTICS

This section provides the detailed timing specifications for the MA17502. Figure 6 depicts the test load used to obtain timing data. Figures 7 through 9 depict the timing waveforms associated with various MA17502 signals. Table 7 provides values for parameters specified in the timing waveforms. All timing values provided in Table 7 are valid over the full military temperature range (-55°C to +125°C), and are measured from 50% point to 50% point (50% of VDD supply voltage, unless otherwise specified). Crosshatching in Figure 7 indicates either a "don't care" or indeterminate state.

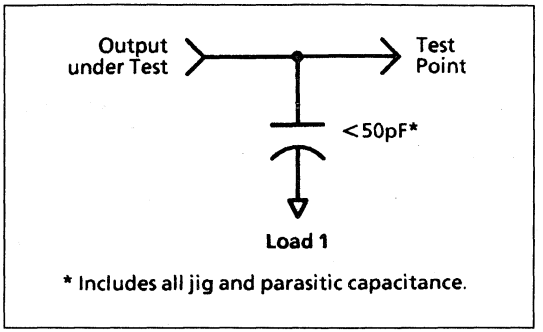


Figure 6: Test Load

Subgroup	Definition
1	Static characteristics specified in Table 9 at +25°C
2	Static characteristics specified in Table 9 at +125°C
3	Static characteristics specified in Table 9 at -55°C
7	Functional tests at +25°C
8a	Functional tests at +125°C
8b	Functional tests at -55°C
9	Switching characteristics specified in Table 7b at +25°C
10	Switching characteristics specified in Table 7b at +125°C
11	Switching characteristics specified in Table 7b at -55°C

Table 7a: Definition of Subgroups

No.	Parameter	Test Condition (1) (2)	Min	Max	Units
1	CLKPC ↑ to Microword 1 Valid	Load 1	-	95	ns
2	CLK02 ↓ to Microword 2 Valid	Load 1	-	41	ns
3	Microword 1 after CLK02 ↓	Load 1	5	-	ns
4	Microword 2 after CLKPC ↓	Load 1	25	-	ns
5	AD Bus to CLKPC ↓	-	10	-	ns
6	T1 to CLKPC ↑	-	20	-	ns
7	PIF to CLKPC ↑	-	20	-	ns
8	IR to CLKPC ↑	-	20	-	ns
9	HOLD to CLKPC ↓	-	15	-	ns
10	RESET to CLKPC ↓	-	15	-	ns
11	AD Bus after CLKPC ↓	-	15	-	ns
12	HOLD after CLKPC ↓	-	15	-	ns
13	RESET after CLKPC ↓	-	15	-	ns
14	T1, PIF, IR after CLKPC ↓	-	0	-	ns

Mil-Std-883, Method 5005, Subgroup 9, 10, 11

Notes: 1. TA = +25°C, -55°C and +125°C tested at VDD = 4.5V and 5.5V.
2. Unless otherwise noted: VIL ≥ 0.0V, VIHTTL ≤ 4.0V; timing measured from 50% to 50% point.

Table 7b: Timing Parameter Values

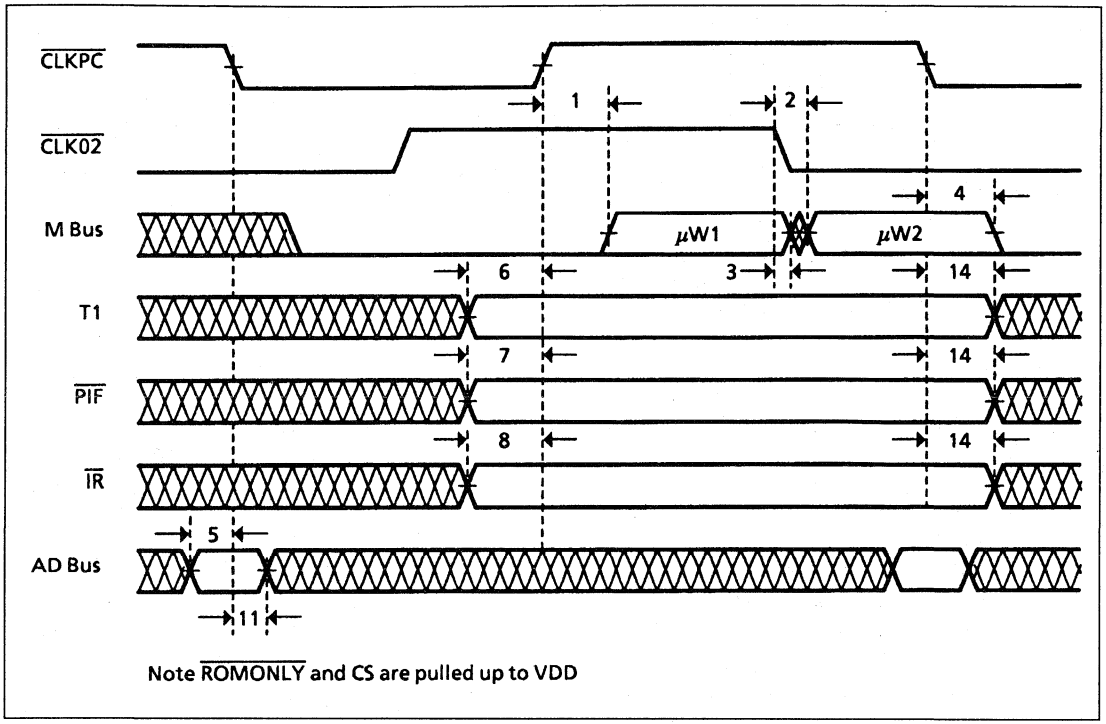


Figure 7: Basic Timing

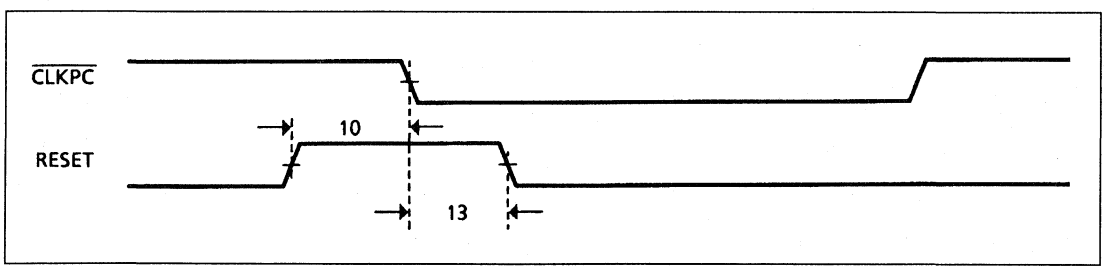


Figure 8: RESET Timing

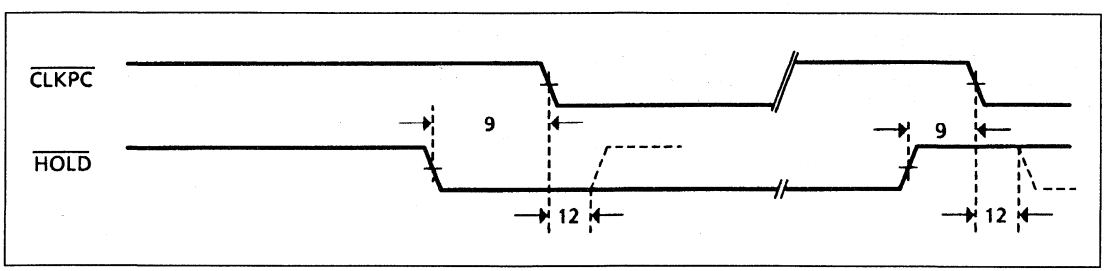


Figure 9: HOLD Timing

7.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 8: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8.0 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Total Dose Radiation Not Exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS}+1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2mA, V_{DD} = 5.5V	-	-	0.5	V
I_{IL}	Input Leakage Current (Note 3)	V_{DD} = 5.5V, V_{IN} = 0V or 5.5V	-	-	±10	µA
I_{OZ}	Output Leakage Current (Note 3)	V_{DD} = 5.5V, V_O = 0V or 5.5V	-	-	±50	µA
I_{IPU}	CS or ROMONLYN Input Pull-up Current (Note 4)	V_{DD} = 5.5V, CS or ROMONLYN = 0V	-	-	-300	µA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V, CLKPCN = CLK02N = 4MHz	-	25	35	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V, CLKPCN = CLK02N = 0MHz	-	5	10	mA

V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, Method 5005, Subgroup 1, 2, 3

Notes: 1. The following signals are CMOS compatible:
a) CMOS inputs: CS, ROMONLYN, T1, IRN, PIFN, CLK02N and CLKPCN
b) CMOS I/O signals: Microcode bus (M00-M19) and Microcode address bus (CC00-CC11)
2. The following signals are TTL compatible:
a) TTL inputs: Address/Data Bus (AD00-AD15), RESET and HOLDN
3. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C
4. CS and ROMONLYN inputs are provided for future microcode expansion and have internal pullup resistors. These signals should be high for normal operation.

Table 9: DC Electrical Characteristics

9.0 PACKAGING INFORMATION

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.508	0.014	-	0.020
c	0.229	-	0.36	0.009	-	0.014
D	-	-	82.04	-	-	3.230
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	22.86 Typ.	-	-	0.900 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	23.4	-	-	0.920
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG413

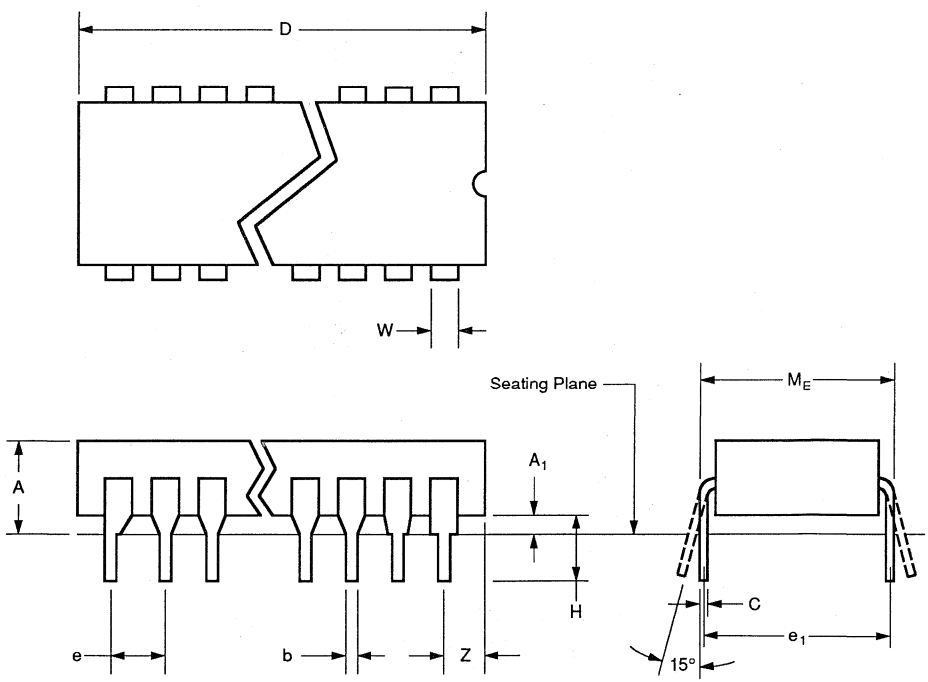


Figure 10a: 64-Pin Ceramic DIL - Package Style C

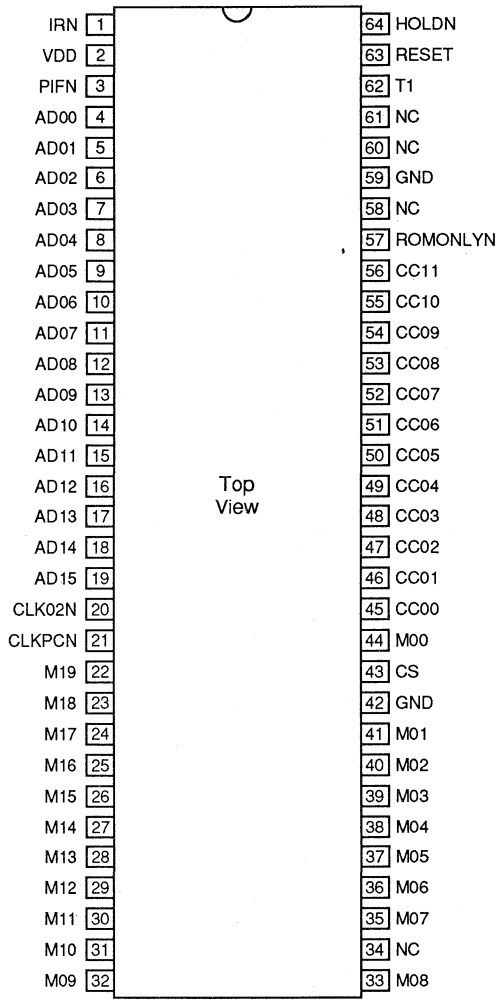


Figure 10b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.905	-	2.21	0.075	-	0.087
b1	-	0.51	-	-	0.020	-
D	18.08	-	18.62	0.712	-	0.733
E	18.08	-	18.62	0.712	-	0.733
e	-	1.02	-	-	0.040	-
Z	1.40	-	1.78	0.055	-	0.070

XG493

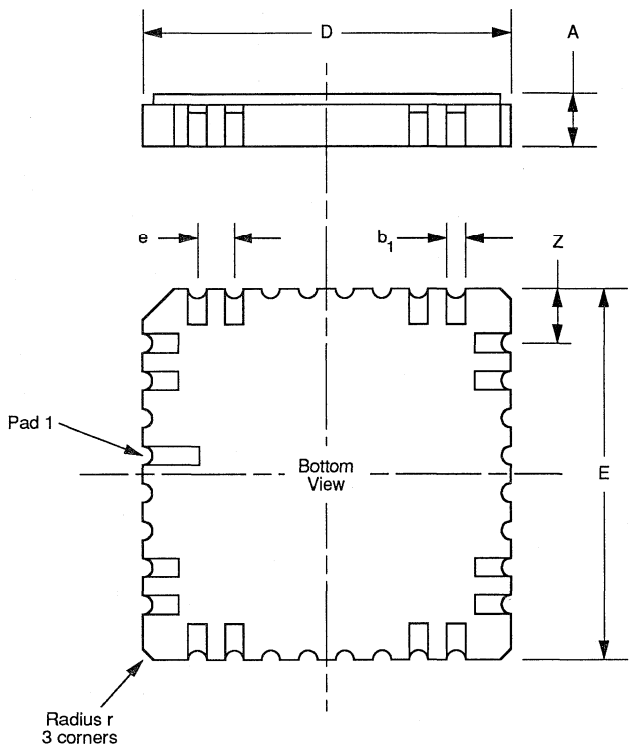


Figure 11a: 64-Pad Leadless Chip Carrier - Package Style L

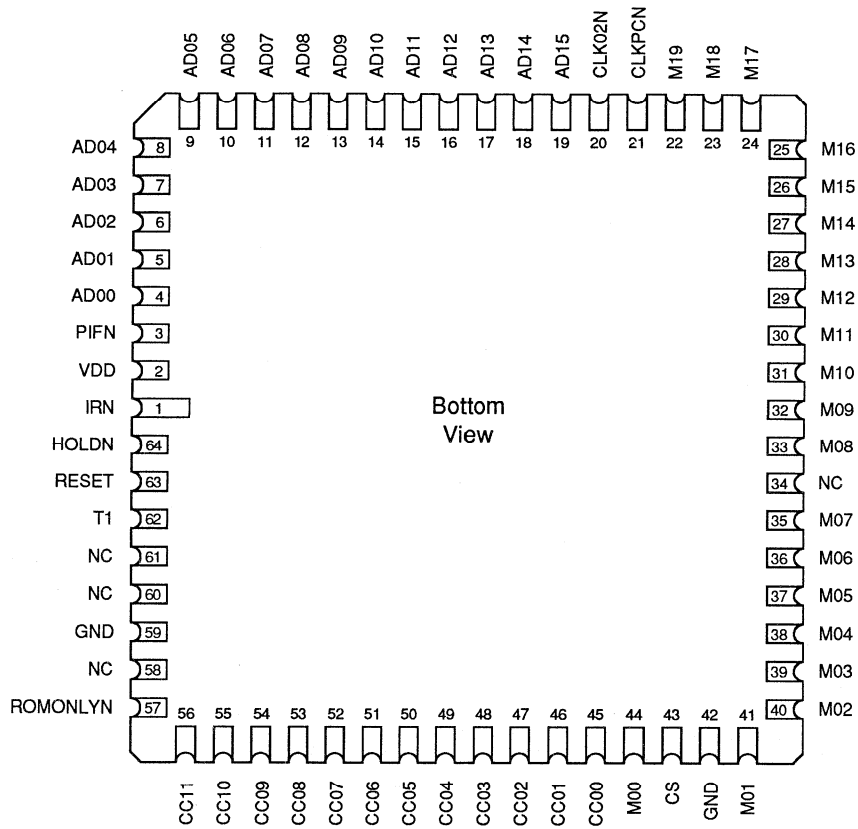


Figure 11b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

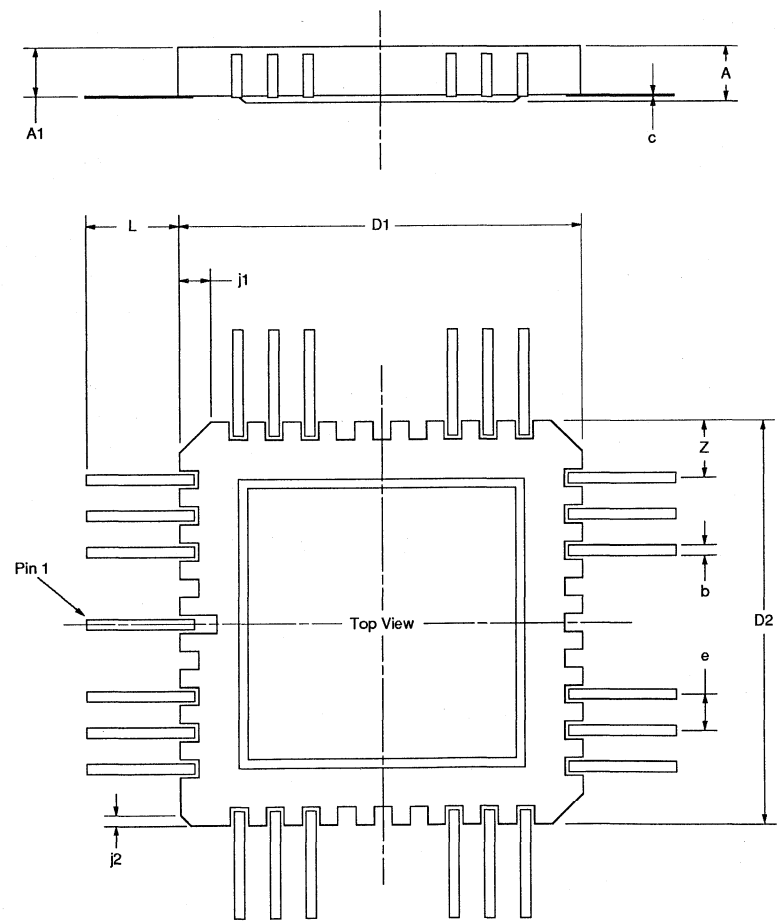


Figure 12a: 68-Lead Topbraze Flatpack - Package Style F

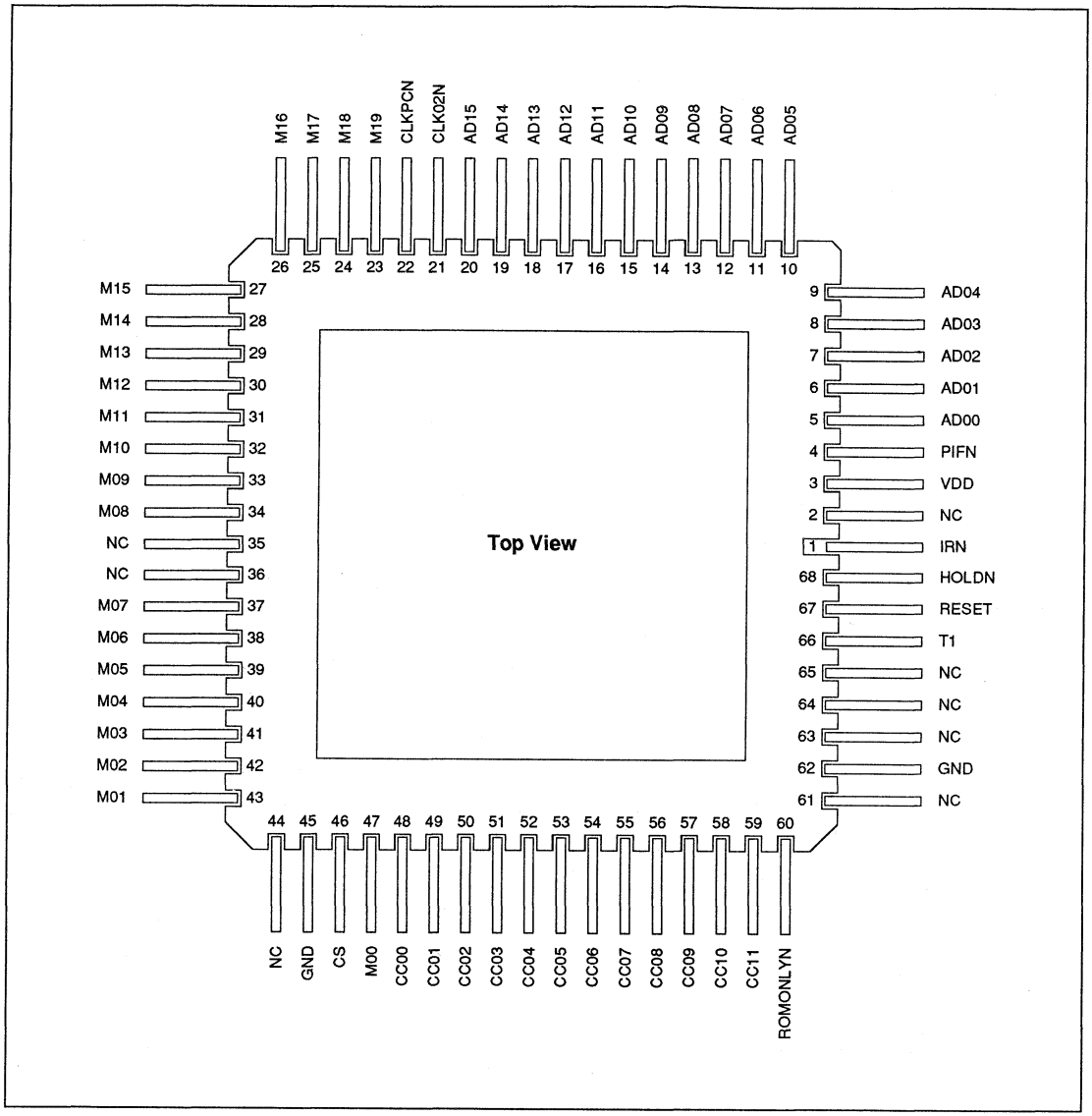


Figure 12b: Pin Assignments

10.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

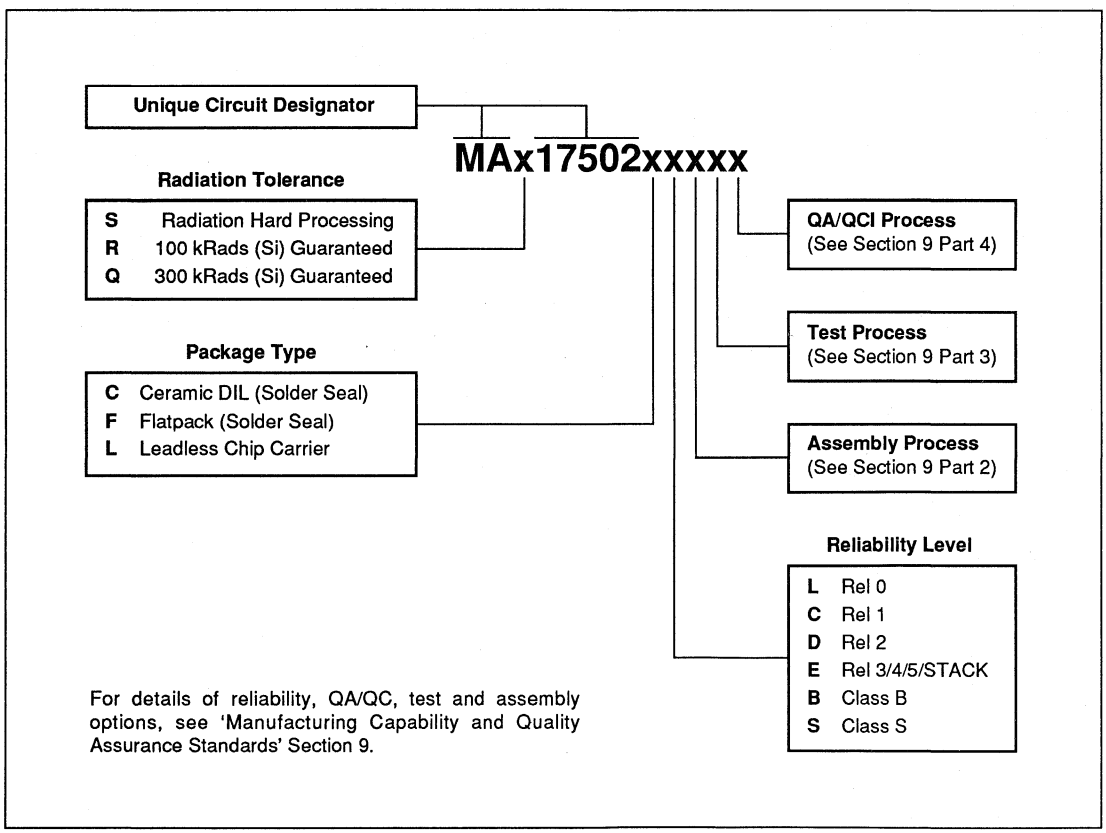
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 10: Radiation Hardness Parameters

11.0 ORDERING INFORMATION



MA17503

RADIATION HARD MIL-STD-1750A INTERRUPT UNIT

The MA17503 Interrupt Unit is a component of the MAS281 chip set. Other chips in the set include MA17501 Execution Unit and the MA17502 Control Unit. Also available is the peripheral MA31751 Memory Management/Block Protection Unit. The Interrupt Unit, in conjunction with these additional chips, implements the full MIL-STD-1750A Instruction Set Architecture.

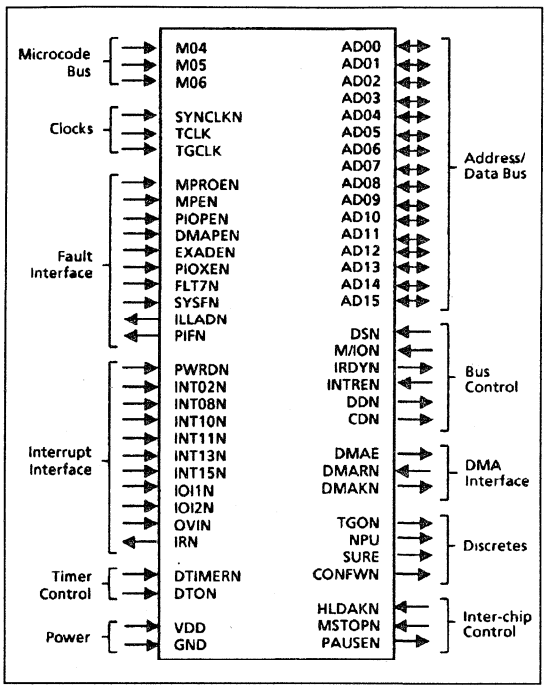
The MA17503 - consisting of the Pending Interrupt Register, Mask Register, Interrupt Priority Encoder, Fault Register, Timer A, Timer B, Trigger-Go Counter, Bus Fault Timer, and DMA interface - handles all interrupt fault, and DMA interfacing, in addition to providing all three hardware timers. The Interrupt Unit also implements 26 of the MIL-STD-1750A specified I/O commands. Table 1 provides brief signal definitions.

The MA17503 is offered in dual-in-line, flatpack or leadless chip carrier packaging. Screening and packaging options are described at the end of this document.

FEATURES

- Mil-Std-1750A Instruction Set Architecture
- Full Performance over Military Temperature Range (-55°C to +125°C)
- Radiation Hard CMOS/SOS Technology
- Interrupt Handler
  - 9 User Interrupt Inputs
  - Pending Interrupt Register
  - Interrupt Mask Register
  - Interrupt Priority Encoder
- Fault Handler
  - 8 User Faults Inputs
  - Fault Register
- Timers
  - Timer A
  - Timer B
- Trigger-Go
- DMA Interface
- Interface Discretes
  - Normal Power-Up
  - Start-Up ROM Enable
  - Configuration Word Enable
- Implements 26 MIL-STD-1750A Specified I/O Commands
- MAS281 Integrated Built-In Self Test
- TTL Compatible System Interface

BLOCK DIAGRAM



1.0 SYSTEM CONSIDERATIONS

The MA17503 Interrupt Unit (IU) is a component of the GPS MAS281 chip set. This chip set implements the full MIL-STD-1750A instruction set architecture. Other chips in the set include the MA17501 Execution Unit (EU) and MA17502 Control Unit (CU). Also available is the peripheral MA31751 Memory Management Unit/Block Protection Unit (MMU(BPU)). Figure 1 depicts the relationship between the chip set components.

The IU provides the interrupt and fault handling interfaces for the chip set. The IU also provides the DMA control interface logic, contains interval Timers A and B, the Trigger-Go Counter, the Bus Fault Timeout timer, and decodes all MIL-STD-1750A specified I/O commands in support of these functions. The EU provides the arithmetic and logical computation resources for the chip set. The EU and IU are each controlled by microcode from the CU. The MMU(BPU) may be configured to provide either 1M-word memory management (MMU) and/or 1K-word memory block write protection (BPU) functions.

As shown in Figure 1, the MAS281 is the minimum processor configuration consisting of an Execution Unit, a Control Unit, and an Interrupt Unit. This configuration is capable of accessing a 64K-word address space. Addition of a MMU configured MA31751 allows access to a 1M-word address space. Addition of a BPU configured MA31751 provides hardware support for 1K-word memory block write protection.

The IU, as with all components of the MAS281 chip set, is fabricated with CMOS/SOS process technology.

Detailed descriptions of the IUs companion chips are provided in separate data sheets. Additional discussions on chip set system considerations, interconnection details, and Digital Avionics Instruction Set (DAIS) mix benchmarking analysis are provided in separate application notes.

SIGNAL	I/O	DEFINITION
AD00 - AD15	I/O/Z	16-Bit Address/Data Bus
M04, M05, M06	I	3 Bits of the Mlcrocode Instruction Word
INTREN	I	Interrupt Unit Microcode Interface Enable
DMAKN	O	DMA Request Acknowledge
DMAE	O	DMA Interface Enable
DMARN	I	DMA Request
M/ION	I	Memory/Input-Output
DSN	I	Data Strobe
SYNCLKN	I	Synchronisation Clock
IRDYN	O	Interrupt Unit Ready
DDN	O	Data Transceiver Dlrection Control
CDN	O	Control Bus Transceiver Direction Control
SYSFN	I	System Fault
FLT7N	I	Fault 7 (Undefined Fault)
PIOXEN	I	Programmed I/O Transfer Error
EXADEN	I	External Address Error
DMAPEN	I	DMA Parity Error
PIOPEN	I	Programmed I/O Parity Lrror
MPEN	I	Memory Parity Error
MPROEN	I	Memory Protection Error
ILLADN	O	Illegal Address
PIFN	O	Instruction Abort
PWRDN	I	Power-Down Interrupt
INT02N	I	Level 2 Interrupt
INT08N	I	Level 8 Interrupt
INT10N	I	Level 10 Interru pt
INT11N	I	Level 11 Interrupt
IOI1N	I	I/O Register Interrupt 1
INT13N	I	Level 13 Interrupt
IOI2N	I	I/O Register Interrupt 2
INT15N	I	Level 15 Interrupt
OV1N	I	Fixed-Point Overflow Interrupt
IRN	O	Interrupt Request
TCLK	I	Clock for Tlmers A and B
TGCLK	I	Trigger Go Timer Clock
DTIMERN	I	Disable Timers
DTON	I	Disable Bus-Fault Timeout
TGON	O	Trigger-Go Timer Overflow
NPIJ	O	Normal Power-up Indicator
SURE	O	Start-up ROM Enable
CONFWN	O	Configuration Word Enable
HLDAKN	I	Hold Acknowledge
MSTOPN	I	Microcode Stop
PAUSE	O	Processor Pause
VDD	I	Power
GND	I	Ground

Table 1: Signal Definitions

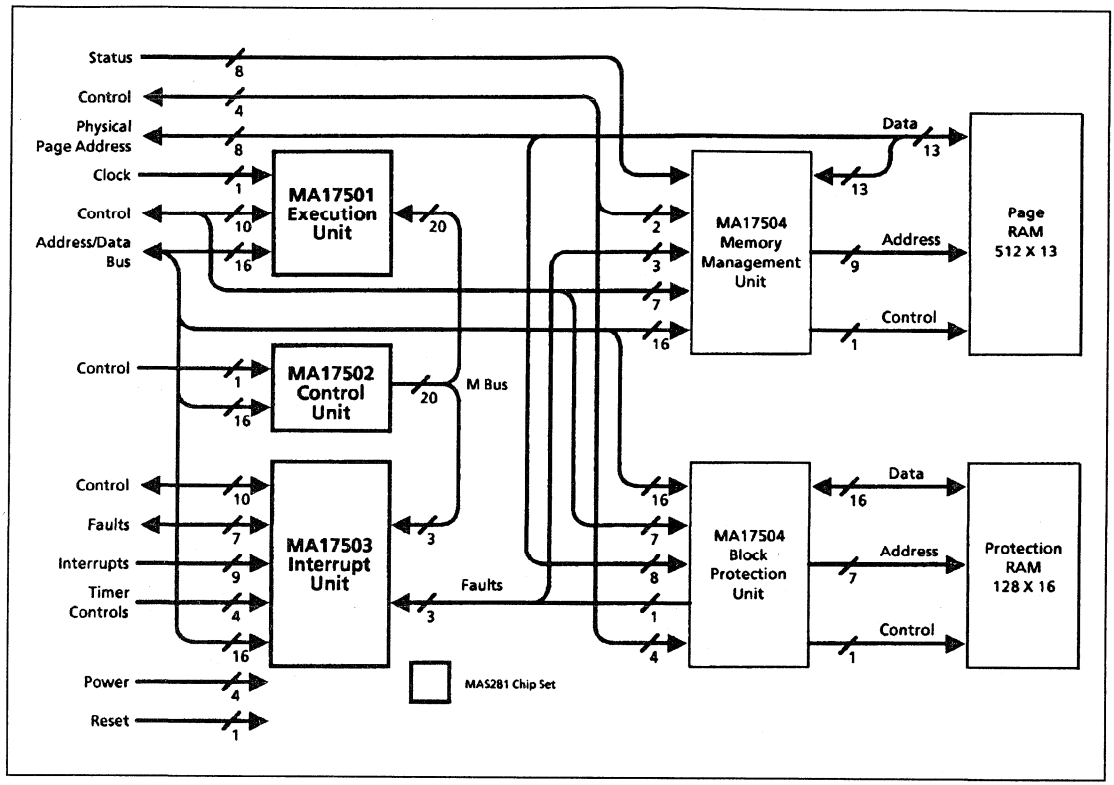


Figure 1

2.0 ARCHITECTURE

The Interrupt Unit consists of a Pending Interrupt Register, Mask Register, Interrupt Priority Encoder, Fault Register, two interval timers, two watchdog timers, DMA Control interface, and both microcode and internal I/O instruction decode logic. Details of these components are depicted in Figure 2 and are discussed below:

2.1 PENDING INTERRUPT REGISTER

The Pending Interrupt Register (PI) is the dedicated 16-bit register that latches all pending interrupt requests and stores them until serviced. The inputs to the PI are buffered by falling-edge detectors to prevent repeat latching of interrupt requests held low longer than required. The PI supports nine external interrupts inputs and seven chip set generated interrupts. The output of the PI is ANDed with the Mask Register to create the interrupt request (IRN) signal for the MA17502 Control Unit. A one in a PI bit position indicates an interrupt is pending and the interrupt level is equal to the bit position.

2.2 MASK REGISTER

The Mask Register (MK) is the dedicated 16-bit register containing the information that filters the PI output to the Priority Encoder and the IRN generation logic. A one in a MK bit position allows the interrupt request, of the same bit position in the PI, to enter the Priority Encoder and cause IRN to drop low. PI bits 1 - 4 and 6 - 15 are maskable.

2.3 INTERRUPT PRIORITY ENCODER

The Interrupt Priority Encoder accepts the enabled, mask filtered, output of the PI and generates a four bit code designating the level of the highest priority pending interrupt. Level zero (PI bit zero) has the highest priority and level 15 (PI bit 15) the lowest. The four bit priority code is placed on the AD Bus during the microcoded interrupt handling routine.

2.4 FAULT REGISTER

The Fault Register (FT) is the dedicated 16-bit register that latches the 15 specified (fault 12 is reserved) faults. The FT supports eight external Fault inputs and three chip-set generated Faults. The output of the FT is ORed together, buffered by a falling-edge detector, and input to the PI to generate the level one interrupt. FT bits 13 - 15 are used to indicate the results of the MAS281 BIT. Once the FT has latched a fault, it can only be cleared via internal I/O command (individual fault bits cannot be cleared).

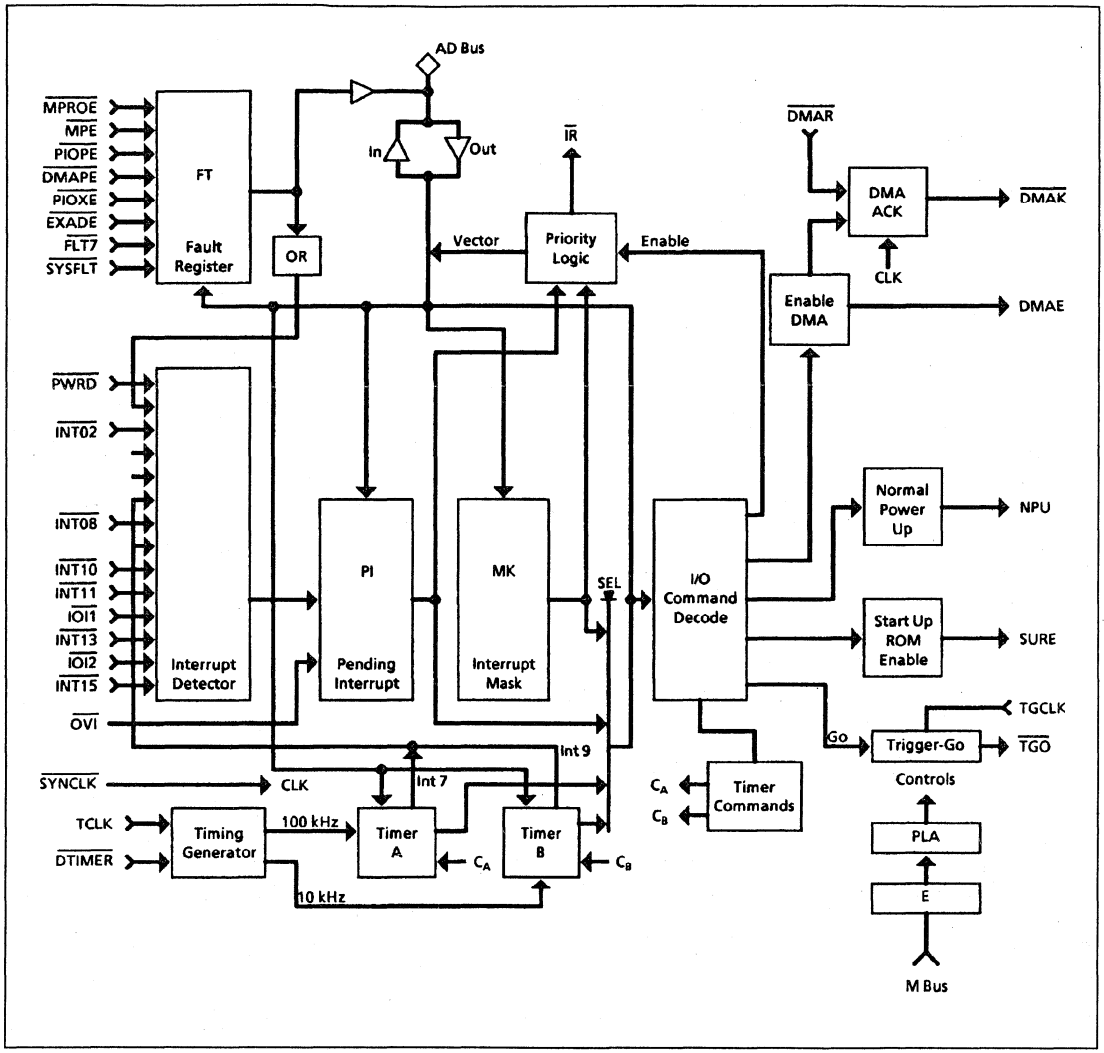


Figure 2: MA17503 Interrupt Unit Architecture

Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT. The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit. When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting fault bit(s). Therefore, a level 1 interrupt would be latched again if there were no anti-repeat logic to prevent a never ending loop of interrupts from occurring.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the RCFR internal I/O command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the internal I/O command RFR, but this command should be used carefully.

2.5 INTERVAL TIMERS

The Interrupt Unit contains both MIL-STD-1750A 16-bit interval timers, A and B. The TCLK input is synchronized with SYNCLKN and increments Timer A once a TCLK period. Timer B is incremented by the synchronized TCLK divided by 10. Timer A overflow sets PI bit 7 and Timer B overflow sets PI bit 9. The timers are controlled via the I/O command decode logic, or they can be disabled via the DTIMERN input.

2.6 WATCHDOG TIMERS

The Interrupt Unit contains two watchdog timers, Trigger-Go and Bus Fault. The Bus Fault timer assures timely completion of all AD Bus cycles by terminating bus cycles over two TCLK (maximum, minimum one TCLK period) periods in duration. This function is automatic, but can be disabled by DTON low. FT bit 5 or 8 is set for terminated I/O transfers or memory transfers, respectively, when the Bus Fault timer expires.

The Trigger-Go timer is an autonomous 16-bit ripple counter incremented by TGCLK. Upon power-up, the Trigger-Go timer begins to count. The GO I/O command resets the timer, thus preventing it from overflowing and causing TGON to drop low. The DTIMERN input prevents the Trigger-Go timer from incrementing.

2.7 DMA CONTROL INTERFACE

The DMA control interface logic is contained in the Interrupt Unit. The interface is composed of the three signals: DMAE, DMARN, and DMAKN. If the interface is enabled, an internal I/O command raises DMAE high to indicate the MAS281's readiness to accept DMA transfer requests (DMARN low). A subsequent low on DMARN causes the IU to respond with DMAKN low. DMAKN low halts the processor and places all AD Bus and bus control lines in the high-impedance state. Control is returned to the MAS281 when DMARN is pulled high again. DTIMERN is the user available way to disable the DMA interface.

2.8 INTERNAL I/O COMMAND DECODE LOGIC

The Interrupt Unit implements the 26 MIL-STD-1750A specified I/O command functions listed in Table 2. The IU also decodes an additional 386 commands that are implemented in the MMU(BPU) and the two Status Word XIO commands that are handled in microcode for AD Bus control. The IU continually monitors AD Bus traffic. When M/ION is low, the IU latches the information present on the AD Bus during the address portion of the bus cycle. This information is subsequently decoded and creates the appropriate control signals to perform the I/O command function.

2.9 MICROCODE DECODE LOGIC

The microcode decode logic can be split into command and control functions. Microcode instruction bits 4, 5 and 6 are decoded as commands for the FT, the interrupt interface, the DMA interface, and the discrete output signal, NPU. The microcode command interface is enabled when INTREN is pulled low and is disabled during DMA and the Hold state. Microcode bits 5 and 6 provide control of DDN during memory read and write cycles, and external I/O cycles.

Operation	Command Code (Hex)	Mnemonic
Output		
Set Fault Register	0401	SFR
Set Interrupt Mask	2000	SMK
Clear Interrupt Request	2001	CLIR
Enable Interrupts	2002	ENBL
Dlsable Interrupts	2003	DSBL
Reset Pending Interrupt	2004	RPI
Set Pending Interrupt Reglster	2005	SPI
Reset Normal Power Up Discrete	200A	RNS
Write Status Word	200E	WSW
Enable Start Up ROM	4004	ESUR
Disable Start up ROM	4005	DSUR
Direct Memory Access Enable	4006	DMAE
Direct Memory Access Disable	4007	DMAD
Timer A Start	4008	TAS
Timer A Halt	4009	TAH
Output Timer A	400A	OTA
Reset Tngger-Go	400B	GO
Timer B Start	400C	TBS
Timer B Halt	400D	TBH
Output Timer B	400E	OTB
Input		
Read Configuration Word	8400	RCW
Read Fault Register Wlthout Clear	8401	RFR
Read Interrupt Mask	A000	RMK
Read Pending Interrupt Reglster	A004	RPIR
Read Status Word	A00E	RSW
Read and Clear Fault Reylster	A00F	RCFR
Input Timer A	C00A	ITA
Input Tlmer B	C00E	ITB

3.0 INTERFACE SIGNALS

All signals comply with the voltage levels of Table 1. In addition, each of these functions is provided with Electrostatic Discharge (ESD) protection diodes. All unused inputs must be held to their inactive state via a connection to VDD or GND.

Throughout this data sheet, active low signals are denoted by either a bar over the signal name or by following the name with an "N" suffix (e.g., DMAKN). Referenced signals that are not found on the MA17503 are preceded by the originating chip's functional acronym in parentheses (e.g., (EU)OSC).

Following is a description of each pin function grouped according to functional interface. The function name is presented first, followed by its acronym, its type, and its description. Function type is either input, output, high impedance (Hi-z), or a combination thereof. Timing characteristics of each of the functions described is provided in Section 5.0.

3.1 POWER LNTERFACE

The power interface consists of one 5V VDD connection and one GND connection.

3.2 CLOCKS

The clock interface, discussed below, provides synchronization for Interrupt Unit operations and the clock inputs for the interval and watchdog timers.

3.2.1 Synchronisation Clock (SYNCLKN)

Input. The MA17501 Execution Unit (EU) generates the SYNCLKN signal for the Interrupt Unit. The Interrupt Unit uses this signal to synchronise system inputs (e.g., interrupts and faults) to the MAS281 machine cycle and to control all other internal functions.

3.2.2 Timer Clock (TCLK)

Input. TCLK is a 100 KHz, user provided clock signal that drives the interval timers A and B, and the Bus Fault timer. TCLK is synchronised to the MAS281 machine cycle, via SYNCLKN, before being sent to the interval timers. This allows the IU to implement the Internal I/O Commands associated with timer operation.

The synchronised version of TCLK drives interval timer A, clocking it once every 10 microseconds. The synchronised TCLK is divided by 10 to provide a 10 KHz clock for driving interval timer B, clocking it once every 100 microseconds.

The unsynchronised TCLK is used to increment the Bus Fault watchdog timer. When DSN drops low, the Bus Fault timer is enabled to count and expires after two TCLK high-to-low transitions.

3.2.3 Trigger-Go Clock (TGCLK)

Input. This user provided clock drives the autonomous on-chip system watchdog timer. The Trigger-Go timer is incremented by the high-to-low transition of TGCLK.

3.3 BUSES

Following is a discussion of the two communication buses connecting the Interrupt Unit to the rest of the three chip set. The AD Bus transfers 16-bit data and commands, while the M Bus communicates microcode control data.

3.3.1 Address/Data Bus (AD Bus)

Input/Output/Hi-z. These signals comprise the multiplexed address and data bus. During internal bus operations, the AD Bus accommodates the transfer of Internal I/O commands and data from the MA17501 Execution Unit to the Interrupt Unit. It also accommodates the transfer of data from the Interrupt Unit to the Execution Unit in response to internal I/O commands. AD00 is the most significant bit position and AD15 is the least significant bit position of both the 16-bit data and 16-bit command. A high on this bus corresponds to a logic 1 and a low corresponds to a logic 0.

Commands on the AD Bus are passed through transparent latches during the low state of input/output SYNCLKN cycles and are latched at the low-to-high transition of SYNCLKN. Data on the AD Bus, is either clocked into the IU by the high-to-low transition of SYNCLKN or placed there by the IU during the low portion of SYNCLKN.

3.3.2 Microcode Bus Bits 4, 5 and 6 (M04, 05 & 06)

Inputs. M04, M05, M06 are bits 4, 5 and 6 of the 20-bit Microcode Bus and are coded in the 40-bit microcode instruction as bits 4, 5 and 6. These bits are latched into the IU at the SYNCLKN high-to-low transition and are decoded for commanding the Fault Register, the DMA interface, the NPU discrete, and for providing the 4-bit priority encoded interrupt vector to the EU. IU microcode command cycles are extended to six (EU)OSC cycles by INTREN low. Microcode bits 5 and 6 provide control of DDN during memory and external I/O cycles. The microcode bus is not latched during DMA or the Hold state (DMAKN or HLDAKN low).

3.4 BUS CONTROL

The following is a discussion of the signals used to control the AD Bus and M Bus. They enable the respective busses at the proper time and control system access to the MAS281 System AD Bus.

3.4.1 Data Strobe (DSN)

Input. The Interrupt Unit receives DSN from the Execution Unit. The DSN high-to-low transition starts the Bus Fault watchdog timer and during successful bus data transfers, the low-to-high transition halts and resets the Bus Fault watchdog timer. DSN is also instrumental in controlling the DDN signal during MAS281 Read/Input bus cycles.

3.4.2 Memory/Input-Output (M/ION)

Input. The Interrupt Unit receives M/ION from the Execution Unit. M/ION low enables I/O command decoding logic M/ION also selects the FT bit to set in response to a low on MPROEN and EXADEN.

3.4.3 Interrupt Unit Ready (IRDYN)

Output. The Interrupt Unit uses the IRDYN signal to cause the Execution Unit clock generation state machine to inject one wait state into Internal I/O machine cycles, thus causing the minimum five (EU)OSC period machine cycle to be extended to a six (EU)OSC period 50% duty cycle machine cycle. Internal I/O machine cycles occur during execution of the IU implemented I/O commands listed in Table 2.

3.4.4 Interrupt Unit Microcode Enable (INTREN)

Input. The Execution Unit provides INTREN to the Interrupt Unit to enable the microcode command interface. When INTREN is low, microcode instruction bits 4, 5 and 6 (latched into the IU microcode register at the SYNCLKN high-to-low transition, if HLDAKN and DMAKN are high) are decoded by the IU as commands for the FT, NPU discrete, internal DMA interface, and interrupt vectoring. INTREN low causes the EU to extend the machine cycle to six (EU)OSC periods.

3.4.5 Data Transceiver Direction (DDN)

Output. DDN is provided to control the directionality of the AD/Data Bus transceivers. DDN is high during data transfers from the MAS281 to the user system and when it is necessary to keep the transceivers from driving the MAS281 System AD Bus. DDN is low during transfers from the user system to the MAS281.

Cycles during which DDN is high include: memory writes, outputs, IU implemented Internal I/O command execution (except Read Configuration Word (RCW)), and all MA17504 MMU(BPU) implemented I/O command execution.

Cycles during which DDN is low include: memory reads (data portion), inputs (data portion), the Configuration Word read (identified by CONFWN, low), and during DMA and Hold cycles (to allow access to the MMU(BPU).

3.4.6 Control Transceiver Direction (CDN)

Output. CDN is provided to control the directionality of the Control Bus (consists of DSN, (EU)AS, M/ION, RD/WN, and IN/OPN) transceivers. CDN is high during all MAS281 directed machine cycles. CDN drops low only when DMAKN or HLDAKN is low, indicating the MAS281 has placed the control bus signals in the high-impedance state. (It is necessary to use transceivers to buffer the control bus, if a shared MMU(BPU) architecture is used, to allow the sharing device access to the MMU(BPU) functions.)

3.5 INTERRUPT INTERFACE

The Interrupt Unit supports 16 levels of prioritised interrupts, nine of which are accessible to the user system. All user accessible interrupts are active low, are buffered with edge detectors to prevent repeat latching of the interrupt, and are latched into the Pending Interrupt register (PI) by the high-to-low transition of SYNCLKN.

The following interrupts do not have dedicated input pins on the MA17503. Level 1, Machine Error Interrupt, is driven by the ORed bits of the Fault register (FT). Levels 7 and 9 are driven by the overflow of Interval Timers A and B, respectively. The Internal I/O command, Set Pending Interrupt (SPI), is used to set interrupt levels 3, 5, and 6 (Floating-Point Overflow, Executive Call, and Floating-Point Underflow, respectively) via microcoded execution.

3.5.1 Power Down Interrupt (PWRDN)

Input. The PWRDN interrupt is the highest priority interrupt, level 0, and is latched into PI bit zero. It is nonmaskable and cannot be disabled.

3.5.2 User Interrupts (INT02N,08N,10N,11N,13N & 15N)

Inputs. Each of these user definable interrupts is latched into the PI register bits 2, 8, 10, 11, 13, or 15, respectively. Level 2 is the highest priority and level 15 is the lowest. These interrupts are maskable and can be disabled.

3.5.3 I/O Registered Interrupts (1011N & 1012N)

Inputs. Each of these interrupts is latched into the PI register bits 12 and 14, respectively. Level 12 is higher than level 14. These interrupts are maskable and can be disabled.

3.5.4 Fixed-Point Overflow (OVIN)

Input. This interrupt is driven by the MA17501 Execution Unit and is latched into the PI register bit 4. The OVIN interrupt is maskable and can be disabled.

3.5.5 Interrupt Request (IRN)

Output. This signal is the logical inclusive OR of the PI bits and is used to signal the MA17502 Control Unit that an interrupt request is pending.

3.6 FAULT INTERFACE

The Interrupt Unit supports 16 registered error condition flags. Eleven of the faults are directly accessible through dedicated input pins. A low on any of these fault inputs is latched into the Fault register (FT) by the high-to-low transition of SYNCLKN. Once a fault is latched, it can only be cleared by clearing the entire FT via Internal I/O command. The latching of any fault causes the level 1 interrupt to be set. Once set and subsequently cleared by the microcoded interrupt service routine, PI bit one cannot be set again until the FT is cleared via internal I/O command. Any unused fault inputs must be pulled-up to VDD.

3.6.1 Memory Protection Error (MPROEN)

Input. A low on this input is used to inform the MAS281 that an access fault, execute or write protection violation has been detected. When the MA31751 MMU(BPU) is used with the MAS281, the MPROEN fault input is provided by the MMU(BPU). FT bit 0 is set if a MAS281 directed memory cycle caused the error and bit 1 is set if a DMA device directed memory cycle caused the error.

Setting FT bit 0 causes PIFN to drop low. This aborts the MIL-STD-1750A instruction that was executing when the error occurred and branches execution to the machine error, level 1 interrupt service routine, if the interrupt is not masked. If the interrupt is masked, execution continues with the next instruction.

FT bit 0 is not latched during DMA or the Hold state (DMAKN or HLDAKN low).

3.6.2 Memory Parity Error (MPEN)

Input. A low on this input indicates a parity error has been detected during a memory transfer. This fault is latched into FT bit 2.

3.6.3 Programmed I/O Parity Error (PIOPEN)

Input. A low on this input indicates a parity error has been detected during an external I/O transfer. This fault is latched into FT bit 3.

3.6.4 DMA Parity Error (DMAPEN)

Input. A low on this input indicates a parity error has been detected during a DMA data transfer. This fault is latched into FT bit 4.

3.6.5 External Address Error (EXADEN)

Input. A low on this input indicates execution of an unimplemented or reserved I/O command has been attempted (M/ION low) and sets FT bit 5, or an attempt has been made to access an unimplemented memory address (M/ION high) and sets FT bit 8.

Provision for detection of these conditions has been made on the MA17503 in the form of a Bus Fault watchdog timer. If during an I/O or memory access cycle the system machine cycle completion circuitry or (EU)RDYN generation logic fails to provide the (EU)RDYN signal within the required amount of time, the Bus Fault watchdog timer will terminate the cycle by forcing IRDYN low and set the appropriate FT bit (FT5 if I/O, FT8 if memory). The minimum Bus Fault watchdog timeout period is one TCLK period, the maximum is two TCLK periods.

Setting FT bits 5 or 8 causes PIFN to drop low. This aborts the MIL-5TD-1750A instruction during which the error occurred and branches execution to the machine error, level 1, interrupt service routine, if the interrupt is not masked. If the interrupt is masked, execution continues with the next instruction.

FT bit 5 and 8 are not latched during DMA or the Hold state (DMAKN or HLDAKN low).

3.6.6 Programmed I/O Transmission Error (PIOXEN)

Input. A low on this input indicates a user defined error has occurred during an I/O transfer. This fault is latched into FT bit 6.

3.6.7 Fault #7 (FLT7N)

Input. This is a user definable (spare) fault input. A low on this input sets FT bit 7.

3.6.8 System Fault (SYSFN)

Input. A low on this input indicates a system Built-In Test error has occurred. This fault is latched into FT bits 13 and 15.

3.6.9 Illegal Address (ILLADN)

FT bits 5 and 8 are set by a low on the EXADEN input or by the Bus Fault watchdog timer overflow. FT bits 5 and 8 are not latched, and ILLADN is held high during DMA or the Hold state (DMAKN or HLDAKN low).

3.6.10 Instruction Abort (PIFN)

Output. A low on this output effects a MIL-STD-1750A instruction abort. When a SYNCLKN high-to-low transition latches FT bit 0, 5, or 8, the following SYNCLKN high-to-low transition causes PIFN to drop low and remain low for one SYNCLKN period (except during DMA and the Hold state, i.e., DMAKN or HLDAKN low).

PIFN directs the MA17502 Control Unit to branch microcode execution to the interrupt vectoring routine for level 1 interrupt servicing. If the level 1 interrupt is masked, execution will resume with the next MIL-STD1750A instruction.

PIFN causes the MA17501 Execution Unit to hold DSN and (EU)AS in their inactive state during the transition from error indication to the beginning of the interrupt servicing routine.

3.7 DMA INTERFACE

The DMA Interface consists of the necessary handshake signals required to effect transfer of control from the MAS281 to a DMA controller and back again.

3.7.1 DMA Transfer Enable (DMAE)

Output. When this output is raised high via execution of the Internal I/O command DMAE, direct memory access requests will be acknowledged by the MAS281. If DMAE is low, direct memory access requests will not be acknowledged by the MAS281.

3.7.2 DMA Transfer Request (DMARN)

Input. A DMA controller pulls this input low to request control of the AD Bus and bus control signals for DMA transfers. DMARN is held low by the DMA controller for the duration of the DMA transfer, and the low-to-high transition indicates the DMA controller is finished using the AD Bus.

3.7.3 DMA Transfer Request Acknowledge (DMAKN)

Output. The Interrupt Unit responds to a low on DMARN, if DMAE is high, by dropping DMAKN low at the SYNCLKN high-to-low transition.

3.8 INTER-CHIP CONTROL

The Inter-Chip Control signals are used to halt the processor (the three-chip set) during the DMA and HOLD cycles and during microcode testing.

3.8.1 Processor Pause (PAUSEN)

Output. This output is low during DMA operations (DMAKN low). PAUSEN is used by the Interrupt Unit to reset and disable the Bus Fault Timeout circuitry. PAUSEN is also used by the MA17501 Execution Unit clock generation circuitry to produce an internal disable signal. This internal disable signal holds CLKPCN and SYSCLK1N low and CLK02N high, which halts processing, and places the DSN, AS, IN/OPN, RD/WN, and M/ION output buffers, and the AD bus I/O buffers in the high impedance state, and drop DDN and CDN low to allow DMA controller access to the MMU(BPU) in shared MMU(BPU) systems.

3.8.2 Hold Acknowledge (HLDAKN)

Input. HLDAKN resets and disables the Bus Fault Timeout circuitry, causes DDN and CDN to be brought low, and prevents latching of microcode commands and decoding. The Execution Unit responds to a Hold state request (execution of BPT, or a low on HOLDN) by pulling HLDAKN low.

3.8.3 Microcode Stop (MSTOPN)

Input. MSTOPN allows microcode to be single-stepped during testing by GEC Plessey Semiconductors and should be pulled up to VDD in customer applications.

3.9 TIMER CONTROL

These Timer Control inputs allow external control of Timers A and B, the Trigger-Go Counter, and the Bus Fault Timeout circuitry.

3.9 1 Disable Timers (DTIMERN)

Input. A low to this input disables Timers A and B and the Trigger-Go counter, and also disables DMA access by forcing DMAE low and DMAKN high. Raising DTIMERN high causes Timers A and B and the Trigger-Go counter to resume counting where they were stopped, and also allows normal DMA operations.

3.9.2 Disable Bus-Fault Timeout (DTON)

Input. A low to this input will reset and disable the Busfault timeout circuitry.

3.10 DISCRETES

Four discrete outputs are provided for system use, all of which are enabled or disabled or both via internal I/O commands.

3.10.1 Trigger-Go Timer Overflow (TGON)

Output. This output drops low whenever the Trigger-Go counter overflows (rolls over to 0000). It returns high when the Trigger-Go counter is reset by software using the GO internal I/O command.

3.10.2 Normal Power-Up Indicator (NPU)

Output. This output is brought low via internal I/O command during module initialization as the first step of BIT. If BIT is completed successfully, NPU is raised high via microcode, and remains high until reset by software via the RNS internal I/O command.

START-UP ROM ENABLE (SURE)

Output. This output is used to enable an externally implemented Start-Up ROM. SURE is brought high via the execution of the ESUR internal I/O command (done by microcode during initialization or by software), and remains high until it is reset by software by using the DSUR internal I/O command. While SURE is high, all memory reads shall access main memory. This feature is utilized via the MOV instruction to effect a non-volatile memory program transfer to faster program execution RAM.

CONFIGURATION WORD ENABLE (CONFWN)

Output. This output is brought low during the data portion of an RCW (Read Configuration Word) internal I/O operation. It is used as an output enable strobe for the externally implemented Configuration Register. Because RCW is an internal I/O command, the read cycle is a fixed six (EU)OSC cycles and is terminated by IRDYN low. RDYN must not be asserted during execution of this command.

4.0 OPERATING MODES

The following discussions detail the MAS281 chip set operating modes from the perspective of the Interrupt Unit. The MAS281 operating modes involving the MA17503 are: (1) initialization, (2) instruction execution, (3) interrupt servicing, (4) fault servicing, (5) DMA support, (6) Hold support, and (7) timer operations.

4.1 INITIALISATION

A microcoded initialisation sequence is executed by the chip set in response to a hardware reset. This routine, as applicable to the Interrupt Unit, disables and masks interrupts, zeroes the Fault register, performs the MAS281 Integrated Built-In Test (BIT), raises the Start-Up ROM enable discrete (SURE), clears and starts timers A and B, resets the Trigger-Go counter, and disables DMA access. The resulting initialised state of the MA17503 is listed in Table 3.

The microcoded BIT exercises all legal microinstruction bit combinations and tests all internally accessible structures of the MAS281 chip set. For the Interrupt Unit this includes the MK, PI, and FT registers, Interrupt Enable/Disable, and Timers A and B. Table 4 details the tests performed by each of the five BIT routines.

If any part of BIT fails, an error code identifying the failed subroutine is loaded into FT bits 13-15, BIT is aborted with NPU left in the low state, initialization is completed, and instruction execution begins at address zero. The coding of the BIT results is shown in Table 4.

NOTE: To complete initialization and pass BIT, interrupt and fault inputs must be high for the duration of the initialization routine. In addition, timers A and B must be clocked for BIT success.

Item	Status
Fault (FT)	Zeroed
Pending Interrupt (PI)	Zeroed
Mask (MK)	Zeroed
Interrupts	Disabled
DMA Access	Disabled
Timer A	Reset and Started
Timer B	Reset and Started
Trigger-Go Timer	Reset and Started

Table 3: Interrupt Initialisation State

BIT	Test Coverage	BIT Fail Codes (FT13, 14, 15)	Cycles
1	Microcode Sequencer IB Register Control Barrel Shifter Byte Operations and Flags	100	221
2	Temporary Registers (T0 - T7) Macrocode Flags Multiply Divide	101	166
3	Interrupt Unit - MK, PI, FT Enable/Disable Interrupts	111	214
4	Status Word Control User Flags General Registers (R0 - R15)	110	154
5	Timer A Timer B	111	763
-	BIT Pass/Fail Overhead	-	26

Note: BIT pass is indicated by all zeros in FT bits 13, 14, and 15

Table 4: MAS281 BIT Summary

4.2 INSTRUCTION EXECUTION

The MAS281 chip set will begin instruction execution upon the completion of initialization. The instruction execution operations that involve the Interrupt Unit are: (1) internal CPU cycles, (2) memory transfers, and (3) input/output transfers. Instruction execution can be interrupted at the end of any individual machine cycle by a DMA request (DMARN low with DMAE high) or at the conclusion of any given instruction by an Interrupt or Hold state request.

4.2.1 Internal CPU Cycles

Microcode controlled IU functions are classified as internal CPU cycles. The IU interprets the three microcode bits, 4, 5, and 6, as a three bit instruction used for control of the FT, internal DMA interface, NPU discrete, and the interrupt priority vector code. The command is latched into the IU at the SYNCLKN high-to-low transition and decoded into control signals if INTREN is low. During these machine cycles, SYNCLKN is six (EU)OSC periods long. During internal CPU cycles, DSN and M/ION are held high by the Execution Unit, causing the IU to hold DDN high. Microcode bits 4, 5, and 6 are not latched or decoded during DMA or the Hold state (DMAKN or HLDAKN low).

4.2.2 Memory Transfers

The IU takes a passive role during memory transfers, i.e., it only controls the DDN signal. Microcode bits 4, 5, and 6 are latched by the SYNCLKN high-to-low transition then bits 5 and 6 are decoded to control the DDN control signal in concert with DSN. If bits 5 and 6 are high (indicating a write), DSN is kept from affecting DDN, which remains high for the entire cycle. If either bit 5 or 6 is low, DSN is allowed to control DDN, which becomes a delayed version of DSN.

4.2.3 Input/Output Transfers

The IU monitors all AD Bus traffic and controls the DDN output as specified. During cycles where M/ION is low, the IU decodes the address/command portion (SYNCLKN high) of the machine cycle. If one of the commands listed in Table 2 is encountered, the specific action takes place at the following SYNCLKN high-to-low transition; the exceptions being "GO" and "RCW". "GO" resets the Trigger-Go Timer at the SYNCLKN low-to-high transition and "RCW" drops CONFWN low during DSN low.

The read and write status word commands ("RSW", "WSW") cause IRDYN to drop low to complete the EU/MMU(BPU) machine cycle. IU decoded I/O command cycles are six (EU)OSC periods long (except for "RCW", there are five (EU)OSC periods).

4.3 INTERRUPT SERVICING

Nine user interrupt inputs and one dedicated input (OVIN) are provided for programmed response to asynchronous system events. A low on any of these inputs will be detected at the high-to-low transition of SYNCLKN and latched into the PI register on the following SYNCLKN high-to-low transition (with the exception of INT02N which is latched into PI when INT02N is first detected). This always occurs whether interrupts are enabled or disabled, or whether specific interrupts are masked or unmasked. (Because INT02N is captured asynchronously, it is possible under rare conditions for the PI bit 2 to remain set after INT02N has been serviced, causing double servicing of the one interrupt. To prevent this, bit 2 of the PI should be cleared at the end of the user service routine).

Each of the nine user interrupt inputs is buffered by a falling-edge detector to prevent repeat latching of requests held low longer than the first SYNCLKN high-to-low transition. An interrupt request input must go back to the high state before request on that input can be detected.

Command	M04, M05, M06
Load Fault Register From AD Bus	001
Read Interrupt Priority Vector Onto AD Bus	010
Raise Normal Power-up Discrete	011
Disable I/O Control of DMA Interface	100
Enable I/O Control of DMA Interface	101

Table 5: Interrupt Unit Microcode Commands

The output of the PI register is continually ANDed with the output of the MK register (level 0 interrupt is not maskable). If interrupts are enabled, and an unmasked interrupt is pending, the Interrupt Request (IRN) output to the Control Unit is asserted. This occurs when one or more interrupts are latched and unmasked. The unmasked pending interrupts are output to the priority encoder where the highest priority pending interrupt is encoded as a 4-bit vector.

After the currently executing MIL-STD-1750A instruction is completed, the Control Unit checks the state of the IRN input. If IRN is asserted, a branch is made to the microcode interrupt service routine. During this routine, the priority encoder's 4-bit vector is read into the Execution Unit, where the vector is used to calculate the appropriate interrupt linkage and service pointers (Table 6). When the EU reads the interrupt priority vector from the IU, the interrupt being serviced is cleared from the PI. If no other interrupts are pending, this also causes the IRN signal to be deactivated.

4.4 FAULT SERVICING

Eight external fault inputs are provided to the interrupt unit. A low on any of these inputs is latched into the FT register at the high-to-low transition of SYNCLKN. The capture of one or more of these faults immediately sets pending interrupt level 1 (machine error) of the PI.

Anti-repeat logic between the FT and PI prevents latching more than a single interrupt into the PI before the user interrupt service routine has cleared the FT. The microcoded interrupt service routine reads the interrupt priority vector from the Interrupt Unit and clears the serviced interrupt from the PI. At this point the PI is ready to latch another interrupt into this bit.

When this microcoded service routine acts on a level 1 interrupt, it clears the PI bit 1, but the FT maintains the interrupting fault bit(s). Therefore, a level 1 interrupt would be latched again if there was no anti-repeat logic to prevent a never ending loop of interrupts from occurring.

Interrupts are serviced at the end of the currently executing instruction if not masked and if interrupts are enabled. System software servicing level 1 interrupts must clear the FT via the RCFR internal I/O command at some point in the routine to allow subsequent faults to latch a level 1 interrupt request. A non-destructive read of the FT is provided by the internal I/O command RFR, but this command should be used carefully.

Faults caused by a low on EXADEN, MPROEN, or Bus Fault Timer expiration (FT 0, 5, 8) require that the currently executing MIL-STD-1750A instruction be aborted. In order to accomplish this, the latching of faults 0, 5, or 8 causes the Interrupt Unit to assert the instruction abort (PIFN) output to both the Execution Unit and the Control Unit Faults 0, 5, and 8 are not latched during DMA cycles or the Hold state (CDN low).

Interrupt Number	Function	Priority(1) Level	Maskable	Disability	Linkage Pointer	Service Pointer
0	Power Down	0	No	No	20	21
1	Machine Error	1	Yes	No	22	23
2	User 0	2	Yes	Yes	24	25
3	Floating Point Overflow	3	Yes	Yes	26	27
4	Fixed Point Overflow	4	Yes	Yes	28	29
5	Executive Call	5	No	No	2A	2B
6	Floating Point Underflow	6	Yes	Yes	2C	2D
7	Timer A	7	Yes	Yes	2E	2F
8	User 1	8	Yes	Yes	30	31
9	Timer B	9	Yes	Yes	32	33
10	User 2	10	Yes	Yes	34	35
11	User 3	11	Yes	Yes	36	37
12	I/O 1	12	Yes	Yes	38	39
13	User 4	13	Yes	Yes	3A	3B
14	I/O 2	14	Yes	Yes	3C	3D
15	User 5	15	Yes	Yes	3E	3F

Note: (1) Level 0 has highest priority, level 15 lowest.

Table 6: Interrupt Vector Assignments

4.5 DMA SUPPORT

DMA data transfers are performed over the system AD bus under the control of the IU DMA interface logic. The user signals that DMA requests will be honored by setting the DMAE output high via the DMAE internal I/O command. The DMA controller may request use of the AD bus by pulling DMARN low, but, unless DMAE is high, all such requests will be ignored. DMARN is acknowledged by raising DMAKN low. This occurs at the first SYNCLKN high-to-low transition after DMARN is pulled low.

When a DMA request is acknowledged (DMAKN low), DDN is dropped low to direct the system data bus transceivers to drive the local AD bus, and CDN is dropped low to disable the control signal buffers. (It is necessary to use transceivers to buffer the control bus if a shared MMU(BPU) architecture is used, to allow the sharing device access to the MMU(BPU) functions).

When the DMA controller relinquishes control of the AD bus (by raising DMARN high), DMA operations are ended by raising DMAKN high at the next SYNCLKN high-to-low transition, and DDN and CDN then resume normal operation.

4.6 HOLD SUPPORT

The Hold interface is handled by the Execution Unit, but the Hold acknowledge (HLDAKN) line is monitored by the Interrupt Unit. When HLDAKN is active, the Interrupt Unit lowers DDN and CDN, resets and disables the Bus-Fault decoding (bits 4-6). When the Hold state is terminated, DDN and CDN resume normal operation.

4.7 TIMER OPERATIONS

Interval Timers A and B, the Trigger-Go Counter and the Bus-Fault timer are all implemented in the Interrupt Unit.

4.7.1 Timers A and B

Timer A is clocked by the TCLK input (which is internally synchronised to SYNCLKN), whereas Timer B is clocked by an internally generated TCLK/10 (also internally synchronized to SYNCLKN). TCLK is required to be a 100KHz pulse train by MIL-STD-1750A. If they are allowed to overflow. Timers A and B will set level 7 and level 9 interrupt requests, respectively. Each timer can be read, loaded, started, and stopped via internal I/O commands.

External control of Timers A and B can be accomplished by asserting the DTIMERN input. When DTIMERN is low, both timers will halt and all internally decoded internal I/O commands which would change their state are disabled (asserting DTIMERN low also disables DMA accesses by driving DMAE low and DMAKN high). Raising DTIMERN high allows normal operations to resume where they left off.

4.7.2 Trigger-Go Counter

The Trigger-Go Counter is clocked by the TGCLK input. DTIMERN low disables and enables counter operations in the same way as Timers A and B. When the Trigger-Go counter overflows, the output discrete TGON drops low and remains low until the counter is reset via the "GO" internal I/Ocommand.

4.7.3 Bus-Fault Timer

This on-chip watchdog timer is provided to monitor all bus operations to ensure timely completion. This hardware timeout circuit is enabled at the start of each memory and I/O transfer (DSN high-to-low transition), and is reset on the following SYNCLKN high-to-low transition (an external ready (RDYN) must have been received by the Execution Unit for this to occur).

If this circuit is not reset within a minimum of one TCLK period or a maximum of two TCLK periods, either bit 3 (if a memory transaction) or bit 5 (if an I/O transaction) of the FT register is set. This causes the current MIL-STD-1750A instruction to be aborted as discussed above. This feature can be disabled externally by pulling DTON low and is not available during DMA or the Hold state (DMAKN or HLDAKN low).

5.0 TIMING CHARACTERISTICS

This section provides the detailed timing specifications for the MA17503 Interrupt Unit. Figure 3 depicts the test loads used to obtain the timing data. Figures 4 through 15 depict the timing waveforms associated with various MA17503 signals. Table 7 lists values for the parameters specified in the timing waveforms. All timing values provided in Table 7 are valid over the full military temperature range (-55°C to +125°C), assume the recommended operating conditions, and are measured from 50% point to 50% point (50% of VDD supply voltage, unless otherwise specified). Crosshatching in Figures 4 through 15 indicates either a ,"don't care" state or indeterminate state.

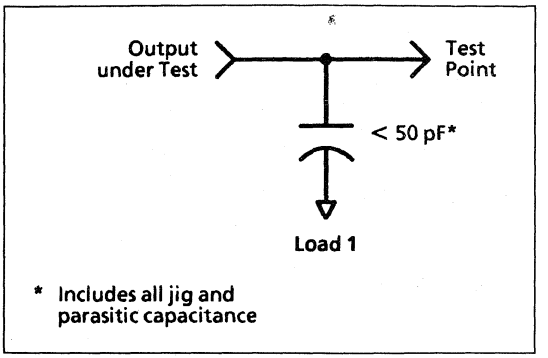


Figure 3: Test Load

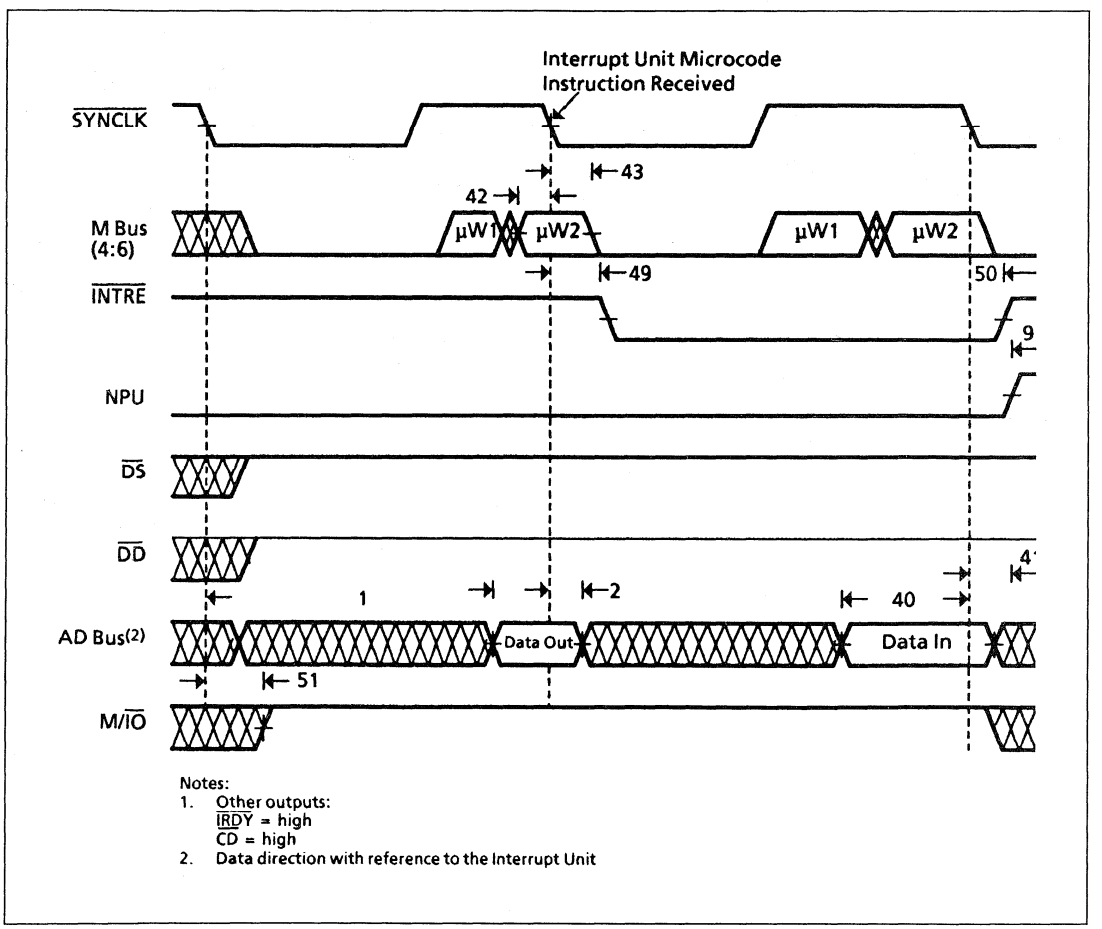
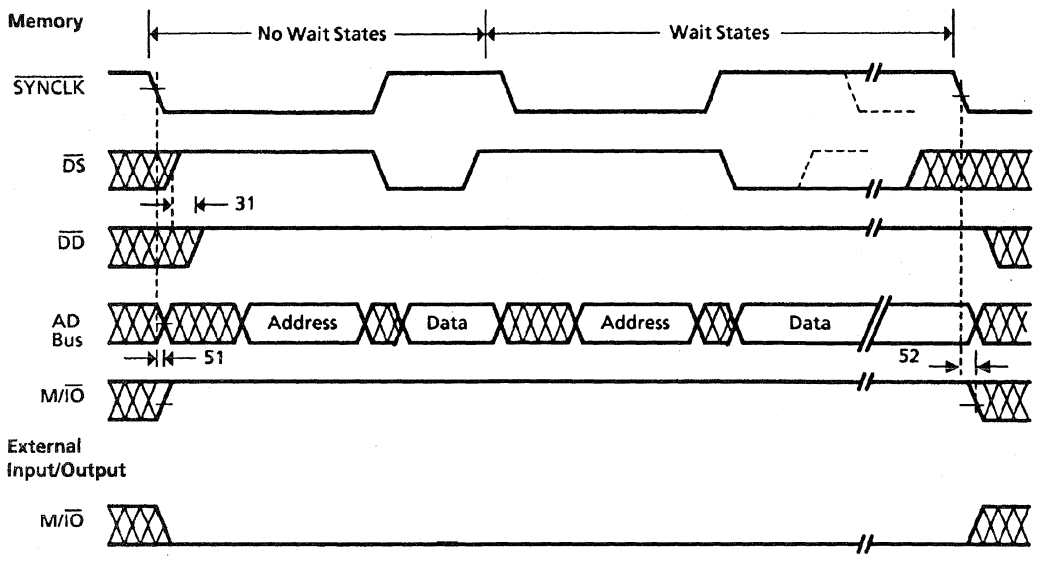
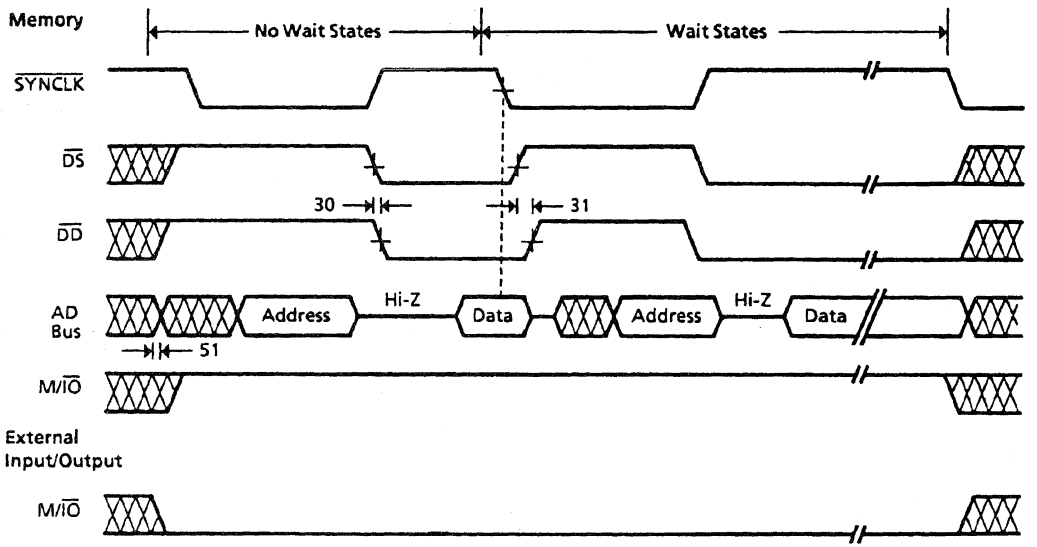


Figure 4: Microcode Operations



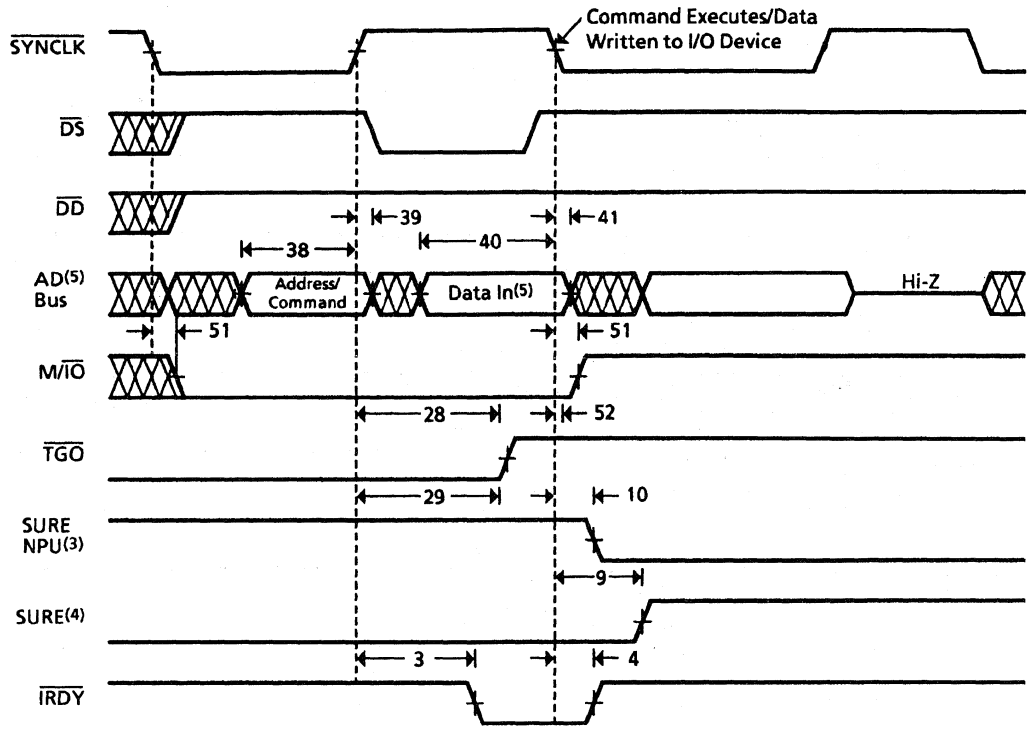
Notes:
1. Dashed timing lines indicate non-wait cycle timing.
2. Other output states:
   CD = high
   IRDY = high
   DMAK = high
   PAUSE = high
3. Other required input states:
   HLDAK = high
   DMAR = high

Figure 5: Write Transfer Timing



Notes:
1. Dashed timing lines indicate non-wait cycle timing.
2. Other output states:
   CD = high
   IRDY = high
   DMAK = high
   PAUSE = high
3. Other required input states:
   HLDAK = high
   DMAR = high

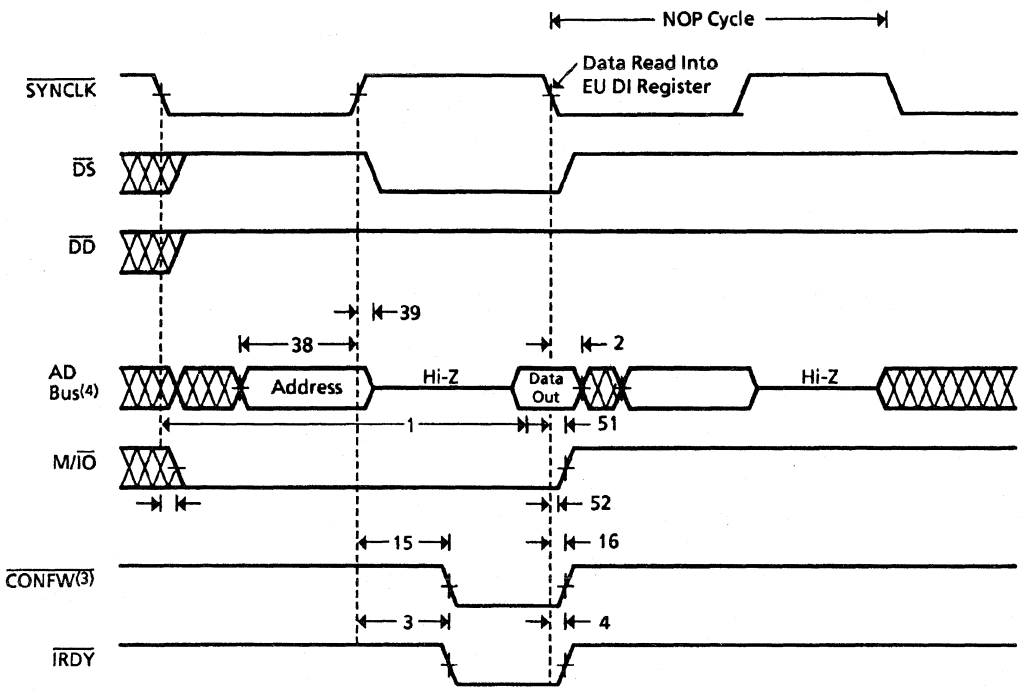
Figure 6: Read Transfer Timing



Notes:

1. Other output states:
   - $\overline{CD}$ = high
   - $\overline{PAUSE}$ = high
   - $\overline{DMAK}$ = high
2. Other required input states:
   - $\overline{HLDAK}$ = high
   - $\overline{DMAR}$ = high
   - $\overline{RDY}$ = high
3. XIO command, RNS.
4. XIO command, ESUR.
5. Data direction with reference to the Interrupt Unit.

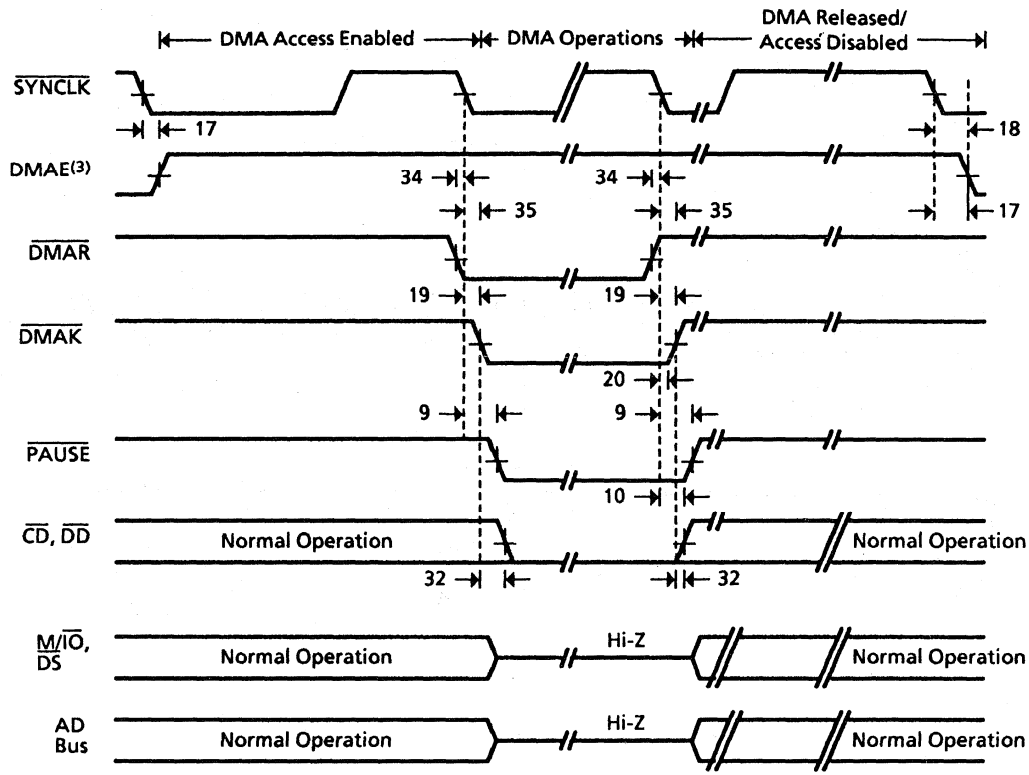
Figure 7: Internal I/O Timing - Write/Command



Notes:

1. Other output states:
   - CD = high
   - PAUSE = high
   - DMAK = high
2. Other required input states:
   - HLDAK = high
   - DMAR = high
3. Active during RCW XIO only.
4. Data direction with reference to the Interrupt Unit.

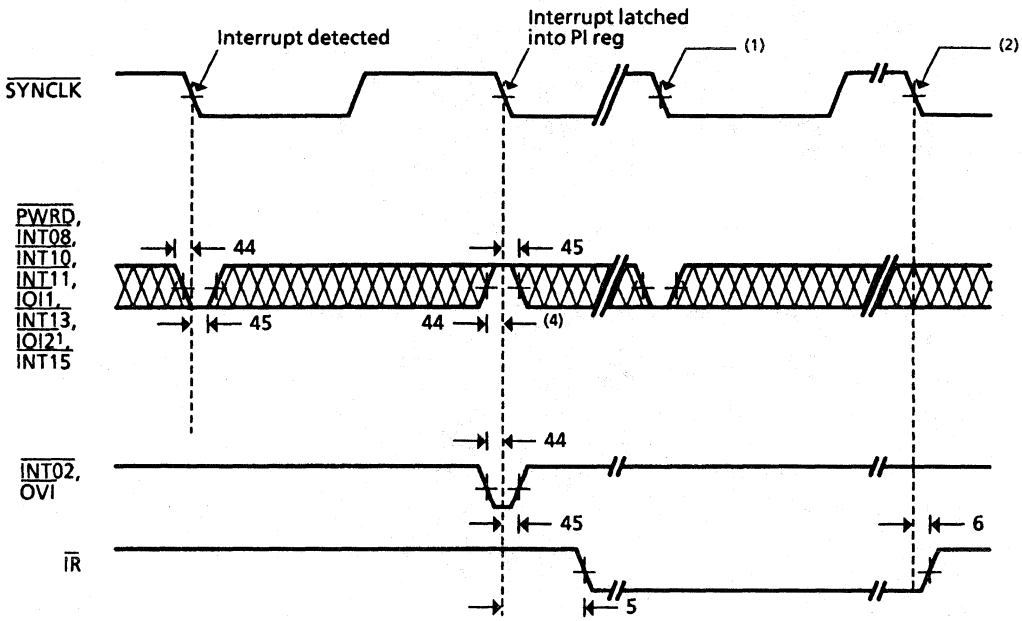
Figure 8: Internal I/O Timing - Read



Notes:

1. Other required input:
   DTIMER = high
2. Other output:
   IRDY = high
3. DMAE is enabled and disabled by XIO commands DMAE and DMAD respectively if the DMA interface has been enabled via microcode.

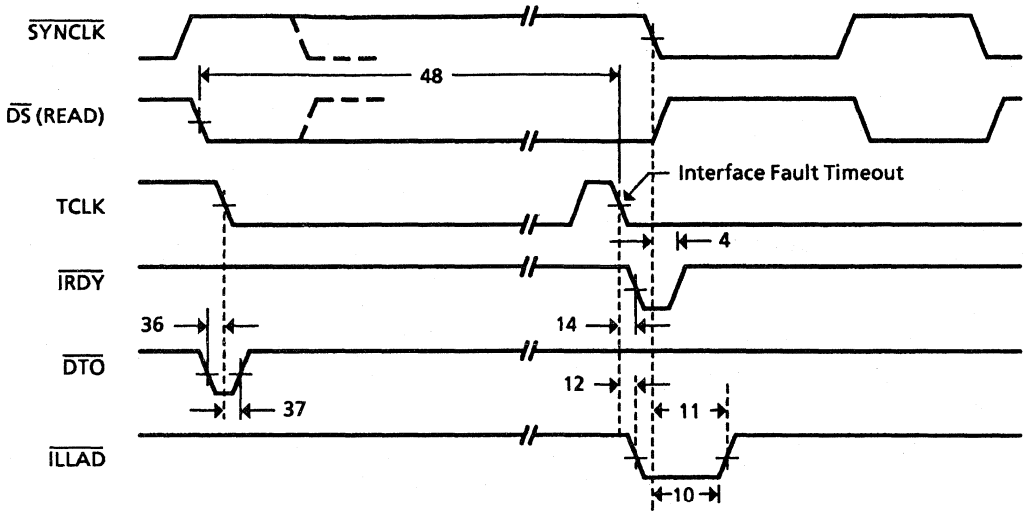
Figure 9: DMA Access/Release Timing



Notes:

1. 1750A instruction completed, microcode interrupt handling routine begins.
2. 3rd machine cycle of microcode routine.
3. Other output:
   $\overline{IRDY}$ = high
   $\overline{CD}$ = high
   $\overline{DMAK}$ = high
   $\overline{PAUSE}$ = high
4. The interrupt input must be detected high by a SYNCLK high-to-low transition (after a low on the interrupt input) before a new interrupt on said input will be detected.

Figure 10: Interrupt Request Timing



Notes:
1. 2TCLK ↓ edges during a continuous $\overline{DS}$ = low are necessary to cause a Bus Fault Timeout.
2. Other required input:
   $\overline{DTO}$ = high
3. Other output:
   $\overline{DMAK}$ = high
   $\overline{PAUSE}$ = high

Figure 11: Bus Fault Timeout Timing

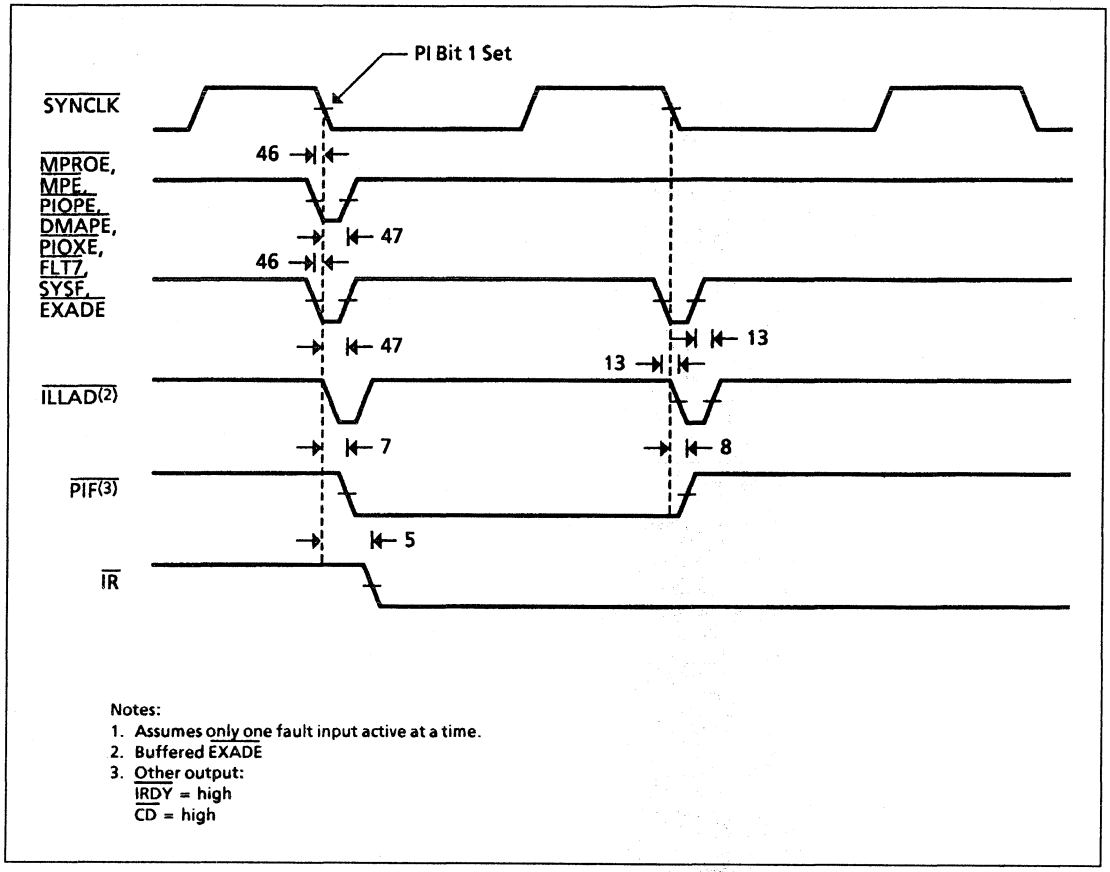


Figure 12: Fault Capture Timing

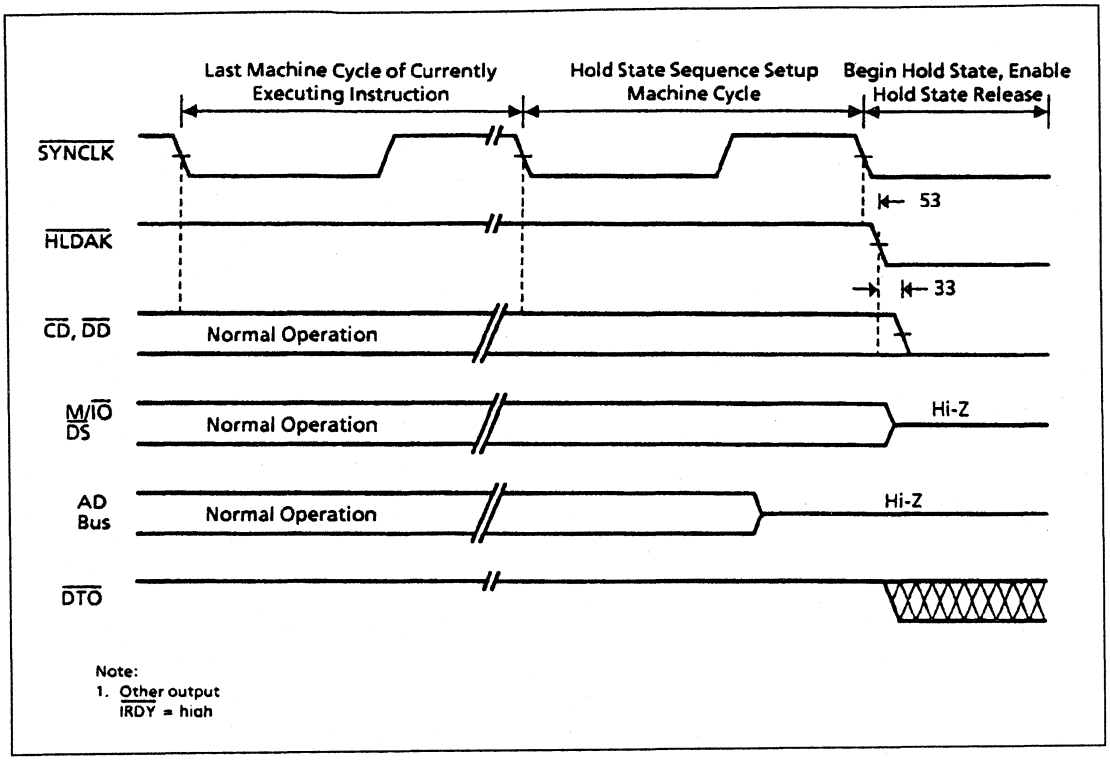


Figure 13: Hold State Generation Timing

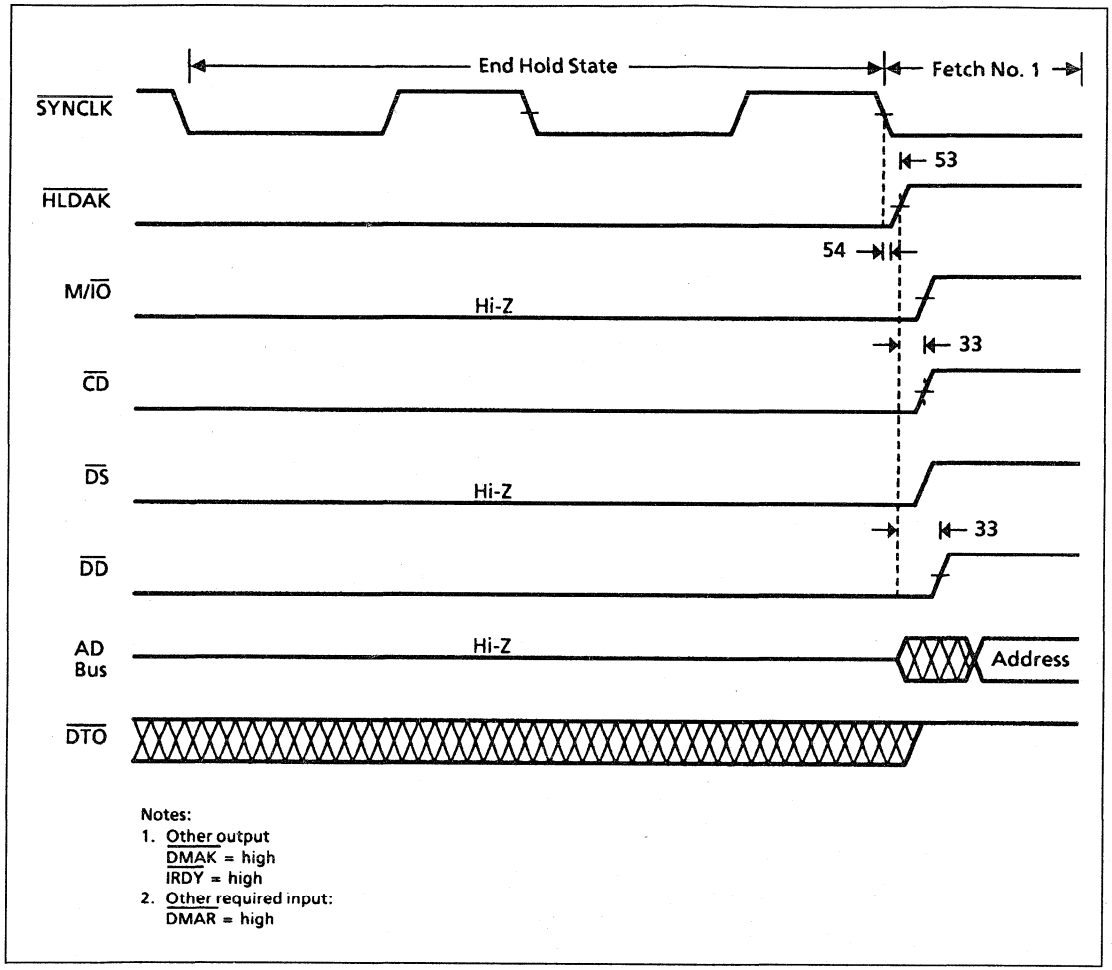


Figure 14: Hold State Termination Timing

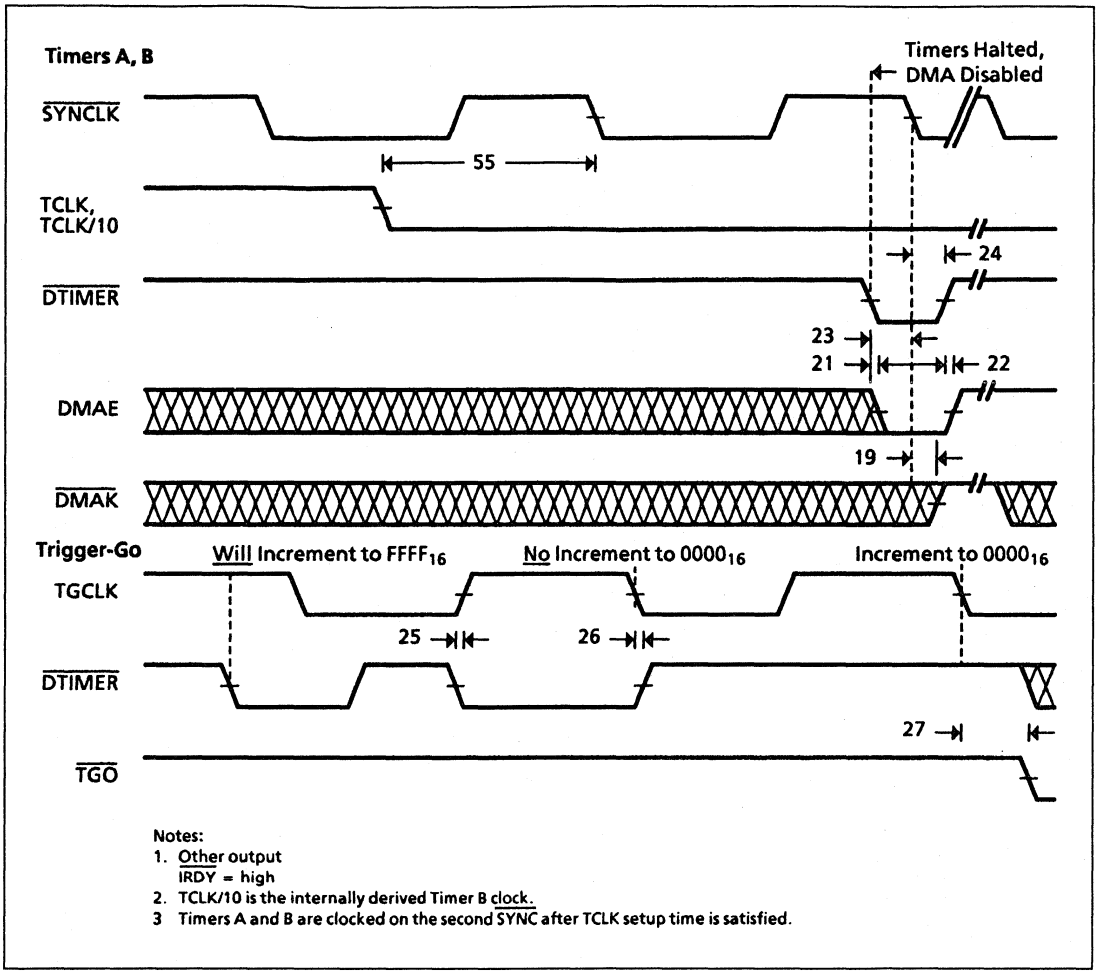


Figure 15: Timer Operations

Subgroup	Definition
1	Static characteristics specified in Table 9 at +25°C
2	Static characteristics specified in Table 9 at +125°C
3	Static characteristics specified in Table 9 at -55°C
7	Functional tests at +25°C
8a	Functional tests at +125°C
8b	Functional tests at -55°C
9	Switching characteristics specified in Table 7b at +25°C
10	Switching characteristics specified in Table 7b at +125°C
11	Switching characteristics specified in Table 7b at -55°C

Table 7a: Definition of Subgroups

No.	Parameter	Test Conditions[1][2]	Min	Typ	Max[3]	Units
1	SYNCLKN ↓ to Data Valid	Load 1	-		3r+100	ns
2	Data Valid after SYNCLKN ↓	Load 1	30		-	ns
3	SYNCLKN ↑ to IRDYN Valid	Load 1	-		40	ns
4	IRDYN Valid after SYNCLKN ↓	Load 1	10		-	ns
5	SYNCLKN ↓ to IRN Valid	Load 1	-		60	ns
6	IRN Valid after SYNCLKN ↓	Load 1	15		-	ns
7	SYNCLKN ↓ to PIFN Valid	Load 1	-		50	ns
8	PIFN Valid after SYNCLKN ↓	Load 1	15		-	ns
9	SYNCLKN ↓ to SURE, NPU, PAUSEN Valid	Load 1	-		50	ns
10	SURE, NPU, ILLADN, PAUSEN after SYNCLKN ↓	Load 1	15		-	ns
11	SYNCLKN ↓ to ILLADN ↑	Load 1	-		75	ns
12	TCLK ↓ to ILLADN ↓ (Bus Timeout)	Load 1	-		75	ns
13	EXADEN to ILLADN Valid	Load 1	-		60	ns
14	TCLK ↓ to IRDYN ↓ (Bus Timeout)	Load 1	-		50	ns
15	SYNCLKN ↑ to CONFWN Valid	Load 1	-		75	ns
16	CONFWN Valid After SYNCLKN ↓	Load 1	10		-	ns
17	SYNCLKN ↓ to DMAEN Valid	Load 1	-		75	ns
18	DMAE Valid after SYNCLKN ↓	Load 1	5		-	ns
19	SYNCLKN ↓ to DMAKN Valid	Load 1	-		50	ns
20	DMAKN Valid after SYNCLKN ↓	Load 1	5		-	ns
21	DTIMERN ↓ to DMAEN ↓	Load 1	-		60	ns
22	DTIMERN ↓ to DMAEN ↑	Load 1	-		60	ns
23	DTIMERN Setup to SYNCLKN ↓		50		-	ns
24	DTIMERN Hold after SYNCLKN ↓		10		-	ns
25	DTIMERN Setup to TGCLK ↑		30		-	ns
26	DTIMERN Hold after TGCLK ↓		12		-	ns
27	TGCLK ↓ to TGON ↓	Load 1	-		150	ns
28	SYNCLKN ↑ to TGON ↑	Load 1	-		75	ns
29	TGON Valid after SYNCLKN ↑	Load 1	15		-	ns
30	DSN ↓ to DDN ↓	Load 1	10		35	ns
31	DSN ↑ to DDN ↑	Load 1	10		35	ns
32	DMAKN to DDN, CDN Valid	Load 1	-		30	ns
33	HLDAKN to DDN, CDN Valid	Load 1	-		50	ns
34	DMARN Setup to SYNCLKN ↓		20		-	ns
35	DMARN Hold after SYNCLKN ↓		10		-	ns
36	DTON Setup to TCLK ↓		30		-	ns
37	DTON Hold after TCLK ↓		10		-	ns
38	Address/Command Setup to SYNCLKN ↑		50		-	ns
39	Address/Command Hold after SYNCLKN ↑		10		-	ns
40	Data Setup to SYNCLKN ↓		50		-	ns
41	Data Hold after SYNCLKN ↓		5		-	ns
42	Microcode Setup to SYNCLKN ↓		10		-	ns
43	Microcode Hold after SYNCLKN ↓		20		-	ns
44	Interrupts Setup to SYNCLKN ↓		20		-	ns
45	Interrupts Hold after SYNCLKN ↓		10		-	ns
46	Faults Setup to SYNCLKN ↓		20		-	ns
47	Faults Hold after SYNCLKN ↓		15		-	ns
48	Bus Fault Timeout Interval (4)		1		2	TCLK
49	INTREN Setup to SYNCLKN ↓		30		-	ns
50	INTREN Hold after SYNCLKN ↓		5		-	ns
51	M/ION Setup to SYNCLKN ↓		40		-	ns
52	M/ION Hold after SYNCLKN ↓		5		-	ns
53	HLDAKN Setup to SYNCLKN ↓		20		-	ns
54	HLDAKN Hold after SYNCLKN ↓		7		-	ns
55	TCLK Setup to SYNCLKN ↓		15		-	ns
56	TCLK Hold after SYNCLKN ↓		10		-	ns

Mil-Std-883, Method 5005, Subgroups 9, 10, 11.

(1) T_A = +25°C, -55°C and +125°C tested at V_{DD} = 4.5V and 5.5V.

(2) Unless otherwise noted: VIL ≥ 0.9V, VIH ≤ 4.0V timing measured from 50% to 50% points.

(3) r = 1OSC period 0.5r implies 50% OSC duty cycle.

(4) Data obtained by characterization or analysis; not routinely measured.

Table 7b: Timing Parameter Values

6.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 8: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7.0 DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Total Dose Radiation Not Exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	V_{SS} = 0	4.5	5.0	5.5	V
V_{IHC}	CMOS Input High Voltage (Note 1)	-	V_{DD}-1	-	-	V
V_{ILC}	CMOS Input Low Voltage (Note 1)	-	-	-	V_{SS}+1	V
V_{IHT}	TTL Input High Voltage (Note 2)	-	2.0	-	-	V
V_{ILT}	TTL Input Low Voltage (Note 2)	-	-	-	0.8	V
V_{OHC}	CMOS Output High Voltage (Note 1)	I_{OH} = -1.4mA, V_{DD} = 4.5V	4.0	-	-	V
V_{OLC}	CMOS Output Low Voltage (Note 1)	I_{OL} = 2mA, V_{DD} = 5.5V	-	-	0.5	V
V_{OHT}	TTL Output High Voltage (Note 2)	I_{OH} = -1.4mA, V_{DD} = 4.5V	3.5	-	-	V
V_{OLT}	TTL Output Low Voltage (Note 2)	I_{OL} = 2mA, V_{DD} = 5.5V	-	-	0.4	V
I_L	Input Leakage Current (Note 3)	V_{DD} = 5.5V, V_{IN} = 0V or 5.5V	-	-	±10	µA
I_{OZ}	Output Leakage Current (Note 3)	V_{DD} = 5.5V, V_O = 0V or 5.5V	-	-	±50	µA
I_{DDOP}	Operating Supply Current	V_{DD} = 5.5V, SYNCLKN = 4MHz	-	5	14	mA
I_{DDST}	Static Supply Current	V_{DD} = 5.5V, SYNCLKN = 0MHz	-	3	10	mA

Mil-Std-883, Method 5005, Subgroup 1, 2, 3.

Notes: 1. The following signals are CMOS compatible:
a) CMOS inputs: INTREN, Microcode Bus, (M04, M05, M06), HLDAKN and SYNCLK.
b) CMOS outputs: PIFN, IRN and IRDYN.

2. The following signals are TTL compatible:
a) DTIMERN, TGCLK, MPROEN, DMAPEN, EXADEN, PIOXEN, FLT7N, SYSFN, OVIN, PWRDN, INT02N, INT08N,INT10N, INT11N, INT12N/IOI1N, INT13N, INT14N/IO12N, INT15N, DTON, DSN, M/ION, DMARN, TCLK and MSTOPN.
b) TTL outputs: SURE, NPU, DDN, TGON, CDN, PAUSED, ILLADN, CONFIG, DMAKN and DMAE.
c) TTL I/O signal: Address/Data Bus (AD00-AD15).

3. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.

Table 9: DC Electrical Characteristics

8.0 PACKAGING INFORMATION

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.508	0.014	-	0.020
c	0.229	-	0.36	0.009	-	0.014
D	-	-	82.04	-	-	3.230
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	22.86 Typ.	-	-	0.900 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	23.4	-	-	0.920
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG413

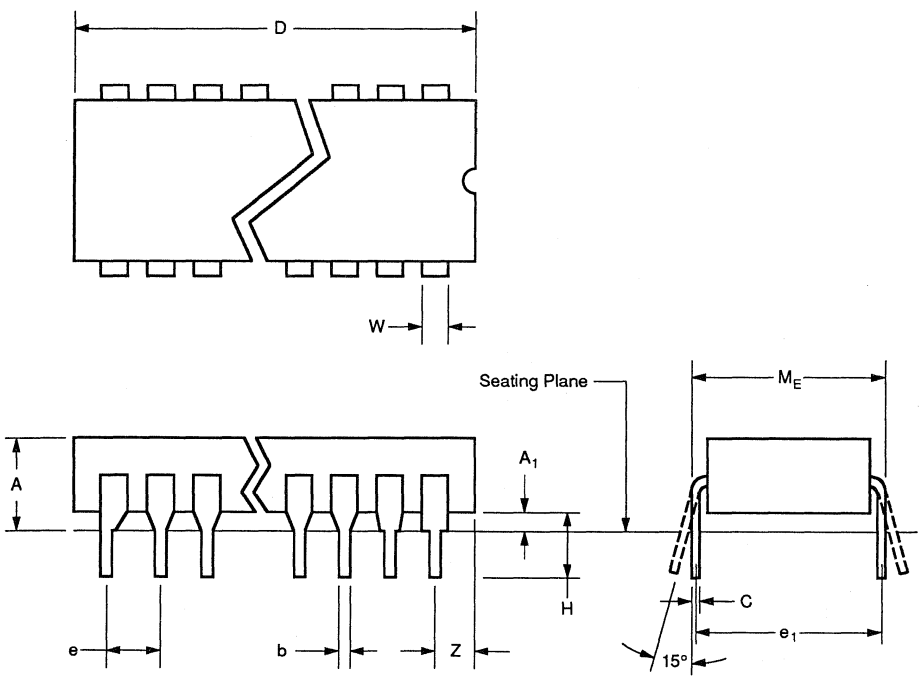


Figure 16a: 64-Pin Ceramic Sidebraze DIL - Package Style C

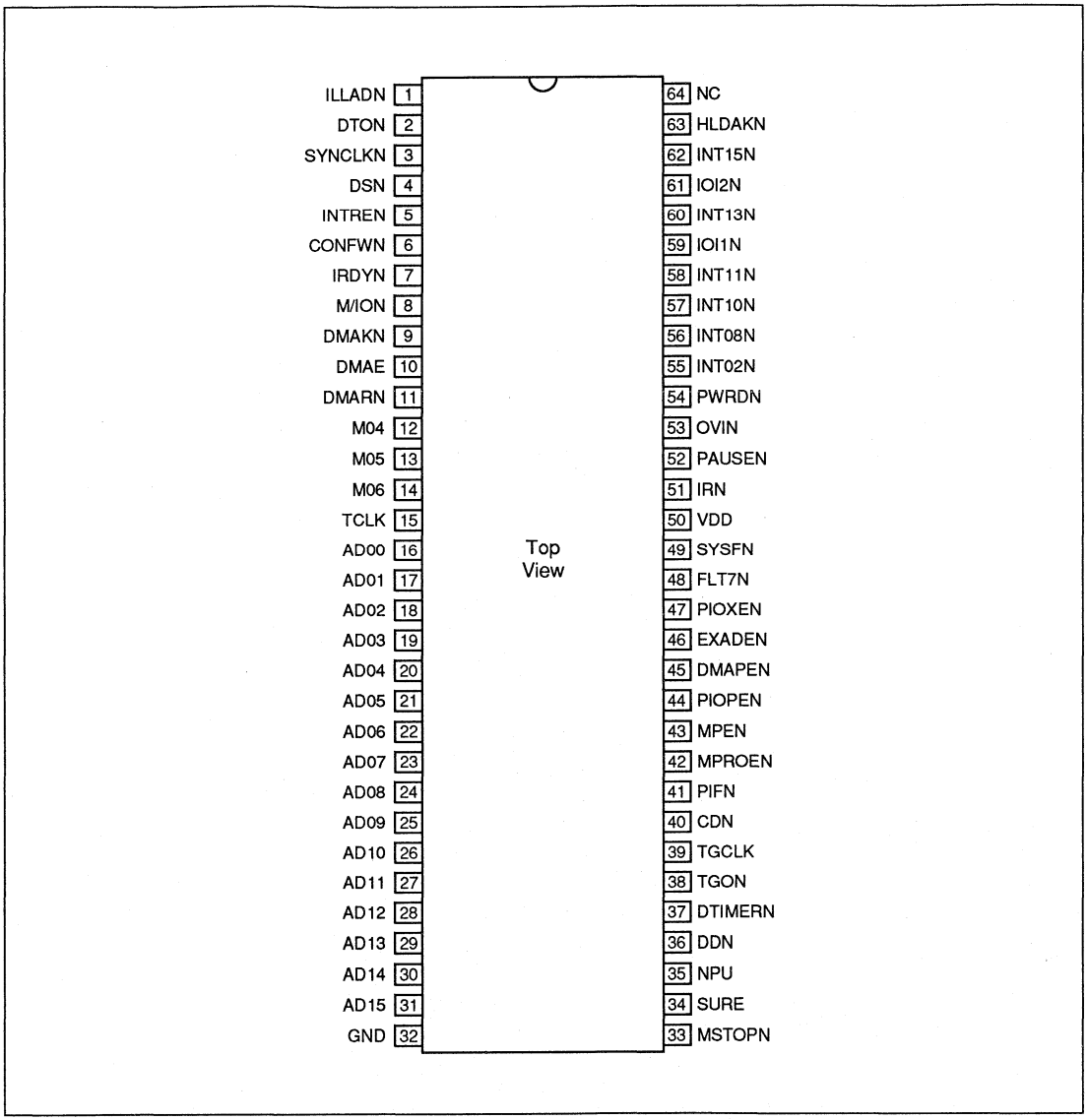


Figure 16b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.905	-	2.21	0.075	-	0.087
b1	-	0.51	-	-	0.020	-
D	18.08	-	18.62	0.712	-	0.733
E	18.08	-	18.62	0.712	-	0.733
e	-	1.02	-	-	0.040	-
Z	1.40	-	1.78	0.055	-	0.070

XG493

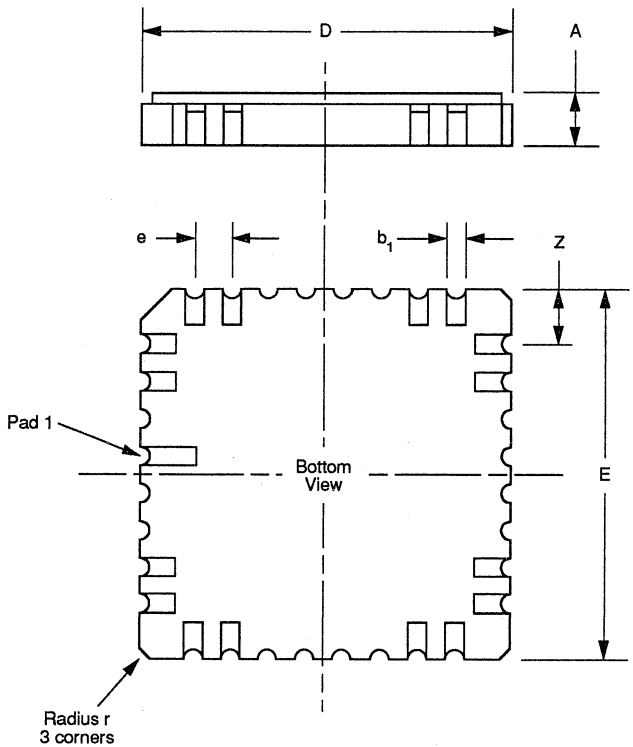


Figure 17a: 64-Lead Leadless Chip Carrier - Package Style L

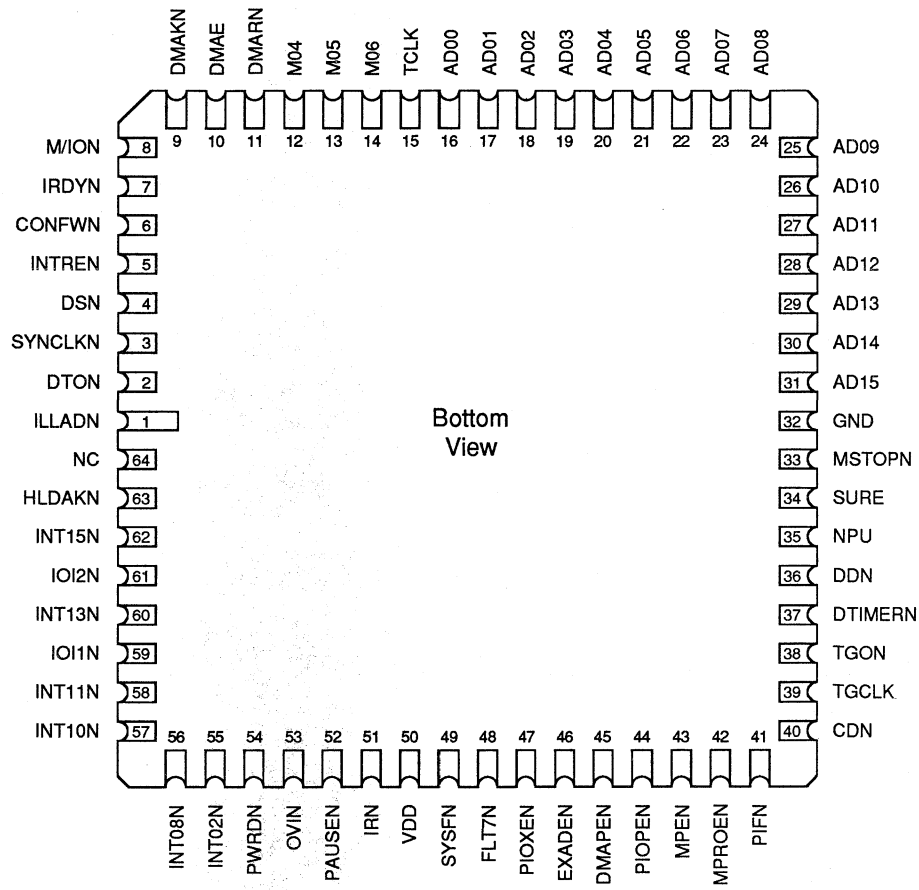


Figure 17b: Pin Assignments

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

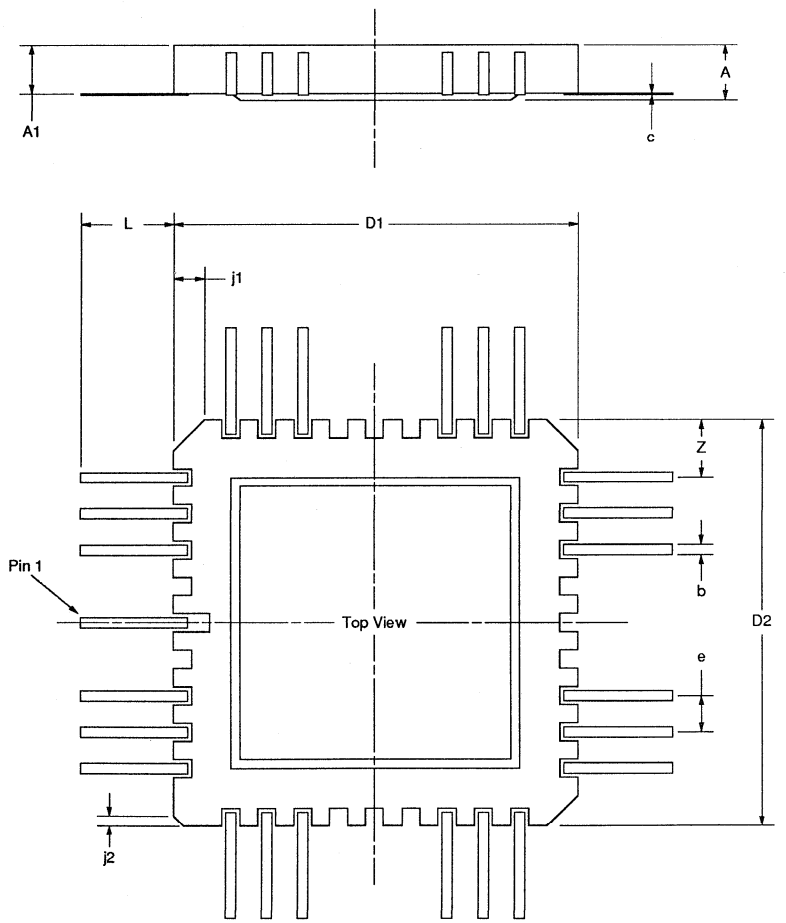


Figure 18a: 68-Lead Topbraze Flatpack - Package Style F

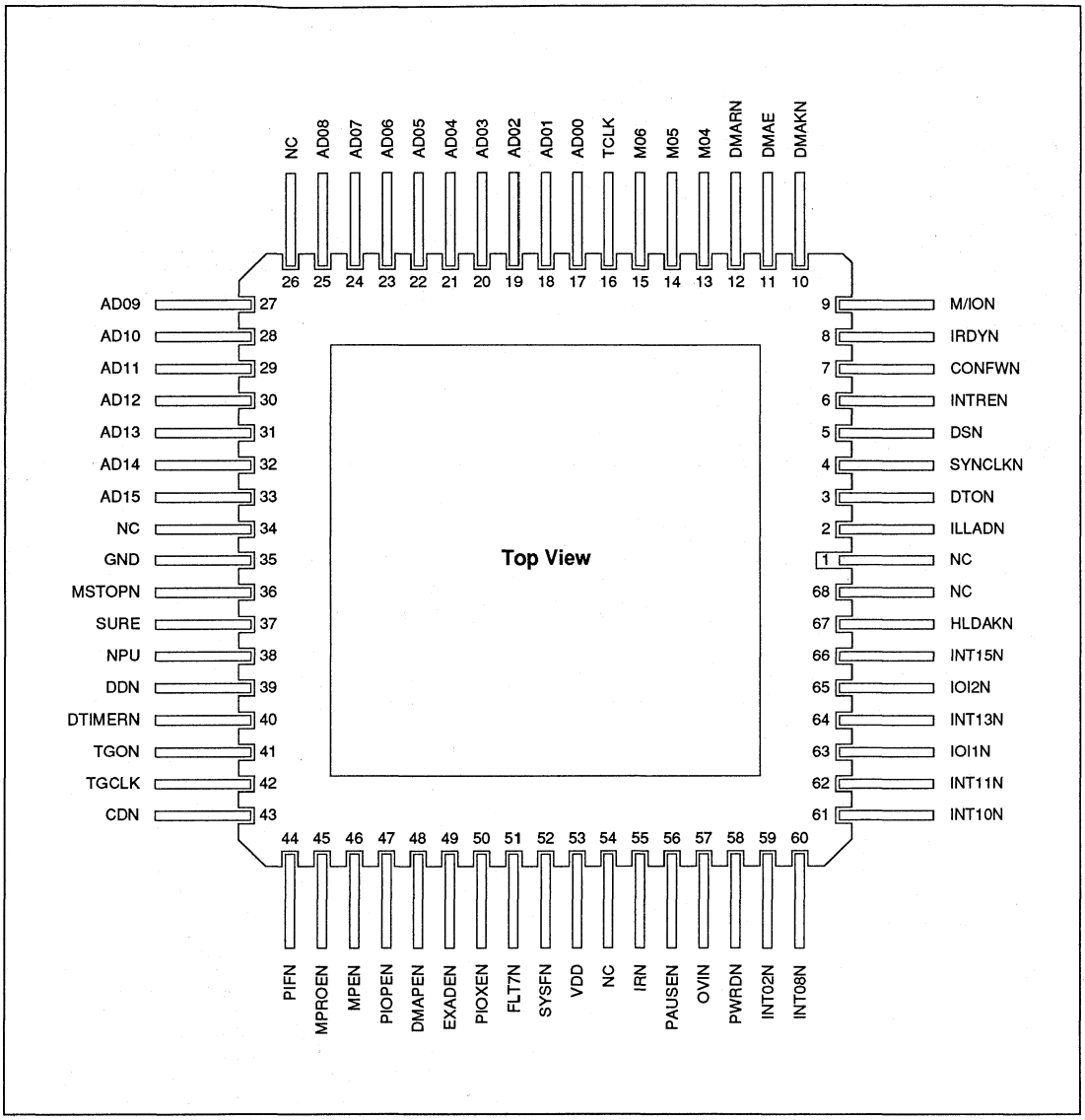


Figure 18b: Pin Assignments

9.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

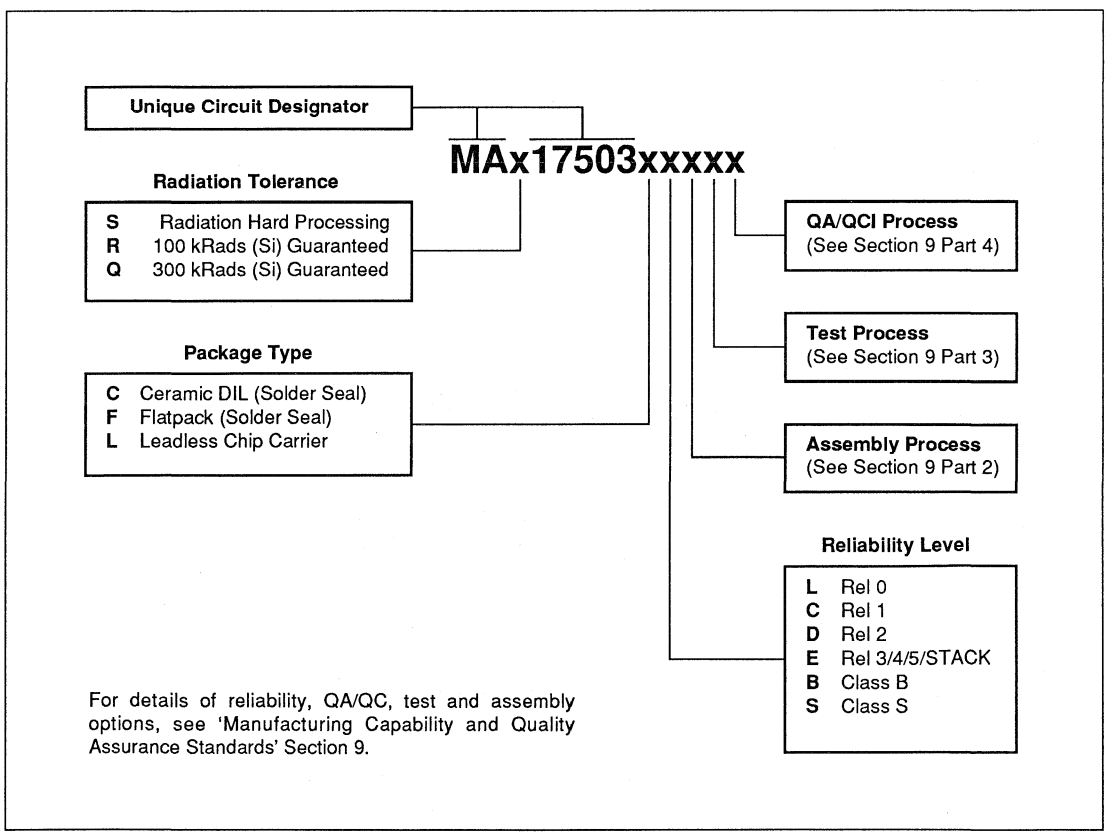
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 10: Radiation Hardness Parameters

10.0 ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

Section 2

Peripherals & Support Circuits

MA31751

MEMORY MANAGEMENT UNIT & BLOCK PROTECTION UNIT

The MA31751 Memory Management Unit/Block Protect Unit (MMU/BPU) is an optional chip which may be used to expand the capabilities of the MA31750.

User configurable, the MA31751 can perform as an MMU, a BPU or both MMU and BPU, conforming to MIL-STD-1750A and 1750B. MMU mapping and BPU protection for 1M words of memory is provided by the internal memory. Up to 16 MA31751 devices can be used to give 16M words of logical mapped onto 8M words of physical address space with protection in 1750B mode.

The MA31751 is designed to have a simple interface to both the CPU and the system bus with the minimal number of control lines. This reduces board space and simplifies system design.

The MA31751 traps the MMU and BPU XIO commands to program and read the logical to physical mapping and memory access control. This provides simple memory management as defined by the MIL-STD-1750.

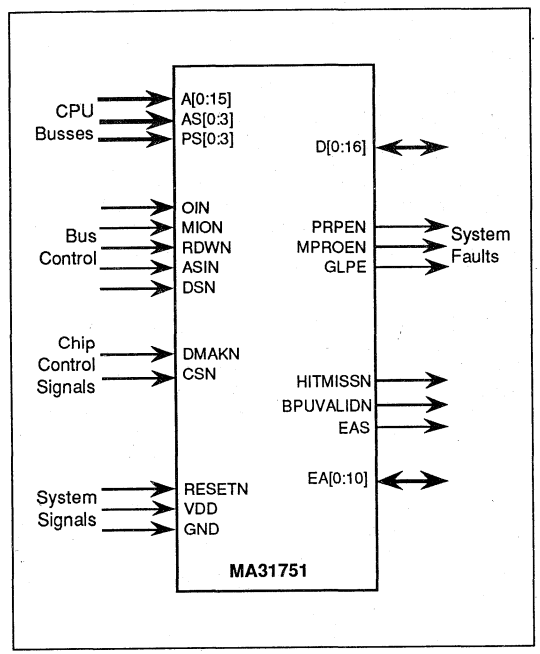


Figure 1: Chip Control Signals

FEATURES

- MIL-STD-1750A/B Compatible
- Radiation Hard CMOS/SOS Technology
- User Configurable as Either a Memory Management Unit (MMU) or a Block Protect Unit (BPU) or Both
- Memory Management Unit Configuration
  - 1 MWord Physical Address Space
  - Access Lock and Key of 4K-Word Blocks
  - Write/Execute Protection of 4K-Word Blocks
- Block Protect Unit Configuration
  - Protection of 1K-Word Blocks
  - Global Memory Write Protection During Initialisation
- Direct Memory Access Support

1.0 DEVICE OPERATION

The MA31751 is an interface device designed to increase the memory addressing capability of the MA31750 CPU. It is user configurable as an MMU and/or a BPU conforming to the MIL-STD-1750A and the proposed MIL-STD-1750B. The MMU provides expanded addressing and full access lock/key protection in both modes, together with write/execute protection on 4K pages.

The BPU allows up to 1M words of memory to be protected in 1K blocks (MIL-STD-1750A). Up to 8M words may be protected by multiple MMU/BPU units (draft MIL-STD-1750B).

In 1750A mode, one MA31751 unit can act as both MMU and BPU for the maximum 1M words of address space. In 1750B mode, up to 8 MA31751 units may be used to provide the maximum BPU functions and up to 16 units for the maximum MMU functions. For any given physical memory location the MMU and BPU function may be split across two MA31751 devices depending on the logical to physical address mapping.

1.1 INITIALISATION

The MA31751 is initialised by the CPU when a system reset occurs. Initially all mappings are set one to one to give a linear 1M word logical to physical mapping. The BPU defaults to no protection on a reset and requires 256 machine cycles (AS pulsing) to set the internal BPU memory. The CPU recognises the presence of the MMU/BPU by the setting of appropriate bits in the configuration register. When the configuration register is read, the MA31751 stores MMU, BPU, parity and 1750 mode information internally. The CPU may change the mapping and access protection when it is in privileged instruction mode using XIO commands 4D00 to 52FF as defined in MIL-STD-1750.

1.2 ADDRESS TRANSLATION AND PROTECTION

The MMU maps system memory into 4K word pages by the mechanism shown in figure 3. A page is a block of physical memory which is uniquely specified by the physical page address, the PPA. A given address within any page is specified by the least significant 12 bits of the CPU address bus. One page register has the physical page address and the access control information relating to one page. There are 512 page registers, organized into 16 sets. The 16 sets are addressed by AS[0:3]. Each set has two groups of page registers, one for operand memory space and one for instruction memory space. These are addressed by OIN. Each group contains 16 page registers accommodating a total of 256 registers for each of operand and instruction memory space.

The MMU also checks for protection violation by comparing the processor state (PS), read from the CPU status word, with the access lock (AL) field in the page register. An additional bit in each page register allows the system to disable writes to operand pages or reads (execution) of instruction pages. If any memory violation occurs, the memory protect output (MPROEN) is asserted low. This typically causes a bus-fault-timeout on the processor which aborts the error cycle.

Figure 2 illustrates the Access Key mapping mechanism. When memory transactions are controlled by the MA31750, the AS[0:3] and PS[0:3] bits necessary to perform the address translation and access protection functions respectively, are obtained from a copy of the processor status word held by the MMU. Modifications to the CPU status word are reflected in the MMU copy.

Figure 4 illustrates the standard way to map the logical CPU addresses, AS[0:3] and PB[0:3] onto the physical extended address bus for both 1750A (a 20-bit physical address) and for 1750B (a 23-bit physical address). Figure 5 shows the various selections to achieve the required memory size and protection.

AL Code	Acceptable Access Key Codes
0	0
1	0,1
2	0,2
3	0,3
4	0,4
5	0,5
6	0,6
7	0,7
8	0,8
9	0,9
A	0,A
B	0,B
C	0,C
D	0,D
E	0,E
F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F

Figure 2: Access Lock and Key Mapping

1.3 BLOCK PROTECTION

The presence of a BPU in the system is determined from the CPU configuration word. A BPU present in the system offers protection of the physical memory in 1k blocks. It takes the physcial address from the EA bus hence the BPU protection cannot start until the MMU lookup has completed and EAS rises. If no MMU is present, the physical address is read from the processor address bus. The address selects the relevant 16 bit word from the BPU RAM or cache. Each bit in this word represents the protection on 1k of physical memory. Any attempt to write a protected block results in an access violation error from the BPU.

NOTE: MIL-STD-1750 states that the MSB of the Block Protect Register (BPR) should protect the least significant address block.

1.4 DIRECT MEMORY ACCESS

The MA31751 supports DMA access within the expanded memory space, including translation and protection. When a DMA controller is performing memory transactions, it must provide the AS[0:3] and PS[0:3] signals to the inputs of the MMU for address translation and access protection.

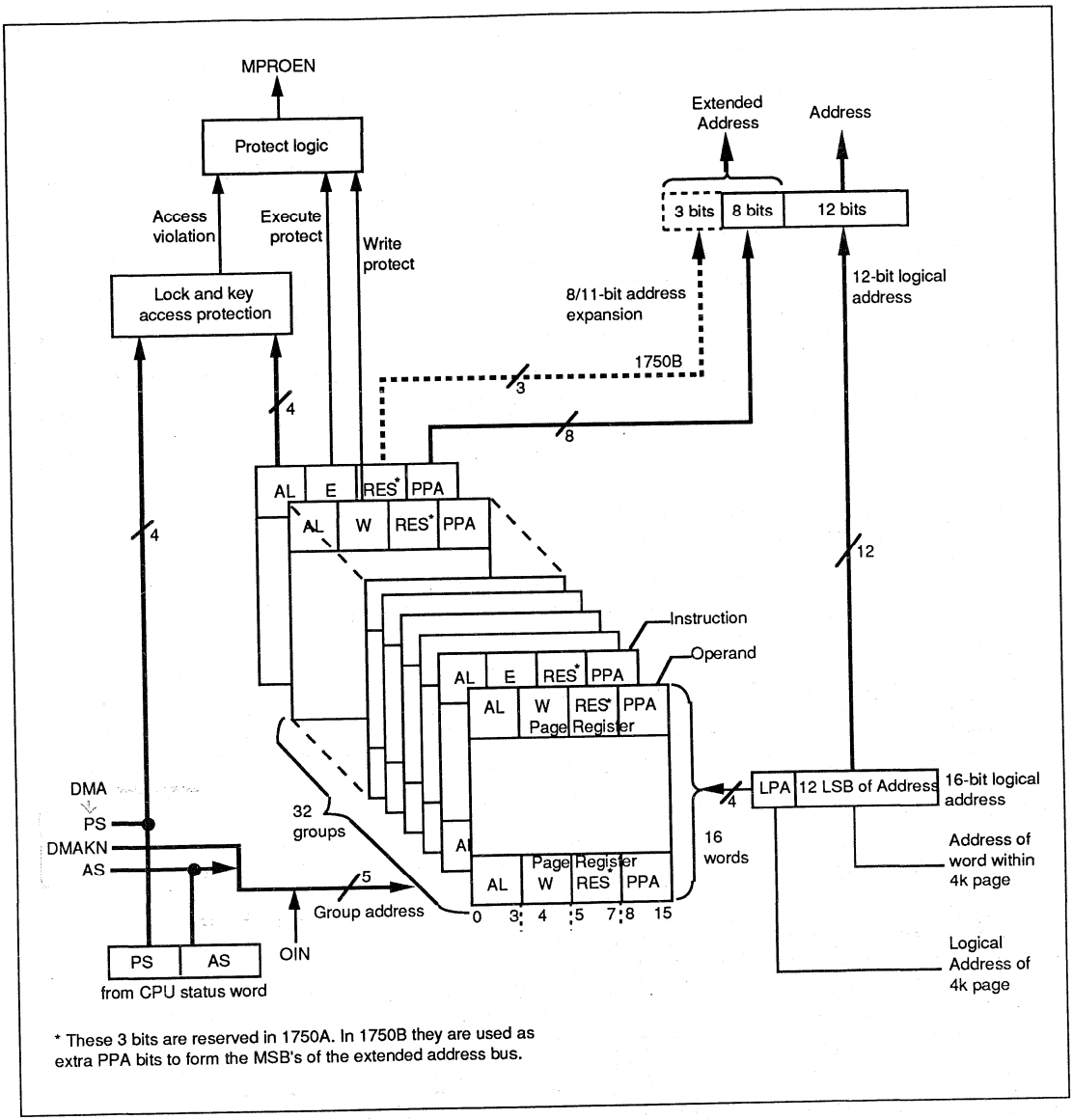


Figure 3: MMU Memory Mapping Mechanism

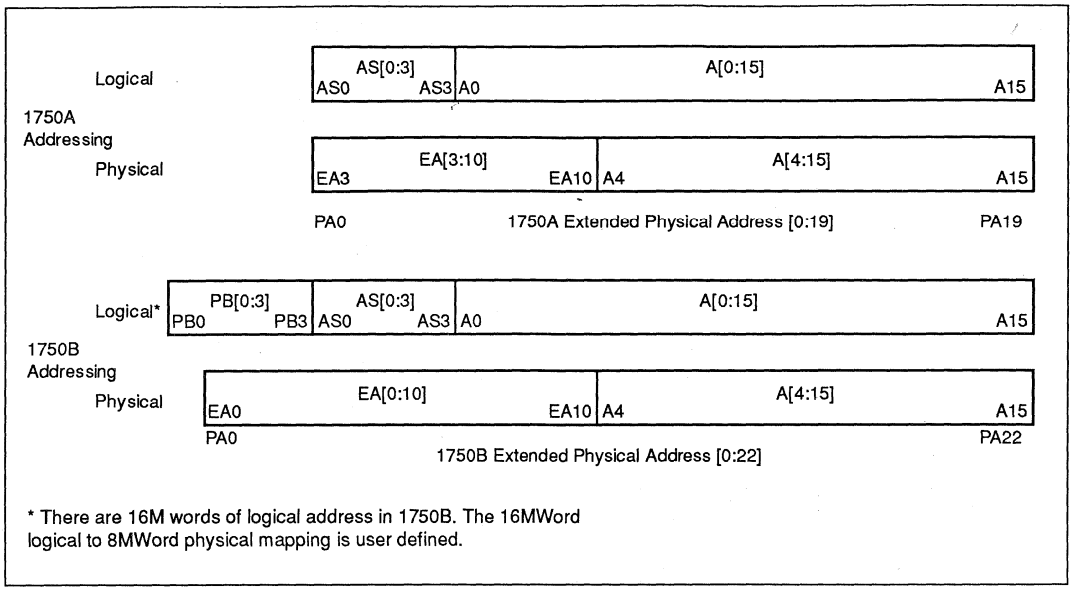


Figure 4: Extended Address Mapping in 1750A/B Mode

Addressable Physical Memory	Addressable Logical Memory	Is BPU Protection Required?	Mode	Number of MMUs	Number of BPUs	Number of MA31751s Required
64KW	64KW	NO	A	0	0	0
1MW	1MW	NO	A	1	0	1
64KW	64KW	YES	A	0	1	1
1MW	1MW	YES	A	1	1	1
64KW	64KW	NO	B	0	0	0
8MW	1MW	NO	B	1	0	1
8MW	2MW	NO	B	2	0	2
8MW	4MW	NO	B	4	0	4
8MW	8MW	NO	B	8	0	8
8MW	16MW	NO	B	16	0	16
64KW	64KW	YES	B	0	1	1
8MW	1MW	YES	B	1	8	8
8MW	2MW	YES	B	2	8	8
8MW	4MW	YES	B	4	8	8
8MW	8MW	YES	B	8	8	8
8MW	16MW	YES	B	16	8	16

Notes: 1. Memory is specified in terms of addressable instruction space.
2. It is assumed that the whole of the physical address space is used in 1750B - if this is not the case the number of MA31751 chips may be reduced.

Figure 5: MA31751 Selection Chart for Varying Memory Requirements

2.0 TIMING CONSIDERATIONS

2.1 MMU TIMINGS

To enable a fast page register look-up time, the MMU has two fast translation cache registers. These hold the address translation information on the 4K memory page which is currently being accessed. When the CPU has control of the system, one cache register is for operand transfers and one for instruction transfers, as these often occur in different pages. The appropriate translation cache register is chosen by the operand/instruction (OIN) signal from the CPU. When a DMA has system control, the caches operate as Read/Write caches, the appropriate cache being selected by the RDWN signal. When either an instruction/read or an operand/write crosses a page boundary, one wait state may be added whilst the translation cache register is updated from internal memory. This system minimises the MMU overhead.

2.2 BPU TIMINGS

A similar caching system is employed in the BPU section of the MA31751 to allow more rapid detection of access violations. If the physical address crosses a 16K block boundary, then one wait state may be added.

Different combinations of cache hits and misses give different access times if the MA31751 is acting as both an MMU and a BPU. If the logical address (from the CPU) gives an MMU cache hit, the physical address is looked-up from the translation cache register (operand or instruction, depending on OIN). If the physical address gives a cache hit, the protection for the block is looked-up in the BPU cache register. This situation (both hits) gives the fastest access time. The access time is a maximum if both logical and physical addresses give cache misses.

3.0 OUTPUTS FROM THE MA31751

3.1 PRPEN

This signal goes active low if a parity error occurs on a memory access, ie. there is a parity error in the MMU page register. There is no parity checking on XIO cycles, (this should be covered by the processor).

3.2 MPROEN

This signal is always low when ASIN is low. On a memory access, with an MMU only present it stays low until the address translation is validated. If the translation is erroneous, it stays low, causing a machine cycle time-out. If a BPU is present with the MMU, an erroneous translation causes the output to stay low. If the translation is correct, MPROEN will still stay low until the BPU check has completed. If there is no block protection set, MPROEN goes high, allowing the cycle to proceed. If the block protection is set, MPROEN stays low and the cycle times out. In a BPU only system, MPROEN indicates whether or not the protection bit is set for the address being accessed.

In a 1750B system with both an MMU and BPU present, MPROEN may glitch between the translation validation and the protection check (as the MMU and BPU functions may be on different devices). In this case, MPROEN should be gated with BPUVALIDN being low before being input to the CPU.

3.3 BPUVALIDN

BPUVALIDN falls to indicate that the output from the BPU is valid. If no BPU is present, BPUVALIDN remains high.

4.0 PIN DESCRIPTIONS

A description of each pin function appears in Figure 6. The acronym is presented first, followed by its function and description. Timing characteristics of each of the functions are shown in section 6.

All CMOS compatible signals are protected by an Electrostatic Discharge (ESD) protection circuit. Throughout this data sheet, active low signals are denoted either by placing a bar over the signal name,or by following the signal name with an "N" suffix, e.g.,DSN.

All unused inputs should be connected to their inactive state and should not be allowed to float.

4.1 SIGNAL DEFINITIONS

Pin Name	Function	Description
SYSTEM BUSSES		
A00-A15	Processor Address Bus	An active-high address bus for addresses and XIO commands. A15 is the LSB.
D00-D16	System Data Bus	Data bus used to transfer data to and from the MMU/BPU. D15 is the LSB and D16 is the parity bit.
EA00-EA10	Extended Address Bus	If the MMU is selected (using CSN) then EA0-EA10 provides the system extended address. EA3-EA10 should be combined with A4-A15 from the processor to give the full 20 bit 1750A system address bus and EA0-EA10 with A4-A15 gives a 23 bit 1750B system address bus. (See Fig 4).During XIO transfers, EA7-10 mimic A0-A3 to present the full processor address to the system. When the MMU is not selected, EA0-EA10 become inputs to allow the BPU to protect the appropriate section of extended memory.
BUS CONTROL		
ASIN	Address Strobe In	The rising edge of this active-high signal generated by the CPU or DMA controller, indicates that a valid address is present on the MA31750.
DSN	Data Strobe	The rising edge of this active-low signal generated by the CPU or DMA controller, indicates that valid data is present on D00-D16 of the MA31750.
EAS	Extended Address Strobe	The rising edge of this active-high signal indicates that a valid and stable extended address is available from the MA31751. This pin becomes an input when no MMU is selected and should be driven from the system address strobe. During XIO cycles, EAS follows ASIN.
MION	Memory / IO Select	This input is used to select between normal operation and command transfer (XIO) mode. A high indicates memory whilst a low indicates IO. This signal is provided by the CPU or the DMA controller.
RDWN	Read / Write Select	This input indicates the direction of data transfer on the data bus. A high level indicates that the processor is reading the bus whilst a low level indicates that the processor is driving the bus. The input is driven by the CPU or the DMA controller.
OIN	Operand / Instruction Select	This input indicates the type of data on the data bus. A high indicates operand data whilst a low indicates the presence of instruction data. The signal is provided by the CPU or the DMA controller.
EXTENDED MEMORY CONTROL		
AS0-AS3	Address State	This bus comes from the DMA controller during DMA accesses. It is used by the MMU as part of the page selection operation. (During CPU operation, this information is read from the MMU's copy of the CPU status word). If no MMU function is required, these inputs should be tied to ground.
PS0-PS3	Processor State	This bus comes from the DMA controller during DMA accesses. It is used by the MMU to provide lock and key protection on page accesses. (During CPU operation, this information is read from the MMU's copy of the CPU status word.) If no MMU function is required, these inputs should be tied to ground.

Figure 6: Pin Description Table

Pin Name	Function	Description
ERROR INDICATION		
MPROEN	Memory Protect Error	The MPROEN output is always asserted low when ASIN is low. On an external memory cycle, MPROEN low at the end of the cycle indicates there has been a protection error in either the MMU or the BPU. A high indicates no error. MPROEN goes high after ASIN rising on XIO cycles.
PRPEN	Page RAM Parity Error	This active-low output is asserted low if a parity error is detected during an MMU/BPU memory transfer.
MISCELLANEOUS		
RESETN	System Reset	Active low device reset input. Should be connected to system reset.
CSN	MMU Chip Select	A low on this input selects the MMU. In a 1750A system, this input may be tied to ground if MMU functions are required, or tied to MION if only BPU functions are required (must be active for XIO cycles when the device may need to respond to an MMU/BPU XIO command.) In 1750B, this input should be derived by decoding the PB[0:3] bus from the CPU. (Note that in 1750B mode, one device is required per implemented page bank.)
BPUVALIDN	BPU enabled and selected	This output becomes active (low) when MPROEN is valid if there is at least one BPU present in the system .
DMAKN	DMA Acknowledge	This active-low input is used to select between the CPU and DMA protection registers within the MA31751, and should be asserted low when the CPU has relinquished control to a DMA in the system. DMAKN active low means that the MMU gets the AS[0:3] and PS[0:3] information from the pins rather than from the internal copy of the CPU Status Word. The signal is driven by the system.
GLPE	Global Protect Enable	This active-high signal goes high in BPU mode following a system reset to indicate that the memory system is globally write-protected. The signal is set low by the XIO MPEN command. GPLE is inactive high when the BPU functions are disabled.
HITMISSN	Cache hit/miss	A high on this output indicates that a memory cycle is a cache hit - a low indicates a cache miss. This output goes low when ASIN is low and rises on memory cycles when a hit has been validated. This output goes high on XIO cycles.
POWER		
VDD	Power Supply	5V DC power supply input.
GND	Ground	0V reference point.

Figure 6: Pin Description Table (continued)

5.0 DC PARAMETERS - ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current through any pin except V_{DD} and GND	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 7: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.1 DC PARAMETERS - NORMAL OPERATING CONDITIONS

			Total dose radiation not exceeding 3x10^5 Rad(si)			
Symbol	Parameters	Conditions	Min	Typ	Max	Units
VDD	Supply voltage	-	4.5	5.0	5.5	V
VIH	Input high voltage	-	80% VDD	-	-	V
VIL	Input low voltage	-	-	-	20% VDD	V
VOH	Output high voltage	IOH=-5mA	VDD-0.5	-	-	V
VOL	Output low voltage	IOL=5mA	-	-	VSS+0.4	V
IIH	Input high current (Note 1)	-	-	-	10	µA
IIL	Input low current (Note 1)	-	-	-	-10	µA
IOZH	I/O tristate high current	-	-	50	-	µA
IOZL	I/O tristate low current	-	-	-50	-	µA
IDDYN	Dynamic supply current	-	-	-	50	mA
IDDS	Static supply current	-	-	0.2	10	mA

VDD=5V±10% over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not measured at -55°C

Figure 8: Operating DC Parameters

Subgroup	Definition
1	Static characteristics specified in Figure 8 at +25°C
2	Static characteristics specified in Figure 8 at +125°C
3	Static characteristics specified in Figure 8 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 10 at +25°C
10	Switching characteristics specified in Figure 10 at +125°C
11	Switching characteristics specified in Figure 10 at -55°C

Figure 9: Definition of Subgroups

6.0 TIMING PARAMETERS

	Parameter	Min	Max	Units
1	DSN falling to data bus active (XIO Read)	-	40	ns
2	DSN falling to data from MMU valid (XIO Read)	-	90	ns
3	Data valid after DSN rising (XIO Read)	10	-	ns
4	Data bus inactive after DSN rising (XIO Read)	-	45	ns
5	Address and control setups to ASIN rising	15	-	ns
6	Address and control hold after ASIN falling	5	-	ns
7	CSN setup to DSN rising (1750B) (XIO)	75	-	ns
8	CSN hold after DSN rising (1750B) (XIO)	0	-	ns
9	Data hold after DSN rising (XIO Write)	10	-	ns
10	Data setup to DSN rising (XIO Write)	5	-	ns
11	ASIN falling to EAS falling	-	30	ns
12	Extended address valid to EAS rising	5	30	ns
13	ASIN rising to EA bus valid (MMU cache hit)	-	40	ns
14	EA bus valid to PRPEN active	5	15	ns
15	ASIN rising to EA bus valid (MMU cache miss)	-	80	ns
16	ASIN rising to MPROEN active (MMU cache hit)	-	60	ns
17	ASIN rising to MPROEN active (MMU cache miss)	-	105	ns
18	ASIN rising to MPROEN active (2 cache hits)	-	60	ns
19	ASIN rising to MPROEN active (1 miss, 1 cache hit)	-	105	ns
20	ASIN rising to MPROEN active (No MMU, BPU miss)	-	50	ns
21	ASIN rising to MPROEN active (MMU and BPU miss)	-	185	ns
22	MPROEN setup to BPUVALIDN falling	5	-	ns
23	ASIN rising to GLPE falling	-	-	ns
24	RESETN falling to GLPE/MPROEN/PRPEN rising	-	-	ns
25	MPROEN valid after ASIN falling	5	-	ns
26	ASIN rising to EAS rising (XIO Cycles)	-	15	ns
27	DMAKN setup to ASIN rising	10	-	ns
28	DMAKN hold after ASIN falling	0	-	ns
29	PS[0:3] to MPROEN valid	5	40	ns
30	PRPEN hold after ASIN falling	10	-	ns

Mil-Std-883, method 5005, subgroups 9, 10 and 11

Figure 10: Timing Parameters

7.0 TIMING DIAGRAMS

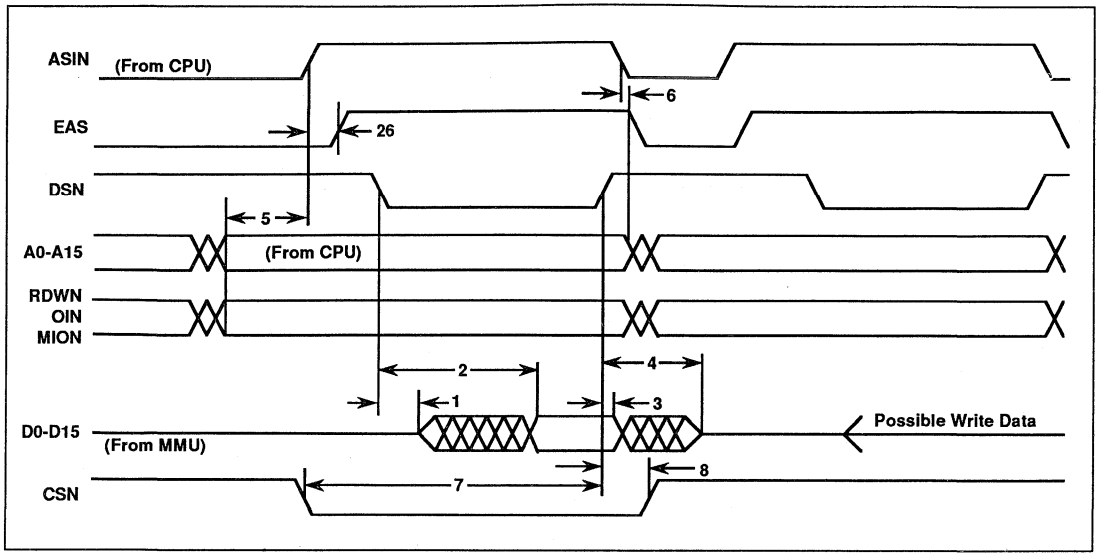


Figure 11: MA31750 XIO Read of MMU

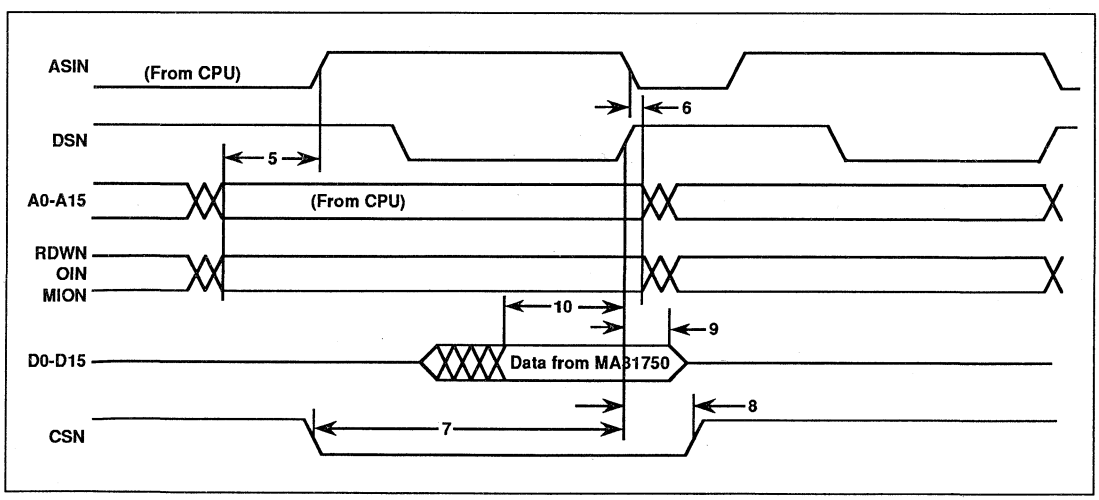


Figure 12: MA31750 XIO Write to MMU

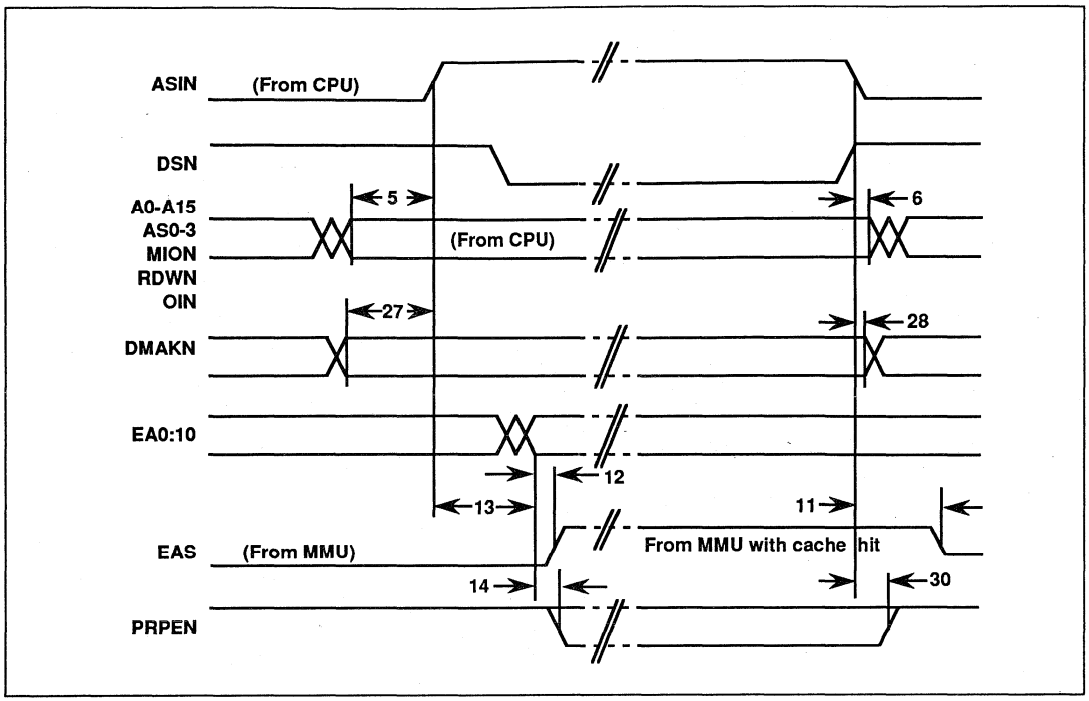


Figure 13: MMU Address Translation (Cache Hit)

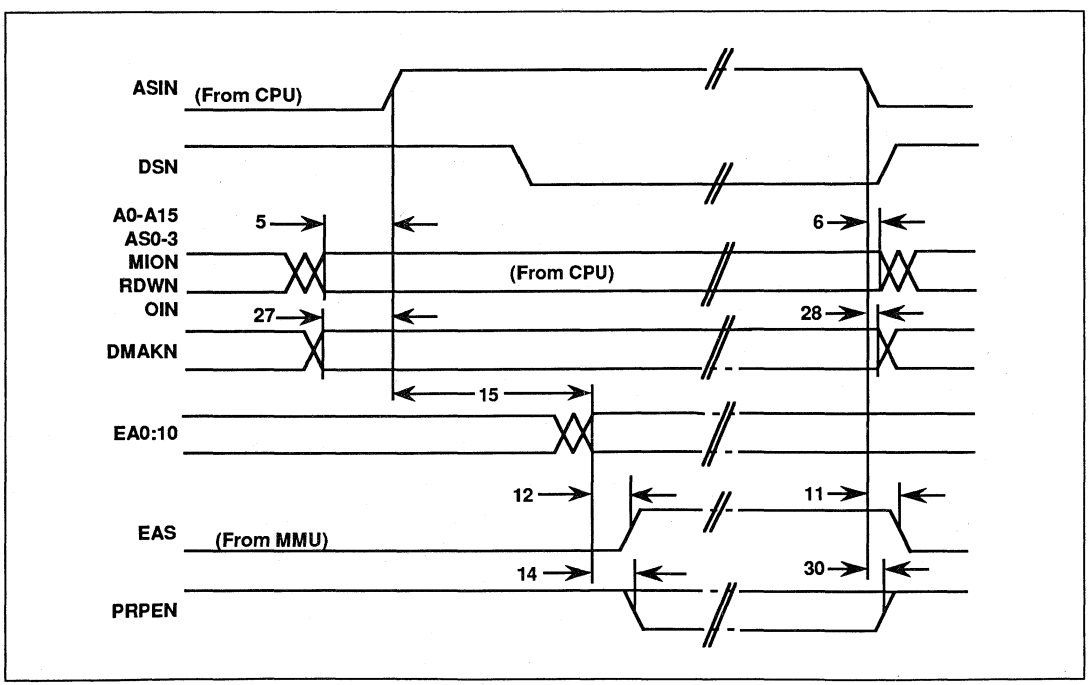


Figure 14: MMU Address Translation (Cache Miss)

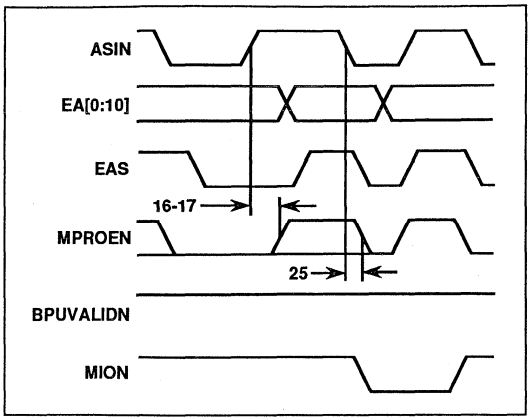


Figure 15: MMU Timing With No BPU

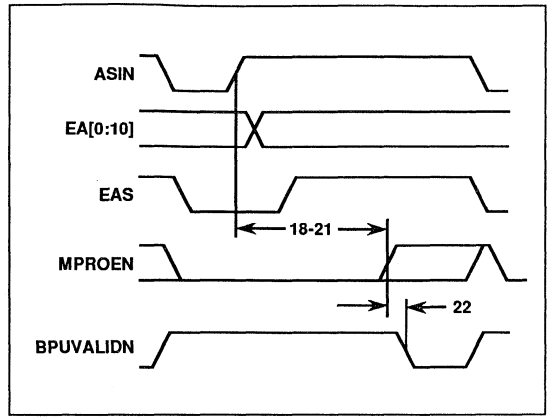


Figure 16: MMU and BPU Timings

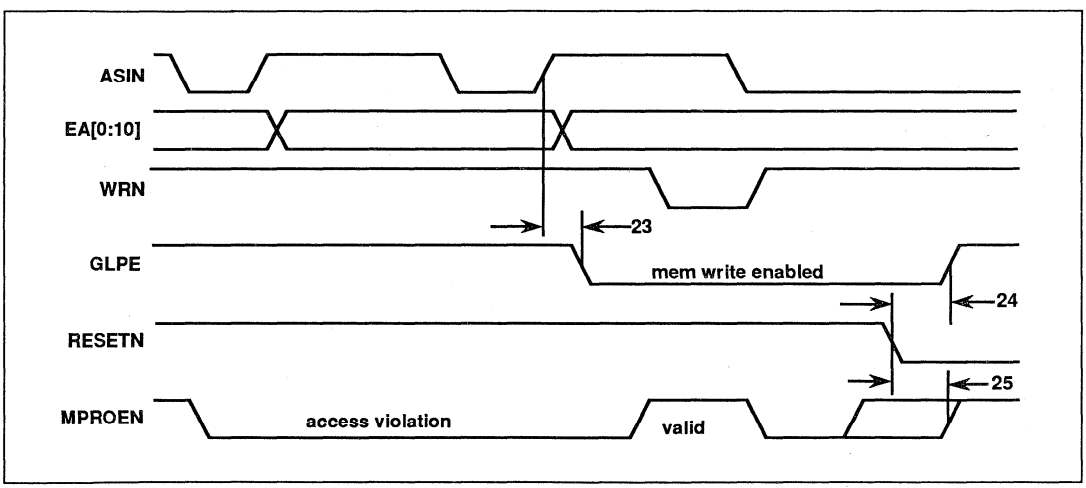


Figure 17: Reset and Enable Timings

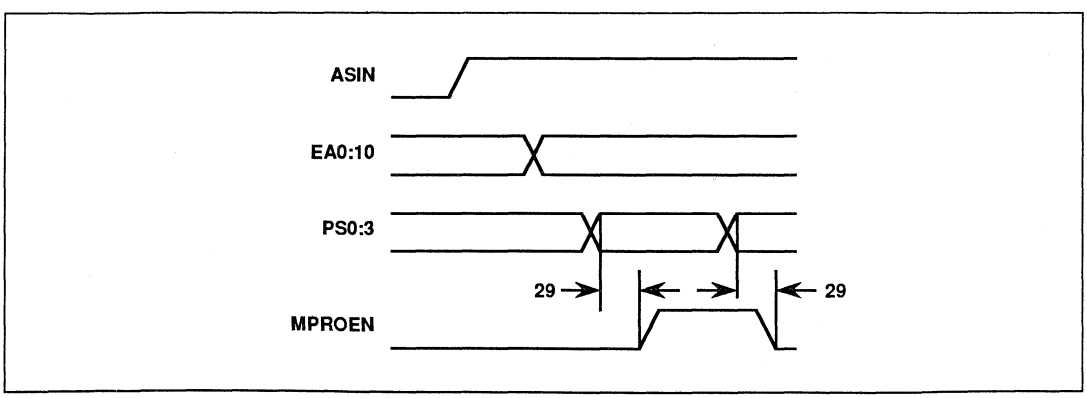


Figure 18: Processor State Timings

8.0 PACKAGING INFORMATION

8.1 FLATPACK PINOUT

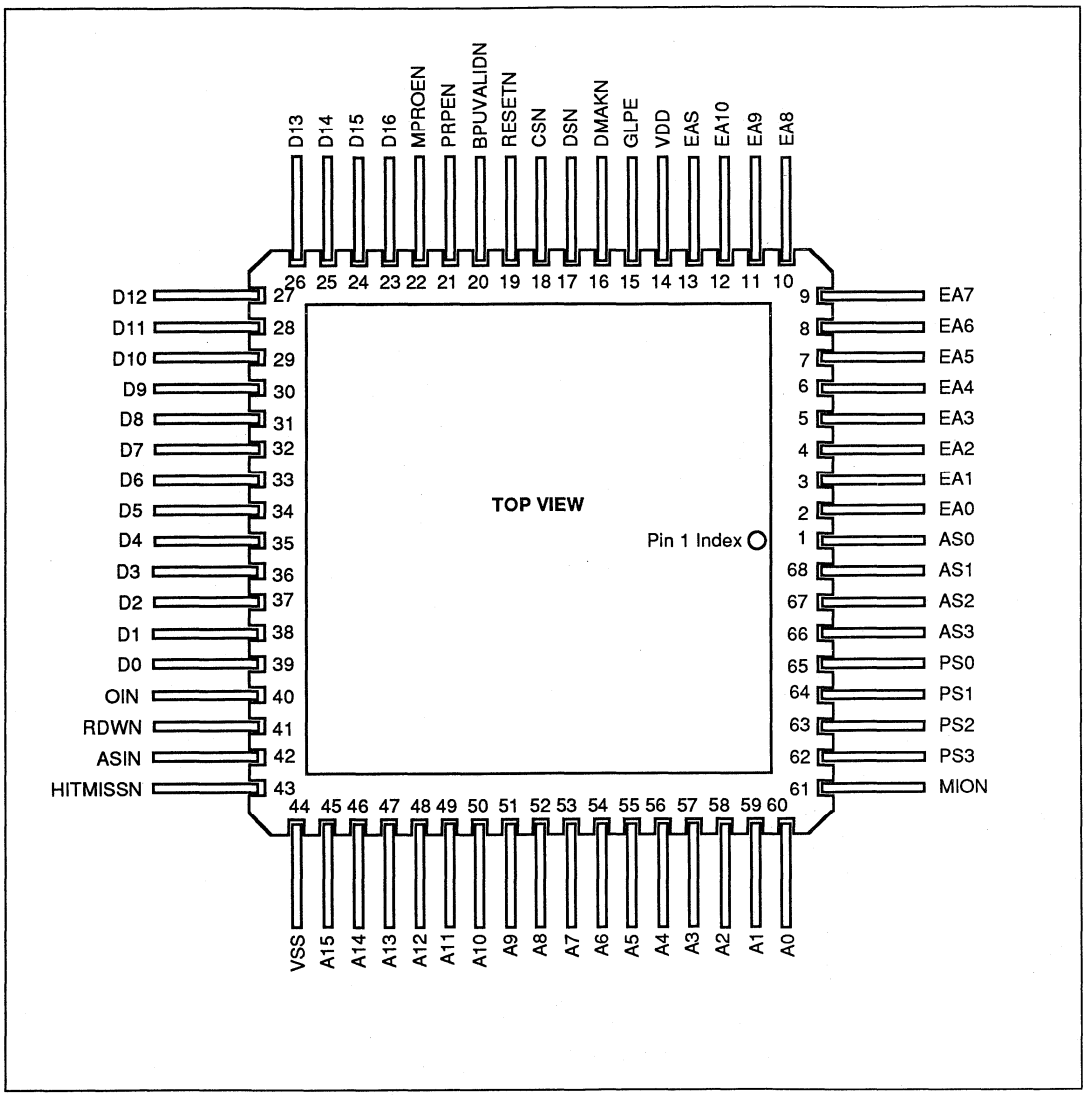


Figure 19: 68 Pin Lead Flatpack - Package Style F

8.2 FLATPACK DIMENSIONAL DRAWING

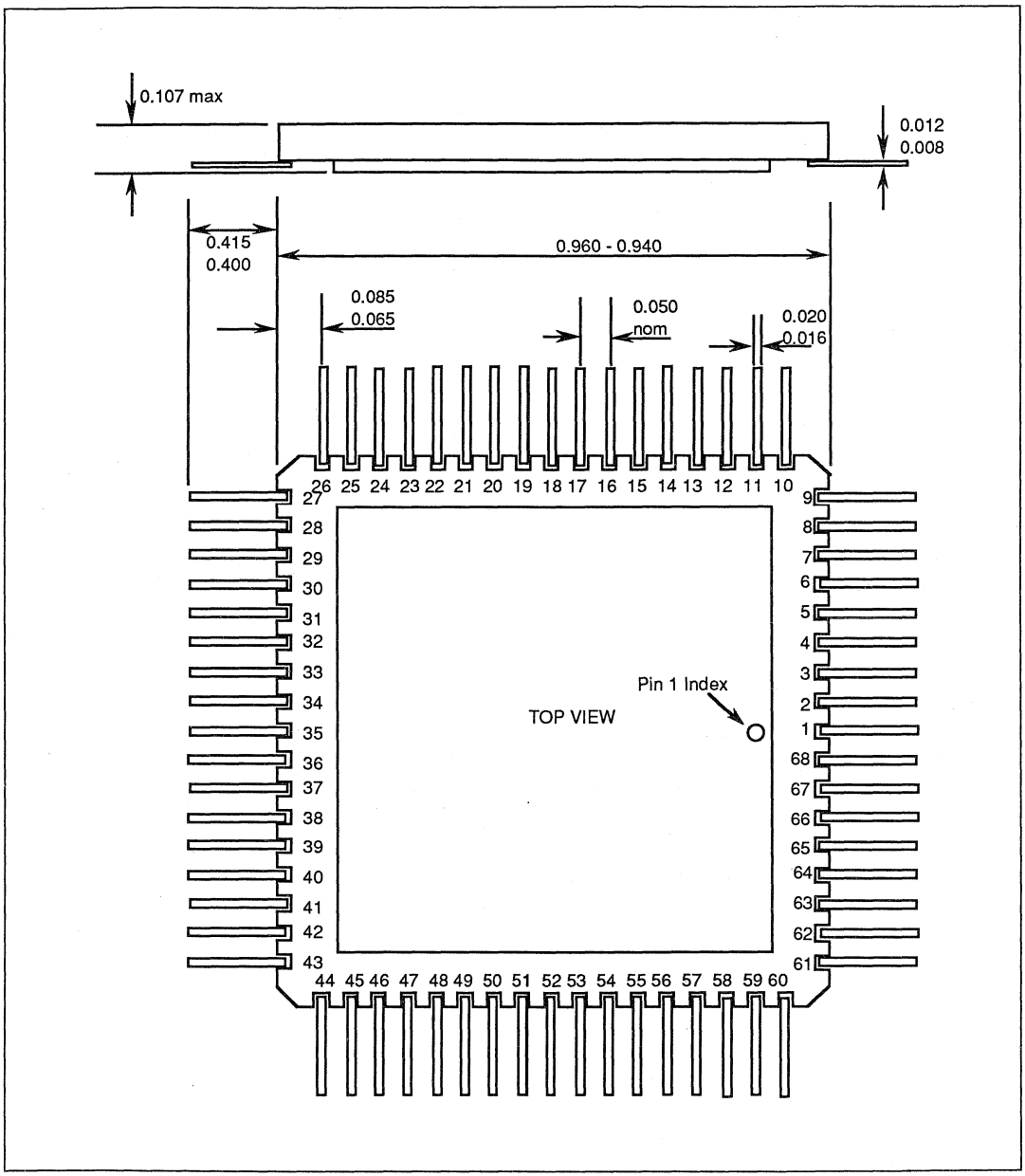
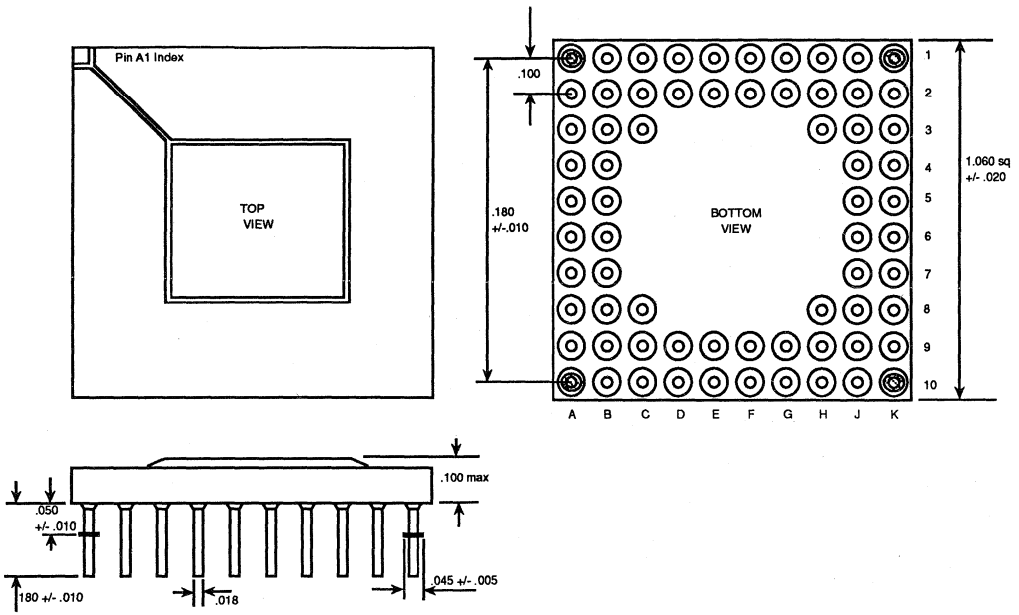


Figure 20: Dimensional Drawing of 68 Pin Lead Flatpack - Package Style F

8.3 PGA PINOUT AND DIMENSIONED DRAWING



Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	PS3	C1	PS0	G9	D7	K3	VDD
A2	A2	C2	PS2	G10	D6	K4	DMAKN
A3	A4	C3	MION	H1	EA3	K5	CSN
A4	A5	C8	GND	H2	EA6	K6	RESETN
A5	A7	C9	ASIN	H3	EA8	K7	PRPEN
A6	A8	C10	D0	H8	D12	K8	MPROEN
A7	A10	D1	AS2	H9	D10	K9	D15
A8	A12	D2	AS3	H10	D8	K10	D11
A9	A13	D9	OIN	J1	EA5		
A10	A15	D10	D1	J2	EA7		
B1	PS1	E1	AS0	J3	EA10		
B2	A0	E2	AS1	J4	GLPE		
B3	A1	E9	D2	J5	DSN		
B4	A3	E10	D3	J6	BPUVALIDN		
B5	A6	F1	EA0	J7	D16		
B6	A9	F2	EA1	J8	D14		
B7	A11	F9	D5	J9	D13		
B8	A14	F10	D4	J10	D9		
B9	HITMISSN	G1	EA2	K1	EA9		
B10	RDWN	G2	EA4	K2	EAS		

Figure 21: PGA Pinout and Dimensioned Drawing

9.0 RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request
** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 22: Radiation Hardness Parameters

10.0 OTHER INFORMATION

Reference: MA31751 Application Note 5 - Detailed Device Description.

Applications support for this and all other GPS SOS products is available now from the GPS applications support team who can be reached on:

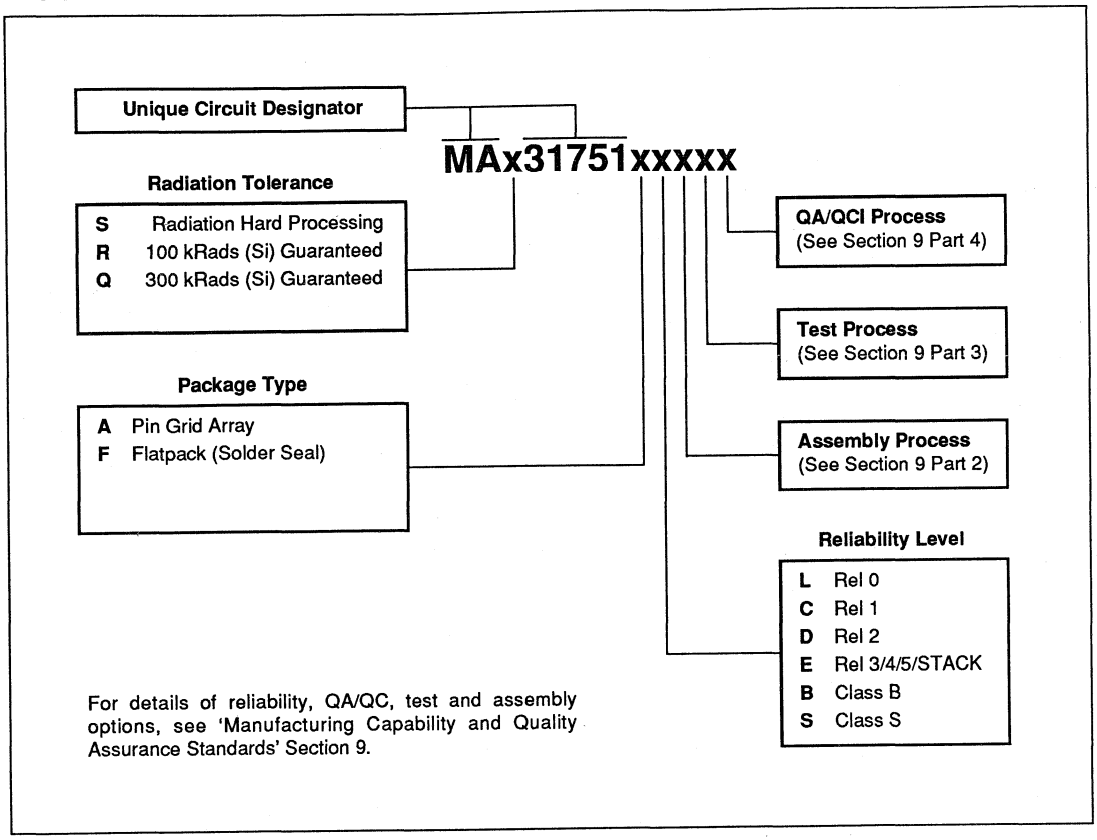
GEC Plessey Semiconductors, Lincoln Industrial Park, Doddington Rd, Lincoln, ENGLAND, LN6 3LF

Tel: (UK) 1522 502274 (direct line)
Fax: (UK) 1522 502393
E-Mail: apps@lincoln.gpsemi.com

Information on pricing and availability of all GPS SOS parts is available from GPS marketing at the same address or:

Tel: (UK) 1522 502394 (direct line)
Fax: (UK) 1522 502277

11.0 ORDERING INFORMATION



MA31751 - Application Note 5

DETAILED DEVICE DESCRIPTION

1.0 INTRODUCTION

The MA31751 is a peripheral device for the MA31750 CPU. It can function as a Memory Management Unit (MMU) and/or a Block Protection Unit (BPU). This application note will detail the internal structure of the device in order to provide a better insight into its operation. It will also provide greater detail of how the device works and should be used.

2.0 MA31751 STRUCTURE

2.0.1 Representation of MA31751 in Memory Translation Mode

Note that the AS and PS busses can come from one of two sources:

1. When the DMA has control of the system, the AS and PS input pins are read.
2. When the CPU has control of the system, the MMU gets its AS and PS values from its internal copy of the CPU status word (updated from the data bus every time the MA31751 detects an XIO address of 0x200E on the address bus).

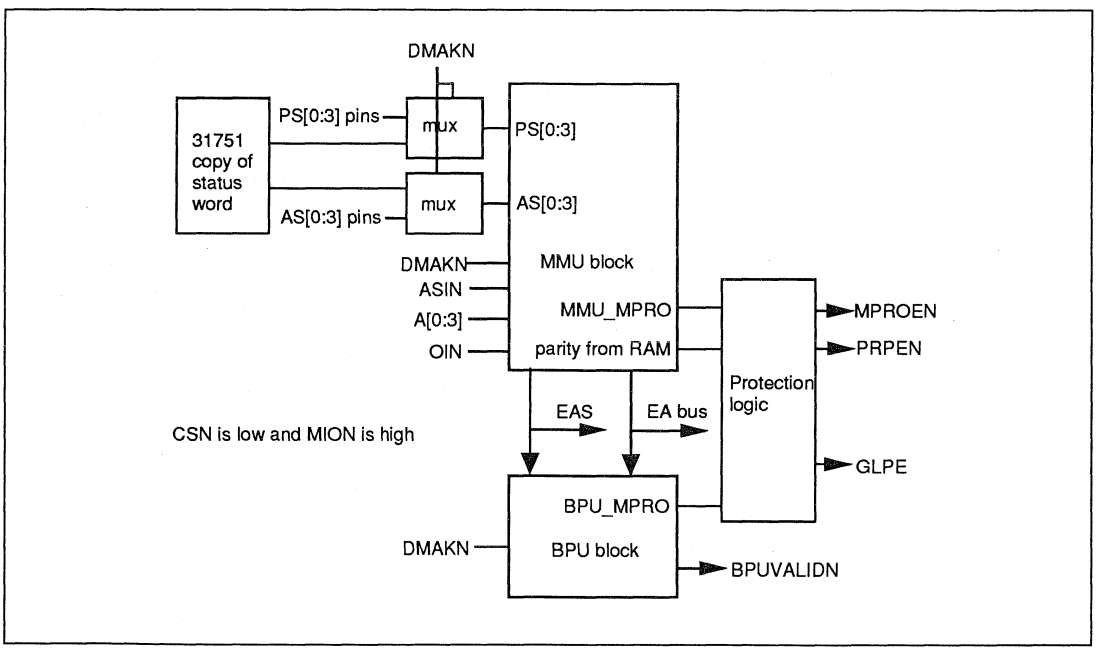


Figure 1: MA31751 in Memory Translation Mode

2.0.2 Representation of MA31751 in XIO Mode

Note that during XIO cycles, the extended address bus and strobe mimic the address bus and strobe from the processor. This enables the extended signals to be used as system signals.

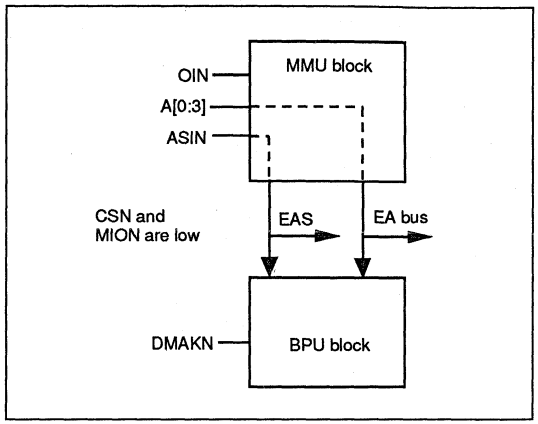


Figure 2: MA31751 in XIO Mode

2.1 THE MMU STRUCTURE

2.1.1 Memory Translation Cycles

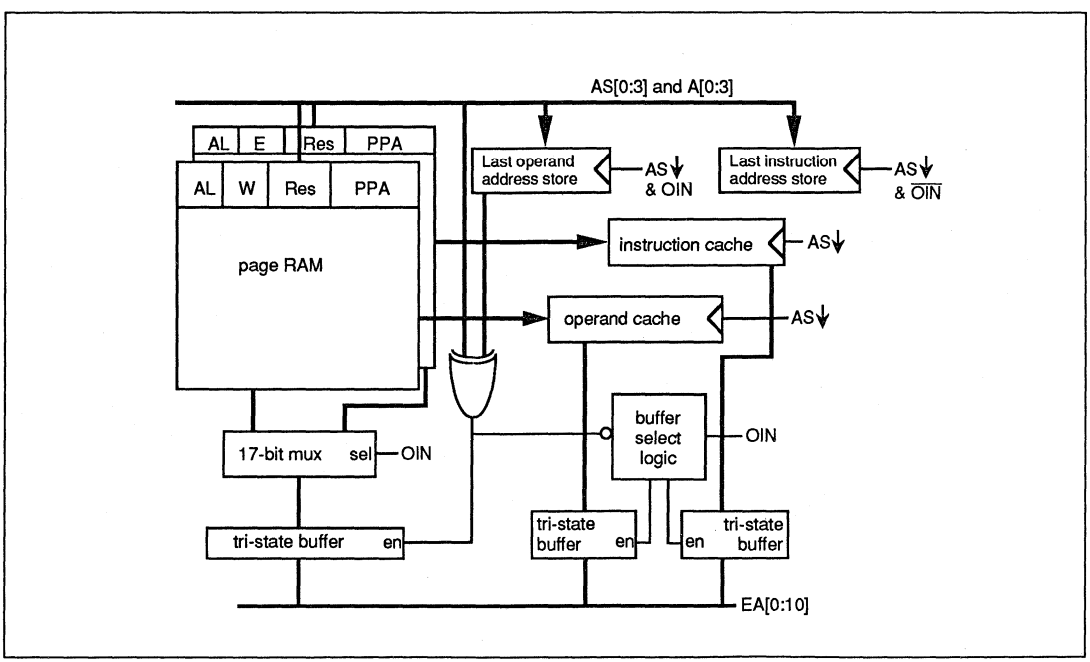


Figure 3: The MMU in Memory Translation Mode

2.1.2 MMU XIO Cycles

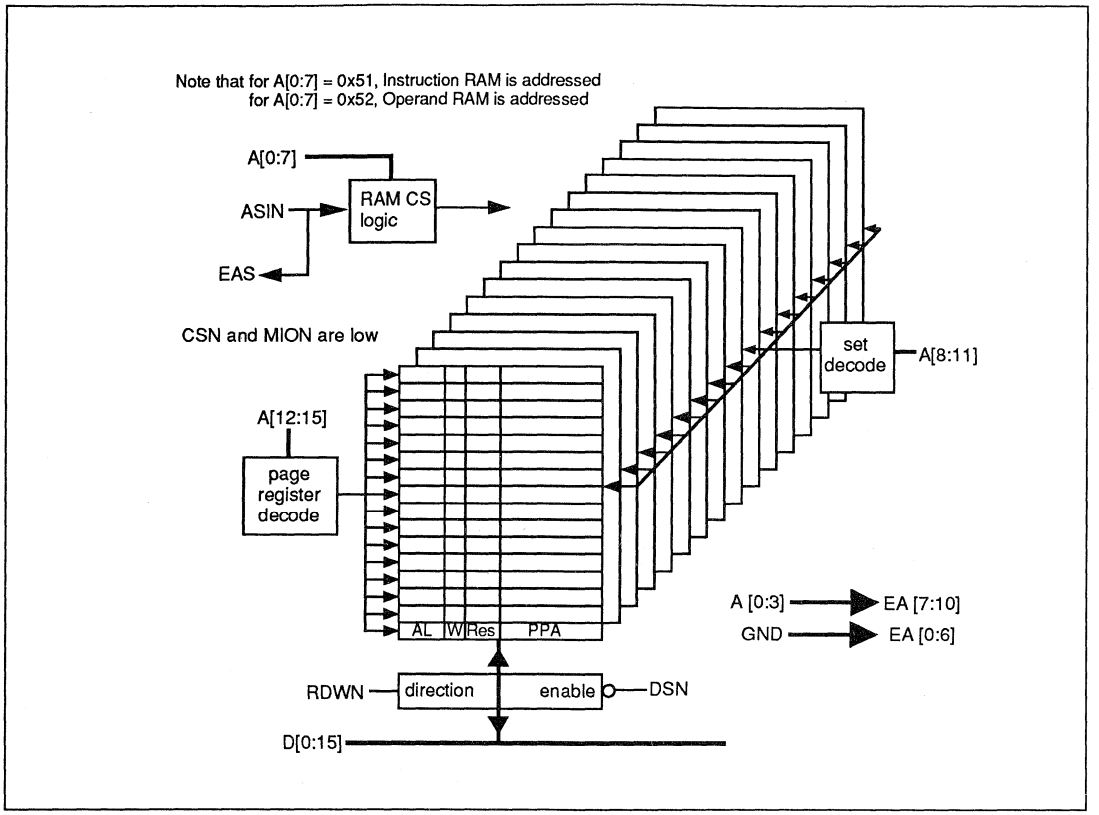


Figure 4: The MMU in XIO Mode

2.1.3 Page RAM

Each 16-bit word within the RAM of the MMU is called a page register. Each page register is made up of a 4-bit Access Lock (AL) field, a 1-bit write/execute field (W/E), a 3-bit extended address field (Res) and an 8-bit PPA (Physical Page Address) field. For a valid memory access to occur, the AL field must fit the Processor State (PS[0:3]) key and the W / E bit must be zero.

The extended address is made up of the PPA (and the Res bits in 1750B). Each page register addresses a 4K block of physical memory. Each memory location within that 4K block is addressed by the 12 least significant address bits from the CPU. The 4K block addressed is called a page.

2.1.4 Cache Memory

There is an input and an output cache on the MMU. The input cache stores the logical address from the CPU as ASIN falls at the end of each cycle. The output cache is updated with data from the RAM during each cache miss cycle (the cache register is transparent until ASIN falling at the end of the cycle). The cache hit or miss signal is generated from a bank of exclusive OR gates which compare the previous logical address in the input cache with the current logical address on the address bus. A cache miss signal is generated if a 4K page boundary has been crossed. If there is a cache hit, then the physical address can be obtained by reading the output cache register, instead of having to access the slower page RAM.

Operand and instruction space have separate caches, multiplexed with the OIN signal, so that data can be written out to one area of memory whilst the program is being executed from another, without having unnecessary cache misses. These operand and instruction caches turn into read and write caches during DMA accesses. (Since the DMA and CPU share the same physical address space, the contents of the caches will be valid.)

A cache miss is forced if there is an XIO write to any MMU page register. This ensures that the cache is always updated to reflect the updated RAM.

2.1.5 The Extended Address Output

There are tri-state buffers on the outputs of the RAM and cache registers. The buffer driving the data from the RAM onto the EA bus is enabled whenever there is a cache miss. The OIN signal is used as a RAM address bit to ensure that the correct RAM location drives the bus. If the cycle is a cache hit cycle, then OIN determines which of the cache registers output onto the EA bus. The extended address output should be combined with address bits A[4:15] from the processor to form the 20-bit address bus in 1750A and the 23 bit address bus in 1750B.

2.1.6 Page RAM Parity

During XIO write cycles to the MMU, a parity bit is written into the page RAM. This is checked only during memory read accesses. If a parity error is detected, the PRPEN output goes active low. Odd or even parity is determined by the relevant bit in the configuration word. (The CPU automatically matches the MMU parity to its own.)

2.2 THE BPU STRUCTURE

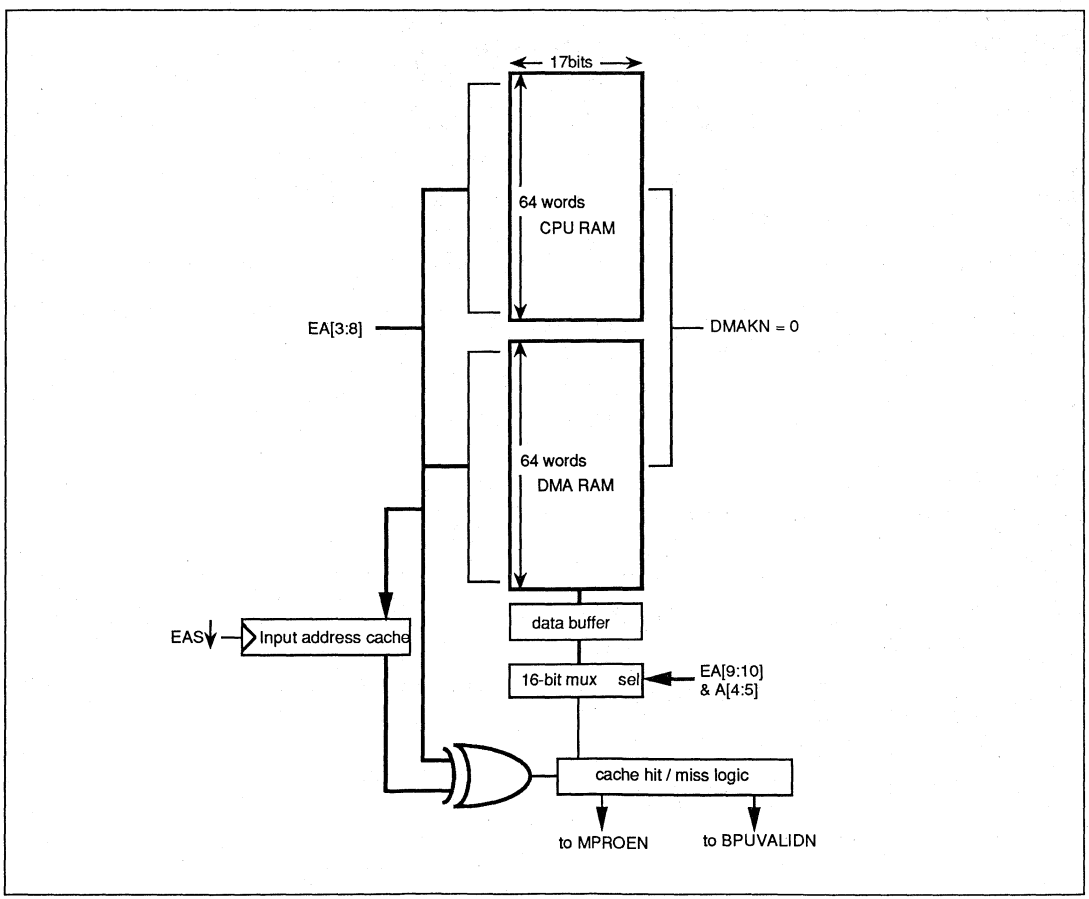


Figure 5: The BPU Structure

2.2.1 BPU RAM

The BPU RAM is arranged in 2 blocks of 64 x 17 bit words (16 bits of block protection information and 1 parity bit). The BPU uses part of the extended address bus (EA[3:8]) to address one 17-bit word. This is read into a buffer. The relevant protection bit from the choice of 16 is then selected by EA[9:10] and A[4:5]. If the protection bit is set, then the logic out of the multiplexor will be such that MPROEN will be active low when BPUVALIDN rises. Each single bit protects the memory addressed by A[6:15] from the CPU ie. each bit protects a 1K block of physical memory.

If the BPU is present in a system with no MMU, no memory expansion is available, therefore the address bus is used as the address input. In this case, A[0:1] are used to select one of the four 17-bit words and A[2:5] are used to select the protection bit from the data buffer (4x16x1K give protection for 64K of memory).

2.2.2 BPU Cache

An input caching system exists in the BPU to capture the physical address. Each extended address is latched into the cache register at the end of the cycle by EAS falling. This is compared to the extended address of the next cycle. If the next extended address is within the same 16K of memory (ie. EA[3:8] remains unchanged), then a cache hit has occurred. This indicates that the data is already valid in the data out buffer and that the BPUVALIDN signal can immediately go active. If a cache miss occurs, then the data out buffer has to be re-loaded from RAM and the cache hit/miss logic delays the BPUVALIDN signal from falling until later in the cycle. MPROEN should be qualified by the falling edge of BPUVALIDN.

2.2.3 BPU Parity

During BPU XIO write commands, the parity bit in the RAM is written by D[16] from the CPU. This parity bit is checked during system memory write accesses. If a parity error is detected, PRPEN is set active low. Odd or even parity is defined by the configuration word.

3.0 INITIALISATION

3.1 CONFIGURATION WORD TRANSLATION

In a system, the user must set up a configuration word to describe that system to the CPU. After a system reset, the CPU reads this configuration register. If the configuration word describes the presence of either an MMU or BPU, then the CPU does 16 XIO writes to address 0x0400, cycling the value on the PB[0:3] bus (but not the PB value in the status word) from 0xF to 0x0. (The CPU does 16 MMU configuration writes even if there is only one MMU present.) The PB bus should be decoded to provide the hardware chip select signals (CSN) for the MA31751 devices in the system. The MA31751 that is chip selected for that particular value of PB[0:3] snoops the address bus for the XIO address 0x0400 and then writes the data on the data bus to its own internal configuration word.

Note that if there are less than 16 MMU's implemented in the system, then 1750 specifies that the value on the PB bus is only legal up to one less than the number of MMUs present. ie. If there are 4 MMUs in the system, only PB[0:1] can be changed. Attempting to set a values of 4 to F on the PB bus results in the status word write being declared as illegal and so it is aborted.

The MA31751 configuration word definition is shown below.

Data Bit	Function	Operation
D[8]	1750A/B mode	1 = A mode
D[9]	MMU present	1 if system uses expanded memory
D[10]	BPU A[0]	BPU address select 0
D[11]	ODDPAR	1 = odd parity
D[12]	BPU A[1]	BPU address select 1
D[13]	BPUEN	1 = enable BPU function
D[14]	MMUEN	1 = address translation enabled
D[15]	BPU A[2]	BPU address select 2

Figure 6: MA31751 Configuration Word

3.2 MMU INITIALISATION

After the completion of the MMU configuration word writes, the MMU page registers must be initialised. The logical addresses from the CPU cycle through from 0x52FF (operands) and 0x51FF (instructions) to 0x5200 and 0x5100. The page registers are written with linear translations in the physical page address fields in the RAM. The remaining fields are written to the default values ie. the AL, W / E and Res fields are set to zeroes.

eg. the page register addressed by 0x52FF will be written with 0x00FF

the page register addressed by 0x512E will be written with 0x002E etc.

All of the page registers are initialised for the MMU at PB[0:3] = 0. The user must ensure that any other MMU's in the system are initialised before they are used.

3.3 BPU INITIALISATION

The BPU RAM initialises to all zeroes. One word is loaded into the RAM on each falling edge of AS. If an MMU is also present in the system, then the BPU initialisation automatically occurs during the MMU initialisation (as there are a sufficient number of active address strobes to initialise the BPU). If however, the MA31751 is set up as a BPU only, then the microprocessor runs through a routine of accessing memory address 0x0000 256 times (but without producing an active DSN signal) to generate the necessary number of AS signals.

3.4 GLPE INITIALISATION

GLPE is the GLobal Protection Enable signal. After reset, this signal is active until deactivated with the XIO MPEN (Memory Protect ENable). If any write (operand) or execute (instruction) attempt is made before this signal is deactivated, then MPROEN will be active low for that cycle.

3.2 LOGICAL AND PHYSICAL ADDRESSING

The logical address from the CPU consists of the 4-most significant address bits, A[0:3] and the address state bus, AS[0:3]. These are inputs to the MMU. During memory cycles they are translated into the physical (extended) address used to address the physically implemented memory. The physical address is output from the MMU.

During XIO cycles, the least significant bits of the extended address mimic A[0:3] so that the system receives the information from the whole CPU address bus.

4.0 MMU OPERATION

For the MMU to function, D[9] and D[14] of the MMU configuration word must be set. (When the user declares the presence of an MA31751 in the system by setting any of the relevant bits in the CPU configuration word, the CPU automatically sets D[9] and D[14] of the MMU configuration word.)

4.1 XIO MODE

When the MION signal is low, and the MMUCSN is active, the MMU snoops the address bus for addresses 0x52xx (0xD2xx) and 0x51xx (0xD1xx). When one of these addresses appears on A[0:15], then the processor is accessing the registers within the MA31751. The address mapping is shown below:

Bits	Value	Mapping
A[0:3]	5	writing register
	D	reading register
A[4:7]	2	operand space
	1	instruction space
A[8:11]		determines the set of page registers to be accessed
A[12:15]		determines the page register within the set to be accessed

Figure 7: MMU XIO Address Translation

4.2 MEMORY TRANSLATION MODE

The MMU functions as a translation device, translating the logical address from the CPU into the physical address used to address the system memory. The logical address from the CPU is made up of the address bus (A[0:15]), the address state bus (AS[0:3]), the page bank bus (PB[0:3]) and the operand/instruction signal (OIN). The PB bus is decoded into the MA31751 CSN signal and is only available in 1750B mode. The AS[0:3] bus and the OIN signal select the set of 16 page registers to be accessed. A[0:3] then select the relevant page register. The PPA is read from the page register and is used to provide 8 bits of the extended address bus. (in 1750B mode, 3 extra address bits are available from the Res field in the page register). A[4:15] access the memory location within the 4K page accessed by the selected page register.

e.g. 1. Assuming the CPU has control of the 1750A system:

a: An MMU XIO WIPR is executed.

MION = CSN = LOW.
A[0:15] = 0x513F
D[0:15] = 0x001D

b: A memory access is made.

MION = HIGH. CSN = OIN = LOW
AS[0:3] = 0x3
A[0:15] = 0xF456

The memory cycle will access page register 15 in set 3. This is the same page register that the WIPR accessed, hence the PPA is 0x1D. Therefore, the memory cycle will fetch the instruction from memory location 0x1D456.

e.g. 2. Assuming the CPU has control of the 1750B system:

a: An MMU XIO WIPR is executed.

MION = LOW.
PB[0:3] = 0x2
A[0:15] = 0x513F
D[0:15] = 0x061D

b: A memory access is made.

MION = HIGH. OIN = LOW
PB[0:3] = 0x2
AS[0:3] = 0x3
A[0:15] = 0xF456

The memory cycle will access 3rd MA31751 (whose CSN signal is an active low output from the PB bus decode). On this device, page register 15 in set 3 is accessed. This is the same page register on the same MA31751 that the WIPR accessed, hence the Res field = 6 and the PPA is 0x1D. Therefore, the memory cycle will fetch the instruction from memory location 0x61D456.

4.3 MEMORY PROTECTION BY THE MMU

The memory is protected in 2 ways by the MMU part of the MA31751. The AL[0:3] field and the PS[0:3] key must match figure 8, and the W/E bit must be zero. If either of these conditions is broken, then the MMU will keep the MRPOEN bit low whilst the CPU is trying to execute an external cycle. The CPU automatically extends the early part of the cycle (AS high, DSN high) until 2 falling edges of TCLK have occurred. The CPU will then abort the cycle, dropping AS low which will sample the active MPROEN signal into the CPU fault register.

AL Code	Acceptable PS Keys
0	0
1	0,1
2	0,2
3	0,3
4	0,4
5	0,5
6	0,6
7	0,7
8	0,8
9	0,9
A	0,A
B	0,B
C	0,C
D	0,D
E	0,E
F	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F

Figure 8: AL Code and PS Key Matching

5.0 BPU OPERATION

5.1 MEMORY PROTECTION

The BPU provides write protection on physical memory in 1K blocks. Because it protects physical memory, the protection is addressed by the extended address bus from the MMU. (If there is no MMU in the system, then there is no memory expansion and the address bus from the CPU is used as the address into the BPU).

EA[3:8] are used to address one 17 bit word from the 64 word block (16 bit data word plus one parity bit). This word drops out of the bottom of the RAM. EA[9:10] and A[4:5] are then used to select one bit of the 16 bit data word . This one bit will represent the protection on the 1K block of memory being address. (1 = write protected). If the address being accessed has the write protection bit set, then the MPROEN output from the MA31751 will be low when BPUVALIDN falls.

5.2 DMA/CPU RAM

The BPU part of the MA31751 consists of 2 blocks of RAM, each configured as 64 x 17 bit words. One RAM is the CPU protection RAM, the other is the DMA protection RAM. DMAKN is the selection signal during memory cycles. During XIO cycles, the DMA RAM has a different address range to the CPU RAM.

e.g. the LMP XIO instruction loads BPU RAM. The most significant address bits are set to 0x50. In 1750A mode the least significant address bits from 0x00 to 0x3F address the CPU RAM and from 0x40 to 0x7F address the DMA RAM.

5.3 ADDRESSING A BPU DEVICE IN IO AND MEMORY SPACE

The LMP and RMP XIO instructions respectively load and read the BPU registers. If a 16 bit data word is written to the XIO address 0x507A, then the 16 x 1K memory blocks protected by that register are at address EA[3:8] = 0x3A with DMAKN = LOW. The MSB of the BPU register protects the lowest memory address through to the LSB in the BPU register protecting the highest memory address in the 16K block. Taking D[4] as an example, this would protect memory at address EA[9:10] = 1 and A[4:5] = 0. Putting these addresses together gives that D[4] in register 7A protects the CPU memory at address 0xOE9000 to 0xOE93FF with DMAKN = LOW. This information could be read from the BPU register using the RMP command 0xD07A and examining D[4].

5.4 ADDRESSING MULTIPLE BPU DEVICES

In 1750A mode, only 1 BPU is legal in a system. However, in 1750B mode, up to 8 BPU devices can be implemented to provide block protection for 1M of memory. Each internal configuration word written to a MA31751 during initialisation has an identifying code in it for the BPU part of the device (address select bits 0:2). This informs each BPU which part of the physical memory it is protecting.

In 1750B mode, the extended address from the MMU is 11 bits wide. The 3 most significant bits (EA[0:2]) are used to address the BPU device - the BPU snoops these bits and when they match the code programmed into that device during configuration, then that BPU becomes active. The physical page address (EA[3:10]) is used in the internal BPU addressing.

The LMP and RMP XIO commands are used to access registers protecting the lowest 2M of memory

The XIO instructions used to address the extra BPU devices are LXMP and RXMP. These only become legal in 1750B mode. The following table relates the XIO commands to the physical address space that they protect:

XIO Command	XIO Address	Protected Memory Address
LMP	0x5000 - 0x507F	0x000000 - 0x0FFFFF
LMP	0x5080 - 0x50FF	0x100000 - 0x1FFFFF
LXMP	0x4D00 - 0x4D7F	0x600000 - 0x6FFFFF
LXMP	0x4D80 - 0x4DFF	0x700000 - 0x7FFFFF
LXMP	0x4E00 - 0x4E7F	0x400000 - 0x4FFFFF
LXMP	0x4E80 - 0x4EFF	0x500000 - 0x5FFFFF
LXMP	0x4F00 - 0x4F7F	0x200000 - 0x2FFFFF
LXMP	0x4F80 - 0x4FFF	0x300000 - 0x3FFFFF
RMP	0xD000 - 0xD07F	0x000000 - 0x0FFFFF
RMP	0xD080 - 0xD0FF	0x100000 - 0x1FFFFF
RXMP	0xCD00 - 0xCD7F	0x600000 - 0x6FFFFF
RXMP	0xCD80 - 0xCDFF	0x700000 - 0x7FFFFF
RXMP	0xCE00 - 0xCE7F	0x400000 - 0x4FFFFF
RXMP	0xCE80 - 0xCEFF	0x500000 - 0x5FFFFF
RXMP	0xCF00 - 0xCF7F	0x200000 - 0x2FFFFF
RXMP	0xCF80 - 0xCFFF	0x300000 - 0x3FFFFF

Figure 9: BPU XIO Address Translation

6.0 IMPLEMENTING THE MA31751 IN THE SYSTEM

The MA31751 has 3 outputs which are used by the system:

6.1 PRPEN

The PRPEN output should be gated with other system parity error signals to produce the PE fault input to the CPU.

6.2 BPUVALIDN

The BPUVALIDN output falls to indicate that the BPU output is valid. If no BPU is present, it stays high.

6.3 MPROEN

The MPROEN output behaviour is as follows:

If ASIN is low, then MPROEN is always low.

When ASIN rises, MPROEN always rises immediately on XIO cycles (ie. if MION is low)

On memory cycles (MION = high), when ASIN is high, the behaviour of MPROEN is dependant on the system configuration:

6.3.1 MMU Only

(ie. the MA31751 configuration word includes mmu_en = 1 and bpu_en = 0)

If CSN = 0, MPROEN stays low until the MMU output is valid (EAS rising).

If CSN = 1, MPROEN = ASIN.

If multiple MA31751 devices are present (a 1750B mode option) then the MPROEN outputs should be ANDed together and input to the MPROEN fault pin on the CPU. MPROEN does not need sampling on an MMU only system.

6.3.2 BPU Only

(ie. the MA31751 configuration word includes mmu_en = 0 and bpu_en = 1)

In 1750A mode, MPROEN stays low until the BPU output is valid (BPUVALIDN falling)

In 1750B mode, there can only be one BPU in a system with no MMU, therefore the BPU is always selected and MPROEN stays low until the BPU output is valid (BPUVALIDN falling)

MPROEN can be directly input to the processor in a BPU only system.

6.3.3 MMU & BPU Present

In 1750A mode,

CSN = 0, MPROEN stays low until BPUVALIDN falling.

CSN = 1, MPROEN = 0 as there is no EAS high, so there is no BPU access. (BPUVALIDN remains high)

In 1750A mode, the MPROEN output can be directly connected to the MPROEN input on the CPU.

In 1750B mode, the active MMU works seperately from the active BPU (as they may be on different devices). This may cause a glitch on MPROEN between the MMU output valid and the BPU output valid. This glitch must be avoided by qualifying the gated MPROEN outputs with any BPUVALIDN output being low.

MA31753

DMA CONTROLLER (DMAC) FOR USE IN AN MA31750 SYSTEM

The MA31753 Direct Memory Access Controller (DMAC) is a peripheral interface circuit design primarily for use with the MA31750 microprocessor. Each DMAC provides up to four independant, prioritised channels each of which can perform DMA transfers between memory and/or I/O devices using the MA31750 bus. Each channel has its own programmable internal priority and can be masked under program control. Further, individual channels have their own associated status and control words enabling an individual channel to be re-programmed without disturbing transfers which may be taking place on other channels. Three basic transfer modes are available:

Direct Memory to I/O peripheral transfers,

Direct I/O to Memory transfers,

Memory to Memory transfers,

I/O to I/O transfers.

The MA31753 interfaces directly to the MA31750 bus, directly supporting on chip parity generation and supporting expanded memory via an MA31751 MMU with either 1 MWord (1750A mode) or 16MWords (1750B mode) of logical memory.

The MA31753 uses System memory to hold address and count information for each transfer. Once this information has been prepared by the processor the DMAC can conduct a number of transfers without further processor intervention.

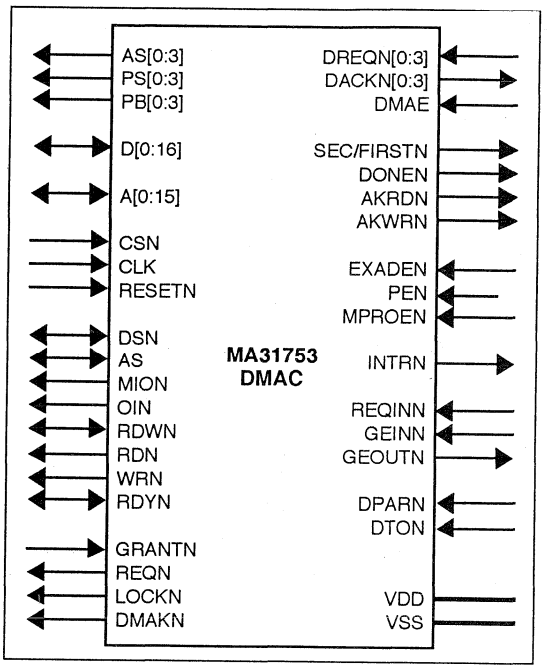


Figure 1: Pin Connections - Top View

FEATURES

- Radiation Hard CMOS SOS Technology
- Four Independant DMA Channels
- MIL-STD-1750A or B Operation in an MA31750 System
- Capable of Processor Independant Table Driven Operation
- Memory to Memory, I/O to Memory, Memory to I/O and I/O to I/O Transfers Supported
- Masking of Individual Channel DMA Requests
- Simple MA31750 Bus Interface
- Single Word, Double Word or Multi-Word Transfers for each of the DMA Channels
- Cascade Interface Allows for Channel Expansion
- Programmable Channel Priority
- Parity Checking Available

1.0 GENERAL DESCRIPTION

The MA31753 DMA controller has 4 channels from which independant transfers can be executed. These channels have programmable priorities and can be masked. They can also be enabled and disabled under software control.

The data can be transferred in several modes - single word mode, double word mode and burst mode. It can be transferred to and from both incrementing and decrementing memory and IO addressing space. The single and double word modes transfer data in 1 or 2 bus cycles when the simple handshaking mechanism is enabled.

If more than 4 channels are required, several DMA controllers can be cascaded together to give channel expansion.

Once a channel has requested a transfer, and the bus arbiter has granted bus control to the DMA, then the DMA issues an acknowledge signal to the channel to be serviced. It also pulses read or write strobes which can be gated with the channel acknowledge signal to provide read and write strobes for the requesting hardware.

DMA instructions can be programmed into memory on the DMA. The transfers defined by these instructions can be executed in sequence if they are "chained together". In this way, DMA transfers can take place continuously with data that is held in seperate memory areas.

There is software access to all internal registers. These registers have parity protection. By setting certain bits in registers, requests can be initiated for area to area transfers on channels 0 and 1. Interrupts for each channel can also be issued.

2.0 INITIALISATION

After RESETN has been removed the DMA is automatically initiated to be disabled with odd parity, the channel priority order is 0, 1, 2, 3, C (C is the cascaded input) and all channels are masked. At this point, before the DMA is used further, the DMA instructions should be programmed into the DMA internal RAM. Once all the instructions needed are in place, the common features (ie. features that apply to all channels) on the DMA can be programmed.These features should be initialised to the users requirements.

The bus parity may be changed immediately after RESETN goes inactive when the MA31750 reads the configuration word ie. When the DMA detects the XIO address 0x8410, it snoops the data bus and latches the parity bit into an internal copy. This internal copy can later be changed by writing to the DMA Mode / Status register.

The DMA enable / disable follows the DMAE input - when this input is high, the DMA device is enabled. When DMAE is low, the DMA is disabled.

The channel priority and masking can be changed by writing to the DMA Mode / Status register.

Once the common characteristics of the DMA have been set up, the DMA individual channels can be programmed. Each channel has a mode register that should be programmed with an instruction number as that channel is activated (by writing the mode word).

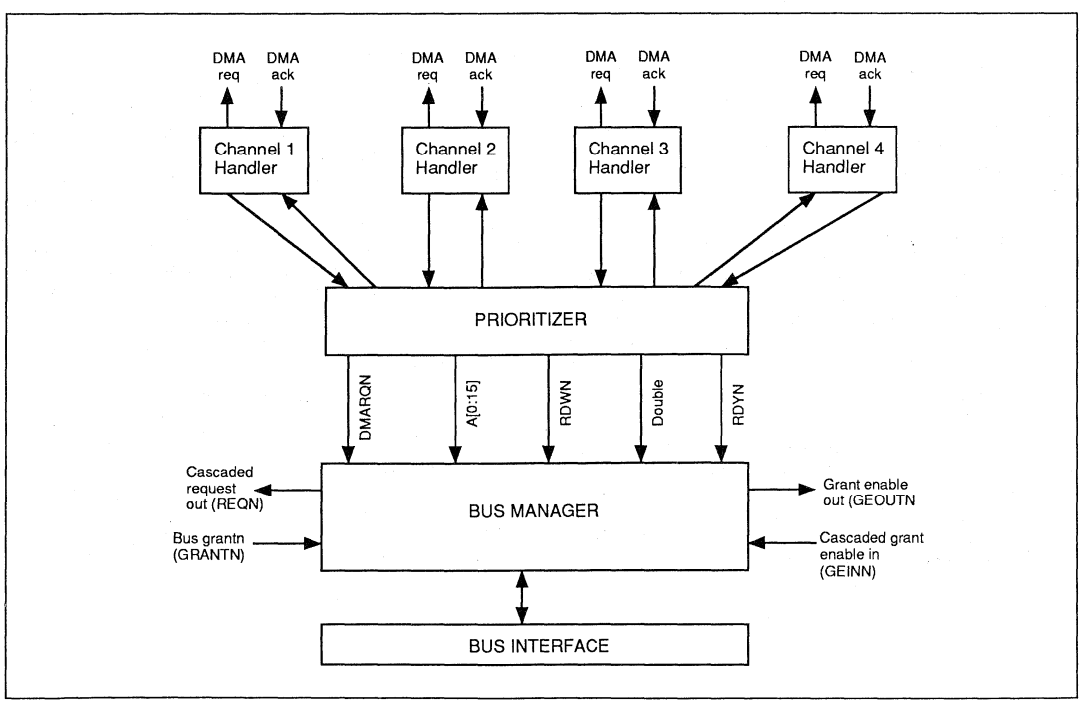


Figure 2: Block Diagram Representing the DMA Controller

3.0 DMA FUNCTIONALITY

Figure 2 shows a block diagram representing the structure of the DMA controller. This figure also shows how the DMA interfaces with the rest of the system.

Each DMA channel has 6 possible modes that it can operate in. These are as follows:

3.1 IDLE MODE

The channel goes into IDLE mode after an active hardware reset or after resetting the status flags. When in IDLE mode, the channel goes into PEND_CHAIN mode when activated by writing the Mode register. No parity check is done on this register write.

3.2 PEND_CHAIN MODE

Once the channel has been activated, it goes from IDLE to PEND_CHAIN mode. In this mode, the first instruction is read (all 8 words). If a parity error is detected, the channel goes to the ERROR mode. If the read is successful, the channel will stay in the PEND_CHAIN mode until either an active request is received or the Channel Request Pending bit is set in the Channel Status Register. At this time, the channel progresses to the PEND_REQ mode.

3.3 PEND_REQ MODE

In this mode, the Mode / Link word is checked to make sure it doesn't de-activate the channel (sending the device back to IDLE mode). If the channel remains active, the device sits in PEND_REQ mode until the system bus arbiter grants the DMA bus control. Once this occurs, the transfer commences and the DMA enters TRANSFER mode.

3.4 TRANSFER MODE

If at any time during the transfer an error occurs, the channel is set into ERROR mode. If the transfers are clean of errors, then the behaviour of the device is dependant on the type of transfer mode that was programmed by the currently executing instruction.

3.4.1 Single/Double Word and External Area to Area Mode

Within these modes, the DMA executes each data transfer seperately, ie. between each single / double word transfer, the request is removed. The DMA goes back into PEND_REQ mode after each transfer and waits for the next request to be granted.

3.4.2 Burst Area to Area Mode

With this type of transfer, the DMA transfers data whilst the bus control is granted. The channel request signal remains active. When control is removed by the arbiter, the device sits in the PEND_TRANS mode until re-granted. If the burst mode is area to area with interval timing, then between each transfer, the channel has to count the interval.

Once a transfer has completed, the channel either sets the EOT bit and sits waiting for this to be reset before it goes back into INIT mode, or the instruction is chained and the channel jumps back to the PEND_CHAIN mode where it can read the next instruction details for the next transfer. If during any transfer mode, the channel is de-activated, the channel goes back to INIT mode. If at any time, an error is detected, the device goes into ERROR mode.

3.5 ERROR MODE

This mode is entered from the PEND_CHAIN mode if a parity error is detected during the instruction register reads. The error mode can also be entered from theTRANSFER mode. This can happen if PEN, MPROEN or EXADEN are activated by trying to access one of the data transfer addreses. An interrupt is generated in this mode. The only way to leave this mode is to reset all the error flags.

3.6 WORD TRANSFER MODES

It is possible to run each channel in single, double, and burst mode transfers.

3.6.1 Single Word Transfer

In single word transfer mode, the generation of each request on a channel causes the DMA controller to issue an external request that lasts for one bus cycle. The request is de-activated before the end of the bus cycle to allow other users to aquire bus control. If the transfer is to or from a device needing longer than one machine cycle (2 CLK cycles) then the cycle can be extended using handshaking of the DMA request and acknowledge lines.

3.6.2 Double Word Transfer

In double word mode, each request on a channel causes the DMA controller to request bus control for 2 machine cycles to allow the transfer of 2 16-bit data words. The data is transferred to consecutive addresses and the bus is locked between each word transfer to protect the transfer. The most significant word to be transferred has the lowest address and is transferred first (following the 1750 standard). The request is de-activated before the end of the second bus cycle to allow other bus users to take control. If an extended cycle is needed, the handshaking mechanism doesn't word in this mode and the RDYN signal must be kept high for as long as required.

3.6.3 Burst Mode

In burst mode, one request to the channel causes the DMA to request bus control for a complete block of data to be transferred. The DMA de-asserts the request line on the last transfer cycle to allow other users to take bus control. Consequently, if the transfers are chained together, the CPU may be able to get bus control between 2 blocks of data transfer. If extended bus cycles are needed, the RDYN mechanism can be used (handshaking does not work in this mode).

3.6.4 Area to Area Mode

In area to area mode, the transfers can be initiated either by external requests or internally generated by the DMA depending on the value in the interval timer (the software generated requests controlleed by the interval timer can only be used on channels 0 and 1). Each request makes the DMA request bus control for 2 machine cycles. The transfers can take place to and from IO and / or memory depending on how the instruction programs the channel. The DMA de-asserts the request during the second cycle unless the instruction has programmed the channel to do "Continuous Internal Request". In this case, the request is only de-asserted on the last cycle of the block. If extended bus cycles are needed, the RDYN mechanism must be used as the handshaking does not work in this mode.

3.6.5 Instruction Chaining

When the first request is received on a channel, it accesses the DMA instruction number that is programmed in the mode word. This instruction is read from internal DMA RAM. This takes 16 CLK cycles (as there are 8 16-bit word in the instruction). Bus control is not needed during these internal RAM accesses. At the end of the 16 CLK cycles, the channel has all the transfer information it needs and can begin to transfer whenever it is granted bus control. Once the transfer has completed, the channel checks that it is in chaining mode and that the instruction is a chained instruction. If so, then as the first instruction completes, the DMA can access the next instruction (again taking 16 CLK cycles) and the transfers can continue as bus control is granted.

3.6.6 Handshaking Mechanism

There is a handshaking mechanism available when using single-word transfer mode. It works as follows:

For a memory read cycle:

1: The IO port issues a request.
2: The DMA requests and is granted bus control. The DMA starts a memory read cycle. As well as the usual control and strobes, the DMA also asserts the DACKN low for the channel that it is responding to. The DACKN signal acts as an IO port select.
3: Once valid data is available on the data bus ie. RDYN has gone low, the DMA asserts AKWRN low. The IO port uses AKWRN as a write strobe.
4: The IO port acknowledges the completed data read by de-asserting DREQN.
5: When the DMA sees DREQN has gone high, it de-asserts DACKN. At this time, the data is still valid and the IO port may latch the data on AKWRN rising or any time in between.
6: The DMA completes the cycle by de-asserting strobes etc.
7: The wait state generator finally de-asserts RDYN.

For a memory write cycle:

1: The IO port issues a request.
2: The DMA aquires bus control and starts a memory write cycle, also asserting DACKN for the relevant channel.
3: The data bus is driven by the IO port. Valid data is available when the IO port de-asserts DREQN. (DACKN is still asserted so valid data must still be driven on the bus).
4: When the DMA senses DREQN high, it writes the valid data from the IO port into memory.
5: The memory write is completed when RDYN goes low.
6: The DMA de-asserts DACKN and hence the IO port stops driving the data bus.

If DREQN is de-asserted 2 or more CLK cycles before AKRDN or AKWRN are asserted, then the handshaking protocol does not apply and the cycle will simply use the RDYN signal going low to terminate the cycle (both AKRDN and AKWRN will rise as AS falls at the end of the cycle).

3.7 INTERRUPT GENERATION

The DMA shall generate an interrupt on the occurrance of any of the following:

- A channel has reached an "End of Transfer" condition and the EOT bit has been set in the channel status register.
- A channel has been stopped because
  a) a bus timeout has occurred. (ie. either DREQN (handshake mode) or RDYN is asserted for more than 256 CLK cycles)
  b) an internal parity error was detected when reading a DMA register with parity.
  c) An odd block length was programmed in double word mode.

The DMA will stop but will not generate an interrupt if EXADEN, MPROEN or PEN are active at the end of an external cycle.

If a parity error is detected whilst writing to the DMA registers, the erroneous write will not let transfers commence. The DMA generates interrupts by pulsing INTRN low. If more than one error occurs simultaneously, INTRN is only pulsed once. The interrupt can only be generated when the DMA is in the ERROR mode. The only way to get out of this mode is to reset all error flags.

3.8 CHANNEL MASKING AND STOPPING

Each channel can be masked individually by setting the relevant bit in the DMA Mode / Status register. If the channel is masked, only external requests are gated out - software requests are still serviced.

Each channel can be stopped by de-activating the channel by writing the Channel Mode register. This register can only be written whilst in PEND_CHAIN mode or awaiting bus control. Once the channel is de-activated, it returns to the IDLE mode.

3.9 PARITY CHECKING

Parity checks are done when DMA registers are being written and when they are being accessed ie. when the instructions are being read.

3.10 SOFTWARE PROGRAMMING

DMA requests can be generated in software by writing the CRQP bit in the Channel Status register. If the channel is active, the DMA will then request bus control. If the DREQN signal on that channel is not active, the DMA finishes the cycle as soon as the memory is ready. There is no handshaking with the IO port. DACKN is deasserted when the memory is ready. If DREQN is asserted but is masked, the handshaking is active and operates normally.

Interrupts can be generated in software by setting either a channel EOT flag or any error flag. This can only be done when the DMA is in PEND_CHAIN mode. If an error flag is set, the device goes straight to ERROR mode. If the EOT flag is set, the device looks as if it has completed the transfer. It will then just sit and wait for the EOT flag to be cleared before entering IDLE mode. If both flags are set simultaneously, the device remains in PEND_CHAIN mode. Setting an error flag when EOT is set resets EOT and the device goes to ERROR mode. Setting EOT when an error flag is set clears the error and the DMA sits in the finish transfer mode.

3.11 CASCADING DMA CONTROLLERS

DMA controllers are cascaded in series. For each DMA added, an extra 4 channels become available. To cascade the devices, the strobes, control signals and address and data busses are connected in parallel. Of the bus arbitration signals, LOCKN and GRANTN should be connected in parallel and REQINN, GEINN and GEOUTN shoudl be daisy-chained. INTRN and PEN can either be ORed together with external glue logic or input to seperate CPU interrupts. Figure 3 shows the cascade connections.

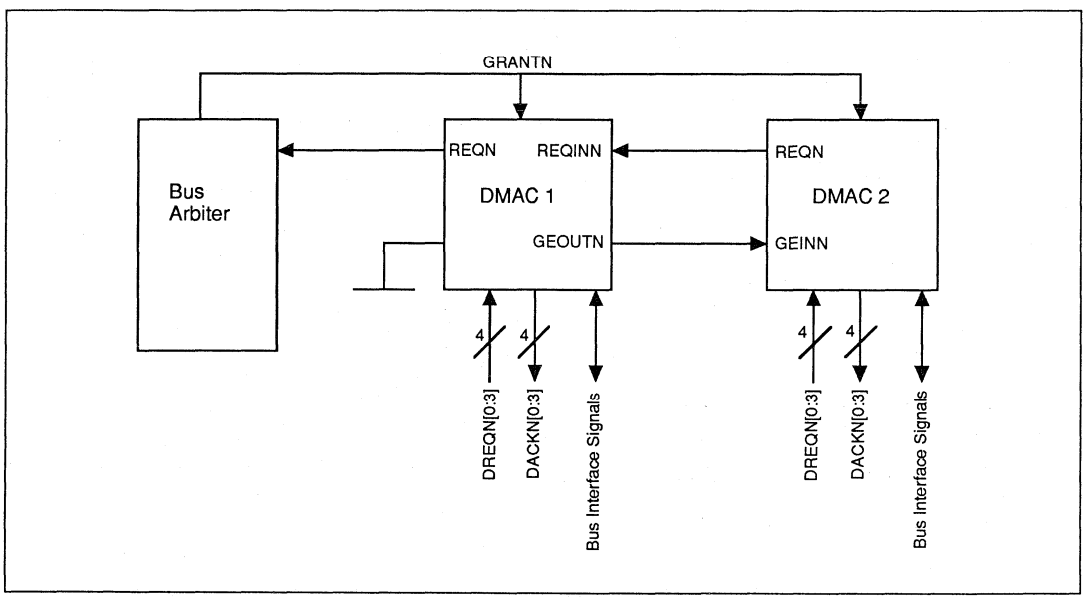


Figure 3: Cascading DMA Controllers

4.0 DETAILED REGISTER DESCRIPTION

The internal registers on the DMA controller can be located in either memory or IO addressing space. 32 words are control registers and 480 words are the DMA instruction registers.

The address lines A[7:15] are used to decode the registers. (A[0:6] are decoded to generate CSN low ie. the user can place the DMA on the address map.)

A[7:15]	Register Content	Parity
0	DMA Instruction	Yes
.	.	.
.	.	.
1DF	DMA Instruction	Yes
1E0	Channel 0 Mode	No
1E1	Channel 0 Remaining words	No
1E2	Channel 0 Area 1 current address	No
1E3	Channel 0 Area 1 current PB/AS/PS	No
1E4	Channel 0 Area 2 current address	No
1E5	Channel 0 Area 2 current PB/AS/PS	No
1E6	Channel 0 Status	No
1E7	DMA Mode / Status 1	No
1E8	Channel 1 Mode	No
1E9	Channel 1 Remaining words	No
1EA	Channel 1 Area 1 current address	No
1EB	Channel 1 Area 1 current PB/AS/PS	No
1EC	Channel 1 Area 2 current address	No
1ED	Channel 1 Area 2 current PB/AS/PS	No
1EE	Channel 1 Status	No
1EF	RESERVED	No
1F0	Channel 2 Mode	No
1F1	Channel 2 Remaining words	No
1F2	Channel 2 Area 1 current address	No
1F3	Channel 2 Area 1 current PB/AS/PS	No
1F4	Channel 2 Area 2 current address	No
1F5	Channel 2 Area 2 current PB/AS/PS	No
1F6	Channel 2 Status	No
1F7	RESERVED	No
1F8	Channel 3 Mode	No
1F9	Channel 3 Remaining words	No
1FA	Channel 3 Area 1 current address	No
1FB	Channel 3 Area 1 current PB/AS/PS	No
1FC	Channel 3 Area 2 current address	No
1FD	Channel 3 Area 2 current PB/AS/PS	No
1FE	Channel 3 Status	No
1FF	RESERVED	No

4.1 MODE REGISTERS

CA read 0: channel not active
write 0: stop channel
read 1: channel active
write 1: start channel
This bit will be set low at an error or EOT condition

Mode 000: Single Word
001: Double Word
010: Burst Mode
011: Not used (channel not started)
100: Area to Area, Memory to Memory
101: Area to Area, Memory to IO
110: Area to Area, IO to Memory
111: Area to Area, IO to IO

A1M Area 1 Mode
For single, double and burst modes
00: Read from memory, incrementing address
01: Read from memory, decrementing address
10: Write to memory, incrementing address
11: Write to memory, decrementing address

Area to area mode
00: Area 1 address constant
01: Area 1 address incrementing
10: Area 1 address decrementing
11: Area 1 address constant

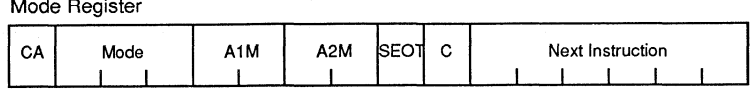
A2M Area 2 Mode (only used in area to area mode)
00: Area 2 address constant
01: Area 2 address incrementing
10: Area 2 address decrementing
11: Area 2 address constant

SEOT 0: Signal 'End of Transfer' at end of current block only of C=0
1: Always signal 'End of Transfer' at end of current block.

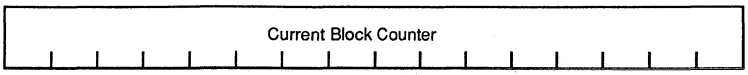
C read 0: Perform no chaining
read 1: Perform chaining using the value of "next Instruction" field as pointer
write 0: Perform no chaining even if defined by current DMA instruction
write 1: Perform chaining as defined by current instruction

Next Inst These 6 bits point to one of the 60 DMA instructions ie. the next instruction to be executed.
If the number is 3C, 3D, 3E or 3F, then the transfer will stop with the current block (ie. no chaining)

Mode Register

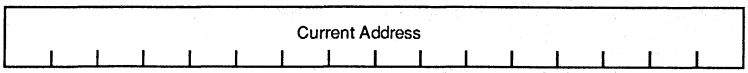


4.2 REMAINING WORD REGISTERS



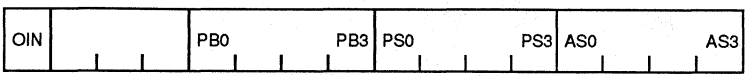
Read access only. These 16-bit registers store the number of words left to be transferred for each area.

4.3 CURRENT ADDRESS REGISTERS



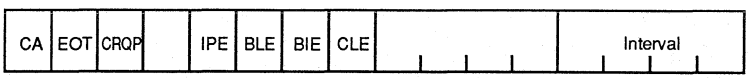
Read access only. These 16-bit registers store the addresses of the current words to be transferred to / from the area represented by the register.

4.4 CURRENT PB / PS / AS REGISTER



Read access only. These 16-bit registers store the current page bank, address and process state information for each area. When the areas have been selected within the IO space, PB, PS and AS shall be zero.

4.5 STATUS REGISTERS



CA 0: Channel not active
1: Channel active
This bit is automatically set to zero at an error or EOT condition.

EOT 0: Channel EOT not reached
1: Channel EOT reached.

CRQP 0: No channel DMA request pending.
1: Channel DMA request pending.
It is not possible to reset this bit as long as a DREQN line is asserted.

IPE 0: No internal parity error
1: Internal parity error when reading DMA register with parity.

BLE 0: No error
1: Block length error (odd block length in double word mode)

BIE 0: No error
1: Bus interface timeout error (caused either by not deasserting DREQN in handshake mode or by a bus timeout)

CLE 0: No error
1: CPU latched error (either MPROEN, EXADEN or PEN)

Interval The interval, in CLK cycles, between each DMA request generated during area to area transfers.

4.6 DMA MODE / STATUS 1

M3	M2	M1	M0	EOT3	EOT2	EOT1	EOT0	ERR	A/B		BP	DMAE	Priority
D0													D15

Mn 0: Channel n not masked
1: Channel n masked

EOTn 0: Channel n "End of Transfer" not reached
1: Channel n "End of Transfer" reached
Read access only. Value can be changed by writing the channel status register.

ERR 0: No error detected
1: Error detected in one or more of the channels
Read access only. Value can be changed by writing the channel status register.

A / B 0: 1750A mode
1: 1750B mode

BP 0: Even bus parity used
1: Odd bus parity used

DMAE 0: DMA requests disabled
1: DMA requests enabled
Read access only

Pri 000: Channel priority 0, 1, 2, 3, C
001: Channel priority 1, 2, 3, 0, C
010: Channel priority 2, 3, 0, 1, C
011: Channel priority 3, 0, 1, 2, C
100: Channel priority C, 0, 1, 2, 3
101: Channel priority C, 1, 2, 3, 0
110: Channel priority C, 2, 3, 0, 1
111: Channel priority C, 3, 0, 1, 2

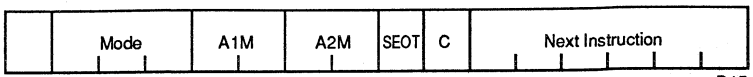
5.0 DMA INSTRUCTIONS

60 DMA instructions are present in the memory or IO space between A[7:15] = 0 and A[7:15] = 1DF. Each DMA instruction comprises of 8 16-bit words. The base address for each instruction is 8*n where n is the instruction number. The instructions are structured as below:

Word number	Content
0	Mode/Link word
1	Block length
2	Area 1 base address
3	Area 1 PB, PS and AS
4	Area 2 base address
5	Area 2 PB, PS and AS
6	Transfer interval
7	Not used

Words 4, 5 and 6 are used only during area to area mode transfers. Word 6 can only be used for channels 0 and 1.

5.1 MODE / LINK WORD



Mode
- 000: Single word
- 001: Double word
- 010: Burst mode
- 011: not used (channel not started)
- 100: Area to Area, Memory to Memory
- 101: Area to Area, Memory to IO
- 110: Area to Area, IO to Memory
- 111: Area to Area, IO to IO

A1M Area 1 Mode

For single, double and burst modes
- 00: Read from memory, incrementing address
- 01: Read from memory, decrementing address
- 10: Write to memory, incrementing address
- 11: Write to memory, decrementing address

Area to area mode
- 00: Area 1 address constant
- 01: Area 1 address incrementing
- 10: Area 1 address decrementing
- 11: Area 1 address constant

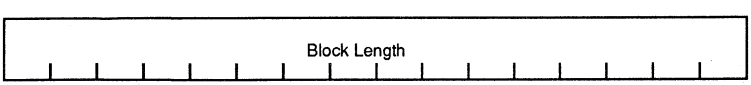
A2M Area 2 Mode (only used in area to area mode)
- 00: Area 2 address constant
- 01: Area 2 address incrementing
- 10: Area 2 address decrementing
- 11: Area 2 address constant

SEOT
- 0: Signal 'End of Transfer' at end of current block only of C=0
- 1: Always signal 'End of Transfer' at end of current block.

C
- read 0: Perform no chaining
- read 1: Perform chaining using the value of "next Instruction" field as pointer
- write 0: Perform no chaining even if defined by current DMA instruction
- write 1: Perform chaining as defined by current instruction

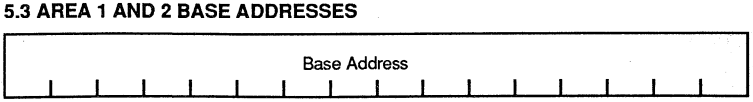
Next Inst These 6 bits give the number of the next instruction to be executed. If the number is 3C, 3D, 3E or 3F, then the DMA transfers will stop with the current block.

5.2 BLOCK LENGTH



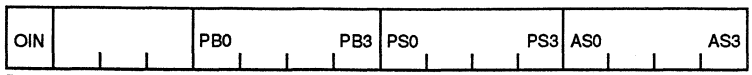
This readable and writable 16-bit word gives the number of words to be transferred for the current DMA block.

5.3 AREA 1 AND 2 BASE ADDRESSES



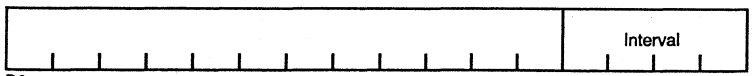
These registers hold the addresses of the first word of memory or IO to be transferred (ie. when the channel is decrementing the address, this register holds the highest address to be transferred.)

5.4 AREA 1 AND 2 PB, PS AND AS



These readable and writable registers store the Page Bank, Processor and Address State information to be used when accessing areas 1 and 2. When areas are defined within IO space, PB, PS and AS are set to zero.

5.5 TRANSFER INTERVAL



This readable and writable register gives the number of CLK cycles between each DMA request generated during area to area transfers. The number entered as the interval value corresponds to a clock cycle interval increasing by 32 as follows:

0	=>	- (externally triggered DMA requests)
1	=>	0 (continuous DMA requests until the block is completed.
2	=>	32
3	=>	64
4	=>	96
..	..	..
14	=>	416
15	=>	448

This function is valid only for transfers on channels 0 and 1. Channels 2 and 3 work ony only on externally triggered requests.

5.6 CONFIGURATION WORD

The DMA controller snoops the system address bus for the XIO address 0x8410. When this appears, the DMA stores the data bus (qualified by DSN low) in an internal copy of the CPU configuration word.

6.0 PIN DESCRIPTIONS

A[0:15]	I/O	A[0] is the most significant bit of this logical address bus. This bus is an input during cycles not assigned to the DMA and is driven during DMA cycles.
PB[0:3]	O	Used in 1750B mode only, this bus provides DMA page bank information which addresses up to 8M of memory. The bus is tri-stated during cycles not assigned to the DMA.
AS[0:3]	O	This bus indicates the current address state of the DMA controller. It is tri-stated during cycles not assigned to the DMA.
PS[0:3]	O	This bus indicates the current process state of the DMA controller. It is tri-stated during cycles not assigned to the DMA.
D[0:16]	I/O	D[0] is the most significant bit of the data bus. During DMA cycles, data is input on read cycles and output on write cycles. D[16] is the parity bit. Odd or even parity is set in the configuration word. Parity is not used during DMA writes to memory.
CLK	I	Input clock signal
RESETN	I	This active low signal resets the DMA.
CSN	I	When low, access to read and write the DMA internal registers is enabled.
AS	I/O	AS high indicates the presence of a valid address on the address bus. This signal is an input on cycles not assigned to the DMA.
DSN	I/O	When low, data strobe indicates the presence of data on the data bus. This signal is an input on cycles not assigned to the DMA.
MION	I/O	If high, this signal indicates that the current cycle is accessing memory space. If low, the current cycle is accessing IO space. Is an input during cycles not assigned to the DMA.
RDWN	I/O	During DMA cycles, this signal goes high to indicate read cycles and low to indicate write cycles. It is an input during non-DMA cycles.
OIN	O	During DMA cycles, this signal goes high to indicate operand cycles and low to indicate instruction cycles. It is tri-stated during non-DMA cycles.
RDN	O	This active low read strobe is tri-stated on non-DMA cycles.
WRN	O	This active low write strobe is tri-stated on non-DMA cycles.
RDYN	I/O	This signal goes active low to indicate that the current bus cycles can be terminated. It is an output on cycles addressing the DMA internal registers, input on cycles controlled by the DMA and is tri-stated during all other cycles.
LOCKN	O	This signal is driven low during the first bus cycle of a double word transfer. It should be used by the bus arbiter to 'lock' bus control to the DMA. It is tri-stated during cycles not assigned to the DMA.
REQN	O	Always driven, this signal goes low to indicate that the DMA requests the bus.
GRANTN	I	Sampled by the DMA on negative CLK edges, this signal goes low to indicate that the DMA has bus control.
DMAKN	O	This output is driven active low by the DMA when it has bus control. It is tri-stated on cycles not assigned to the DMA.
DONEN	O	This signal is pulsed low for one CLK cycle when any of the four DMA channels reaches an 'end of transfer' condition.
REQINN	I	Sampled by the DMA on negative CLK edges, a low on this input indicates that a cascaded, lower priority DMA is requesting the bus. This input should be tied high in a single DMA system.
GEINN	I	This active low signal is used to qualify the GRANTN signal for cascaded DMA devices. This signal should be tied low on the first DMA of the chain.
GEOUTN	O	This active low output indicates that a lower priority DMA will be granted the bus when the GRANTN signal is asserted low from the arbiter. It is used to cascade DMA devices by connecting to the GEINN pin of the next DMA.
INTRN	O	This active low interrupt request signal pulses low when an 'end of transfer' or an internal error condition are detected.
PEN	I	The DMA samples PEN on AS falling. If an error condition is sampled, the transfer on the DMA channel is stopped and the CLE bit is set in the Channel Status Register.
DMAE	I	An active high input to indicate that the DMA is enabled. If this input is low, internal requests are supressed, there is no response to external requests and REQINN is gated out internally.
DPARN	I	A low on this signal resets and disables checking of the parity bit (D[16])
DTON	I	A low on this signal resets and disables the bus fault timeout circuitry.
MPROEN	I	This input is sampled on AS falling when the DMA has bus control. If an active low is sampled, the transfer stops on the channel concerned and the CAE (addressing error) bit is set in the channel status register. An interrupt may be generated.
EXADEN	I	This input is sampled on AS falling when the DMA has bus control. If an active low is sampled, the transfer stops on the channel concerned and the CAE (addressing error) bit is set in the channel status register. An interrupt may be generated.
DREQN[0:3]	I	Sampled by the DMA on negative CLK edges, a low on this bus initiates a DMA transfer providing the corresponding channel is correctly set up and is not masked. When the pin is pulled high, the ongoing bus cycle will terminate.
DACKN[0:3]	O	During a transfer, the DMA drives the relevant channel acknowledge low to indicate that the DMA is ready for the data. The low to high transition at the end of the cycle is initiated by the condition DREQN high and RDYN low.
SEC/FIRSTN	O	A high indicates that the first word in a transfer is occuring. A low indicates that the second word in a double word transfer is occuring.
AKRDN	O	This active low strobe indicates that the DMA is driving the data bus.
AKWRN	O	This active low strobe indicates that the DMA is inputting data from the data bus.

TIMING DIAGRAMS

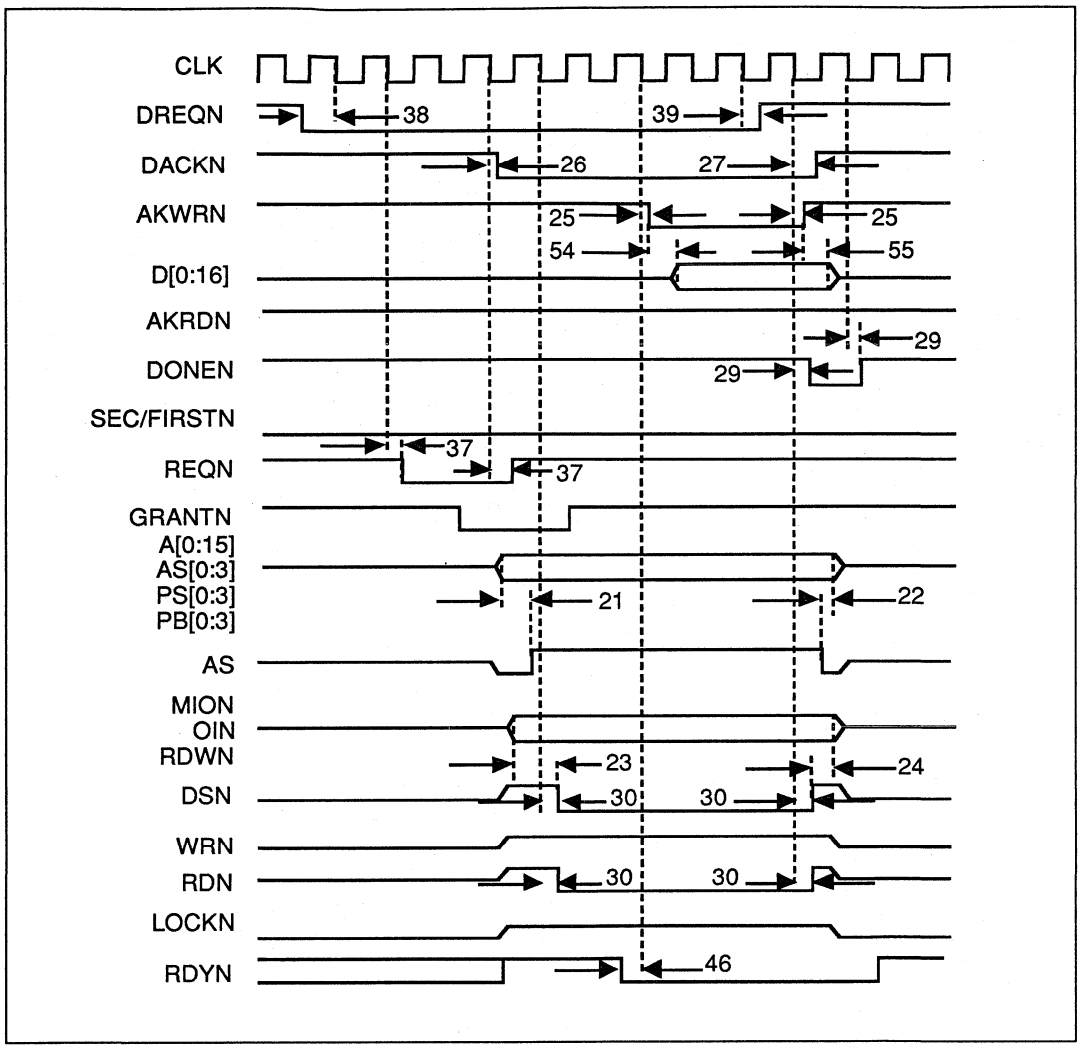


Figure 4: Single Cycle With Handshake, Memory Read

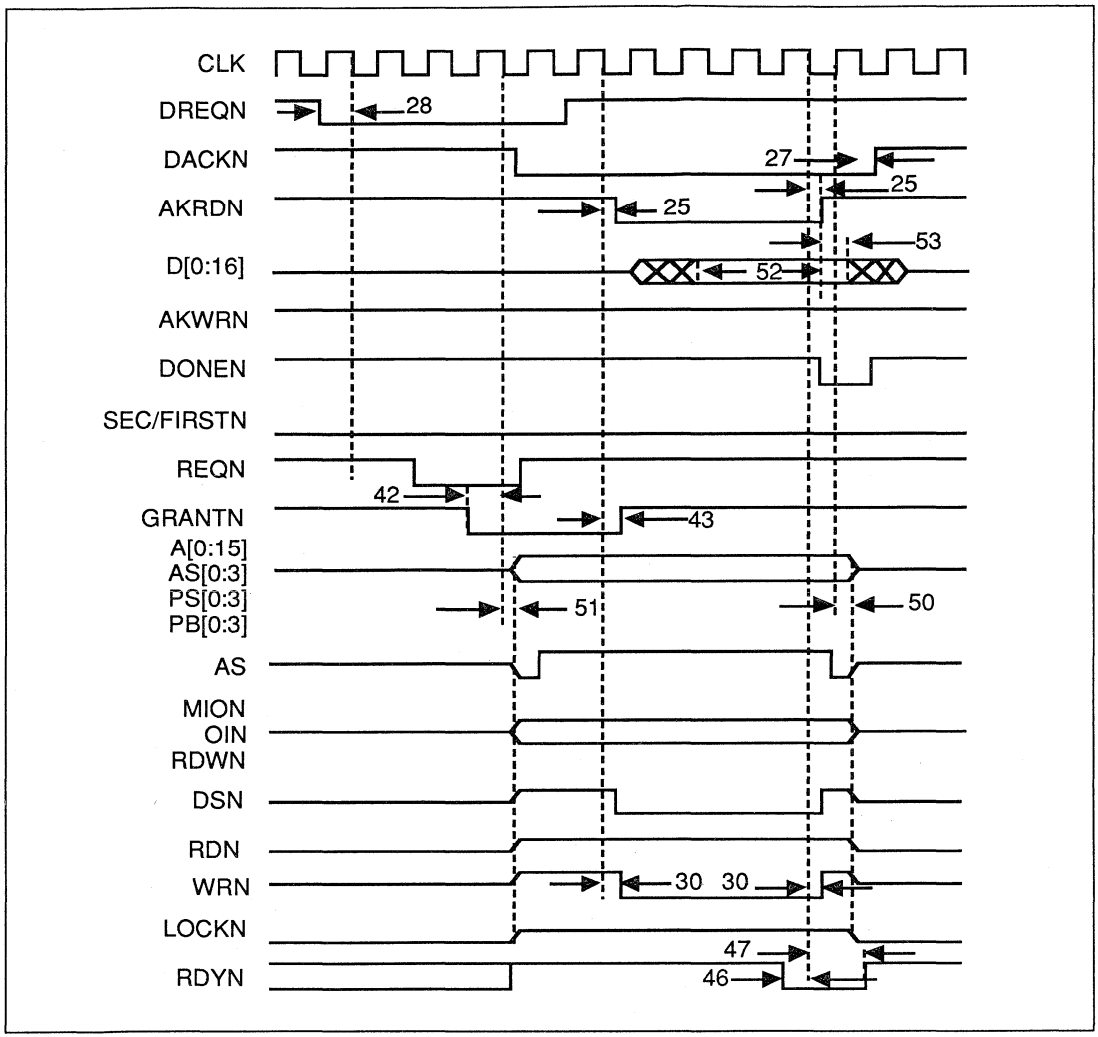


Figure 5: Single Cycle With Handshake, Memory Write

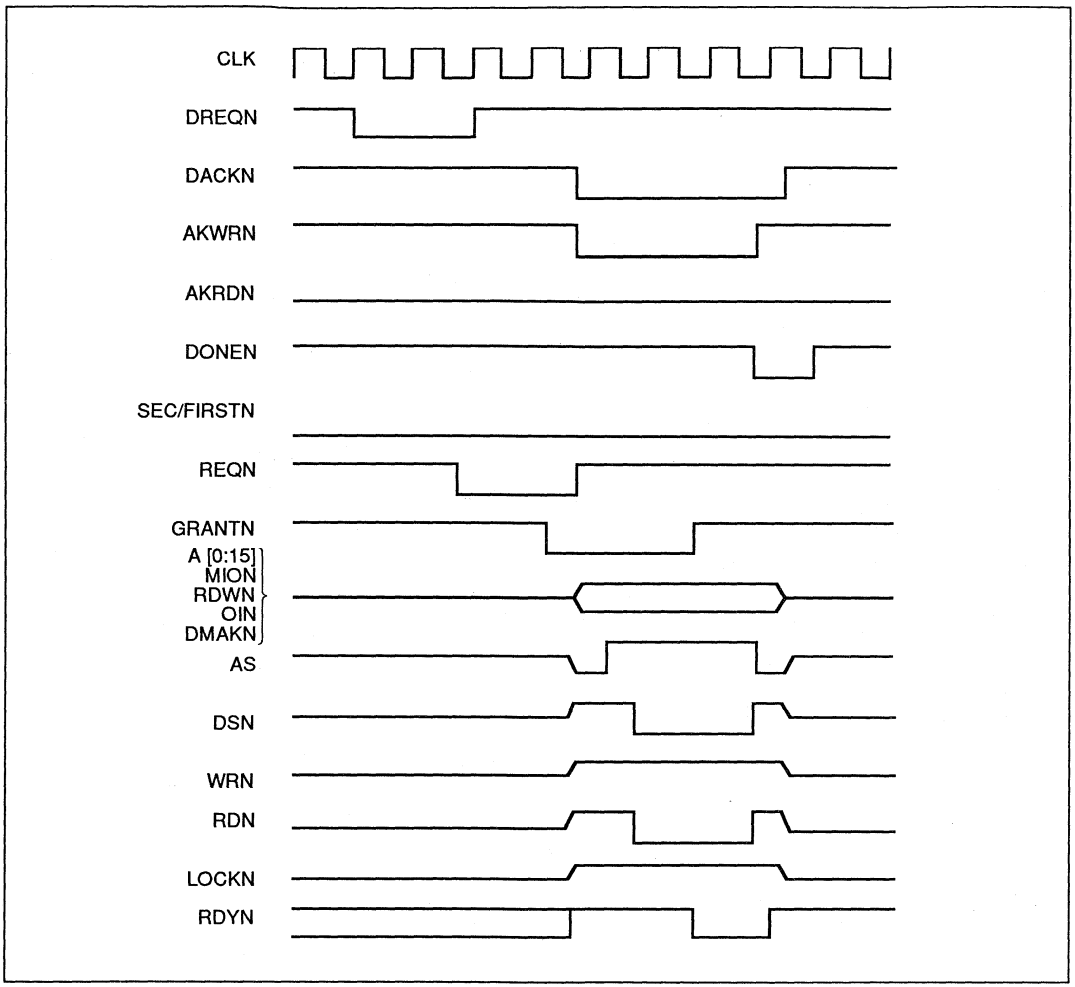


Figure 6: Single Cycle Without Handshake, Memory Read

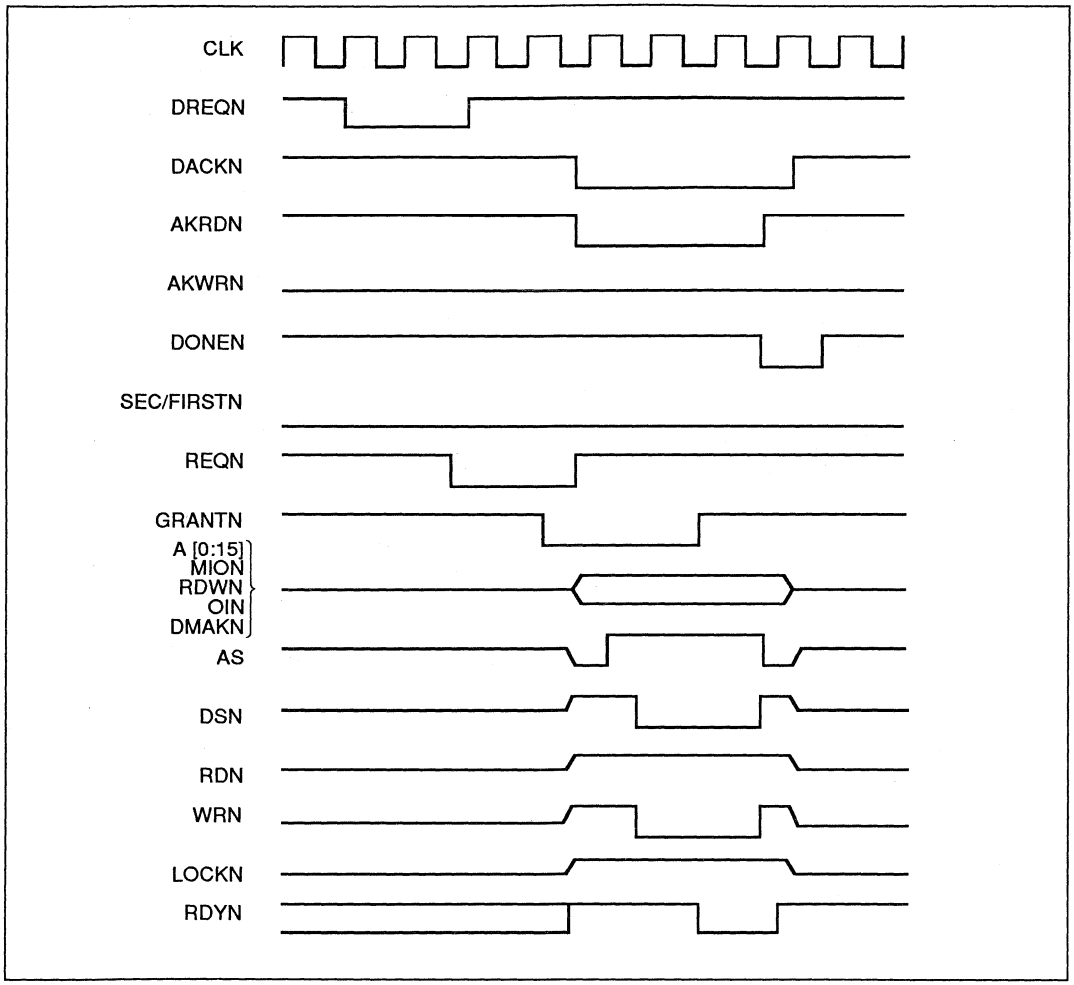


Figure 7: Single Cycle Without Handshake, Memory Write

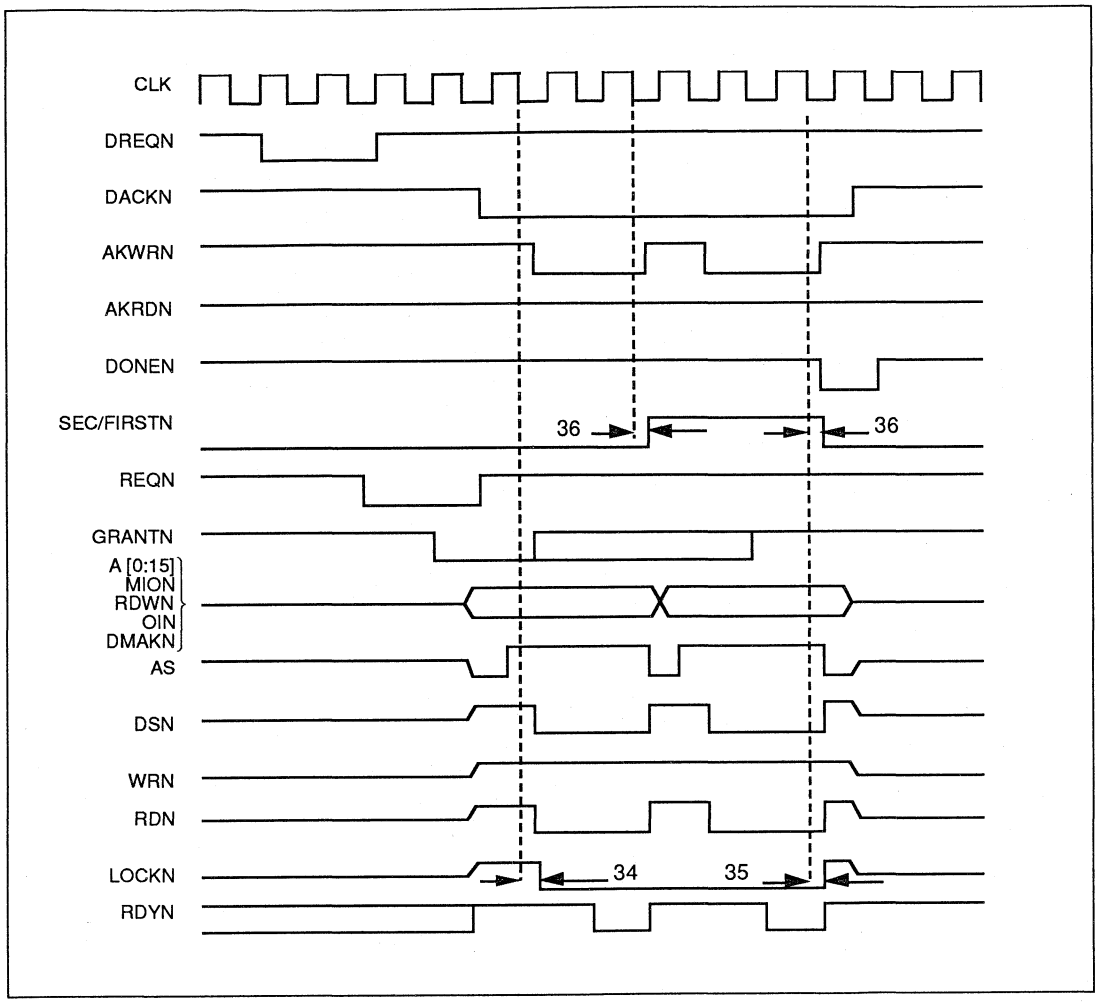


Figure 8: Double Mode, Memory Read

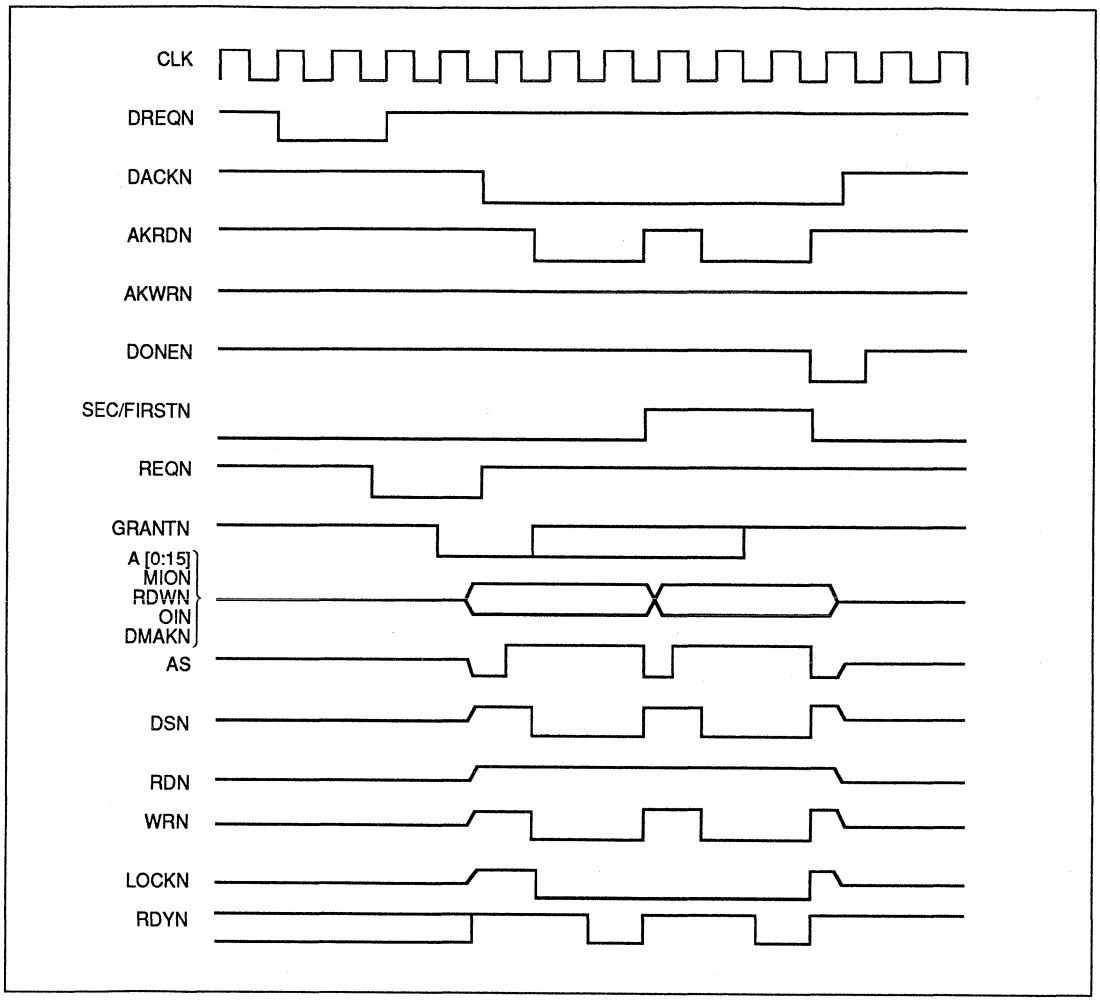


Figure 9: Double Mode, Memory Write

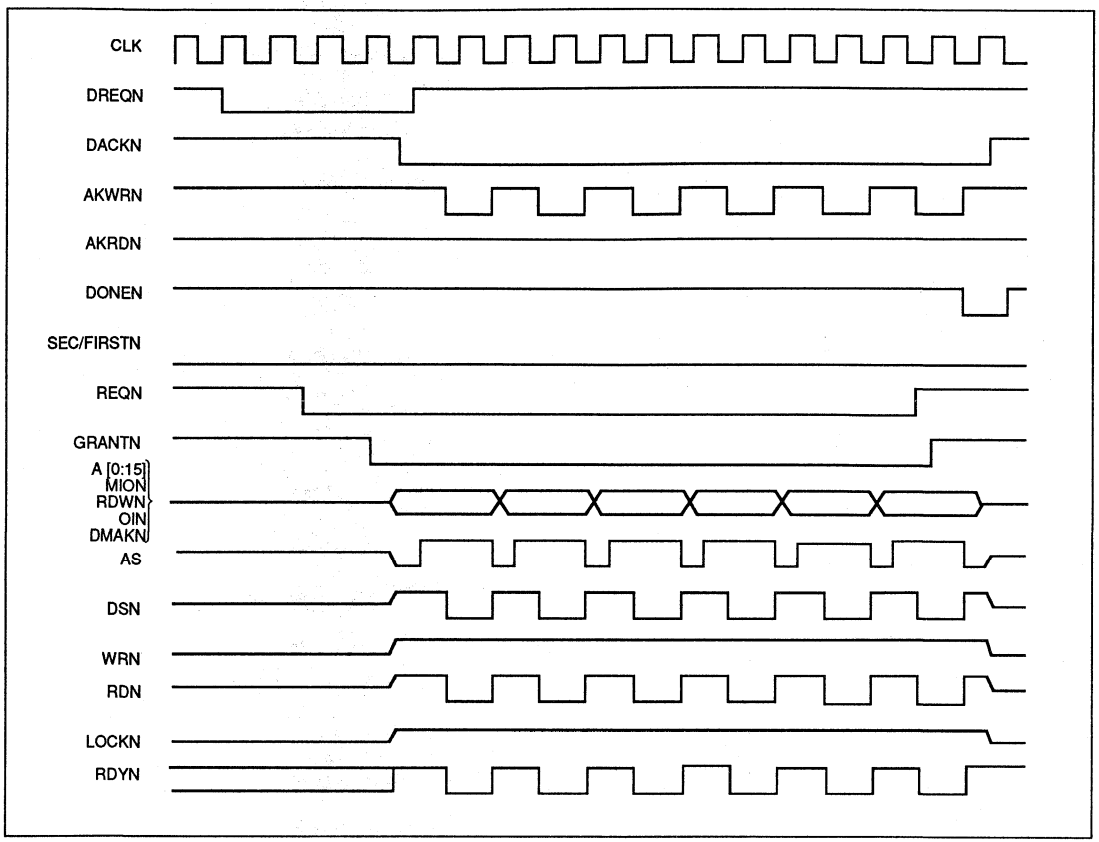


Figure 10: Burst Mode 6 Words, Memory Read

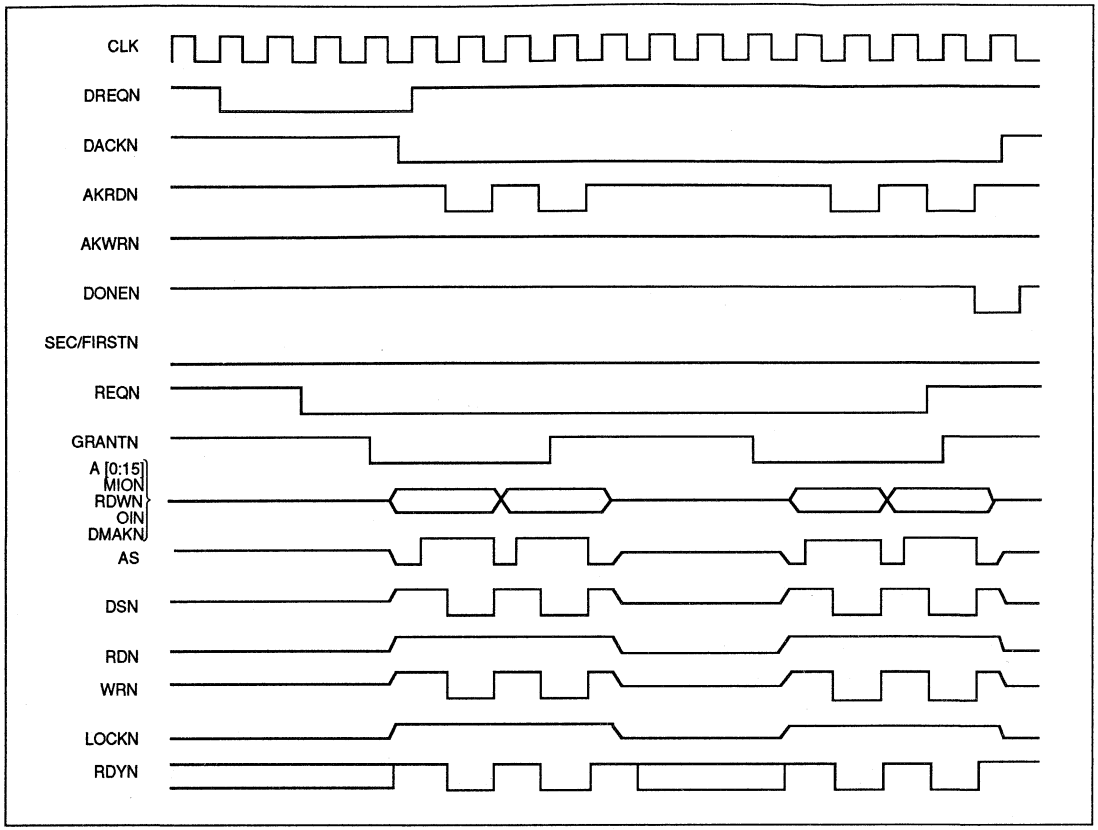


Figure 11: Burst Mode 4 Words, Memory Write (with interruption of the block)

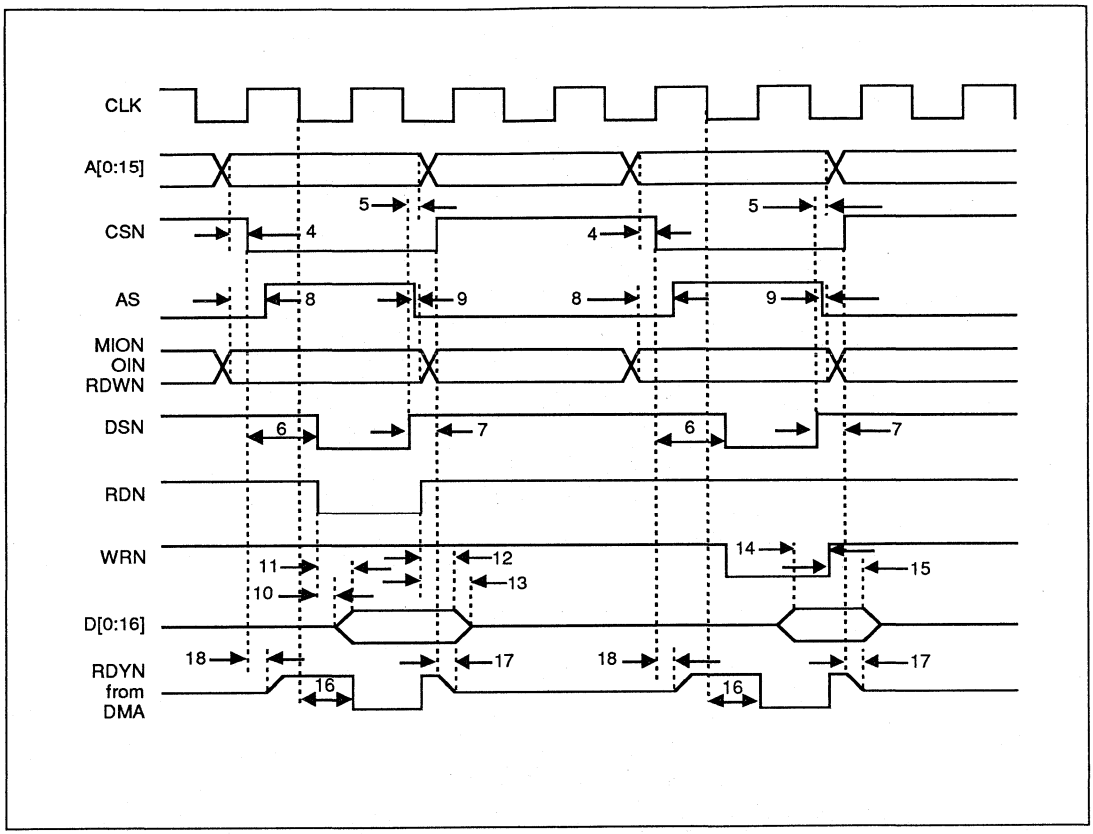


Figure 12: DMA XIO read and write cycles

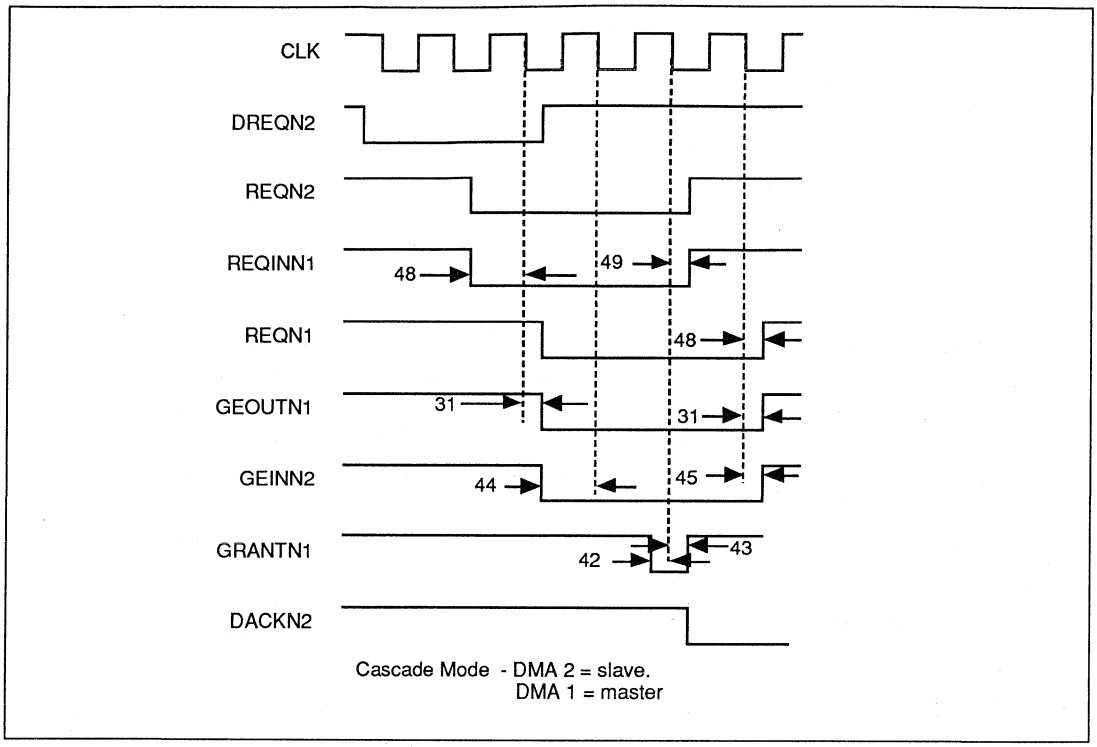


Figure 13: Cascade Mode

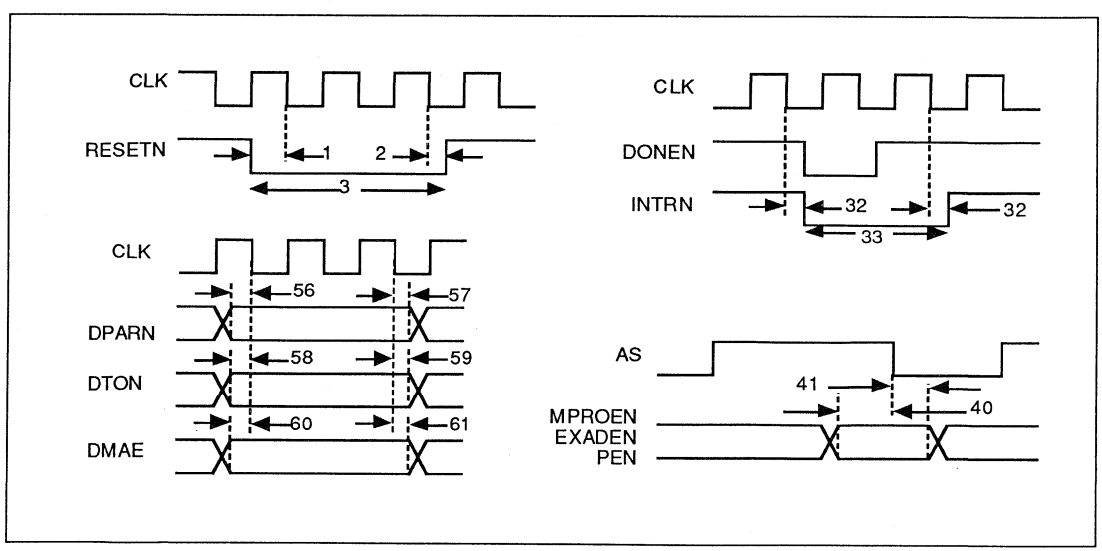


Figure 14: Miscellaneous Timings

No.	Description	Min	Max	Units
1	RESETN setup to CLK falling		-	ns
2	RESETN hold after CLK falling		-	ns
3	RESETN pulse wdth		-	ns
4	A[0:15] setup to CSN falling (DMA XIO)		-	ns
5	A[0:15] hold after DSN rising (DMA XIO)		-	ns
6	CSN setup to DSN falling (DMA XIO)		-	ns
7	CSN hold after DSN rising (DMA XIO)		-	ns
8	MION, OIN, RDWN setup to AS rising (DMA XIO)		-	ns
9	MION, OIN, RDWN hold after AS falling (DMA XIO)		-	ns
10	RDN falling to D[0:16] driven (XIO read)			ns
11	RDN falling to D[0:16] valid (XIO read)			ns
12	RDN rising to D[0:16] invalid (XIO read)			ns
13	RDN rising to D[0:16] tri-state (XIO read)			ns
14	D[0:16] setup to WRN rising (XIO write)		-	ns
15	D[0:16] hold after WRN rising (XIO write)		-	ns
16	CLK falling to RDYN valid (DMA XIO)			ns
17	CSN rising to RDYN tri-state (DMA XIO)			ns
18	CSN falling to RDYN driven (DMA XIO)			ns
19	CLK rising to AS rising			ns
20	CLK falling to AS falling			ns
21	A[0:15], AS[0:3], PS[0:3], PB[0:3] valid to AS rising			ns
22	A[0:15], AS[0:3], PS[0:3], PB[0:3] valid after AS falling			ns
23	MION, OIN, RDWN valid to DSN falling			ns
24	MION, OIN, RDWN valid after DSN rising			ns
25	CLK falling to AKRDN, AKWRN valid			ns
26	CLK falling to DACKN[0:3] falling			ns
27	CLK falling to DACKN[0:3] rising			ns
28	CLK falling to DMAKN valid			ns
29	CLK falling to DONEN valid			ns
30	CLK falling to DSN, RDN, WRN valid			ns
31	CLK falling to GEOUTN valid			ns
32	CLK falling to INTRN valid			ns
33	INTRN pulse width			ns
34	CLK falling to LOCKN falling			ns
35	CLK falling to LOCKN rising			ns
36	CLK falling to SEC/FIRSTN valid			ns
37	CLK falling to REQN valid			ns
38	DREQN[0:3] setup to CLK falling		-	ns
39	DREQN[0:3] hold after CLK falling		-	ns
40	EXADEN, MPROEN, PEN setup to AS falling		-	ns
41	EXADEN, MPROEN, PEN hold after AS faling		-	ns
42	GRANTN setup to CLK falling		-	ns
43	GRANTN hold after CLK falling		-	ns
44	GEINN setup to CLK falling		-	ns
45	GEINN hold after CLK falling		-	ns
46	RDYN setup to CLK falling		-	ns
47	RDYN hold after CLK falling		-	ns
48	REQINN setup to CLK falling		-	ns
49	REQINN hold after CLK falling		-	ns
50	CLK rising to busses, strobes and control signals (note 1) tri-state			ns
51	CLK falling to busses, strobes and control signals (note 1) driven			ns
52	D[0:16] setup to AKRDN rising		-	ns
53	D[0:16] hold after AKRDN rising		-	ns
54	D[0:16] valid after AKWRN falling			ns
55	D[0:16] valid after AKWRN rising			ns
56	DPARN setup to CLK falling		-	ns
57	DPARN hold after CLK falling		-	ns
58	DTON setup to CLK falling		-	ns
59	DTON hold after CLK falling		-	ns
60	DMAE setup to CLK falling		-	ns
61	DMAE hold after CLK falling		-	ns

Mil-Std-883, Method 5005, Subgroups 9, 10, 11.
TL = Low CLK period (ns), TH = High CLK period (ns).
Test Conditions: Vdd = 5.0V ±10%, Temperature = -55°C to 125°C, Vil = 0.0V, Vih = Vdd.
Output loads: All test load 1 unless otherwise specified.
Output Threshold: 50% Vdd (Load 1), Vss+1V, Vdd-1V (Load 2).
Note 1: A[0:15], AS[0:3], PS[0:3], PB[0:3], MION, OIN, RDWN, DMAKN, AS, DSN, RDN, WRN, LOCKN

Figure 15: Timing Parameters

RATING AND CHARACTERISTICS

Parameter	Min.	Max.	Units
Supply voltage	-0.5	7	V
Input voltage	-0.3	VDD+0.3	V
Current through any I/O pin	-20	20	mA
Operating temperature	-55	125	°C
Storage temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Figure 16: Absolute Maximum Ratings

Parameter	Min.	Max	Units
Clock Frequency (CLK)	0	16	MHz
Recommended Clock duty cycle	45	55	%

Vdd=5V±10% over full operating temperature range
Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Figure 17: Operating AC Electrical Characteristics

			Total dose radiation not exceeding $3x10^5$ Rad(Si)			
Symbol	Parameters	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input high voltage	-	80% V_{DD}	-	-	V
V_{IL}	Input low voltage	-	-	-	20% V_{DD}	V
V_{CKH}	CLK input high voltage	-	V_{DD}-0.5	-	-	V
V_{CKL}	CLK input low voltage	-	-	-	V_{SS}+0.5	V
V_{OH}	Output high voltage	I_{OH}=-3mA	V_{DD}-0.5	-	-	V
V_{OL}	Output low voltage	I_{OL}=5mA	-	-	V_{SS}+0.4	V
I_{IH}	Input high current (Note 1)	-	-	-	10	µA
I_{IL}	Input low current (Note 1)	-	-	-	-10	µA
I_{OZH}	I/O tristate high current (Note 1)	-	-	-	50	µA
I_{OZL}	I/O tristate low current (Note 1)	-	-	-	-50	µA
I_{DDYN}	Dynamic supply current @ 16MHz	-	-	-	80	mA
I_{DDS}	Static supply current	-	-	-	10	mA

Vdd=5V±10% over full operating temperature range
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not tested at low temperature (-55°C)

Figure 18: Operating DC Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 18 at +25°C
2	Static characteristics specified in Figure 18 at +125°C
3	Static characteristics specified in Figure 18 at -55°C
7	Functional characteristics specified in Figure 17 at +25°C
8A	Functional characteristics specified in Figure 17 at +125°C
8B	Functional characteristics specified in Figure 17 at -55°C
9	Switching characteristics specified in Figure 15 at +25°C
10	Switching characteristics specified in Figure 15 at +125°C
11	Switching characteristics specified in Figure 15 at -55°C

Figure 19: Definition of MIL-STD-883, Method 5005 Subgroups

PIN ASSIGNMENTS AND OUTLINES

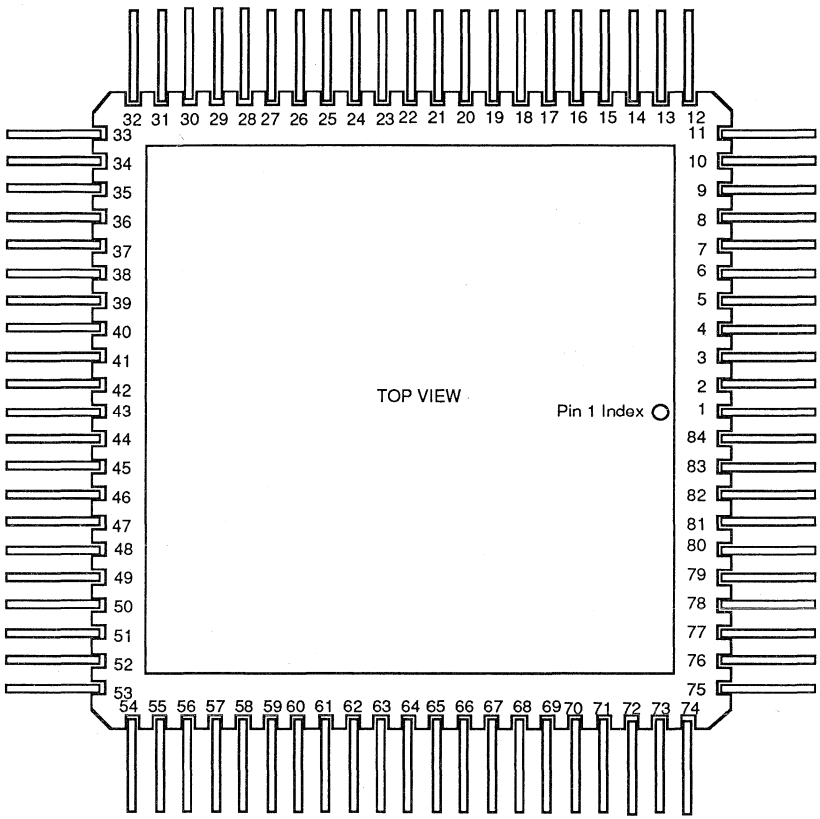
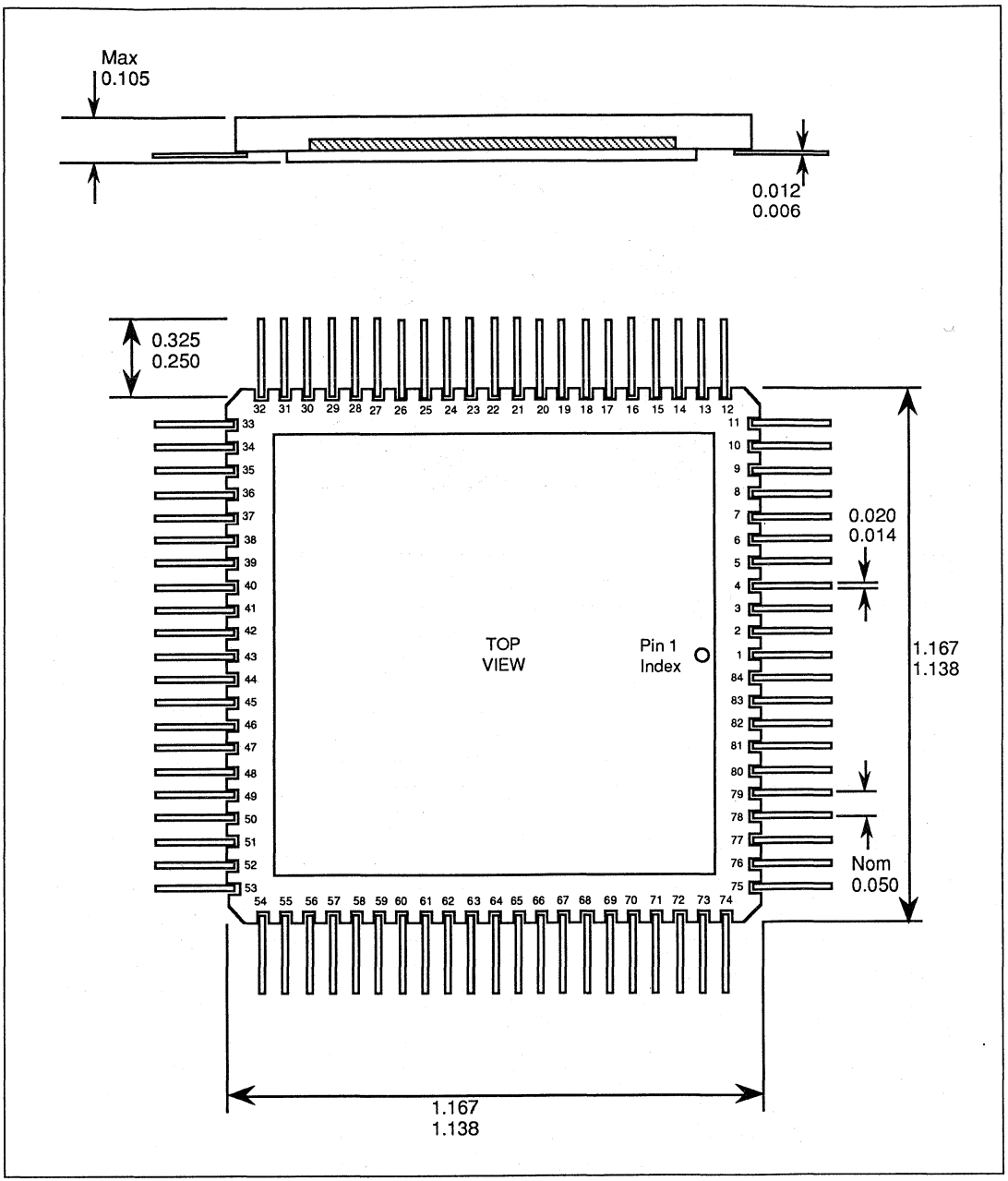
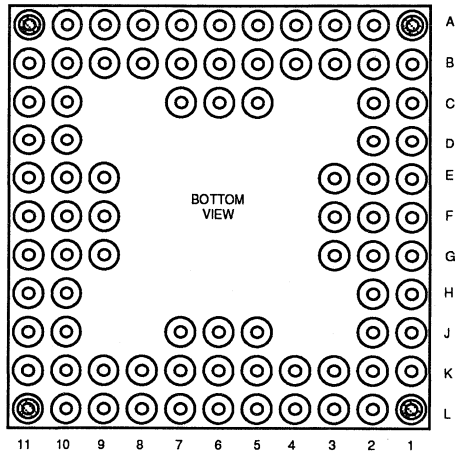


Figure 20: 84-Lead Flatpack - Package Style F



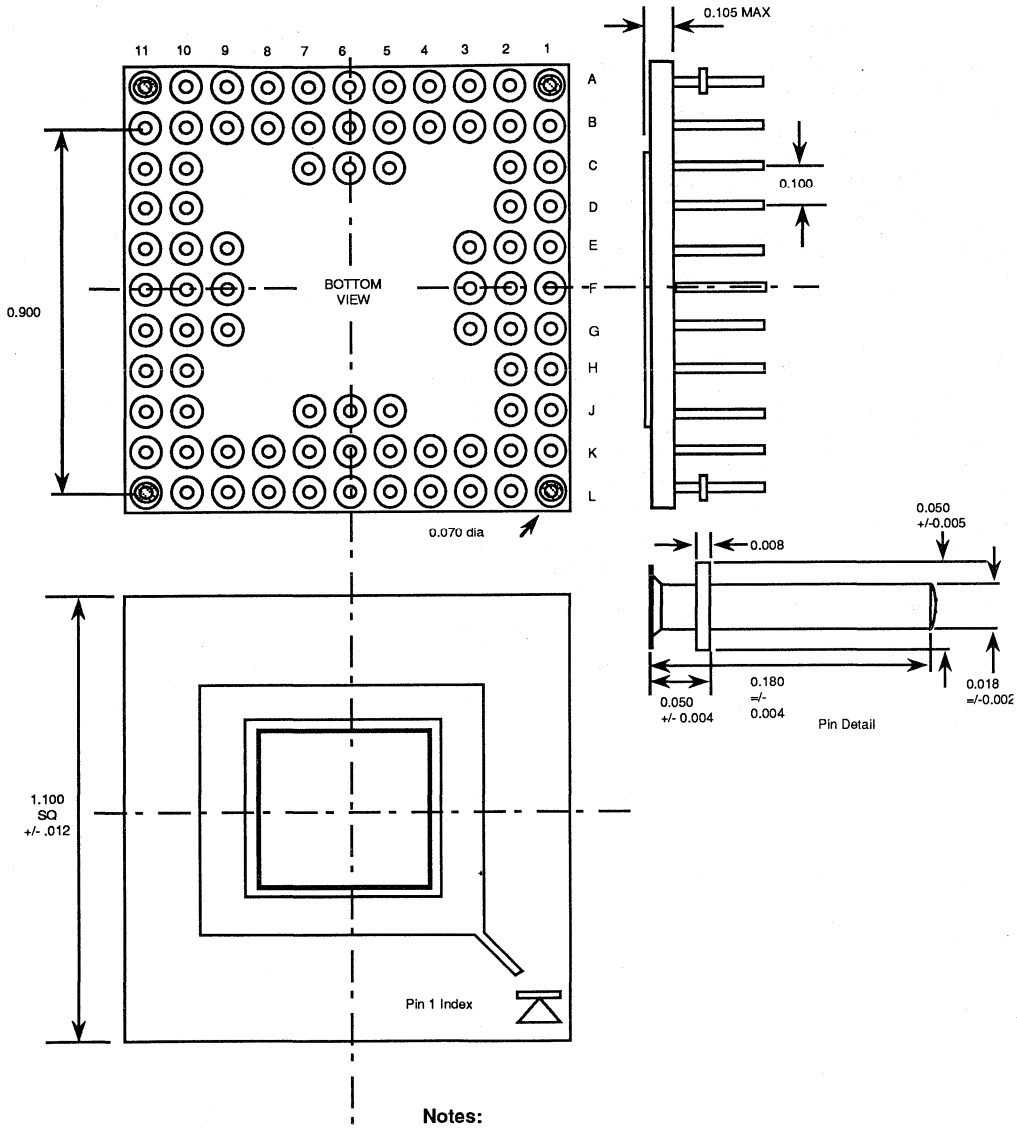
NOTE: All dimensions shown in inches

Figure 21: 84-Lead Flatpack - Package Style F



A1		B11		F9		K2	
A2		C1		F10		K3	
A3		C2		F11		K4	
A4		C5		G1		K5	
A5		C6		G2		K6	
A6		C7		G3		K7	
A7		C10		G9		K8	
A8		C11		G10		K9	
A9		D1		G11		K10	
A10		D2		H1		K11	
A11		D10		H2		L1	
B1		D11		H10		L2	
B2		E1		H11		L3	
B3		E2		J1		L4	
B4		E3		J2		L5	
B5		E9		J5		L6	
B6		E10		J6		L7	
B7		E11		J7		L8	
B8		F1		J10		L9	
B9		F2		J11		L10	
B10		F3		K1		L11	

Figure 22: 84-Pin Grid Array - Package Style A



Notes:

1. ▒ represents gold plating 50 microns min. over 100 microns nominal nickel.
2. All dimensions are in inches.
3. Default tolerances ±1% not less than 0.005
4. Ceramic is 92% Alumina.

Figure 23: 84-Pin Grid Array - Package Style A

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to total dose radiation levels, each wafer lot will be approved when all sample devices pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL STD 883 test method 1019, Ionizing Radiation (Total Dose).

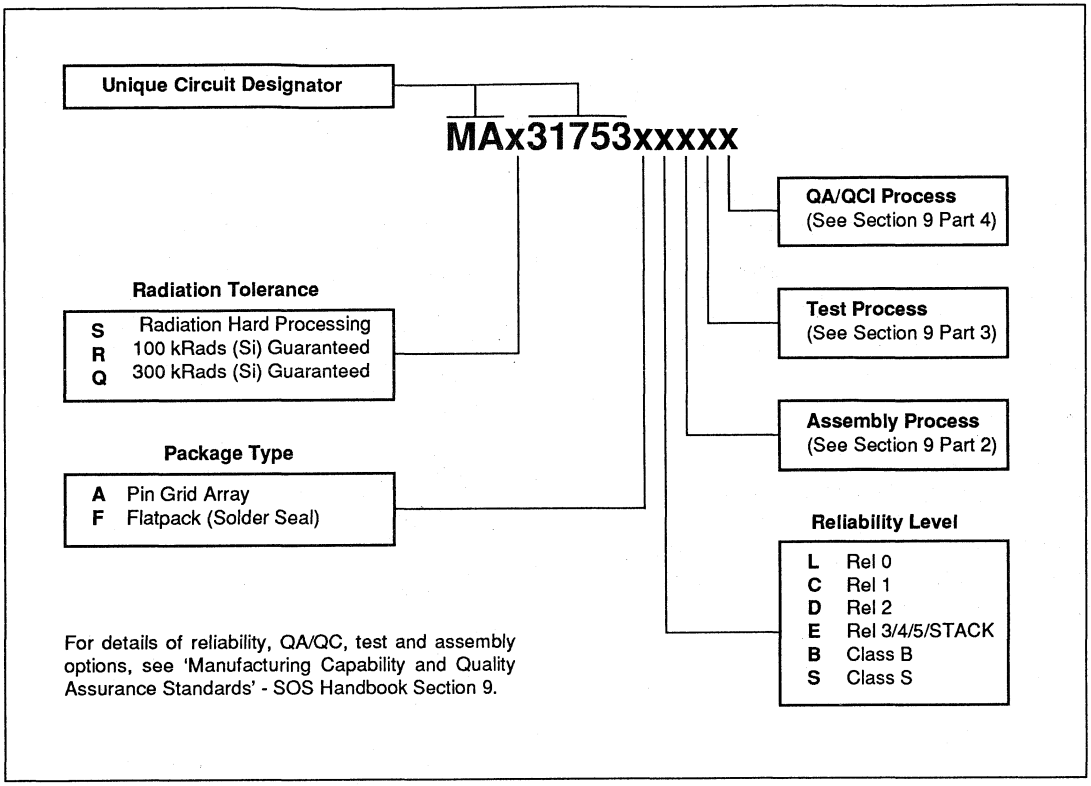
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 24: Radiation Hardness Parameters

ORDERING INFORMATION



MA31754

PERIPHERAL SUPPORT CHIP (PSC)

The MA31754 is a Peripheral Support Chip (PSC) designed to provide those features which are commonly required in an MA31750 processor system. It can be used to replace much of the external logic associated with wait state generation, bus arbitration and address decoding. This reduces the power consumption, weight, complexity and cost of the system, whilst increasing its performance and overall reliability.

FEATURES

- Radiation Hard CMOS SOS Technology
- Versatile Decoding Scheme for IO Address Space
- Support for Non-Volatile Memory Management Including On-Circuit Board Programming/Reprogramming
- System Bus Arbiter and Ready State Generator
- Support for EDAC Testing
- Independent Watchdog Timer
- On-Board Mission Timer and Real Time Clock Function
- System Reset Generator
- Two Simple Serial Interfaces

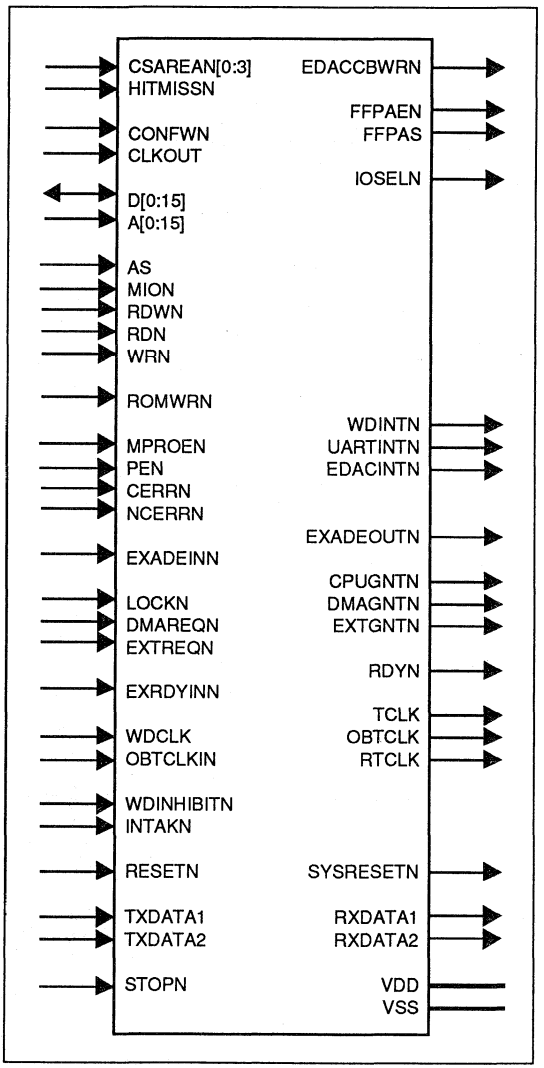


Figure 1: Pin Connections - Top View

1. FUNCTIONAL DESCRIPTION

The MA31754 Processor Support Chip (PSC) is a single chip device providing much of the support circuitry for systems based on the MA31750 microprocessor. The PSC is capable of supporting system with the additional, optional configurations of MMU/ BPU (MA31751), EDAC (MA31755), parity, DMA controller (MA31753) and external system bus interface.

1.1 RESET GENERATION

The PSC generates system reset to the CPU and any other associated logic which requires a reset. The system reset output pin becomes active (low) whenever the RESETN input to the PSC becomes active and remains low 10 clock cycles after RESETN has become inactive. Alternatively, should the ROMWRN input be active during RESETN low, then the system reset output will remain active until both RESETN and ROMWRN have become inactive, or for 10 clock cycles - whichever is the longer.

SYSRESETN will also be set active low if there is no response to the WD interrupt after a timeout period has elapsed. Again, SYSRESETN stays low for 10 clock cycles or until ROMWRN goes high - whichever is the longer.

1.2 CONFIGURATION SENSING

Upon reset the processor determines the hardware configuration of the system by reading a configuration register on the local data bus. At the same time the PSC samples the same configuration data for its own use. A description of the bit allocation within the CPU configuration word is shown following in figure 2.

Bit No.	Meaning
0	MMU select bit 0
1	BPU select bit 0
2	Console select
3	MMU select bit 1
4	Level / Edge sensitive interrupts
5	MMU select bit 2
6	Parity odd / even
7	Built in Test on reset
8	Start up ROM present
9	DMA present
10	1750A/B select
11	Instruction Set Expansion
12	BPU Select 1
13	BPU Select 2
14	Reserved
15	External system interface accesses (physical or logical)

Figure 2: Configuration Register Bit Allocation

1.3 READY GENERATION

The PSC incorporates a programmable RDYN generator which is used to drive the CPU RDYN input indicating the completion of bus access cycles.

For each memory block (defined by a CSAREAN signal going active low), it is possible to independently define 0 to 15 wait states for read accesses and 0 to 15 wait states for write accesses, for both MMU cache hit and miss occurrances.

The correct number of memory wait states which are to be inserted, should be programmed into the Memory Ready (MR) Registers. There are 4 of these MR registers, one for each of the chip selected areas CSAREAN[0:3]. Each has the same basic structure shown in figure 3.

Read/Write Address for CS0 MR Register - 0x9F13/0x1F13
Read/Write Address for CS1 MR Register - 0x9F14/0x1F14
Read/Write Address for CS2 MR Register - 0x9F15/0x1F15
Read/Write Address for CS3 MR Register - 0x9F16/0x1F16

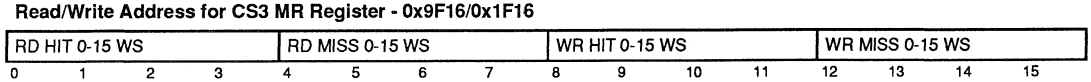


Figure 3: Memory Ready Register Structure

The mapping of these registers onto physical memory is done by external address decoding logic which outputs the Chip select inputs to the PSC.

Note: The HIT/MISS reference is so that different numbers of wait states can be added depending on whatever the cycle is an MMU cache hit or cache miss (determined by the HIT/MISSN signal input to the PSC).

Extra wait states can be added by taking the EXTRDYINN signal high. The wait state count does not start until EXTRDYINN goes low, ie. RDYN goes low, the programmed number of wait states after EXTRDYINN has gone low.

RDYN is also generated for accesses to User IO address space. The required number of waitstates is programmed in the User IO Control Register.

When SYSRESETN and ROMWRN are low, the ready generator automatically inserts 15 waitstates into every external cycles. These cycles can be used for programming an EEPROM device across the external interface.

1.4 ADDRESS RANGE VALIDATION

The following conditions will all cause the PSC to send an 'External Address Error' (EXADEOUTN) signal to the CPU:

- Any attempt to address the User IO areas where the address is beyond the Last Implemented User IO Address specified in the User IO Command Register.
- All non-implemented IO commands. Also 1750B mode commands will be illegal in 1750A mode.
- Any attempt to address the Unimplemented Spare IO areas unless the enable bit in the User IO Command Register is set.
- The input EXADEINN being active low.

1.5 FIRST-FAILING PHYSICAL ADDRESS CAPTURE CONTROL SIGNALS (FFPAEN AND FFPAS)

A First Failing Physical Address (FFPA) Register can be implemented as an external register in the system. The enable signal, FFPAEN, can be used as the output enable signal. FFPAEN becomes active when the FFPA register is read. The strobe, FFPAS, can be used to clock the address information into the latch. FFPAS latches the address into the register at the end of every external machine cycle until a relevant error is detected. The latching then stops until the FFPA register has been read. Any of the following signals sampled active low will cause the FFPAS to stop latching the FFPA register: EXADEOUTN, CERRN, NCERRN, PEN, MPROEN. An error code and transfer type could also be recorded in this register - see below for suggestions.

Suggested First Failing Physical Address Register - Read Address 0x9F0B

EA(3:10)								EA(0:2)			CPUGNTN	DMAGNTN	EXTGNTN	Users	
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1.6 BUS ARBITRATION

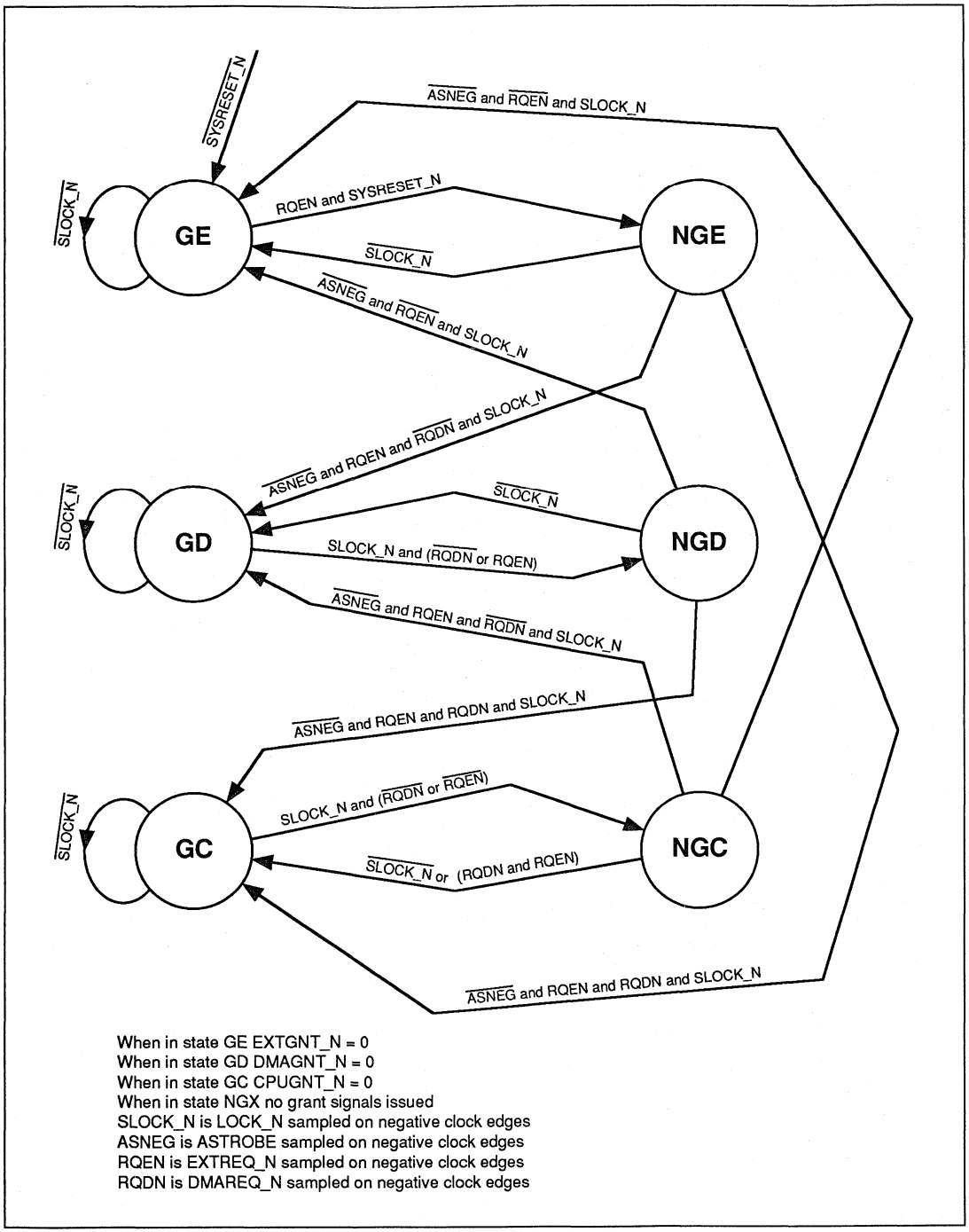
The PSC contains a Bus Arbiter which allocates the system bus to up to three different bus-units. These are, in order of priority, highest first:

1. An external controller working with logical or physical addresses and having a request/grant protocol not using the system clock.
2. A local system DMA controller.
3. The CPU.

Any unit which is configured in the system can request control of the bus by asserting the relevant RQN signal low. In the case of the external interface and the local DMA controller, the incoming RQN signal is sampled on negative going clock edges.

When the current bus cycle finishes (and there are no grant signals issued), the request lines are checked. The request from the highest priority bus-unit is acknowledged by the Arbiter by asserting the relevant GNTN signal low, thus granting the unit use of the next bus cycle. This unit will be granted the bus until either it ceases to request the bus or a request of higher priority is detected. If no incoming requests are waiting when the current cycle ends, the CPU is granted the bus.

At reset, the Arbiter grants the system bus to the External Interface. The external interface remains granted until SYSRESETN goes inactive. The "grant by request" system then starts.



When in state GE EXTGNT_N = 0
When in state GD DMAGNT_N = 0
When in state GC CPUGNT_N = 0
When in state NGX no grant signals issued
SLOCK_N is LOCK_N sampled on negative clock edges
ASNEG is ASTROBE sampled on negative clock edges
RQEN is EXTREQ_N sampled on negative clock edges
RQDN is DMAREQ_N sampled on negative clock edges

Figure 4: State Diagram for the Bus Arbitration Block

1.7 INTERRUPT SYNCHRONISATION AND ACKNOWLEDGE

There are 3 interrupts output from the PSC. The WDINTN is not sampled and cannot be masked or disabled. The active interrupt is cleared by the INTAKN signal indicating that the WD interrupt is being serviced.

The EDACINTN can be set by CERRN, NCERRN or PEN going active. CERRN and NCERRN are sampled as they come from combinational logic which may glitch. EDACINTN can be masked and/or disabled by the relevant bits in the PSC Interrupt Register. The interrupt is cleared by the relevant INTAKN going active.

The UARTINTN is activated by signals generated internally within the PSC. This interrupt can be masked or disabled by the PSC Interrupt Register. The interrupt is activated when any one of the FE, OE, PE, BD, RxBF or TxBE bits are set in the UART control and status register. The bit set in the interrupt register will indicate whether the error occured in UART 1 or 2. UART1 and UART2 are both masked by MASK and enabled by EU. They both cause UARTINTN to go active if they are unmasked and enabled. UARTINTN is cleared by the relevant INTAKN going active.

The functionality of this block is derived from the "Interrupt Masking and Allocation" register (figure 5). The mapping of the PSC interrupts onto the CPU interrupts is defined by the "Interrupt Mapping" register (figure 6).

Interrupt Allocation Register - Read/Write Address - 0x9F09/0x1F09

EDAC Interrupt Status and Control								UART Interrupt Status and Control							
CE	NCE	PE	ECE	ENCE	EPE	Mask	-	CE	NCE	UART1	ECE	ENCE	EU	Mask	UART2
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

CE	EDAC Correctable Error status	Can set both interrupts. If this bit is set then the PSC has sampled an error on the CERRN input.
NCE	EDAC Non-correctable Error status	Can set both interrupts. If this bit is set then the PSC has sampled an error on the NCERRN input.
PEN	PSC Parity Error status	Can set EDACINTN only. If this bit is set then the PSC has sampled an error on the PEN input.
UART	PSC UART error status	Can set UARTINTN only. If this bit is set then an internal UART error has occurred.
ECE	Enable Correctable Error	Enable EDAC Correctable Error to interrupt output.
ENCE	Enable Non-correctable Error	Enable EDAC Non-correctable Error to interrupt output.
EPEN	Enable Parity ERROR	Enable Parity Error to interrupt output (EDACINTN only).
EU	Enable UART Error	Enable UART Error to interrupt output (UARTINTN only).
MASK	Mask interrupt	If either of these bits are set high, then the relevant interrupt cannot be issued. As soon as the mask bit is cleared, the interrupt will go active if a fault has occurred. The interrupt outputs are automatically masked during EDAC online memory testing.

Figure 5: Bit Allocation for Interrupt Allocation Register

Interrupt Mapping Register - Read/Write Address - 0x9F17/0x1F17

Res				UART LP				EDAC LP				WD LP			
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Figure 6: Interrupt Mapping Register

If the interrupts are level sensitive and are to be cleared by INTAKN going active, it is necessary to define which interrupt inputs on the CPU are driven by which interrupt outputs from the PSC. This enables the correct interrupt (the one being serviced) to be cleared. Bits 11:14 of the linkage pointer of the relevant interrupts should be entered into the mapping register. Eg. If the WDINTN output on the PSC is connected to the PWRDN input on the CPU, the bits 0000 should be entered into bits 12:15 of the mapping register. This is derived from the PWRDN linkage pointer 0x0020. If UARTINTN is connected to INT15N, the mapping register has 1111 in bits 4:7 (from the LP 0x003E). The full list of available (external interrupt) linkage pointers and code for the mapping register is shown in figure 7.

CPU Interrupt	Linkage Pointer	Map Code
PWRDN	0x0020	0000
INT02N	0x0024	0010
INT08N	0x0030	1000
INT10N	0x0034	1010
INT11N	0x0036	1011
IOI1N	0x0038	1100
INT13N	0x003A	1101
IOI2N	0x003C	1110
INT15N	0x003E	1111

Figure 7: Mapping PSC Interrupts onto CPU Interrupts

1.8 WATCHDOG TIMER

The PSC implements a watchdog timer/counter which is driven by a 1kHz clock, typically implemented as a simple R-C oscillator. The counter, which is implemented as bits 8-15 of the Watchdog Timer register, is loaded upon reset or when an XIO write to the watchdog refresh register is performed. The value loaded into the counter is held in the watchdog time-out register. Subsequently the counter is decremented until it reaches zero, at which point the counter is stopped and a watchdog interrupt is generated. The watchdog counter will be re-loaded and restarted once an interrupt acknowledge has been received. An additional control bit - WD Reset - allows the watchdog Elapse timer to reset the system should a timeout have occurred and no interrupt response have been received within a further 16ms.

Following a reset the WD time-out register is preset to 255 and the counter is thus enabled for 255ms. During operation this limit may be reprogrammed to any 8 bit value under software control - thus varying the time-out period between 1 and 255ms.

The WD function may be inhibited either by asserting the WDinhibit input or by setting the WDinhibit bit in the PSC control register. The inhibit becomes the logical OR of either of these two. Whilst inhibited the WD counter is frozen and no WD interrupts will be generated. Once both inhibit signals are inactive, the operation of the WD timer will resume as normal. STOPN going low will also stop the WD timer from incrementing.

A time-out may also be forced via software by setting the WDForceElapse control bit whilst the WD inhibit is inactive.

Watchdog Control Register - Read/Write Address - 0x9F01/0x1F01

FoEl	WDER	Mask	IntS	IntC	Inhb	Stat	Res	Watchdog Timeout Limit							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

FoEl	Force Elapse	Forces WD timer to the elapsed state (if inhibit not set). This will trigger an interrupt if the WD interrupt mask bit is not set.
WDER	WD Elapse Reset	When this bit is set and the WD counter reaches zero a WD elapse interrupt is issued. If no system response is performed during the following 16ms the system is restarted by asserting the SYSRESETN line low.
Mask	Mask WD Interrupt	The Elapse reset counter is not started until this interrupt is asserted.
IntS	WD Interrupt Status	This bit is set low when a WD interrupt becomes active. It is cleared again on the INTAKN signal used to clear the interrupt.
IntC	WD Interrupt Clear	Writing a 1 to this bit clears the WD interrupt and restarts the WD timer.
Inhb	Inhibit Count	Halts the WD counter at its current state and resets the WD interrupt.
Stat	Status	Set to 0 to indicate the WD is in the RUN state and all Inhibited states. 1 indicates any other state (WD not OK).

Figure 8: Watchdog Control Register Bit Allocation

Watchdog Timer Register - Read/Write Address - 0x9F0A/0x1F0A

								Current Watchdog Timer Value							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Writing any data to this register causes the watchdog timer to restart. The register will be loaded with the Watchdog Timeout Limit in the WD control register. A read access to this register reads the current WD timer value.

1.9 PSC CONTROL REGISTER

The PSC Control Register collects together some miscellaneous control bits as shown.

PSC Control Register - Read/Write Address 0x9F00/0x1F00

RES	RES	ECBE	RES	RES	EExt	RES	RES	RES	SC/2	Timer clock divider					
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

RES	Reserved
ECBE	EDAC Check Bit Write Enable Bit. Active high to enable the write
EExt	1 Enables External Interface accesses to the local 31750 system
SC/2	Serial clock divide by 2 (UART - 19200/9600 baud). 1 gives 9600 baud
Timer clock divider	System clock is divided by 5 times the value in this register to produce TCLK

Figure 9: PSC Control Register Bit Allocation

1.10 USER IO CONTROL REGISTER

User IO Control Register - Read/Write Address - 0x9F03/0x1F03

IO RDY 0-15 Wait States				DACh	SExp	User IO Address, Read: 0000-03FF/Write: 8000-83FF									
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

IO RDY 0-15 WS		Defines number of wait states required when accessing User IO space and the First Failing Physical Address Register.
DACh	Disable Address Check	Disables User IO address checking when asserted high.
SExp	Enable Spare IO areas	The Unimplemented Spare IO command area is made available to the user when this bit is asserted.
User IO Address	Address of Last Implemented User IO command	An EXADEOUTN fault is generated if an attempted access to the User IO area has an address greater than that specifed here. This value limits the User IO space to between 0000 and 03FF for reads and 8000 and 83FF for writes.

Figure 10: Bit Allocation for User IO Control Register

1.11 CLOCKS AND TIMERS

3 clocks are input to the PSC. The WDCLK is an independant clock, input only to the watchdog timer. CLKOUT is the input clock (output from the CPU). This is divided by the value programmed in the control register to produce the 100KHz TCLK output.

OBTCLKIN should be a clock with a very tight specification on the frequency. This is divided by the factor in the OBT Prescale Register to provide the OBTCLK output. The OBTCLK is then further scaled by the value in the Real Time Clock Division Register to produce the RTCLK output. The OBTCLK also increments the two 16-bit On-Board Timer Registers, (these make up a 32-bit counter). These OBT Registers are cleared when the OBT Prescaler Register is written. When STOPN goes active low, the PSC goes into test mode. In this mode, the OBT counter registers can be written to enable testing procedures. STOPN active also inhibits the OBTCLK, RTCLK and TCLK outputs.

On-Board Timer Register 1 - Read/Write Address - 0x9F0F/0x1F0F

OBT (16 most significant bits)															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

On-Board Timer Register 2 - Read/Write Address - 0x9F10/0x1F10

OBT (16 least significant bits)															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

OBT Prescale Register - Read/Write Address - 0x9F11/0x1F11

Prescale Factor															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

Real Time Clock Division Register - Read/Write Address - 0x9F12/0x1F12

RTC Division Factor															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

1.12 SERIAL INTERFACES

Two simple bidirectional interfaces are provided, allowing asynchronous receive and transmit with a standard communications protocol (RS-232). The baud rate is user-definable and is produced from the system clock by an on-chip divider network.

UART 1 and 2 Control & Status Register

LEcE	SPE	SPAR	ERR	SBRK	RxE	StB	TxE	BD	RxBF	FE	OE	PE	TxBE	RxRY	TxRY
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

UART Transmit Data Register

-	-	-	-	-	-	-	-	Transmit Serial Data							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

UART Received Data Register

0	0	0	0	0	0	0	0	Receive Serial Data							
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

LEcE	Local Echo Enable. When this bit is high, the UART transmit data will echo the receive data.
SPE	Serial line Parity is Enabled when this bit is high.
SPAR	0 = serial line Parity is even. 1 = serial line Parity is odd.
ERR	Error Reset - FE, OE, and PE are cleared when this bit is set high.
SBRK	Force Break Interrupt - when this bit is high, the UART interrupt is forced active.
RxE	UART receive enable.
StB	0 = 2 stop bits on the serial line. 1 = 1 stop bit on the serial line.
TxE	UART transmit enable.
BD	Break Detect. This bit is set high when a break character is received.
RxBF	Receive Buffer Full.
FE	1 = Framing Error.
OE	1 = Overrun Error.
PE	1 = Parity Error.
TxBE	Transmitter Buffer Empty.
RxRY	Receiver Ready.
TxRY	Transmitter Ready.

Serial Data Format

The serial line is held high if no data is present. The start of a data byte is marked by a low start bit. This is immediately followed by 8 data bits, a parity bit (when enabled) and one or two stop bits (both high).

Receiver

There is a 32-byte long buffer on the receiver, to allow incoming data to be faster than the UART can output parallel data. The receiver checks for the following errors:

(i) Parity errors (PE is set if error found).
(ii) Framing errors (FE is set if the number of stop bits is incorrect).
(iii) Overrun errors (OE is set if the receiver buffer is full).

Transmitter

There is also a 32-byte long buffer on the transmitter. This allows the incoming data from the parrallel data bus to be faster than the UART can transmit. The transmitter adds a start bit, a parity bit and 1/2 stop bits according to the defined configuration. When the local echo is enabled, the transmitter outputs the received data.

Break Detect and Force

If the receiver detects a break, it causes a UART interrupt to be set. A break is defined as a low on the serial line for at least the duration of the start bit, the data bits and the programmed number of parity and stop bits. It is possible to transmit a break from the UART by setting the SBRK bit in the UART status and control register. Once this bit is set, the transmitter will continue to output break characters until the bit is cleared or until the PSC is reset.

Baud Rate

The PSC has an on-board baud rate generator which is programmable to work at 9600 or 19200 baud. The baud rate is generated from CLKOUT. The programming is done in the control register.

1.13 EDAC TEST FACILITY

The PSC output, EDACCBWRN, should be used as the write strobe for the check bit memory. If this is done, the EDAC can be tested by independantly writing the data and check bit memories, eg. A normal write, with check bits, is executed. The ECBE bit in the control register is then reset to zero to disable the check bit write strobe. The data memory is then re-written with 1 or 2 errors. ECBE is set high and the data word is read back through the EDAC. If 1 error was set, the correction facility on the EDAC is checked. If 2 errors were set, the EDAC detection facility is checked.

1.14 THE STOP FUNCTION

When STOPN is asserted low, the PSC stops all internal timers and clock outputs. This allows testing of the watchdog and on-board timers under software control.

2. PSC REGISTER ADDRESS SUMMARY AND INITIALISATION DATA

The PSC registers are placed in IO space and may be accessed via XIO or VIO commands issued by the CPU. The register addresses and their default (start-up) values are shown in figure 11.

Output	Input	Register	Initial State
1F00	9F00	(PSC) Control Register	0x 247F
1F01	9F01	Watchdog Control Register	0x 50FF
N/A	9F02	System Configuration Register	As CPU configuration register
1F03	9F03	User IO Control Register	0x F3FF
1F06	9F06	UART 1 Control & Status Register	0x 0204
1F07	N/A	UART 1 Transmit Data Register	0x 0000
N/A	9F08	UART 1 Receive Data Register	0x 0000
1F09	9F09	Interrupt Allocation Register	0x 0C04
1F0A	9F0A	Watchdog Timer Register	0x 00FF
N/A	9F0B	First Failing Physical Address Register	0x 0000
1F0C	9F0C	UART 2 Control & State Register	0x 0204
1F0D	N/A	UART 2 Transmit Data Register	0x 0000
N/A	9F0E	UART 2 Receive Data Register	0x 0000
1F0F	9F0F	On-Board Timer Register 1 (MSBs)	0x 0000
1F10	9F10	On-Board Timer Register 2 (LSBs)	0x 0000
1F11	9F11	USO Prescaler Register	0x 0001
1F12	9F12	Real-Time Clock Division Register	0x C350
1F13	9F13	CS0 Memory Ready Register	0x FFFF
1F14	9F14	CS1 Memory Ready Register	0x FFFF
1F15	9F15	CS2 Memory Ready Register	0x FFFF
1F16	9F16	CS3 Memory Ready Register	0x FFFF
1F17	9F17	Interrupt Mapping Register	0x 0D20

Figure 11: PSC Register Allocation Map

3. PIN DESCRIPTIONS

Busses

D[0:15]	I/O	System data bus. D00 is the most significant bit.
A[0:15]	I	System address bus (active high).

Strobes

AS	I	System address strobe. Indicates the presence of address information on the system address bus. This signal is produced by the current bus master.
MION	I	Memory/IO select. Asserted high by the current bus master during a memory access, low during an IO transfer.
RDWN	I	Read/Write select. Asserted high by the current bus master when data is being read into the bus master, low when data is being written from the bus master.
RDN	I	Read strobe. The rising edge of this signal indicates that data is being read by the current bus master.
WRN	I	Write strobe. The rising edge of this signal indicates that data is being written by the current bus master.
EDACCBWRN	O	Active low write strobe used for check bit memory writing. Can be disabled for EDAC test purposes.
FFPAS	O	Active high strobe used to latch the first failing Physical Address Register. Disabled after a fault has occurred until the FFPAR has been read.

Clock Signals

TCLK	O	Timer clock signal.
WDCLK	I	Oscillator input used by the watchdog timer.
OBTCLKIN	I	Ultra Stable clock oscillator input used for the On-Board Timer function.
OBTCLK	O	On-Board Timer clock output.
RTCLK	O	Real Time clock output.
CLKOUT	I	From the CPU, this clock is used as the PSC input clock.

Chip Select Signals

CSAREAN[0:3]	I	Active low indicates which area of memory is currently chip selected.
IOSELN	O	User IO area select. This output is asserted low to allow access to the user IO area as defined in MIL-STD-1750. The area is programmable within the PSC.

Bus Control

CPUGNTN	O	CPU bus grant. Sampled by the CPU on CLKOUT falling, an active low informs the processor that it has control of the system. If no other devices is granted, system control defaults to the CPU.
DMAGNTN	O	DMA bus grant. Sampled by the DMA on CLK falling, this pin is asserted low to inform the DMA that it is the current bus master.
EXTGNTN	O	External bus grant. This pin is asserted low to inform an external system that it is the current bus master.
LOCKN	I/O	Bus lock. This signal is sampled on each falling CLKOUT edge. If low, the bus arbiter will not allow the busses to be reassigned to another bus master.
DMAREQN	I	DMA bus request. This active low signal is driven low by an external DMA controller when it requests the bus, and is sampled on falling CLKOUT edges.
EXTREQN	I	External bus request. This active low signal is driven low by an external bus master when it requests the bus, and is sampled on falling CLKOUT edges.

Interrupts

WDINTN	O	Watchdog interrupt. This output is asserted low if an internal watchdog timeout occurs.
UARTINTN	O	Internal UART interrupt. This output is asserted low by either of the internal UARTs (or by an EDAC or parity error). The interrupt must be unmasked if it is to go active.
EDACINTN	O	EDAC interrupt. This output is asserted low if the NCERRN, CERRN or PEN inputs become active when enabled, and the interrupt is unmasked.
INTAKN	I	Interrupt acknowledge. This active low signal is asserted low by the CPU following receipt of an interrupt. It is used within the PSC to reset level sensitive interrupts.

Figure 12: Pin Descriptions

Faults

MPROEN	I	Memory protect error. Sampled on falling AS.
PEN	I	Parity Error input. Indicates that a parity fault has occurred on the most recent data bus transaction (input sampled on rising DSN).
EXADENINN	I	External address error. This active low input indicates that a memory access is outside the decoded address space.
EXADEOUTN	O	This active low output indicates that a memory or IO access error has occured. It can be activated by EXADEINN going low (memory error) or by the internal IO address decode flagging an error.
NCERRN	I	Non-correctable error. (active low) The system EDAC asserts this signal to indicate that a non-correctable error has occurred. Sampled on rising DSN.
CERRN	I	Correctable error. (active low) The system EDAC asserts this signal to indicate that a correctable error has occurred. The EDAC will have corrected the data if the EDAC 'correct' bit is set. Sampled on rising DSN.

UARTS:

RXDATA1	I	Serial interface received data, input to UART 1.
RXDATA2	I	Serial interface received data, input to UART 1.
TXDATA1	O	Serial interface transmit data, output from UART1.
TXDATA2	O	Serial interface transmit data, output from UART2.

Miscellaneous:

CONFWN	I	Configuration word read strobe.
SYSRESETN	O	System reset (active low). Held active either 10 clock cycles or until ROMWRN is inactive - whichever is the longer.
RESETN	I	Reset input for system (active low). Rising edge starts the SYSRESETN count.
WDINHIBITN	I	Disables (suspends) the watchdog timeout function.
EXRDYINN	I	External ready signal (active low) - forces RDYN low.
RDYN	O	Goes low to indicate that the current bus cycle can terminate.
ROMWRN	I	Non volatile memory write enable. If this signal is active low at reset, the external interface is granted and SYSRESETN is extended. If asserted after reset, the signal enables writing to non-volatile memory (Start-Up-ROM is enabled). Asynchronous, sampled on negative CLKOUT edges.
STOPN	I	This active low input is sampled on negative CLKOUT edges. When asserted, the WD timer and the OBT stop and the TCLK output is inhibited.
FFPAEN	O	Active low, this output should be used to enable the data from the first failing Physical Address Register onto the data bus. The enable goes active during a read of XIO address 0x 9F0B.

Figure 12: Pin Descriptions (continued)

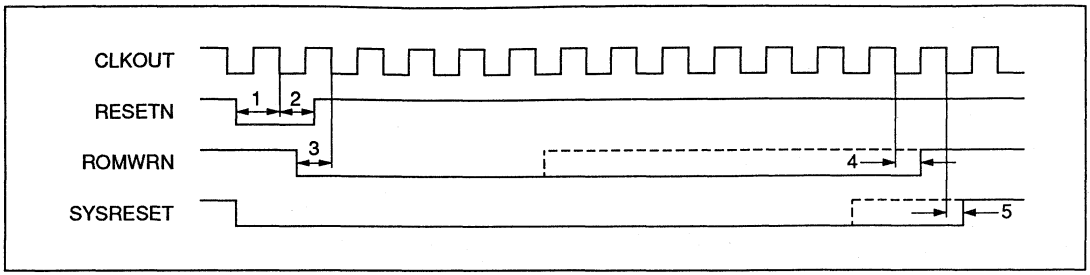


Figure 13: Reset Logic

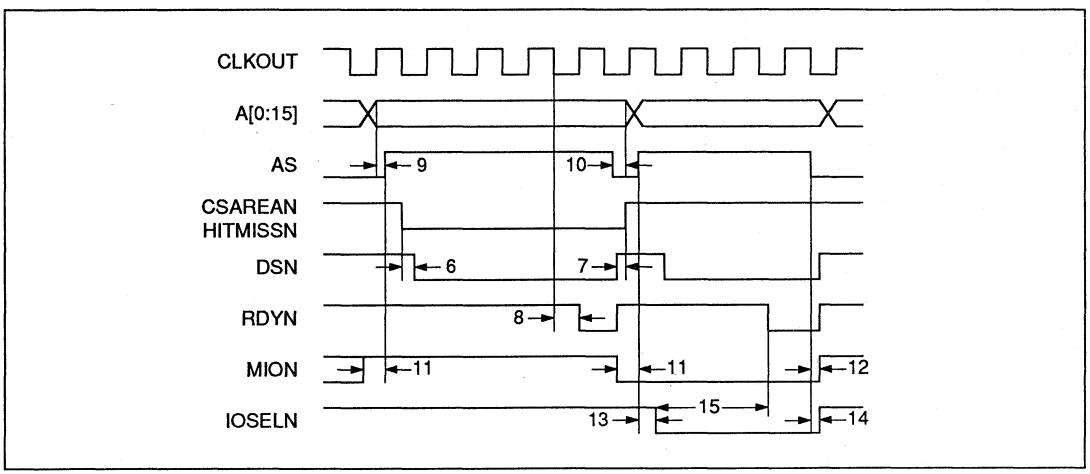


Figure 14: Wait State Generator

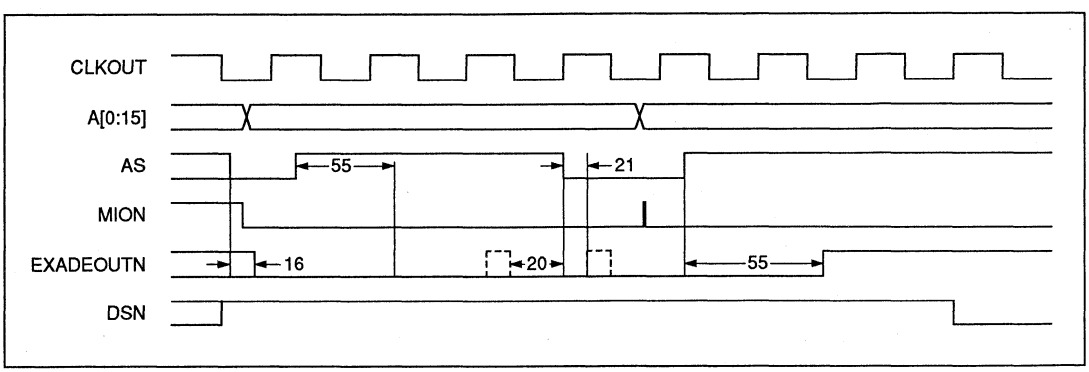


Figure 15: IO Address Range Validation

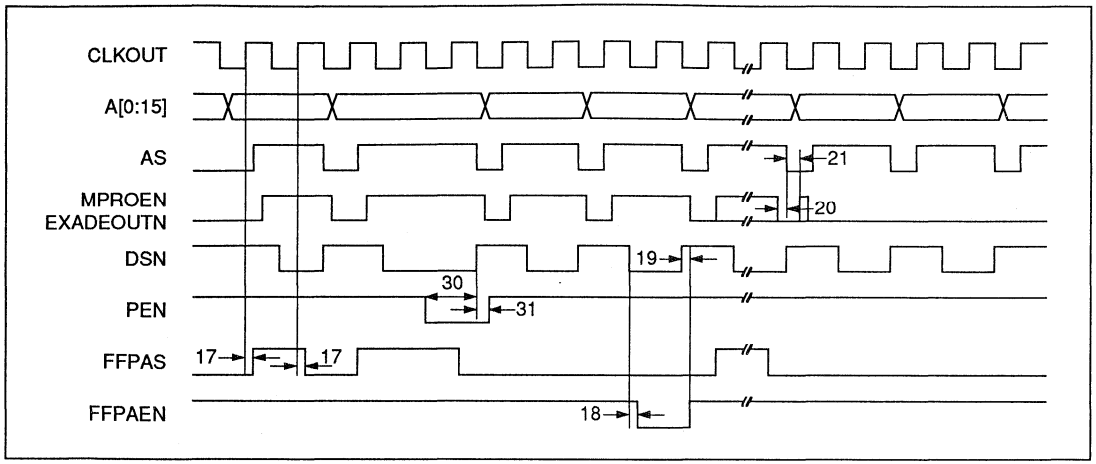


Figure 16: First Failing Physical Address Register Control

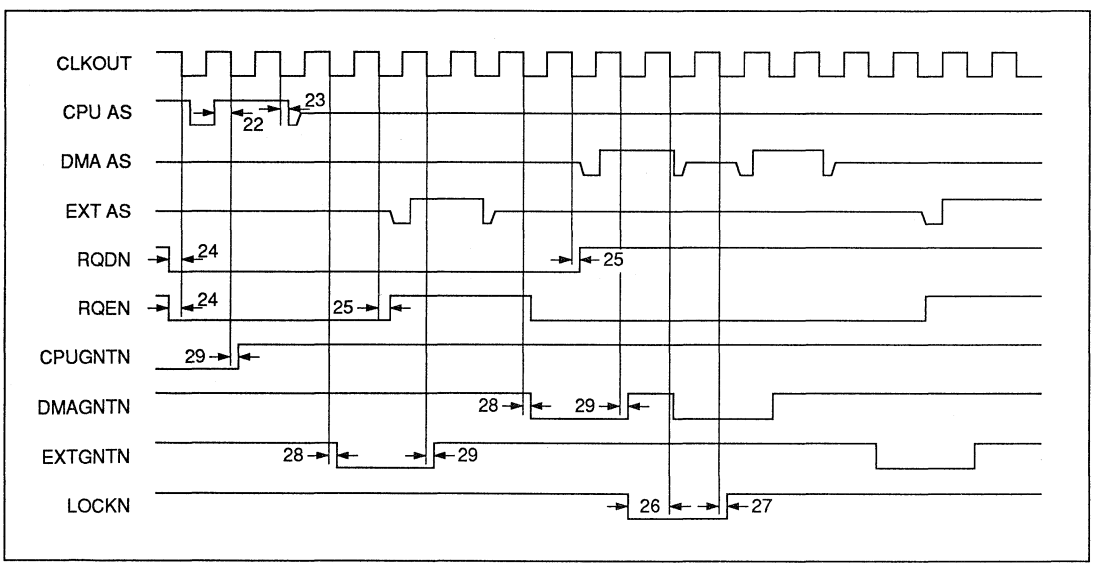


Figure 17: Bus Arbitration

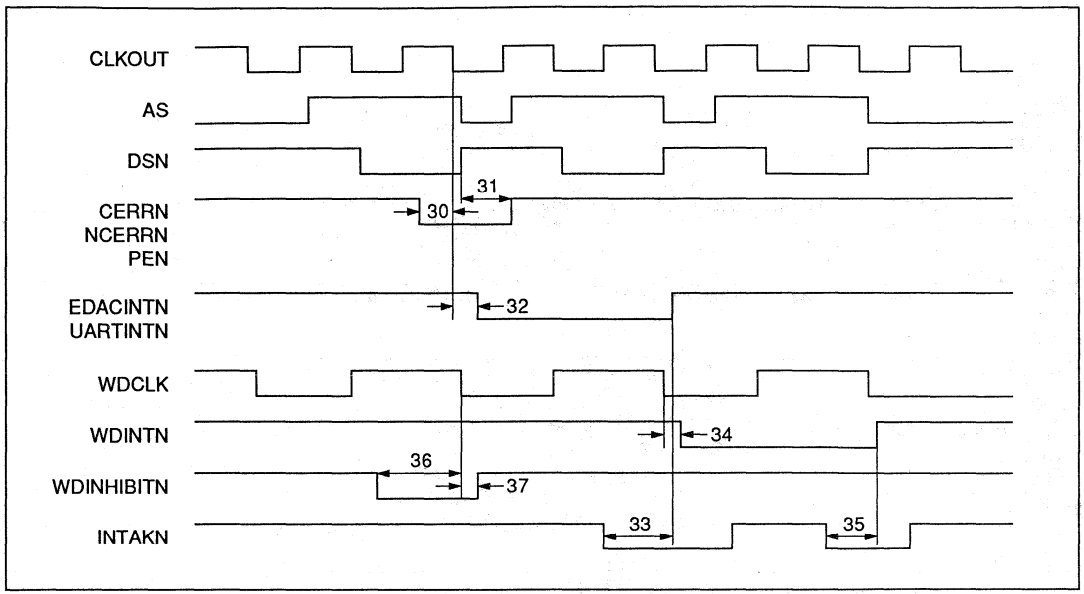


Figure 18: Interrupt Timings

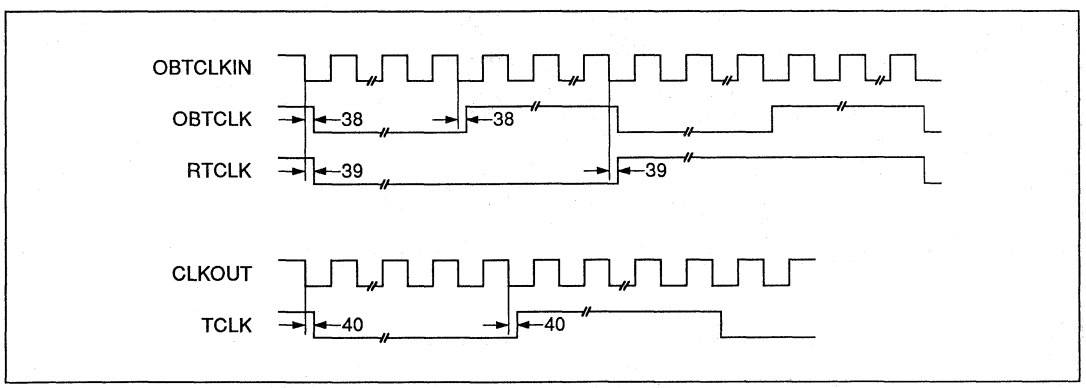


Figure 19: Clock Generation Logic

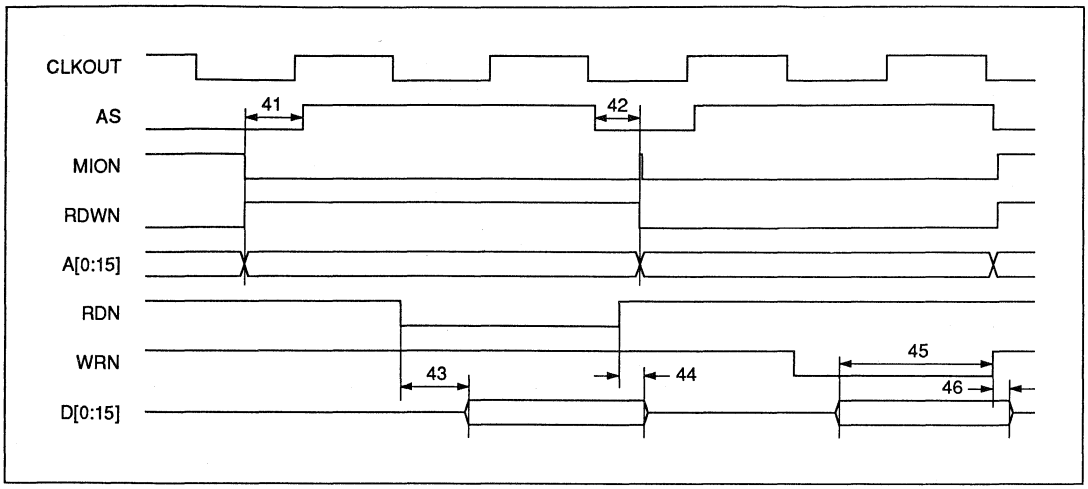


Figure 20: Reading and Writing Registers

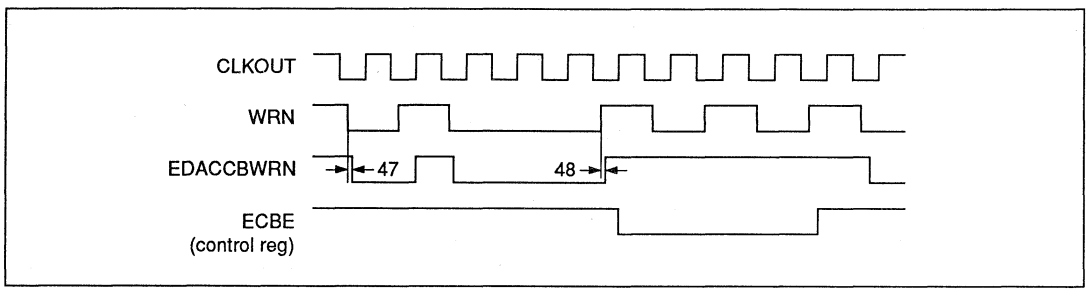


Figure 21: Check Bit Write Strobe Timings

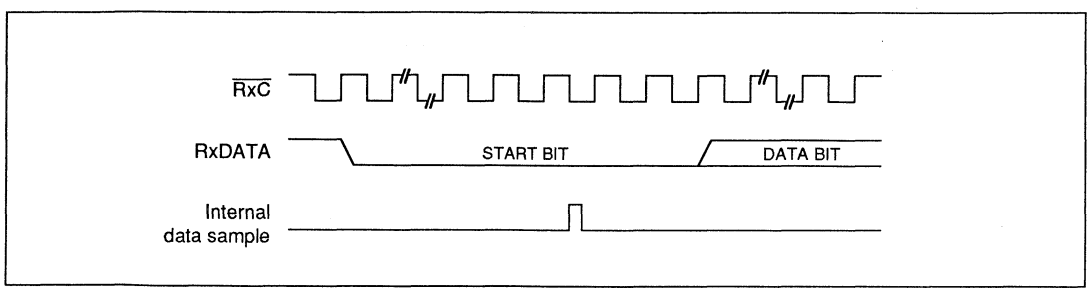


Figure 22: Receive Clock and Data

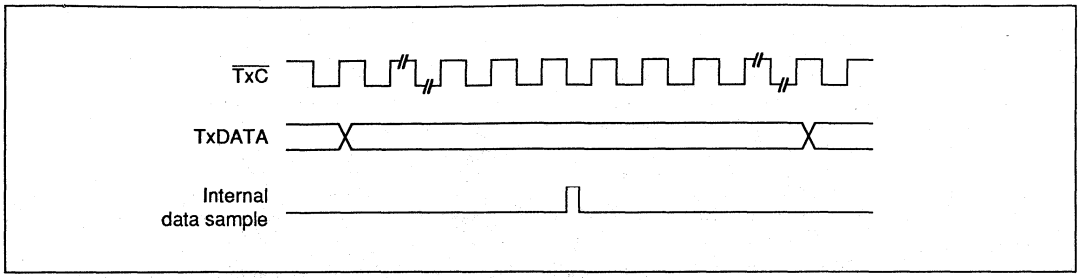


Figure 23: Transmitter Clock and Data

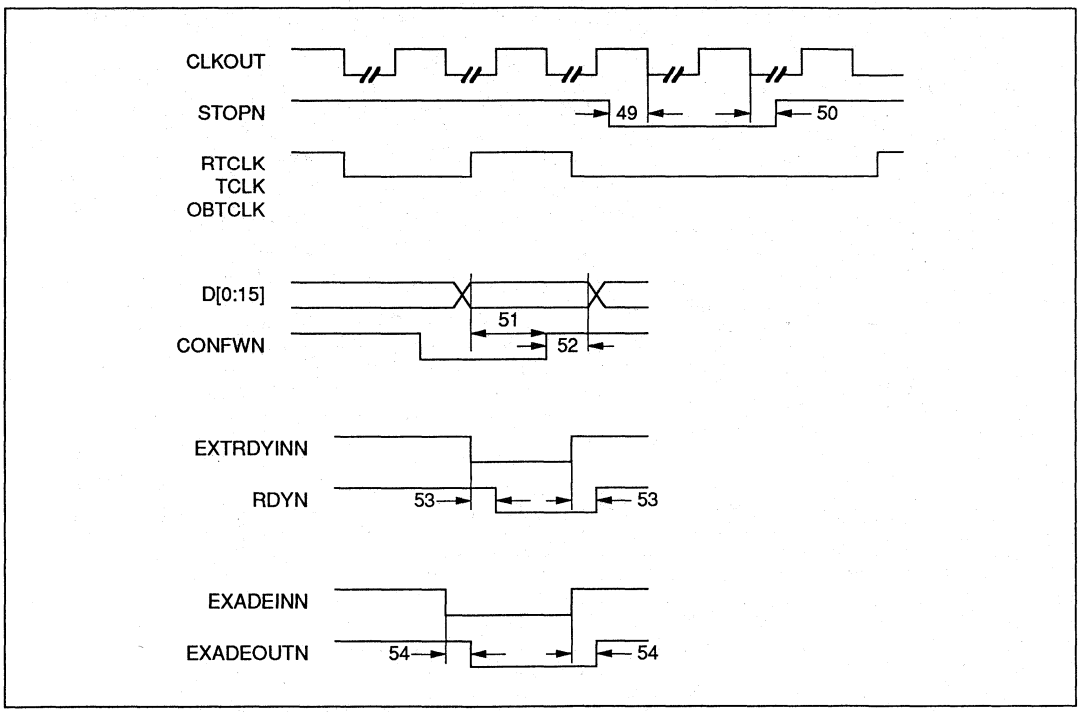


Figure 24: Miscellaneous Timings

No.	Parameter	Min.	Max.	Units
1	RESETN setup to CLKOUT falling			ns
2	RESETN hold after CLKOUT falling			ns
3	ROMWRN setup to CLKOUT falling			ns
4	ROMWRN hold after CLKOUT falling			ns
5	CLKOUT falling to SYSRESETN valid			ns
6	CSAREAN/HITMISSN setup to DSN falling			ns
7	CSAREAN/HITMISSN hold after DSN rising			ns
8	CLKOUT falling to RDYN falling			ns
9	Address setup to AS rising			ns
10	Address hold after AS falling			ns
11	MION setup to AS rising			ns
12	MION hold after AS falling			ns
13	AS rising to IOSELN valid			ns
14	AS falling to IOSELN valid			ns
15	IOSELN falling to RDYN falling			ns
16	AS falling to EXADEOUTN falling			ns
17	CLKOUT rising to FFPAS valid			ns
18	DSN falling to FFPAEN falling			ns
19	DSN rising to FFPAEN rising			ns
20	MPROEN/EXADEOUTN setup to AS falling			ns
21	MPROEN/EXADEOUT hold after AS falling			ns
22	AS setup to CLKOUT falling			ns
23	AS hold after CLKOUT falling			ns
24	RQEN/RQDN setup to CLKOUT falling			ns
25	RQEN/RQDN hold after CLKOUT falling			ns
26	LOCKN setup to CLKOUT falling			ns
27	LOCKN hold after CLKOUT falling			ns
28	CLKOUT falling to CPUGNTN/DMAGNTN/EXTGNTN falling			ns
29	CLKOUT falling to CPUGNTN/DMAGNTN/EXTGNTN rising			ns
30	CERRN/NCERRN/PEN setup to DSN rising			ns
31	CERRN/NCERRN/PEN hold after DSN rising			ns
32	CLKOUT falling to EDACINTN/UARTINTN falling			ns
33	INTAKN falling to EDACINTN/UARTINTN rising			ns
34	WDCLK falling to WDINTN falling			ns
35	INTAKN falling to WDINTN rising			ns
36	WDINHIBITN setup to WDCLK falling			ns
37	WDINHIBITN hold after WDCLK falling			ns
38	OBTCLK valid after OBTCLKIN falling			ns
39	RTCLK valid after OBTCLKIN falling			ns
40	TCLK valid after CLKOUT falling			ns
41	Address, MION and RDWN setup to AS rising			ns
42	Address, MION and RDWN hold after AS falling			ns
43	Data valid after RDN falling			ns
44	Data valid after RDN rising			ns
45	Data setup to WRN rising			ns
46	Data hold after WRN rising			ns
47	EDACCBWRN falling after WRN falling			ns
48	EDACCBWRN rising after WRN rising			ns
49	STOPN setup to CLKOUT falling			ns
50	STOPN hold after CLKOUT falling.			ns
51	Data setup to CONFWN rising			ns
52	Data hold after CONFWN rising			ns
53	EXTRDYINN valid to RDYN valid			ns
54	EXADEINN valid to EXADEOUTN valid			ns
55	AS rising to EXADEOUTN valid			ns

† This timing includes MA31751 Setup Cycles and Built In Test Cycles.
Mil-Std-883, Method 5005, Subgroups 9, 10, 11.
Note: TL = Low CLK period (ns), TH = High CLK period (ns).
Test Conditions: Vdd = 5.0V ±10%, Temperature = -55°C to 125°C, Vil = 0.0V, Vih = Vdd.
Output loads: All test load 1 unless otherwise specified.
Output Threshold: 50% Vdd (Load 1), Vss+1V, Vdd-1V (load2).

Figure 25: Timing Parameters

CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 26: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Max	Units
Clock Frequency (CLKOUT)	0	16	MHz
Recommended Clock Duty Cycle	45	55	%

Vdd=5V±10% over full operating temperature range.
Mil-Std-883, method 5005, subgroups 7, 8A, 8B.

Figure 27: Operating AC Electrical Characteristics

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)		Units
			Min	Max	
V_{DD}	Supply Voltage	-	4.5	5.5	V
V_{IH}	Input High Voltage	-	80%V_{DD}	-	V
V_{IL}	Input Low Voltage	-	-	20%V_{DD}	V
V_{CKH}	CLKOUT Input High Voltage	-	V_{DD}-0.5	-	V
V_{CKL}	CLKOUT Input Low Voltage	-	-	V_{SS}+0.5	V
V_{OH}	Output High Voltage	I_{OH} = 3mA	V_{DD}-0.5	-	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA	-	V_{SS}+0.4	V
I_{IH}	Input High Current (Note 1)	-	-	10	µA
I_{IL}	Input Low Current (Note 1)	-	-	-10	µA
I_{OZH}	I/O Tristate High Current (Note 1)	-	-	50	µA
I_{OZL}	I/O Tristate Low Current (Note 1)	-	-	-50	µA
I_{DDYN}	Dynamic Supply Current @16MHz	-	-	110	mA
I_{DDS}	Static Supply Current	-	-	10	mA

V_{DD}=5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3.
Note 1: Guaranteed but not tested at low temperature (-55°C).

Figure 28: Operating DC Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 28 at +25°C
2	Static characteristics specified in Figure 28 at +125°C
3	Static characteristics specified in Figure 28 at -55°C
7	Functional characteristics specified in Figure 27 at +25°C
8A	Functional characteristics specified in Figure 27 at +125°C
8B	Functional characteristics specified in Figure 27 at -55°C
9	Switching characteristics specified in Figure 25 at +25°C
10	Switching characteristics specified in Figure 25 at +125°C
11	Switching characteristics specified in Figure 25 at -55°C

Figure 29: Definition of MIL-STD-883, Method 5005 Subgroups

PIN ASSIGNMENTS AND OUTLINES

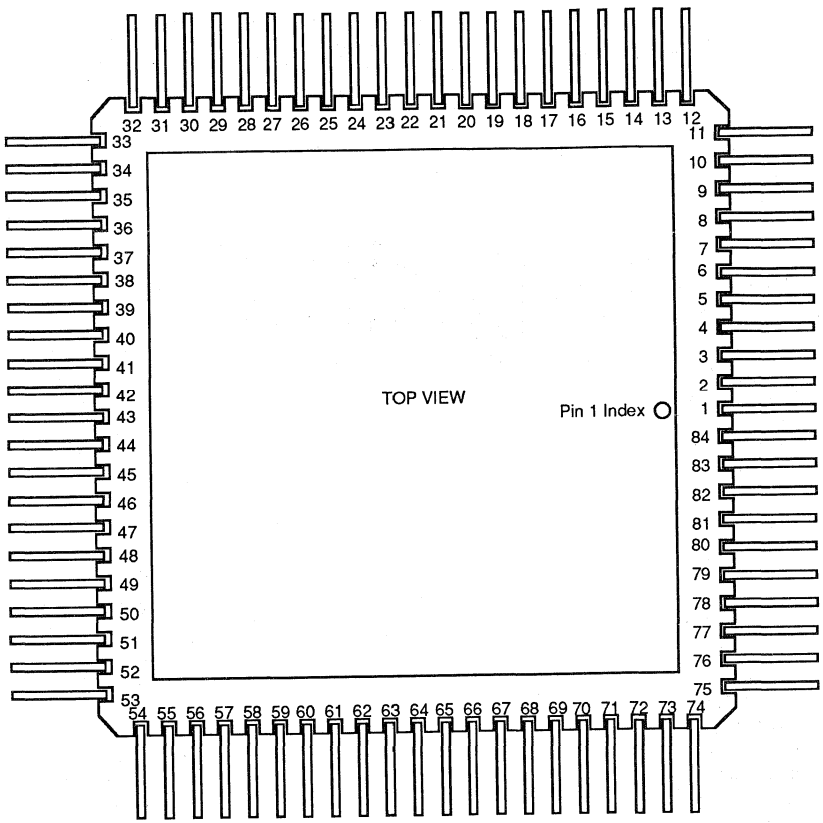


Figure 30: 84-Lead Flatpack - Package Style F

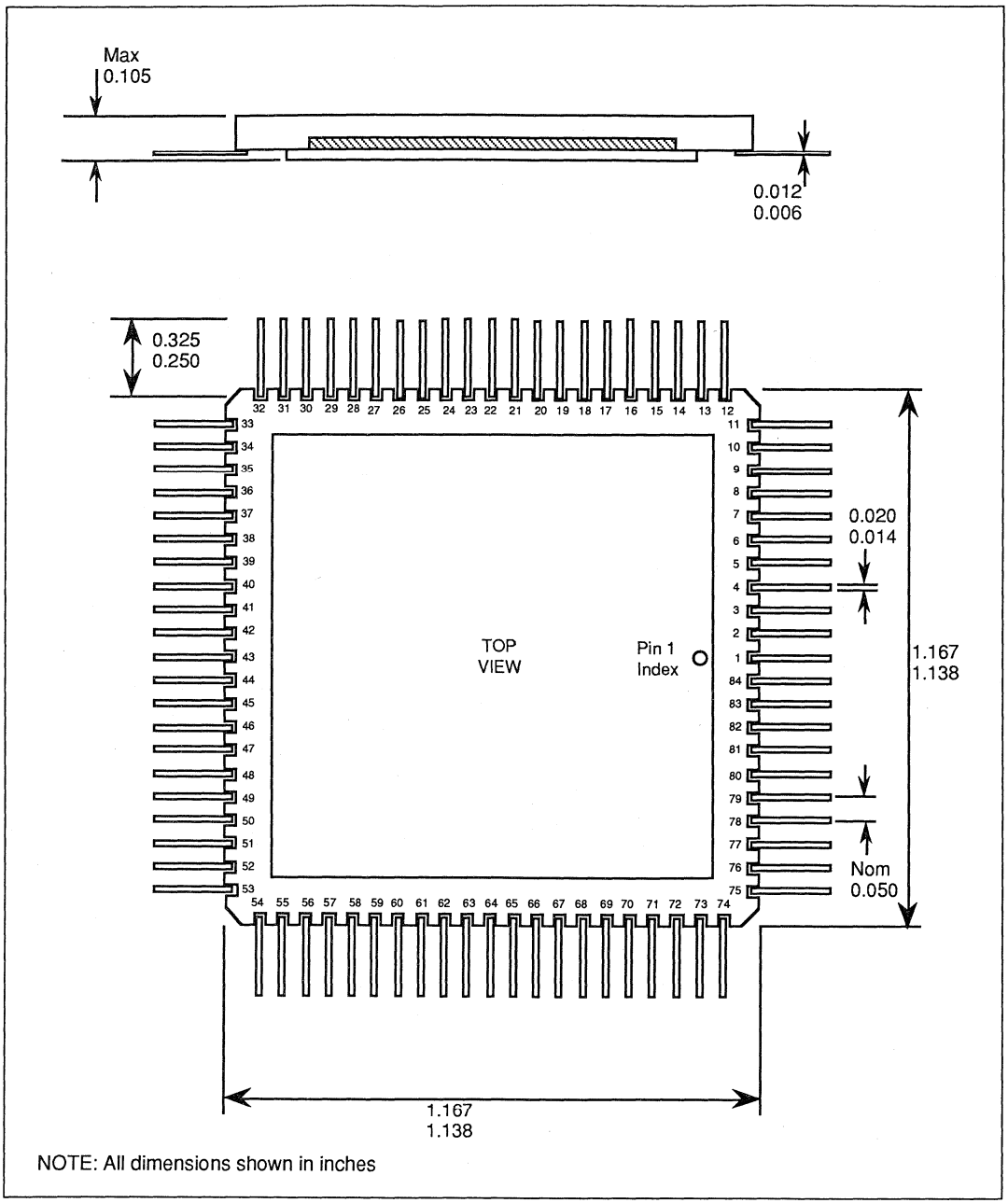
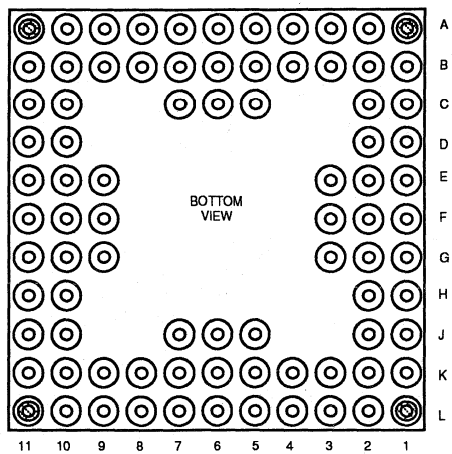
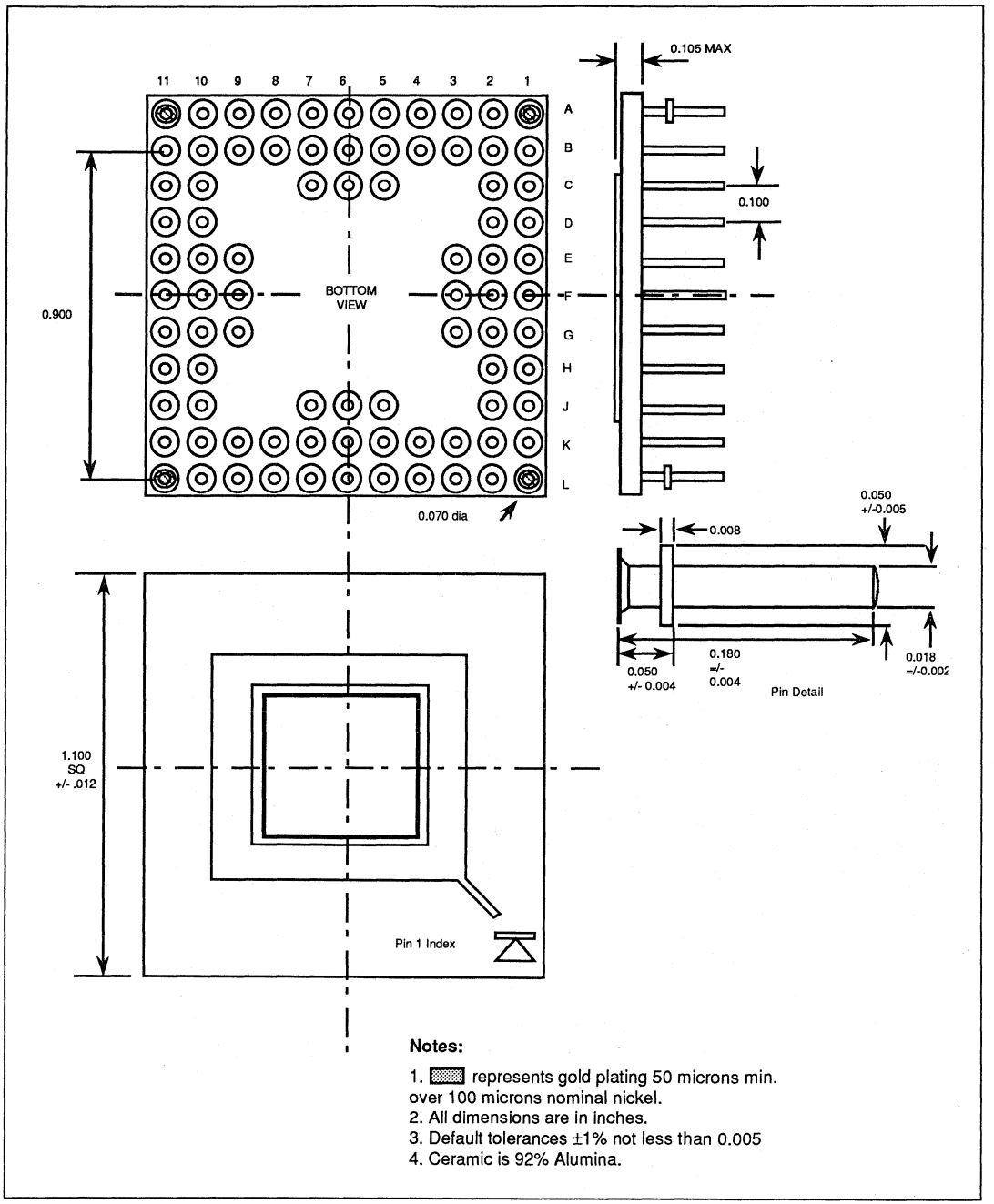


Figure 31: 84-Lead Flatpack - Package Style F



A1		B11		F9		K2	
A2		C1		F10		K3	
A3		C2		F11		K4	
A4		C5		G1		K5	
A5		C6		G2		K6	
A6		C7		G3		K7	
A7		C10		G9		K8	
A8		C11		G10		K9	
A9		D1		G11		K10	
A10		D2		H1		K11	
A11		D10		H2		L1	
B1		D11		H10		L2	
B2		E1		H11		L3	
B3		E2		J1		L4	
B4		E3		J2		L5	
B5		E9		J5		L6	
B6		E10		J6		L7	
B7		E11		J7		L8	
B8		F1		J10		L9	
B9		F2		J11		L10	
B10		F3		K1		L11	

Figure 32: 84-Pin Grid Array - Package Style A



Notes:

1. ▨ represents gold plating 50 microns min. over 100 microns nominal nickel.
2. All dimensions are in inches.
3. Default tolerances ±1% not less than 0.005
4. Ceramic is 92% Alumina.

Figure 33: 84-Pin Grid Array - Package Style A

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019 Ionizing Radiation (total dose).

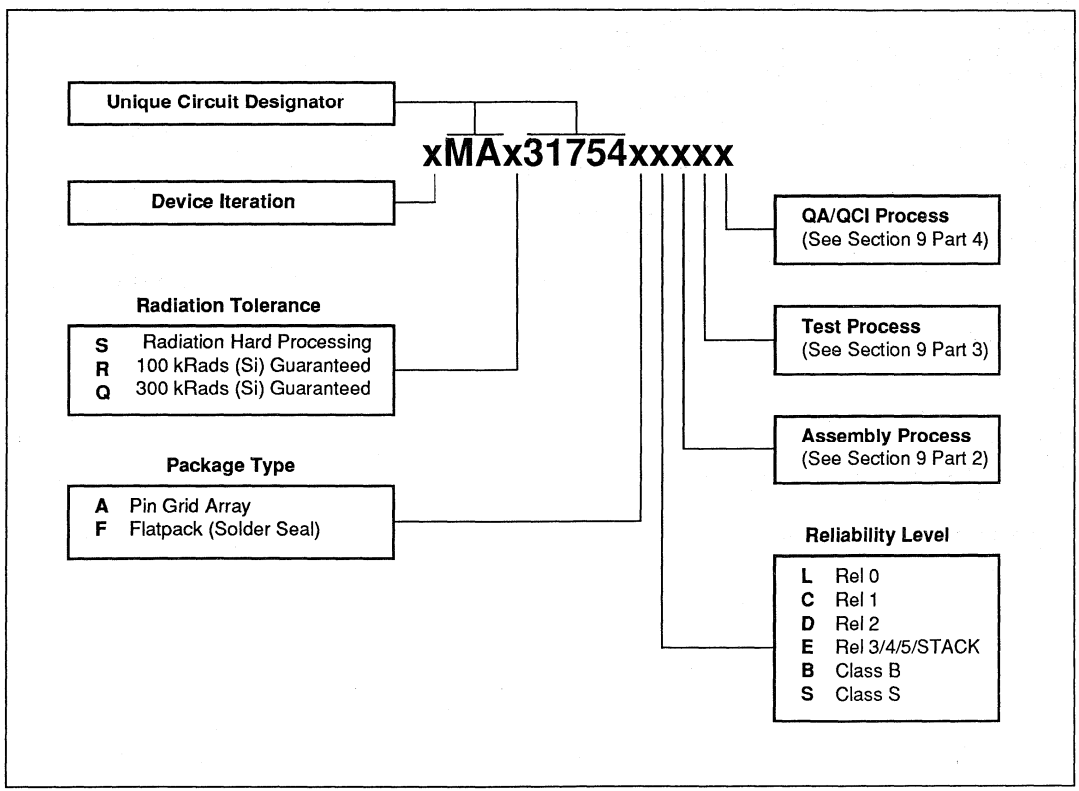
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 34: Radiation Hardness Parameters

ORDERING INFORMATION



DS3572-2.3

MA31755

16-BIT FEEDTHROUGH ERROR DETECTION & CORRECTION UNIT (EDAC)

The MA31755 is a 16 bit Error Detection and Correction Unit intended for use in high integrity systems for monitoring and correcting data values retrieved from memory. The EDAC is placed in the data bus between the processor and the memory to be protected. Extra check bits added at each memory location are programmed transparently by the EDAC during a processor write cycle. The entire checkword and data combination is verified on read cycles. If any one bit in the incoming data stream is at fault the EDAC can correct the fault transparently, presenting the corrected 16-bit value to the processor. An error in two bits can be detected but cannot be corrected. Both the correctable and uncorrectable error conditions are signalled to the system to allow the processor to take action as required. Parity is passed through the device unchanged as data bus bit 16.

Tri-statable bus transceivers with a high drive capability are incorporated at the MD and CB busses which allows the usual bus driver devices to be removed and reduces the overall timing overhead imposed on the data bus. Although designed primarily for MA31750 application, this part may be used in almost any 16-bit processor system requiring high data integrity.

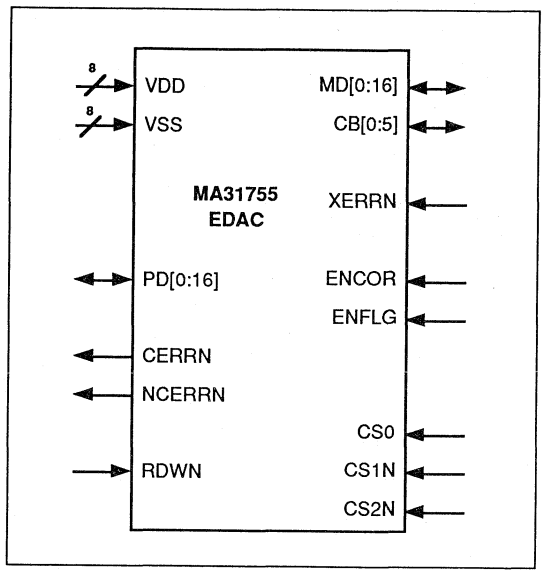


Figure 1: Chip Signals

FEATURES

- Fast Feedthrough (35ns Detect and Correct Cycle)
- 16-Bit Operation with 6 Check Bits
- Radiation Hard CMOS/SOS Technology
- Feedthrough Operation
- Error Corrected/Uncorrected Flags
- High Drive Capability on Memory Busses

1. PIN DESCRIPTIONS

POWER

VDD x8	Input	-	Supply - 5V nominal (all must be connected)
VSS x8	Input	-	Circuit 0V reference (all must be connected)

BUSSES

PD[0:16]	I/O	Active High	Processor data bus + parity bit (bit 16)
MD[0:16]	I/O	Active High	Memory data bus + parity bit (bit 16)
CB[0:5]	I/O	Active High	Memory check bit bus

ERROR FLAGS AND CONTROL

CERRN	Output	Active Low	Asserted low when a correctable (1 bit) error occurs (ENFLG must be asserted high)
NCERRN	Output	Active Low	Asserted low when an uncorrectable error occurs (ENFLG must be asserted high)
XERRN	Input	Active Low	External error feedthrough to NCERRN line.
ENCOR	Input	Active High	Enables correction of data when high. Data is passed through uncorrected when this line is low.
ENFLG	Input	Active High	Enables the flagging of incorrect data when high. When this line is low the two error flag lines are held inactive.

DEVICE AND BUFFER CONTROL

CS2N	Input	Active Low	Enables device and output buffers.
CS1N	Input	Active Low	Enables device and output buffers.
CS0	Input	Active High	Enables device and output buffers.
RDWN	Input	-	High indicates a read cycle, low indicates a write cycle.

2. FUNCTIONAL DESCRIPTION

2.0 GENERAL

The EDAC is of feedthrough type with 16 data bits, 1 parity bit and 6 check bits, giving the ability to correct all single bit errors and detect all double bit errors. Errors in more than two bits may result in any combination of error flags being raised and the data may be arbitrarily modified by the correction circuitry.

The EDAC is placed in the data bus between the processor and the memory to be protected. It forms the interface between the 23-bit memory bus and the 17-bit processor bus. Tri-statable bus transceivers with a high drive capability are incorporated at both busses.

2.1 TESTING THE EDAC AND MEMORY SYSTEM

No specific hardware for testing is provided by the MA31755 since this would compromise the speed performance of the part in normal operation. However, it is possible to fully test the EDAC function and the generation of the error signals without this. The system should provide a means by which the check bit memory may be dynamically write-enabled and disabled - this may be provided by gating write strobe on the check bit memory with a latched control bit. By writing first with check bits enabled, then with them disabled, suitable seed values may be constructed which have the required pattern of bits to test each feature of the EDAC operation. A similar approach may be taken when testing the check bit memory.

By disabling the EDAC (asserting ENCOR low) the processor may have direct access to the unmodified 17-bit data from the memory. Suitable test patterns may be applied to test each memory location as required.

2.2 BUS CONTROL

There are four signals which control the drive status of the EDAC external busses: RDWN, CS2N, CS1N and CS0. The relationship to each other and to the EDAC busses is shown in Figure 2 below. The timing of these signals is shown in Figures 6 and 7.

RDWN	CS2N	CS1N	CS0	Bus state	
				Processor	Memory
X	High	X	X	Tristate	Tristate
X	X	High	X	Tristate	Tristate
X	X	X	Low	Tristate	Tristate
High	Low	Low	High	Output	Input
Low	Low	Low	High	Input	Output

Figure 2: Bus Control

2.3 INTERNAL OPERATION

2.3.1 Check Bit Generation

On write cycles the processor data word, PD[0:15], and the processor parity bit ,PD[16], are passed directly to the memory data bus, MD[0:15], and the memory parity bit, MD[16].

The check bits, CB[0:5], are derived by 6 parity generators operating on sets of 8 bits of the processor data word, PD[0:15], as shown in Figure 3 below:

CB	Parity	PD															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Even			X	X				X	X	X	X	X				X
1	Even		X			X	X	X	X		X		X			X	
2	Odd	X			X			X				X		X	X	X	X
3	Odd		X	X			X						X	X	X	X	X
4	Even	X				X	X	X	X	X		X			X		
5	Even	X	X	X	X	X				X	X			X			

Figure 3: Check Bit Generation

2.3.2 Syndrome Generation

The syndrome generation logic checks the sense of the check bits with respect to the memory data word. Six 9-input parity checkers generate the syndrome bits, SY[0:5], according to figure 4 below:

SY	Parity	MD																CB					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	0	1	2	3	4	5
0	Even			X	X				X	X	X	X	X				X	X					
1	Even		X			X	X	X	X		X		X			X			X				
2	Odd	X			X			X				X		X	X	X	X			X			
3	Odd		X	X			X						X	X	X	X	X				X		
4	Even	X				X	X	X	X	X		X			X							X	
5	Even	X	X	X	X	X				X	X			X									X

Figure 4: Syndrome Generation

If there are no errors in the memory data word, MD[0:15], or the check bits, CB[0:5], then all of the syndrome bits, SY[0:5], will be set low.

A single bit error in the memory data word, MD[0:15], will cause 3 syndrome bits to be set high. However, a single bit error in the check bits, CB[0:5], will cause only 1 syndrome bit to be set high. A two bit error in the memory data word and/or the check bits will cause either 2, 4, 5 or 6 syndrome bits to be set.

Three or more errors in the memory data word and/or the check bits will cause an undefined number of syndrome bits to be set. This will cause the operation of the device in respect of the states of CERRN, NCERRN and data on the PD bus to be unpredictable.

2.3.3 Correction

With no syndrome bits set data will pass through from the MD bus to the PD bus unchanged. When a single bit error occurs in the memory data word, MD[0:15], the three syndrome bits which are set identify which data bit is in error. The correction logic decodes these syndrome bits and will correct the error provided the correction enable input, ENCOR, is high.

2.3.4 Flag Generation

The correctable error flag,CERRN, is driven low whenever 1 or 3 syndrome bits are set and flags are enabled (ENFLG=1).

The non-correctable error flag, NCERRN, is driven low whenever 2, 4, 5 or 6 Syndrome bits are set and flags are again enabled (ENFLG=1). NCERRN will also be driven low should the external error input, XERRN, be driven low at any time. Note: this external error feedthrough from XERRN to NCERRN operates independently of ENFLG and the Chip Select inputs (CS0, CS1N & CS2N).

Flags are enabled provided the ENFLG input is high and the device is selected. Note: the flags are not disabled on write cycles and therefore can indicate errors on write operations caused by faults on the Memory Data Bus and the Check Bit Bus.

2.3.5 Internal Structure

Figure 5 below shows the internal block diagram representing the internal architecture of the MA31755.

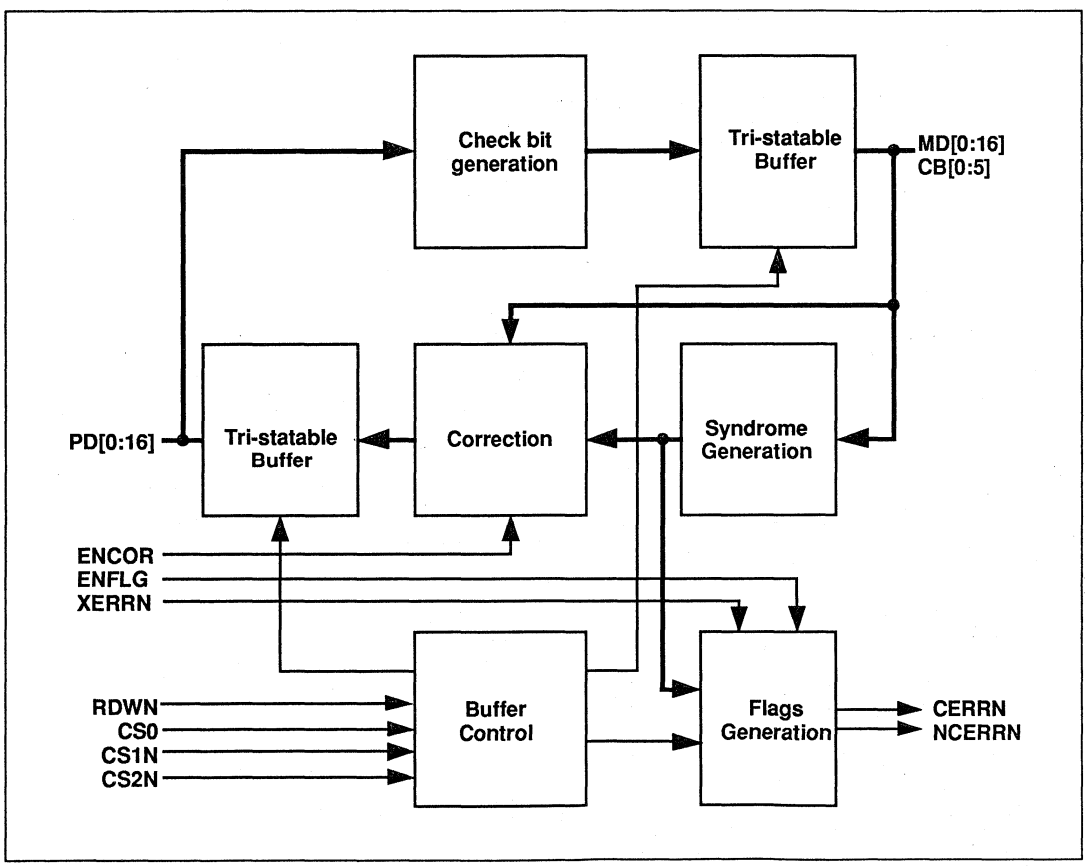


Figure 5: Block Diagram of the Internal Architecture of the MA31755

3. TIMING DIAGRAMS

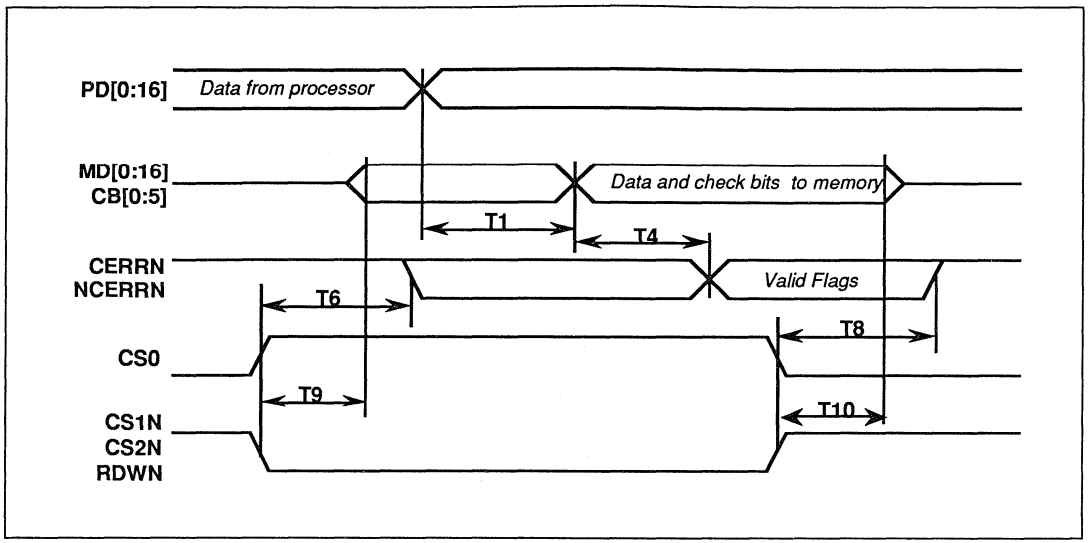


Figure 6 : Processor Write Timings (ENFLG = 1)

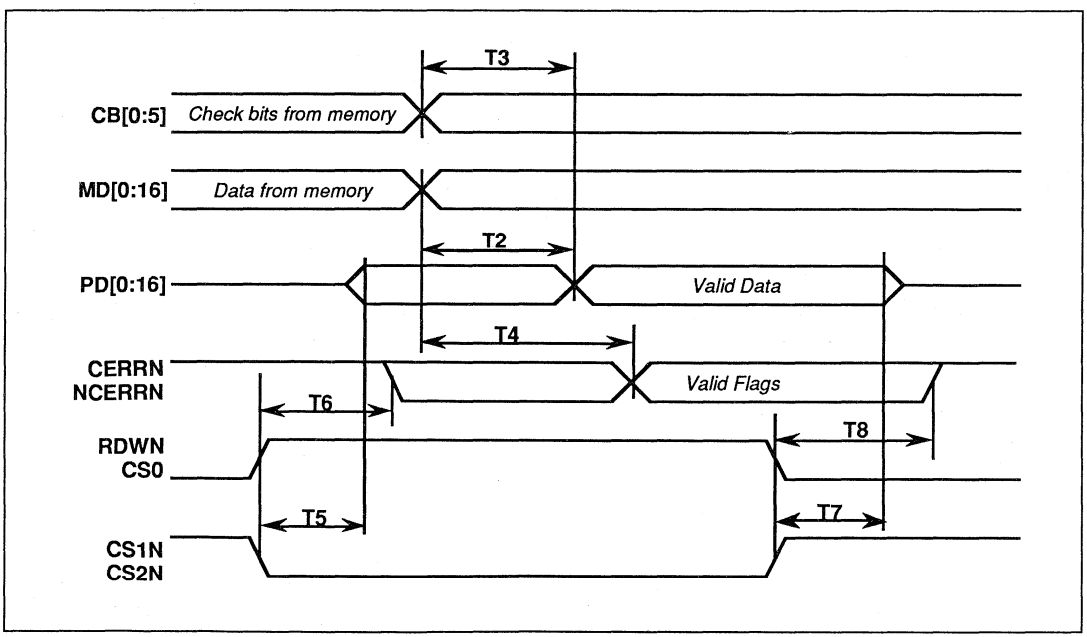


Figure 7: Processor Read Timings (ENCOR and ENFLG=1)

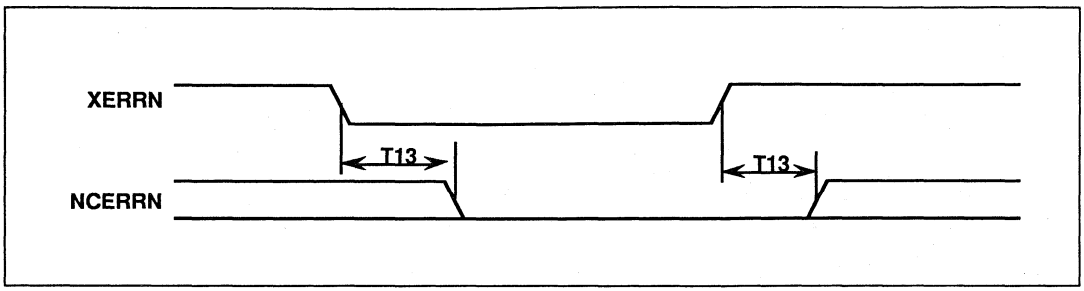


Figure 8: External Error Feedthrough Timing (ENFLG=X ,CS0=X, CS1N /CS2N=X)

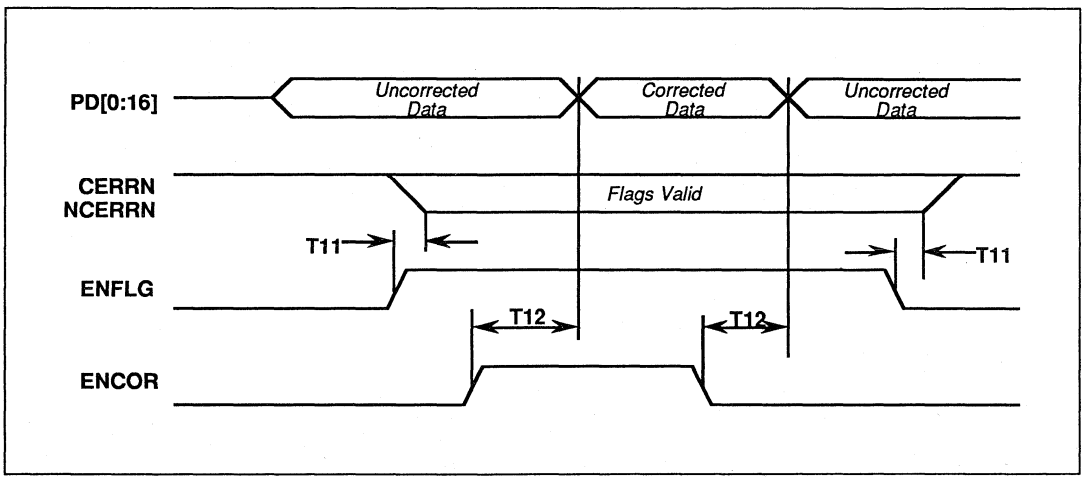


Figure 9: Correction and Error flag enable/disable timings (CS0=1, CS1N/CS2N = 0)

4. AC CHARACTERISTICS

Parameter	Description	Min	Max	Units	Notes
T1	PD[0:16] to MD[0:16] , CB[0:5] valid	-	25	ns	CL = 150pF
T2	MD[0:16] to PD[0:16] valid	-	30	ns	CL = 50pF
T3	CB[0:5] to PD[0:16] valid	-	35	ns	CL = 50pF
T4	MD[0:16] to CERRN and NCERRN valid CB[0:5] to CERRN and NCERRN valid	-	40	ns	CL = 50pF
T5	RDWN, CS0 rising to PD[0:16] driven (processor read) CS1N, CS2N falling to PD[0:16] driven (processor read)	5	20	ns	CL = 50pF
T6	CS0 rising to error flags changing CS1N, CS2N falling to error flags changing	-	25	ns	CL = 50pF
T7	RDWN, CS0 falling to PD[0:16] Hi-Z CS1N,CS2N rising to PD[0:16] Hi-Z	-	30	ns	CL = 50pF
T8	CS0 falling to error flags high CS1N, CS2N rising to error flags high	-	25	ns	CL = 50pF
T9	RDWN, CS1N and CS2N falling to MD[0:16] and CB[0:5] driven (processor write) CS0 rising to MD[0:16] and CB[0:5] driven (processor write)	5	20	ns	CL = 150pF
T10	CS0 falling to MD[0:16] and CB[0:5] Hi-Z RDWN, CS1N, CS2N rising to MD[0:16] and CB[0:5] Hi-Z	5	25	ns	CL = 150pF
T11	ENFLG to CERRN and NCERRN valid	-	20	ns	CL = 50pF
T12	ENCOR to PD[0:16] valid	-	20	ns	CL = 50pF
T13	XERRN to NCERRN valid	-	10	ns	CL = 50pF

Mil-Std-883, method 5005, subgroups 9, 10, 11

Figure 10: Timing Parameters

5. DC CHARACTERISTICS AND RATINGS

Symbol	Description	Min.	Max.	Units
VDD	Supply voltage	-0.5	7	V
VI	Input voltage	-0.3	VDD+0.3	V
TA	Operating temperature	-55	+125	°C
TS	Storage temperature	-65	+150	°C

Figure 11: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Description	Min	Max	Unit	Notes
VOH	Output high voltage	Vdd- 0.5	-	V	IOH = 15mA on MD[0:16] / CB[0:5] IOH = 5mA on other outputs.
VOL	Output low voltage	-	Vss+0.5	V	IOL = -15mA on MD[0:16] / CB[0:5] IOL = -5mA on other outputs.
VIH	Input high voltage	Vdd-1.5	-	V	
VIL	Input low voltage	-	Vss+1.5	V	
IIL, IIH (Note 1)	Input current high/low	-	10	uA	
IOZ (Note 1)	Output tri-state leakage	-	0.1	mA	VO = 0 to VDD
ISS	Standby current	-	10	mA	
IDD	Operating current	-	100	mA	

Conditions VDD = 4.5 to 5.5V, TA = -55 to +125°C
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Worst case at TA = +125°C, guaranteed but not tested at TA = -55°C.

Figure 12: Operating Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 12 at +25°C
2	Static characteristics specified in Figure 12 at +125°C
3	Static characteristics specified in Figure 12 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 10 at +25°C
10	Switching characteristics specified in Figure 10 at +125°C
11	Switching characteristics specified in Figure 10 at -55°C

Figure 13: Definition of Subgroups

6. APPLICATIONS INFORMATION

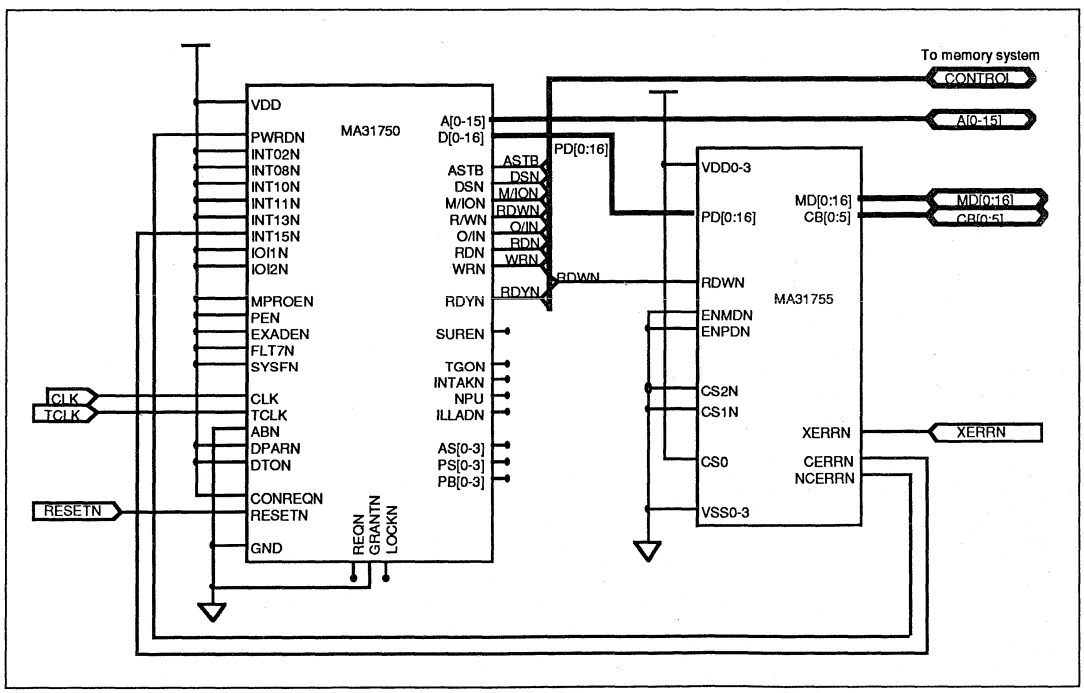


Figure 14: Basic System Diagram for the MA31755 with the MA31750

7. PACKAGING

The device will be supplied in a 68-pin PGA for development with a 68-pin flatpack option for flight parts.

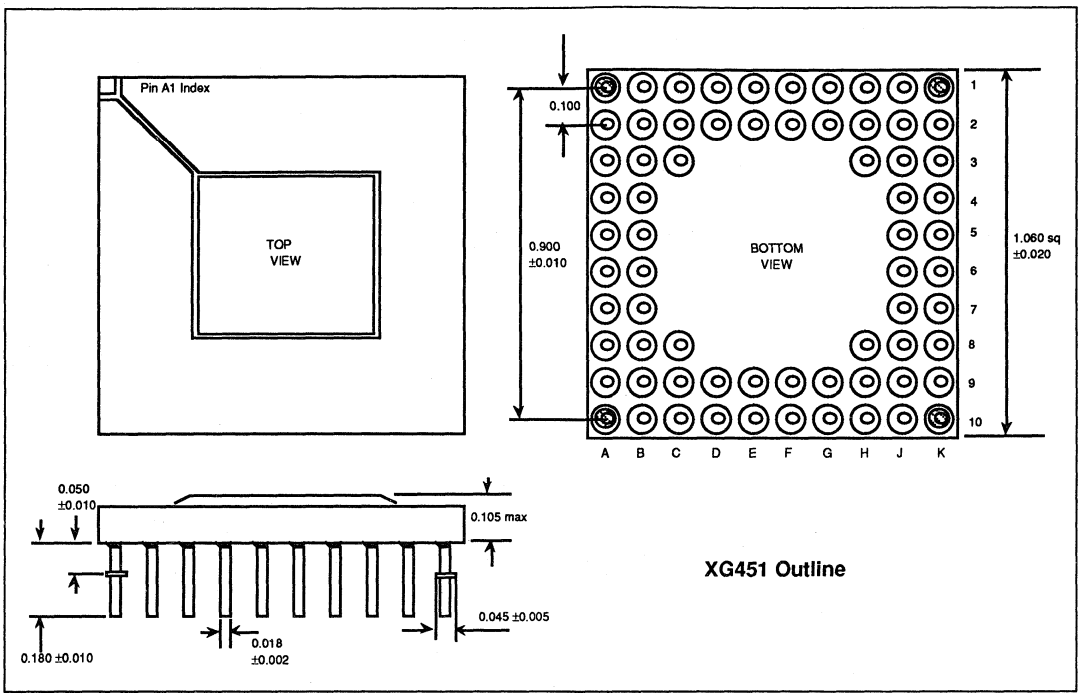


Figure 15: Dimensioned Drawing for the 68-pin PGA Package

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	CB05	C1	CB02	G9	CS0	K3	MD08
A2	NCERRN	C2	CB04	G10	PD00	K4	MD06
A3	RDWN	C3	VDD	H1	MD15	K5	VDD
A4	PD16	C8	VDD	H2	MD12	K6	NC
A5	PD14	C9	PD07	H3	VDD	K7	MD04
A6	VDD	C10	PD04	H8	VDD	K8	MD03
A7	PD13	D1	CB00	H9	ENFLG	K9	MD01
A8	PD11	D2	CB01	H10	CS1N	K10	ENCOR
A9	PD10	D9	PD05	J1	MD13		
A10	PD08	D10	PD03	J2	GND		
B1	CB03	E1	GND	J3	MD10		
B2	GND	E2	NC	J4	MD07		
B3	CERRN	E9	PD02	J5	GND		
B4	XERRN	E10	PD01	J6	MD05		
B5	PD15	F1	VDD	J7	MD02		
B6	GND	F2	NC	J8	MD00		
B7	PD12	F9	GND	J9	GND		
B8	PD09	F10	VDD	J10	CS2N		
B9	GND	G1	MD16	K1	MD11		
B10	PD06	G2	MD14	K2	MD09		

Figure 16: Pinout for the 68-pin PGA Package

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

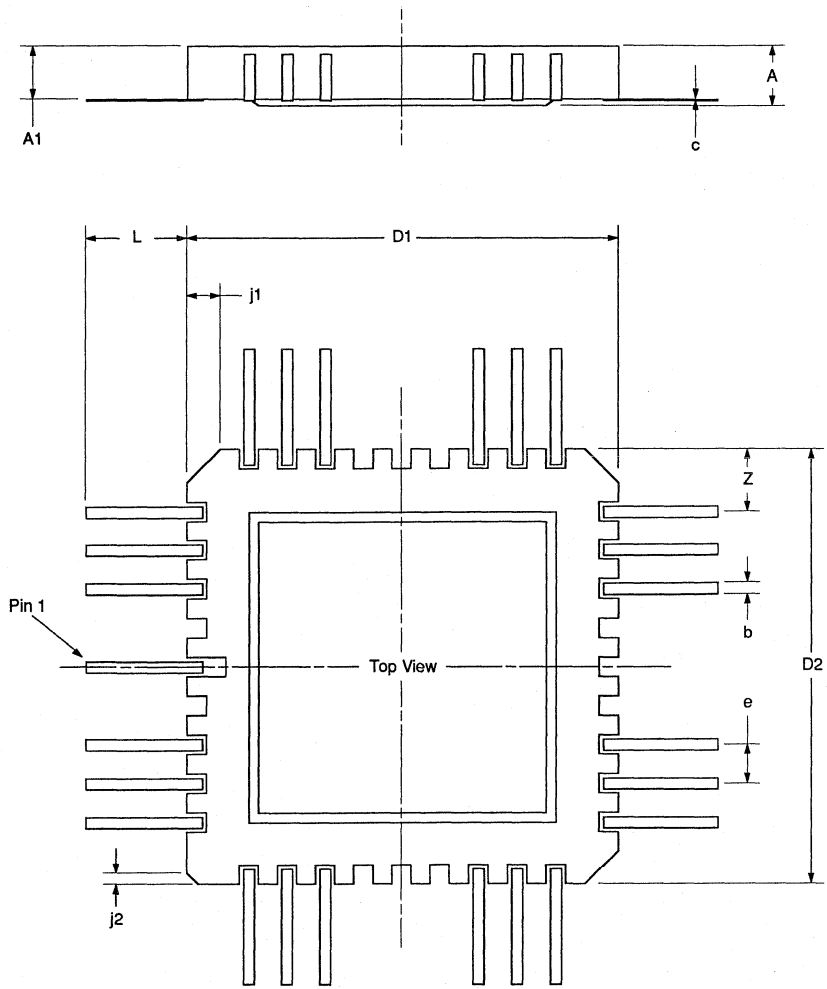


Figure 17: Dimensioned Drawing for the 68-pin Flatpack Package Topbraze

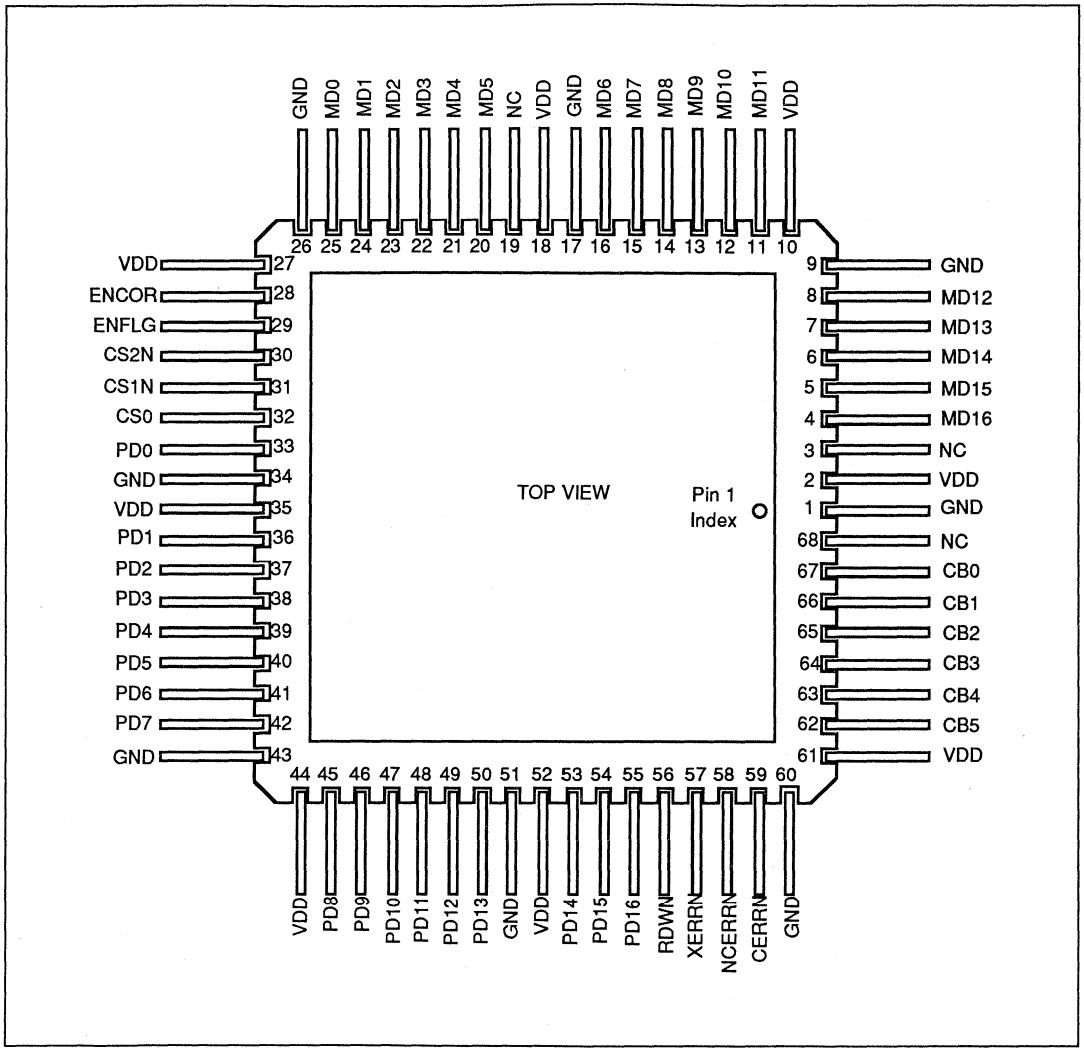


Figure 18: Pinout for the 68-pin Flatpack Package

8. RADIATION TOLERANCE

8.1 TOTAL DOSE RADIATION TESTING

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

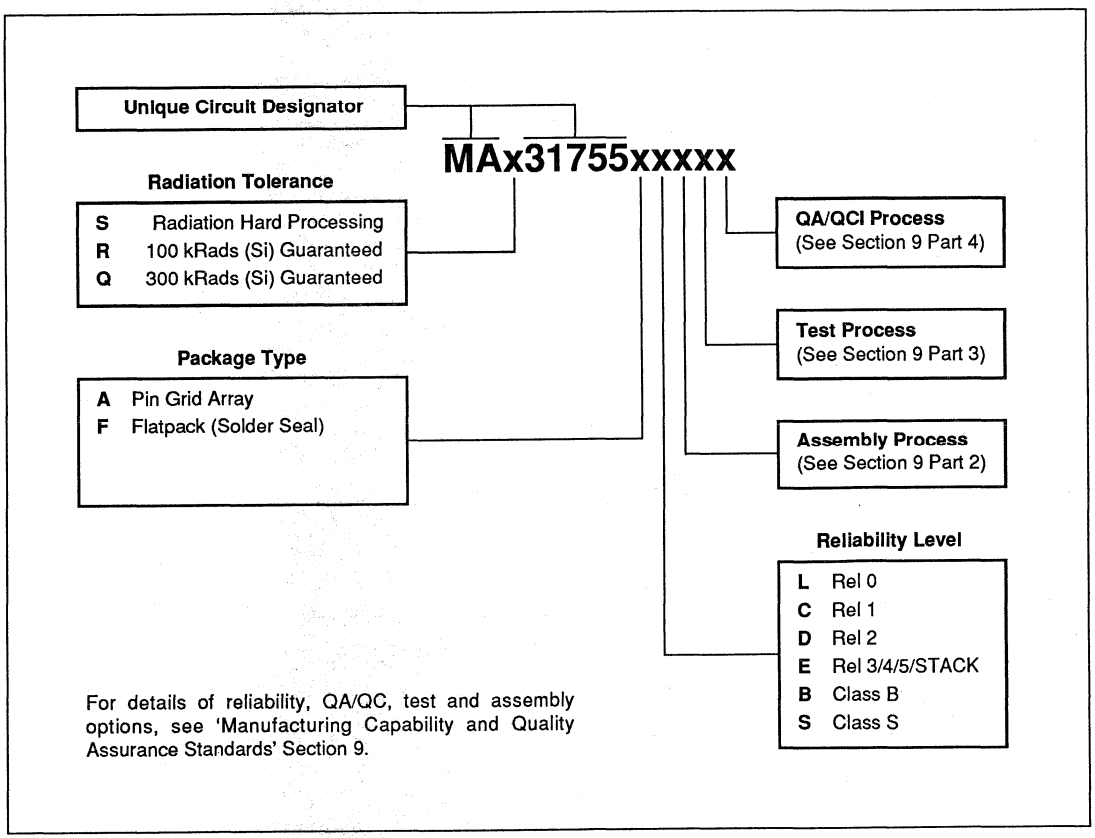
Total Dose (Function to specification)*	$5x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 19: Radiation Hardness Parameters

9. ORDERING INFORMATION



MA31755 - Application Note 1

EDAC ALGORITHMS ON THE MA31755

1. GENERAL

EDACs provide the error detection and correction facilities by generating a code (the check bits) from the data word. These check bits are stored in memory with the associated data word. When the data word is read back, the check bits associated with it will indicate to the EDAC if there have been any errors. The EDAC then takes the appropriate action.

The MA31755 has 6 check bits (CB[0:5]) to be used with 1 or 4 bit wide memory chips. It has a very fast feed through time and it has no test features built in to it.

2. CHECK BIT GENERATION

The Check Bit Generation logic produces six check bits from the incoming User Data Word UD[0:15] by masking it according to Table 5 below: i.e. to create CB[5], bits 13, 12, 8, 7, 6, 5, 4 and 0 of the data word are XORed together.

These check bits are appended onto the 16 bits of user data to form a 22 bit word. The 8 check bits are stored to give error detection and correction for memory chips 1 bit and 4-bits wide.

CB	Parity	UD (write cycles)															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5	Even (XOR)			X	X				X	X	X	X	X				X
4	Even (XOR)		X			X	X	X	X		X		X			X	
3	Odd (XNOR)	X			X			X				X		X	X	X	X
2	Odd (XNOR)		X	X			X						X	X	X	X	X
1	Even (XOR)	X				X	X	X	X	X		X			X		
0	Even (XOR)	X	X	X	X	X				X	X			X			

3. SYNDROME GENERATION

The Syndrome Generation logic produces the Syndrome bits from analysis of the incoming Memory Data MD[0:15] and its associated Check Bits, according to the following table :

SY	Parity	MD (read cycles)															MC					
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	5	4	3	2	1	0
5	Odd			X	X				X	X	X	X	X				X					
4	Odd		X			X	X	X	X		X		X			X		X				
3	Even	X			X			X				X		X	X	X			X			
2	Even		X	X			X						X	X	X	X				X		
1	Odd	X				X	X	X	X	X		X			X						X	
0	Odd	X	X	X	X	X				X	X			X								X

4. THE SYNDROME WORD

4.1 NO ERRORS

If there are no errors in the read data or check bits, then all the syndrome bits will be set to one. Flags are inactive.

4.2 SINGLE ERROR

A single error in the data word, MD[0:15], read from memory, causes three syndrome bits to be set low in the syndrome word.

e.g. If MD[14] is incorrect, syndrome bits 4, 2 and 0 will be set low.
If MD[12] is incorrect, syndrome bits 5, 3 and 0 will be set low.

The syndrome bits thus set form a code which indicates which bit of the data is incorrect (the codes are shown in the syndrome table). For example, if MD[14] was incorrect, the syndrome word would have bits 4, 2 and 0 set low. The syndrome decoder in the EDAC decodes the information in the syndrome word and recognises that MD[14] is incorrect. The error flag CERRN is set to indicate that there has been a correctable error. If the device is in correct mode, the EDAC inverts (and hence corrects) MD[14].

If there is a single error in the check bit word, only one bit of the syndrome word is set low.

For example, if MC[5] is incorrect, syndrome bit 5 will be low. EDAC decoding causes the error flag CERRN to be set but no correction is done as the check bit bus is not used by the system.

4.3 DOUBLE ERRORS

If two errors occur, the number of bits set in the syndrome word will be either 2, 4 or 5. The NCERRN error flag will be activated to indicate that errors are present but cannot be corrected.

e.g. If MD[14] and MD[12] are incorrect, syndrome bits 5, 4, 3 and 2 will be set (bit 0 cancels out in XNOR function)

4.4 TRIPLE ERRORS

If three errors occur, they can always be detected for all memory chip configurations ie. the 2, 4 or 5 bits set low in the syndrome word by 2 errors cannot be cancelled out by the 3 or 1 bits set low due to the extra error. The device must be in detect mode to prevent false correction occurring.

e.g. If MD[14], MD[12] and MD[8] are incorrect, bits 5 and 4 cancel out and bits 3, 2 and 1 are set low. This is decoded by the EDAC as being a correctable error on MD[2]. The CERRN flag is set and correction would take place if the device was in correct mode. This would cause more errors. However, if the device was in detect mode, and the CERRN and NCERRN flags were ORed together to generate an unspecified error flag, then 3 errors would always be detected. (On the MA31755, CERRN can be fed into the XERRN input, making the NCERRN output a general error flag.)

4.5 QUADRUPLE ERRORS

The 6 check bit code can be used to provide error detection for up to four errors if these errors occur in the following groups: MD[0:3], MD[4:7], MD[8:11] and MD[12:15]. It can be seen that within each group of four data bits, there is no combination of errors that would cause no syndrome bits to be set (and hence no error flag). The device can be in either detect or correct mode to flag any number of errors in a 4-bit wide memory chip. Note that for 3 errors, the CERRN flag may be active due to three syndrome bits being set. However, no correction will take place as the code to indicate which bit is in error will not match up to any bit in the data word.

e.g. If MD[14], MD[13] and MD[12] are incorrect, syndrome bits 5 and 2 cancel out and bits 4, 3 and 0 are set. Although this will set the CERRN flag, no correction will occur as this syndrome code does not match up with any code representing an incorrect data bit.

5. RADIATION EFFECTS

If a system is exposed to radiation and memory corruption occurs as a result of this, the chances are that the corruption will be confined to a single memory chip. If this memory chip is one bit wide, usually only one bit of the data word would be corrupted and the 6-check bit code can be used to give error detection and correction. If, however, the system requirement is for 4-bit wide memory chips, the 6 check bit code can provide only error detection. (If there are 3 or 4 errors, the flags are not reliable, as described in section 4.)

If a 6-bit check word is used with 8-bit wide memory chips, and radiation corrupts one chip, no error may be flagged.

e.g. errors in MD[7], MD[6], MD[2] and MD[1] cancel each other out and as no bits are set in the syndrome word, no errors are flagged.

MA31756

SINGLE CHIP PERIPHERAL CONTROLLER FOR THE MA31750

The MA31756 is a single chip peripheral controller for the MA31750. It is designed to interface the MA31750 to different peripherals with a minimum of external components. Together with the MA31750, it forms a complete microcontroller system, targeted to embedded control applications. The MA31756 offers a variety of on-chip resources:

- 960 words of RAM
- Four 16-bit Timers
- 4-Channel Packet Telecommand front-end with BCH Code Decoder
- 16-bit CRC Generator
- 16-Channel, 4-level Interrupt Controller
- 4-Channel Interrupt driven by DMA Controller
- Chip Select and Wait State Generator
- 8- bit Memory Interface
- MA31750 Configuration Word
- Bus Arbiter
- Clock Oscillator
- 61 General Purpose IO Pins

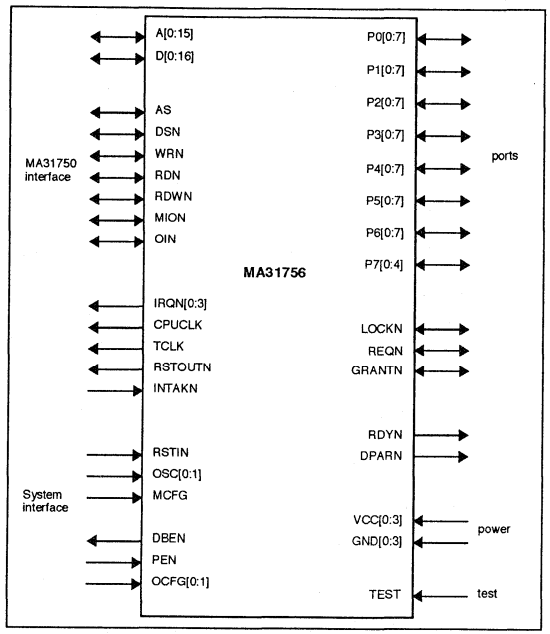


Figure 1: MA31756 Pin Out

1.0 ARCHITECTURE

The MA31756 interfaces directly to the address, data and control busses of the MA31750, requiring no external components. It generates the system clock, reset and all necessary strobes required by the MA31750.

The architecture of the MA31756 can be seen in Figure 2. It is based on 2 de-coupled internal busses, one for the external memory interface, and one for the on-chip RAM and IO devices. This feature allows simultaneous instruction fetch and IO transfer, thereby increasing the maximum IO rate and providing more deterministic execution times in real-time systems.

1.1 INTERNAL MEMORY

The internal memory and registers of the MA31756 are mapped into pre-defined areas of the MA31750 memory space. The MA31756 contains 960 words of general purpose, parity protected RAM and 64 special function registers (SFRs), used to control and monitor the on-chip peripherals.

1.2 EXTERNAL BUS INTERFACE

The on-chip bus controller generates all necessary strobes required by external memory and the MA31750. It divides the memory space into 8 banks, each with its own chip select signal and programmable number of wait states.

The bus controller can interface both 8 and 16-bit wide memory to the system. Up to 127 Kwords (or 191 Kword with shadow PROM) of memory can be connected to an MA31756 based system with no glue logic other than buffers.

One extra bus master (in addition to the MA31750) can be connected, allowing external DMA access to all system memory.

1.3 INTERRUPT SYSTEM

The interrupt controller supports mechanisms for fast and flexible responses to interrupt requests generated from various internal or external units. A total of 16 interrupts can be allocated, each one assigned to one of four priority levels. Each priority level has an interrupt request output pin associated with it, connected directly to the interrupt request inputs on the MA31750.

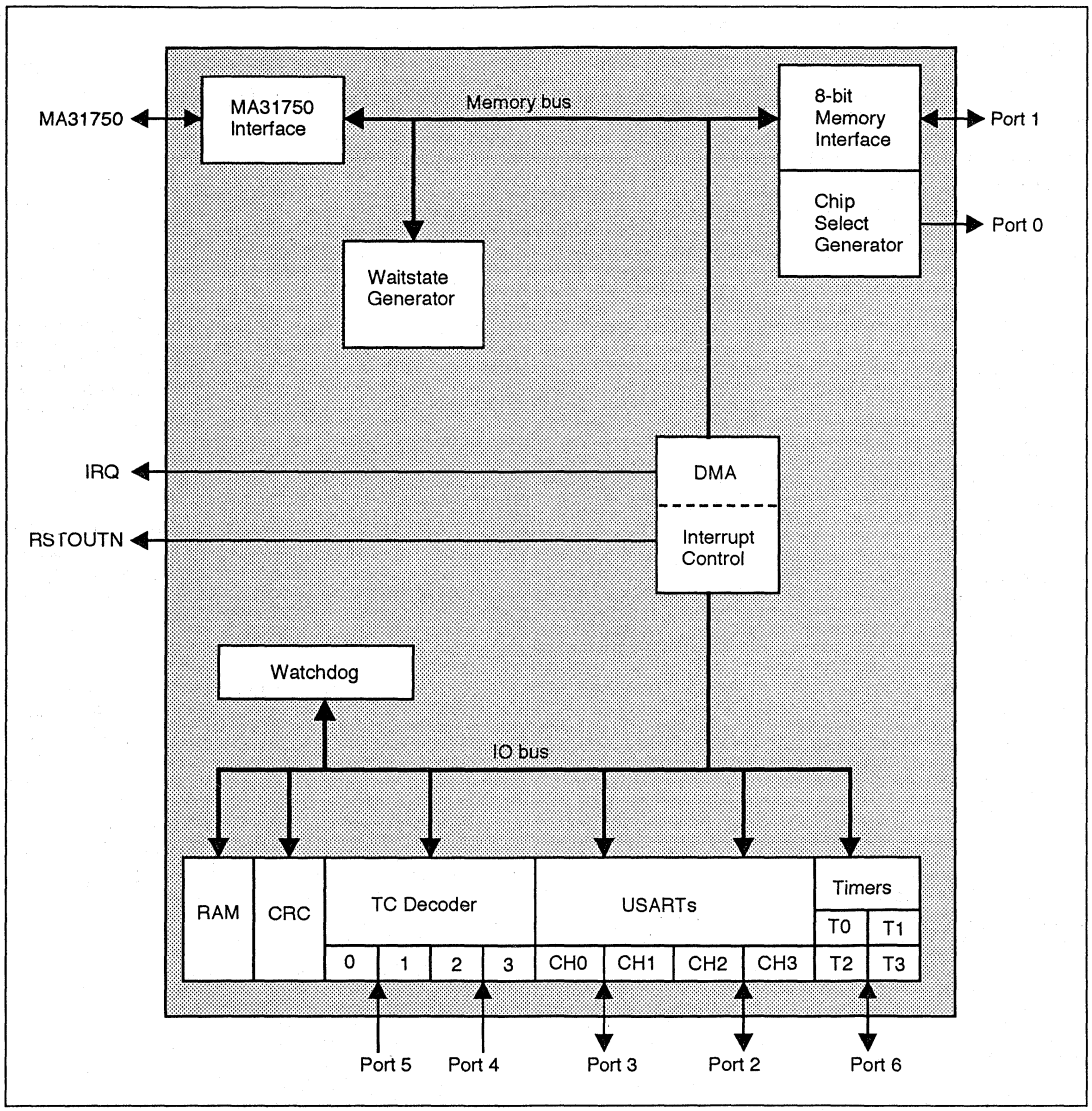


Figure 2: MA31756 Internal Architecture

1.4 DMA CONTROLLER

The DMA controller provides four independent interrupt driven DMA channels, each capable of moving data between any parts of the memory space. Each DMA channel has a counter which is implicitly decremented after each transfer. When this counter reaches zero, an interrupt is generated (if the associated interrupt is enabled). The DMA controller reads or writes blocks of data without involving the MA31750.

1.5 MULTIPLE MA31756 CONNECTIONS

Multiple MA31756 devices can be connected in order to increase the peripheral controlling capabilities of the microcontroller system.

In a multiple MA31756 system, there is an MA31756 acting as a master and a number of MA31756 devices acting as slaves. The slave MA31756s can be configured in 2 different modes - slave A mode or slave B mode.

An MA31756 configured in slave A mode is connected to the master using the secondary bus master interface and thus only one slave A type is supported. Slave A mode can drive the external bus and is therefore able to perform external DMA accesses.

MA31756s configured in slave B mode act as peripherals activated by a chip select signal from the master or a slave A mode MA31756. Slave B type devices cannot perform external DMA accesses.

1.6 TIMER UNIT

The timer unit represents a multi-functional timer / counter structure which may be used for different time related tasks such as event timing and counting, pulse width measurement and pulse generation. The unit contains four 16-bit timers, independently configurable as timer, gated timer or counter. The input clock can be derived from an internal programmable prescalar or an external port. The timers can be concatenated to form 32, 48 or 64-bit timers. The count direction (up or down) is programmable and can be altered dynamically via an external port. A special decoder allows direct interfacing of quadrature encoded incremental encoders (position / velocity sensors).

1.7 SERIAL CHANNELS

Serial communications with other microcontrollers, processors, terminals or other peripheral components is provided by four serial interfaces (USARTs) with identical functionality. They are compatible with commonly used serial protocols, supporting baud rates up to 1MBaud. The baud rate can be generated from the timers or from one dedicated baud rate generator.

In addition to the ordinary 8-bit data frames, a special wake-up mode is provided for multiprocessor communication. Using the internal DMA controller allows movement of large data blocks with minimum CPU overhead.

Hardware error detection capabilities are provided to detect parity, framing and overrun errors.

1.8 TELECOMMAND FRONT-END

The telecommand front-end provides a simple but versatile building block to implement CCSDS packet telecommand decoders. It includes four 16-bit input registers, a start pattern recognizer and a 7-bit BCH syndrome generator. The unit makes it possible to implement a complete 4-channel decoder, including a command pulse distribution unit (CPDU), with a CPU load of approximately 10 KIPs (8 Kbit/sec bit rate).

1.9 CRC GENERATOR

A hardware 16-bit CRC (Cyclic Redundant Code) generator is provided to accelerate encoding and decoding of CRC checksums. It uses the polynomial $x^{16} + x^{12} + x^5 + 1$, and can encode 8 or 16 bits at a time.

1.10 WATCHDOG TIMER

The watchdog timer provides a mechanism to detect malfunctioning for long periods. The watchdog is always enabled and thus the system operation is always monitored. If, due to hardware or software errors, the watchdog is not serviced on time, it will underflow, pulling the RSTOUTN signal low and resetting the system.

1.11 CLOCK GENERATOR

The internal clock generator generates the internal MA31756 clock and the external MA31750 clock signals (both the MA31750 system clock and the MA31750 timer clock), using an external crystal. The MA31750 clock can be stopped during power down mode. The MA31756 clock is always running at its nominal frequency.

1.12 IO PORTS

The MA31756 provides 61 IO lines, organised into three 16-bit ports and one 13-bit port. All ports are word addressable, and nibble-wise programmable as inputs or outputs. Each port has an alternate input or output function associated with it (Port 0 is connected to the chip select generators, port 1 to the 8-bit bus interface, port 2 and 3 to the USARTs, port 4 and 5 to the telecommand front-end, port 6 to the timers and port 7 to miscellaneous functions). When an alternate function is not used, the corresponding port may be used as a general IO port.

2.0 APPLICATIONS

Using the large number of IO ports, an MA31756 based system can be interfaced to almost any type of equipment. The chip-select generator provides a means to simply map both 8 and 16-bit peripherals into the address space of the MA31750. If additional memory is needed in the system, the combined use of 8-bit and 16-bit memory must be traded off against system performance.

2.1 REMOTE TERMINAL UNIT

A remote terminal unit (RTU) can be implemented using the USARTs in TTC-B-01 mode for the digital channels and an external A/D converter for the analogue. External multiplexers, decoders and driver have to be added to interface the requested number of channels. The external multiplexers and decoders can be controlled by some of the unused IO ports.

To off-load the CTU, the RTU can have pre-defined scanning tables defining which channels to be sampled and how often The sampled data can be formatted into telemetry packets and transferred to the CTU either through one of the USARTs, or over an OBDH bus.

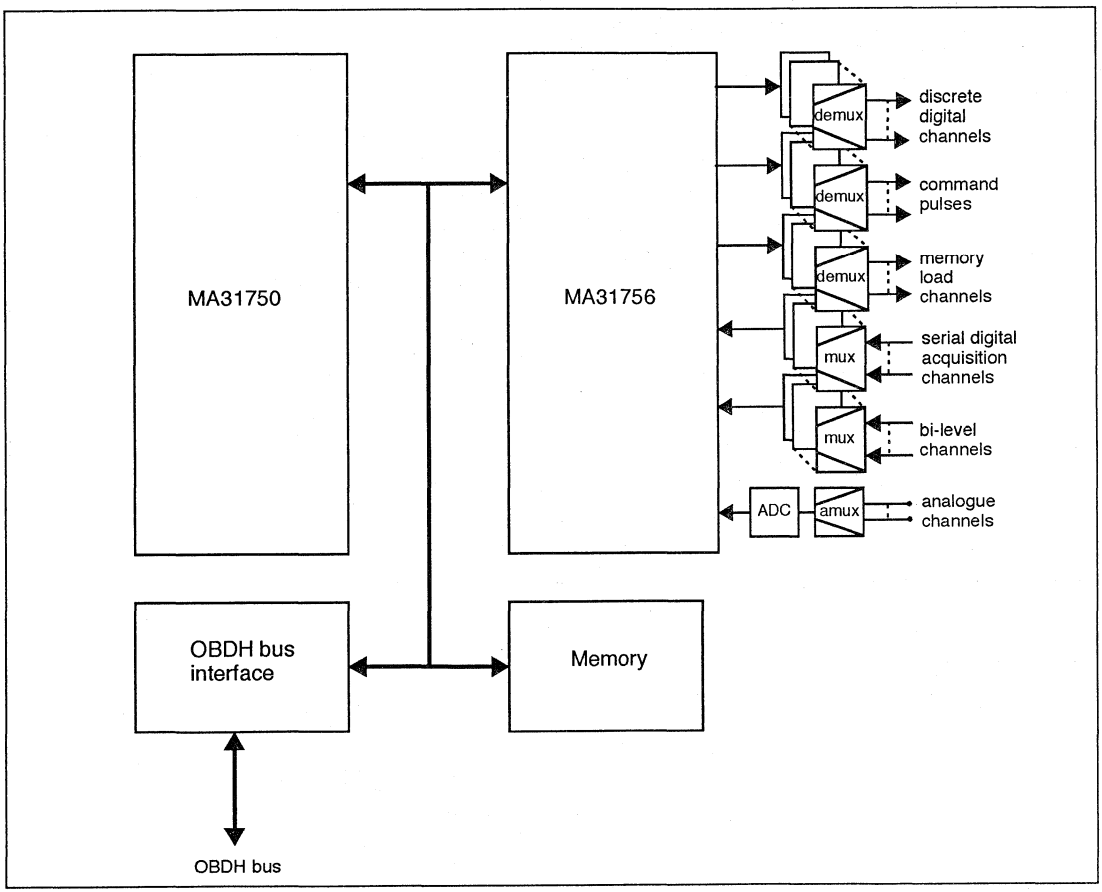


Figure 3: Remote Terminal Unit (RTU)

2.2 TELECOMMAND DECODER

With the on-chip packet telecommand front-end, it is possible to implement a complete 4-channel packet telecommand decoder without any external components.

Accepted telecommand segments can be transferred to the CTU through on of the USARTs or through a mission specific, external interface. Using one of the programmable timers, a command pulse distribution unit (CPDU) can also be integrated. The CLCW and house-keeping data can be provided through the USARTs. If authentication is used, an external PROM will have to be added to store mission specific configuration data. Without authentication, the required mission parameters can be read through unused IO ports, thereby eliminating the need for an external PROM.

Since most of the processing is done by the MA31756, it is estimated that the system can be in power-down mode for more than 95% of the time, thereby minimising the power consumption.

2.3 EMERGENCY TM / TC SYSTEM

An emergency TM/ TC system provides a last communication and reconfiguration link to a satellite. Its main characteristics should be low complexity, weight and power consumption, together with high reliability and autonomy.

Using the MA31750 / MA31756, it is possible to implement an emergency system consisting of a packet TC decoder, a CPDU, a data acquisition unit and a telemetry formatter. The only additional components required are a configuration PROM and buffers and drivers. Using one of the USARTs in synchronous mode for the telemetry output, the emergency system can be connected directly to the receiver / transmitter without any additional data buffering.

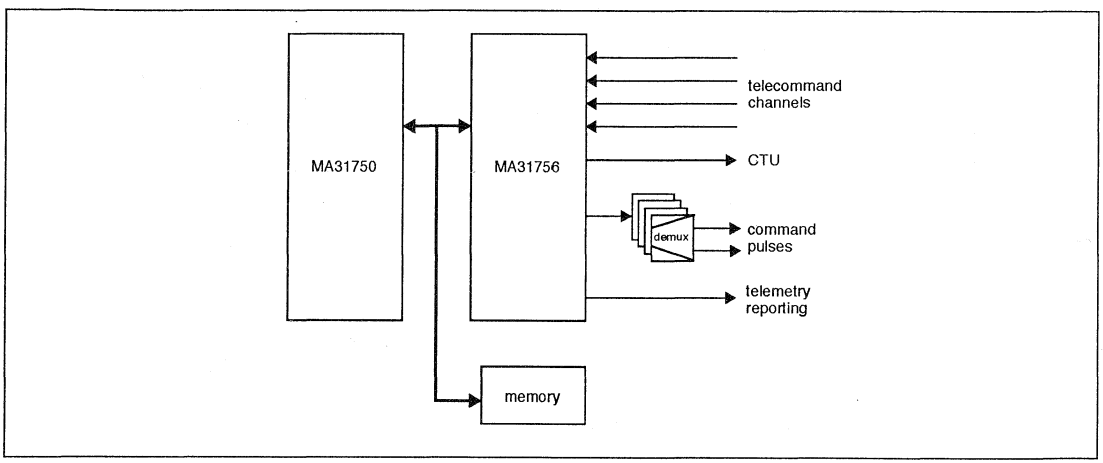


Figure 4: Telecommand Decoder

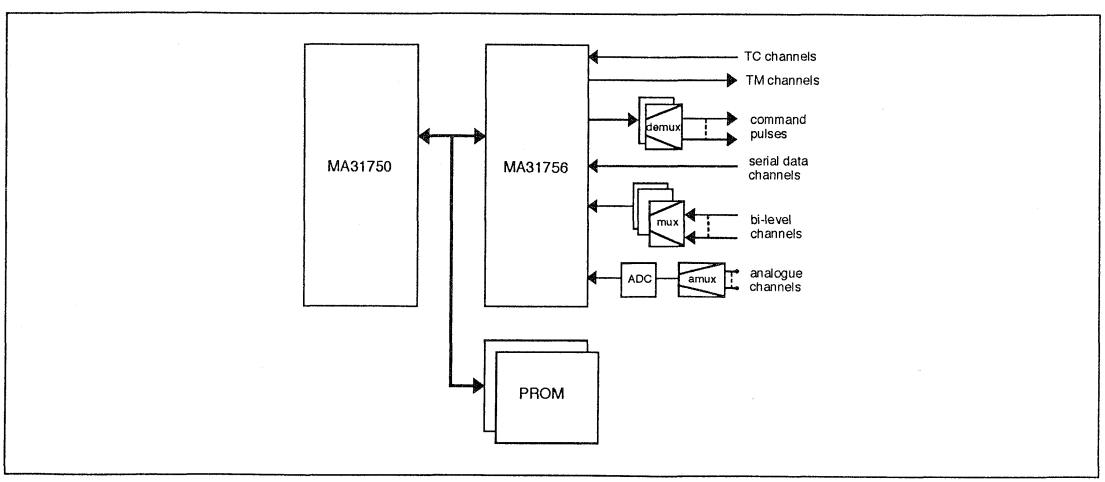


Figure 5: Emergency TM / TC System

2.4 INTEGRATED CTU

For small satellites, it can be beneficial to integrate as many functions as possible in the central terminal unit (CTU). Using the on-chip peripherals of the MA31756, and by connecting more than one MA31756 together, it is possible to integrate a telecommand decoder, an RTU and a CTU in one system. Due to the largely autonomous operation of the on-chip peripherals, less than 20% of the MA31750 throughput should be required to maintain the decoder and RTU functions, leaving 80% for other CTU tasks.

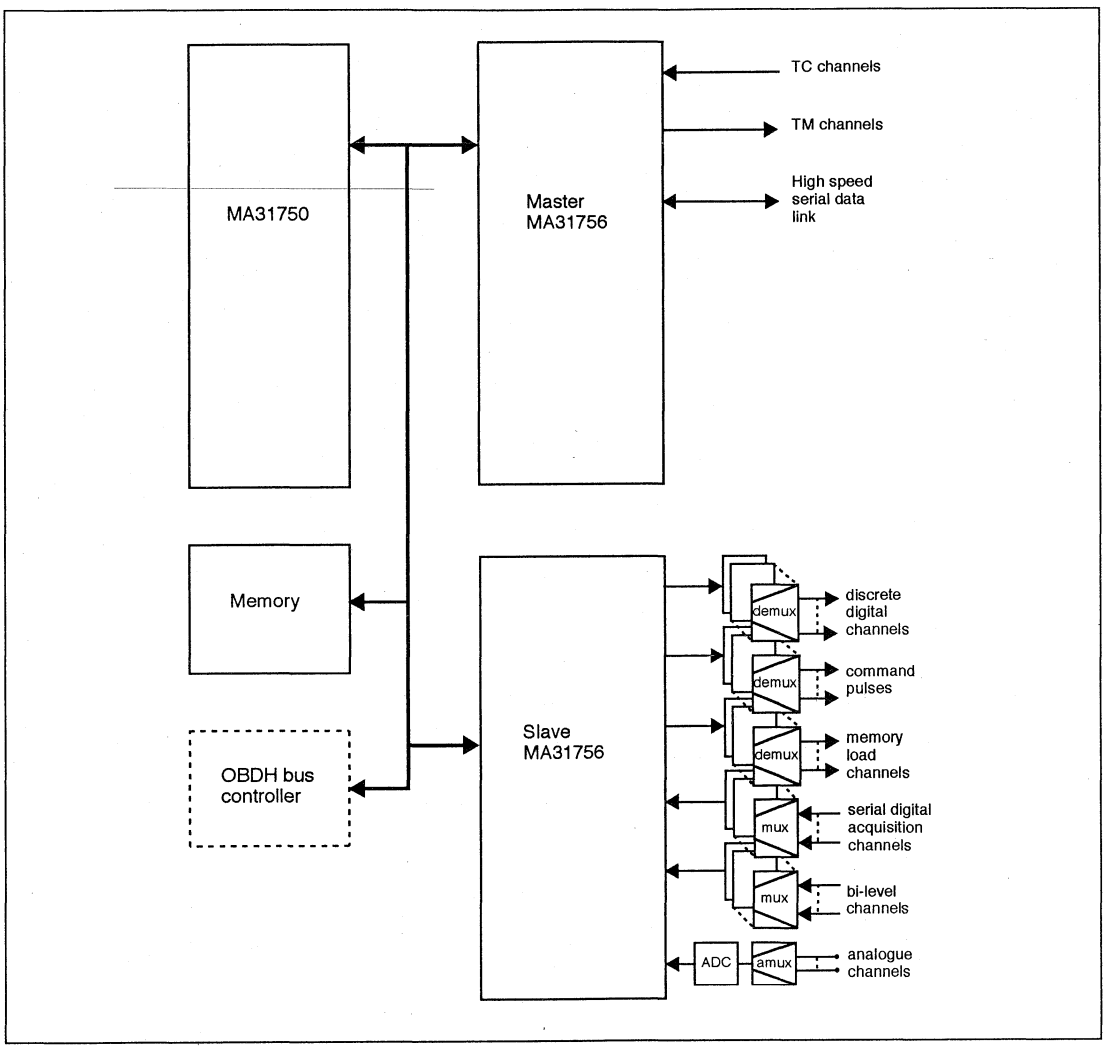


Figure 6: Integrated CTU

3.0 PIN DESCRIPTIONS

3.1 MA31750 INTERFACE

Name	Function	Description
A[0:15]	Address bus	These active high bi-directional signals provide the address for any memory cycle in the system. A[0] is the most significant address bit.
D[0:16]	Data bus	These bi-directional active high signals transfer the data to and from the MA31756. D[0] is the most significant bit while D[15] the least. D[16] is used to supply the parity bit.
AS	Address strobe	This active high bi-directional signal indicates that a valid address is present on the address bus. It has a weak pull-down to maintain a stable value during power down and bus owner switching. In slave B mode is an active high input that indicates that the MA31756 has been selected.
DSN	Data strobe	This active low bi-directional signal provides the data strobe. Provided with a weak pull-up.
RDWN	Read/write strobe	This bi-directional signal indicates whether the current bus cycle is a read cycle (high) or write cycle (low)
WRN	Write strobe	This active low bi-directional signal provides the write strobe. Provided with a weak pull-up.
RDN	Read strobe	This active low bi-directional signal provides the read strobe. Provided with a weak pull-up.
MION	Memory/IO strobe	This bi-directional signal indicates whether the current bus cycle references the memory (high) or the IO (low)space.
OIN	Operand/instruction strobe	This bi-directional signal indicates whether the current bus cycle references an operand (high) or an instruction (low).
RDYN	Bus ready	When high, this active low output indicates that additional waitstates should be inserted in the current bus cycle. When low, it indicates that the bus cycle may be terminated.
DPARN	Disable parity	This active low output is asserted during read accesses to areas of the memory space which are not provided with a parity bit.
LOCKN	Bus lock	This active low input indicates that the MA31750 has locked the external bus, ie. that no other transfer should take place in the memory space. If the MA31756 is in slave A mode, this pin is an active low output that indicates to the master MA31756 that the slave A MA31756 will own the bus in the following cycle. In slave B mode this pin should be left open.
REQN	Bus request	This active low input indicates that the MA31750 will require the external bus in the following cycle. If the MA31756 is in slave A mode, this pin is an active low output driven low when the MA31756 will require the bus in the following cycle. In slave B mode this pin should be left open.
GRANTN	Bus grant	This active low output indicates that the MA31750 has been granted the bus and may start a transfer in the following cycle. If the MA31756 is in slave A mode, this pin is an active low input asserted by the master MA31756 to indicate that access to the external bus has been granted. In slave B mode this pin should be left open.
IRQN[0:3]	Interrupt request	These active low outputs indicate that an interrupt request has been generated by the on-chip peripherals. IRQN[0] is assigned to interrupt level 0, IRQN[1] to level 1, IRQN[2] to level 2, and IRQN[3] to level 3.
INTAKN	Interrupt acknowledge	This active low input indicates that the MA31750 is servicing an interrupt. If INTACKN is asserted together with AS, then IRQN[0:3] will be de-asserted. Further assertion will only occur after a write cycle to the interrupt pending register (IPER) has taken place.
RSTOUTN	System reset output	This active low output is asserted when the watchdog underflows or when RSTIN is asserted. It stays asserted for 32 clock cycles after RSTIN is de-asserted
CPUCLK	System clock	This output provides the system clock for the MA31750
TCLK	MA31750 timer clock	This output provides the clock for the MA31750 timer clock
TEST	Test input	This active high input is used for test purposes. It should always be tied to ground during operation.

3.2 SYSTEM INTERFACE

Name	Function	Description
OSC[0:1]	Oscillator inputs	To generate the system clock, an external crystal can be connected between OSC[0] and OSC[1]. If an external clock source is used, it should be connected to OSC[0] while OSC[1] should be left open.
RSTIN	Reset input	This active low input will reset the MA31756 if asserted. To ensure proper reset, this input must be asserted for at least 16 system clock cycles.
DBEN	Data buffer enable	This active low output is asserted when a valid bus transfer in the memory address space is detected, not addressing any of the internal memory or registers of the MA31756 or the 8-bit area. This signal should be used to enable data bus buffers for external memory or peripherals connected directly to the MA31750 busses.
MCFG	Memory configuration	This input enables the 8-bit memory interface at reset time.
PEN	Parity error	This active low input is sampled on the falling edge of AS
OCFG[0:1]	Operation mode configuration	This input selects the operating mode of the MA31756. Four different modes are possible: master without slave A, master with slave A, slave A, slave B.
P0[0:7] P1[0:7] P2[0:7] P3[0:7] P4[0:7] P5[0:7] P6[0:7] P7[0:4]	I/O Ports	These ports can be used as general purpose I/O ports. They can be programmed to serve as inputs or outputs through the system configuration register. Each port has an alternative function associated with it, which takes precedence if activated.

3.3 POWER

Name	Function	Description
VCC[0:3]	Power input	These input provide the power to the MA31756. The nominal voltage level shall be +5V, 10%
GND[0:3]	Ground	These inputs provide the ground connection to the MA31756.

3.4 ALTERNATIVE PORT FUNCTIONS

3.4.1 Timer Ports

Name	Port	Function	Description
T0CLK	P6[0]	Timer 0 clock	If timer 0 is in counter mode, this port will be configured as input providing the timer 0 clock. In gated timer mode this input pin is used to gate the timer clock.
T0UD	P6[1]	Timer 0 count direction	If the CDX bit is set in the timer 0 control register, this port will be configured as input, controlling the count direction of the timer.
T0OUT	P6[2]	Timer 0 output	If the OLE bit is set in timer 0 control register, this port will be configured as output, toggling every time timer 0 overflows or underflows
T1OUT	P6[3]	Timer 1 output	If the OLE bit is set in timer 1 control register, this port will be configured as output, toggling every time timer 1 overflows or underflows
T2CLK	P6[4]	Timer 2 clock	If timer 2 is in counter mode, this port will be configured as input, providing the timer 2 clock. In gated timer mode this input pin is used to gate the timer clock.
T2UD	P6[5]	Timer 2 count direction	If the CDX bit is set in the timer 2 control register, this port will be configured as input, controlling the count direction of the timer.
T2OUT	P6[6]	Timer 2 output	If the OLE bit is set in timer 2 control register, this port will be configured as output, toggling every time timer 2 overflows or underflows
T3OUT	P6[7]	Timer 3 output	If the OLE bit is set in timer 3 control register, this port will be configured as output, toggling every time timer 3 overflows or underflows

3.4.2 USART Ports

Name	Port	Function	Description
TDX0 TDX1 TDX2 TDX3	P2[0] P2[4] P3[0] P3[4]	USART serial output	If the USART transmitter is enabled, this port will be configured as output, providing the transmitted data
RDX0 RDX1 RDX2 RDX3	P2[1] P2[5] P3[1] P3[5]	USART serial output	If the USART receiver is enabled, this port will be configured as input, providing the receiver data
CTSN0 CTSN1 CTSN2 CTSN3	P2[2] P2[6] P3[2] P3[6]	USART clear to send	If the USART flow control is enabled, this port is configured as an active low input, providing the clear-to-send signal to the USART0 transmitter
RTSN0 RTSN1 RTSN2 RTSN3	P2[3] P2[7] P3[3] P3[7]	USART request to send	If the USART flow control is enabled, this port is configured as an active low output, providing the request-to-send signal to the USART0 receiver

3.4.3 Telecommand Front End Ports

Name	Port	Function	Description
TCS[0] TCS[1] TCS[2] TCS[3]	P4[0] P4[3] P4[6] P5[1]	TC sample inputs	The active high inputs provide the sample signals for telecommand channels
TCD[0] TCD[1] TCD[2] TCD[3]	P4[2] P4[5] P5[0] P5[3]	TC data inputs	These active high inputs provide the data for telecommand channels.
TCC[0] TCC[1] TCC[2] TCC[3]	P4[1] P4[4] P4[7] P5[2]	TC clock inputs	These active high inputs provide the clock signals for telecommand channels

3.4.4 8-Bit Memory Interface

Name	Port	Function	Description
DB[0:7]	P1[0:7]	8-bit data bus	If the 8-bit memory interface is used, these ports will be configured as the bi-directional active high 8-bit data bus. DB[0] is the most significant
WR8N	P5[5]	Write strobe	If the 8-bit memory interface is used, this port will be configured as an active low output, providing the write strobe for the 8-bit area
A16	P5[6]	Byte enable	If the 8-bit memory interface is used, this port will be configured as an active high output, providing an extra address bit, This output is asserted when the lower byte of a word is accessed.
PAR8	P5[7]	Parity bit	If the 8-bit memory interface is used, this port will be configured as a bi-directional active high port, providing the parity bit for the 8-bit area

3.4.5 Chip Select Signals

Name	Port	Function	Description
CSN[0:3]	P0[0:3]	Chip select generator 0 outputs	If chip select generator 0 enabled, these ports will be configured as active low outputs
CSN[4:7]	P0[4:7]	Chip select generator 1 outputs	If chip select generator 1 enabled, these ports will be configured as active low outputs

3.4.6 Miscellaneous Functions

Name	Port	Function	Description
REQXN	P7[0]	Bus request	In the master with slave A mode or in the master without slave A mode if the secondary bus master interface is enabled, this port will be configured as an active low input, providing the request signal from the secondary bus master.
GRANTXN	P7[1]	Bus grant	In the master with slave A mode or in the master without slave A mode if the secondary bus master interface is enabled, this port will be configured as an active low output, indicating that the secondary bus master will own the bus in following cycle.
LOCKXN	P7[2]	Bus lock	In the master with slave A mode or in the master without slave A mode if the secondary bus master interface is enabled, this port will be configured as an active low input, indicating that the secondary bus master wishes to retain the bus for next cycle.
ADBEN	P7[3]	Alternate data buffer enable	If the ADR and or ADW bits in the memory configuration register is set then this port will be configured as an active low output, providing the alternate data buffer strobe
MRDYN	P7[4]	Memory ready	If the ERY bit in the system configuration register is set, then this port will be configured as active low input, providing a mean to extend a bus cycle to cope with slow peripherals. Waitstates will be inserted in the current bus cycle until this input is asserted, overruling the pre-programmed number of waitstates.

4.0 SPECIAL FUNCTION REGISTER

4.1 SPECIAL FUNCTION REGISTERS MEMORY MAP

Mnemonic	Function	Addr
SYSR	System configuration register	FFC0
MCR	Memory configuration register	FFC1
CCR	Chip select control register	FFC2
MWR	Memory waitstate register	FFC3
IPRI0	Interrupt priority register 0	FFC4
IPRI1	Interrupt priority register 1	FFC5
IMR	Interrupt mask register	FFC6
PDR	Port direction register	FFC7
IOPR0	I/O port register 0	FFC8
IOPR1	I/O port register 1	FFC9
IOPR2	I/O port register 2	FFCA
IOPR3	I/O port register 3	FFCB
DCCR0	DMA channel control register 0	FFCC
DCCR1	DMA channel control register 1	FFCD
DCCR2	DMA channel control register 2	FFCE
DCCR3	DMA channel control register 3	FFCF
DSAR0	DMA source address register 0	FFD0
DSAR1	DMA source address register 1	FFD1
DSAR2	DMA source address register 2	FFD2
DSAR3	DMA source address register 3	FFD3
DDAR0	DMA destination register 0	FFD4
DDAR1	DMA destination register 1	FFD5
DDAR2	DMA destination register 2	FFD6
DDAR3	DMA destination register 3	FFD7
UCR0	USART 0 control register	FFD8
UCR1	USART 1 control register	FFD9
UCR2	USART 2 control register	FFDA
UCR3	USART 3 control register	FFDB

Mnemonic	Function	Addr
USR0	USART 0 status register	FFDC
USR1	USART 1 status register	FFDD
USR2	USART 2 status register	FFDE
USR3	USART 3 status register	FFDF
UDR0	USART 0 data register	FFE0
UDR1	USART 1 data register	FFE1
UDR2	USART 2 data register	FFE2
UDR3	USART 3 data register	FFE3
ICR	Interrupt configuration register	FFE4
CWR	Configuration word register	FFE5
DICR	DMA interrupt configuration register	FFE6
DCSR	DMA command/status register	FFE7
TVR0	Timer value register 0	FFE8
TVR1	Timer value register 1	FFE9
TVR2	Timer value register 2	FFEA
TVR3	Timer value register 3	FFEB
TCR0	Timer control register 0	FFEC
TCR1	Timer control register 1	FFED
TCR2	Timer control register 2	FFEE
TCR3	Timer control register 3	FFEF
TRLR0	Timer reload register 0	FFF0
TRLR1	Timer reload register 1	FFF1
TRLR2	Timer reload register 2	FFF2
TVRLR3	Timer reload register 3	FFF3
TCR	Telecommand control register	FFF4
TCDR	Telecommand data register	FFF5
IIR	Interrupt identification register	FFF6
IPER	Interrupt pending register	FFF7
WDR	Watchdog register	FFF8
BRR	Baud rate register	FFF9
TCLKR	MA31750 timer clock register	FFFA
		FFFB
CHR	CRC 16-bit holding register	FFFC
CH8R	CRC 8-bit holding register	FFFD
CSYNR	CRC syndrome register	FFFE
		FFFF

DS3574-3.3

MA28151

RADIATION HARD PROGRAMMABLE COMMUNICATION INTERFACE

The MA28151 is based on the industry standard 8251A Universal Synchronous Asynchronous Receiver/Transmitter (USART), modified for data communications with the MAS281 microprocessor.

The MA28151 is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission.

Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART signals the CPU whenever it receives a character for transmission or whenever it receives a character for the CPU. The CPU can read the complete status of the USART at any time, including data transmission errors and control signals such as SYNDET and TxEMPTY.

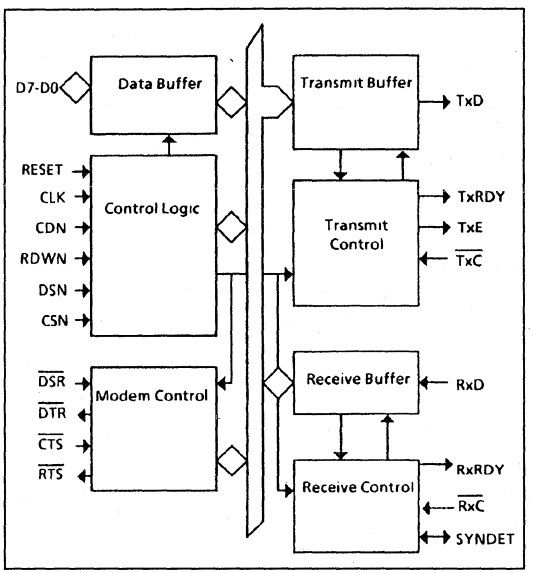


Figure 1: MA28151 Block Diagram

FEATURES

- Radiation Hard to 1MRad(Si)
- Latch Up Free, High SEU Immunity
- Silicon-on-Sapphire Technology
- Synchronous 5 - 8 Bit Characters; Internal or External Character Synchronisation; Automatic Sync Insertion
- Asynchronous 5 - 8 Bit Characters; Clock Rate - 1, 16 or 64 Times Baud Rate; Break Character Generation, 1 ½ or 2 Stop Bits
- All Inputs and Outputs are TTL Compatible
- Compatible with the MAS281 (MIL-STD-1750A) Microprocessor

The MA28151 is based on the industry standard 8251A USART, modified for use with the MAS281 processor, incorporating the following features:

1. MA28151 has double-buffered data paths with separate I/O registers for control status, data in and data out, which considerably simplifies control programming and minimizes CPU overhead.
2. In synchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
3. A refined Rx initialisation prevents the Receiver from starting when in the "break" state, preventing unwanted interrupts from the disconnected USART.
4. At the conclusion of a transmission, the TxD line will always return to the marking state unless SBRK is programmed.
5. Tx Enable logic enhancement prevents a Tx Disable command from prematurely halting transmission of the previously written data before completion. The logic also prevents the transmitter from turning off in the middle of a word.
6. When external Sync Detect is programmed, Internal Sync Detect is disabled and an External Sync Detect status is provided via a flip-flop, which clears itself upon a status read.
7. The possibility of a false sync detect is minimized in two ways: by ensuring that if double character sync is programmed, the characters will be continuously detected and by clearing the Rx register to all 1's whenever Enter-Hunt command is issued in Sync mode.
8. When the MA28151 is not selected, the RDWN and DSN lines do not affect the internal operation of the device.
9. The MA28151 Status can be read at any time but the status update will be inhibited during status read.
10. The MA28151 is free from extraneous glitches, providing higher speed and better operating margins.
11. Synchronous Baud rate is from DC to 64K.
12. Asynchronous Baud rate is from DC to 19.2K.

1. FUNCTIONAL DESCRIPTION

1.1 GENERAL

The MA28151 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for use with the MAS281 microprocessor. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The MA28151 can support most serial data techniques in use, including IBM bi-sync.

In a communication environment, an interface device must convert parallel format system data into serial format for transmission, and convert incoming serial data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear transparent to the CPU for the simple input or output of byte-oriented system data.

1.2 DATA BUS BUFFER

This 3-state, bidirectional, 8-bit buffer is used to interface the MA28151 to the system data bus. Data is transmitted or received by the buffer upon execution of OUTput or INput instructions from the CPU.

Control word, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-in and Data-out registers are separate 8-bit registers, communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register, which store the various control formats for the device's functional definition.

1.3 RESET

A high on this input forces the MA28151 into idle mode. The MA28151 will remain at idle until its functional definition is programmed with a new set of control words. Minimum RESET pulse width is 6 tcy (clock must be running).

The device can also be put into the idle state by a command reset operation .

1.4 CLOCK (CLK)

The CLK input is used to generate internal device timing and is normally connected to the clock generator (OSC) of the system.

Please note: None of the external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

1.5 DATA STROBE (DSN)

This input indicates that a data transfer is taking place. During a CPU write operation the MA28151 reads data from the bus on the rising edge of DSN. During a read operation the MA28151 can output data while DSN is low. Data is valid on the rising edge of DSN.

1.6 READ/WRITE SELECT (RDWN)

A high on the RDWN input indicates a read of data or status information from the MA28151. A low on this input indicates a transfer of data or control words into the MA28151. The RDWN line is valid only when DSN is low. Figure 2 summarises the MAS28151 read/write operati ons.

1.7 CONTROL/DATA (CDN)

This input, in conjunction with the DSN and RDWN inputs, informs the MA28151 that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0= DATA

CDN	RDWN	DSN	CSN	ACTION
0	1	0	0	28151 TO CPU
0	0	0	0	CPU TO 28151
1	1	0	0	STATUS TO CPU
1	0	0	0	CPU TO CONTROL
x	x	1	0	BUS TRISTATE
x	x	x	1	BUS TRISTATE

Figure 2: Read/Write Control

1.8 CHIP SELECT (CSN)

A low on this input selects the MA28151. No reading or writing will occur unless the device is selected. When CSN is high, the Data Bus is in the float state and the DSN and RDWN lines have no effect on the chip.

1.9 MODEM CONTROL

The MA28151 has a set of control inputs and outputs which can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

1.10 DATA SET READY ($\overline{\text{DSR}}$)

The $\overline{\text{DSR}}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{\text{DSR}}$ input is normally used to test modem conditions such as Data Set Ready.

1.11 DATA TERMINAL READY ($\overline{\text{DTR}}$)

The $\overline{\text{DTR}}$ output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{\text{DTR}}$ output signal is normally used for modem control such as Data Terminal Ready.

1.12 REQUEST TO SEND ($\overline{RTS}$)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request To Send.

1.13 CLEAR TO SEND ($\overline{CTS}$)

A low on this input enables the MA28151 to transmit serial data if the Tx Enable bit in the Command byte is set to a high. If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx disable command, before shutting down.

1.14 TRANSMITTER BUFFER

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset, or when Tx Enable or $\overline{CTS}$ = 1, or the transmitter is empty.

1.15 TRANSMITTER CONTROL

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

1.16 TRANSMITTER READY (TxRDY)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the falling edge of DSN (with RDWN low) when a data character is loaded from the CPU.

Note that when using the polled operation, the TxRDY status bit is not masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data input Register.

1.17 TRANSMITTER EMPTY (TxE)

When the MA28151 has no characters to send, the TxEMPTY output will go high. It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of transmission mode, so that the CPU can turn the line around in the half-duplex operational mode.

In the Synchronous mode, a high on the TxEMPTY output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being automatically transmitted as fillers. TxEMPTY does not go low when the SYNC characters are being shifted out.

1.18 TRANSMITTER CLOCK ($\overline{TxC}$)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1,1/16 or 1/64 the $\overline{TxC}$.

For Example:
If Baud Rate equals 110 Baud
$\overline{TxC}$ equals 110Hz in the 1x mode
$\overline{TxC}$ equals 1 72KHz in the 16x mode
$\overline{TxC}$ equals 7.04KHz in the 64x mode
The falling edge of $\overline{TxC}$ shifts the serial data out of the MA28151.

1.19 RECEIVER BUFFER

The Receiver accepts serial data, converts the data to parallel format, checks for bits or characters that are unique to the communications techniques and sends an assembled character to the CPU. Serial data is input to the RxD pin and is clocked in on the rising edge of RxC.

1.20 RECEIVER CONTROL

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialisation circuit prevents the MA28151 from mistaking an unused input line for an active low data line in the break condition. Before starting to receive serial characters on the RxD line, a valid 1 must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (start bit) is enabled. This feature is only active in the asynchronous mode and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts as the result of a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

1.21 RxRDY (RECEIVER READY)

This output indicates that the MA28151 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation. RxEnable, when off holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY,

the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, the overrun error will be set and the old character will be lost.

1.22 $\overline{RxC}$ (RECEIVER CLOCK)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 of the Receiver Clock.

For example:
Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz in the 1 x mode:
$\overline{RxC}$ equals 4800 Hz in the 16x mode
$\overline{RxC}$ equals 19.2 KHz in the 64x mode.
Baud Rate equals 2400 Baud if
$\overline{RxC}$ equals 2400Hz in the 1x mode
$\overline{RxC}$ equals 38.4 KHz in the 16x mode;
$\overline{RxC}$ equals 153.6 KHz in the 64x mode.
Data is sampled into the MA28151 on the rising edge of $\overline{RxC}$.

Note: In most communications systems, the MA28151 will be handling both the transmission and reception operations of a single link. Consequently the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

1.23 SYNC/BREAK DETECT (SYNDET/BRKDET)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode, low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go high to indicate that the MA28151 has located the SYNC character in the Receive mode. If the MA28151 is programmed to use double Sync characters (bi-sync), the SYNDET will go high in the middle of the last bit of the second Sync character.

SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the MA28151 to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the high input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

1.24 BREAK (ASYNC MODE ONLY)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences including the start bits, data bits, and parity bits. Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

C/D	ACTION
1	MODE INSTRUCTION
1	SYNC CHARACTER 1 (SYNC ONLY) *
1	SYNC CHARACTER 2 (SYNC ONLY) *
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION

Note: The second sync character is skipped if mode instruction has programmed the MA28151 to single character mode. Both sync characters are skipped if mode instruction has programmed the MA28151 to async mode

Figure 3: Typical data block

2. OPERATION DESCRIPTION

2.1 GENERAL

The complete functional definition of the MA28151 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the MA28151 to support the desired communications format. These control words will program the: Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, Even/Odd/Off Parity, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the MA28151 is ready to perform its communication functions. The TxRDY output is raised high to signal the CPU that the MA28151 is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the MA28151. Alternatively, the MA28151 receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised high to signal the CPU that the MA28151 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The MA28151 cannot begin transmission until the TxEnable (Transmitter Enable) bit is set in the Command instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

3. PROGRAMMING THE MA28151

3.1 MODE AND COMMAND INSTRUCTIONS

Prior to starting data transmission or reception, the MA28151 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the MA28151 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:
1. Mode Instruction
2. Command Instruction

3.1.1 Mode Instruction

This instruction defines the general operational characteristics of the MA28151. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the MA28151 by the CPU, SYNC characters or Command Instructions may be written.

3.1.2 Command Instruction

This instruction defines a word that is used to control the actual operation of the MA28151.

Both the Mode and Command Instruction must conform to a specified sequence for proper device operation. The Mode instruction must be written immediately following a Reset operation, prior to using the MA28151 for data communications.

All control words written into the MA28151 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the MA28151 at any time in the data block during the operation of the MA28151. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation. This automatically places the MA28151 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

3.2 MODE INSTRUCTION DEFINITION

The MA28151 can be used for either Asynchronous or Synchronous data communications. To understand how the Mode Instruction defines the functional operation of the MA28151, the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant data bus bits will hold the data; unused bits are 'don't care' when writing data to the MA28151, and will be zeros when reading the data from the MA28151.

3.3 TEST MODE

The Mode Instruction can be used to select a scan path test facility. In this mode a test vector is read in through RxD and read out in TxD. For further information of test mode please contact GEC Plessey Semiconductors.

3.4 ASYNCHRONOUS MODE (TRANSMISSION)

Whenever a data character is sent by the CPU the MA28151 automatically adds a Start bit (low level), followed by the data bits (least significant bit first,) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The Character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16 or 1/64 times that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the MA28151 the TxD output remains high (marking) unless a Break (continuously low) has been programmed.

3.5 ASYNCHRONOUS MODE (RECEIVE)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16x or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If a parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the receiver requires only one stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the MA28151. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched.

If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the MA28151.

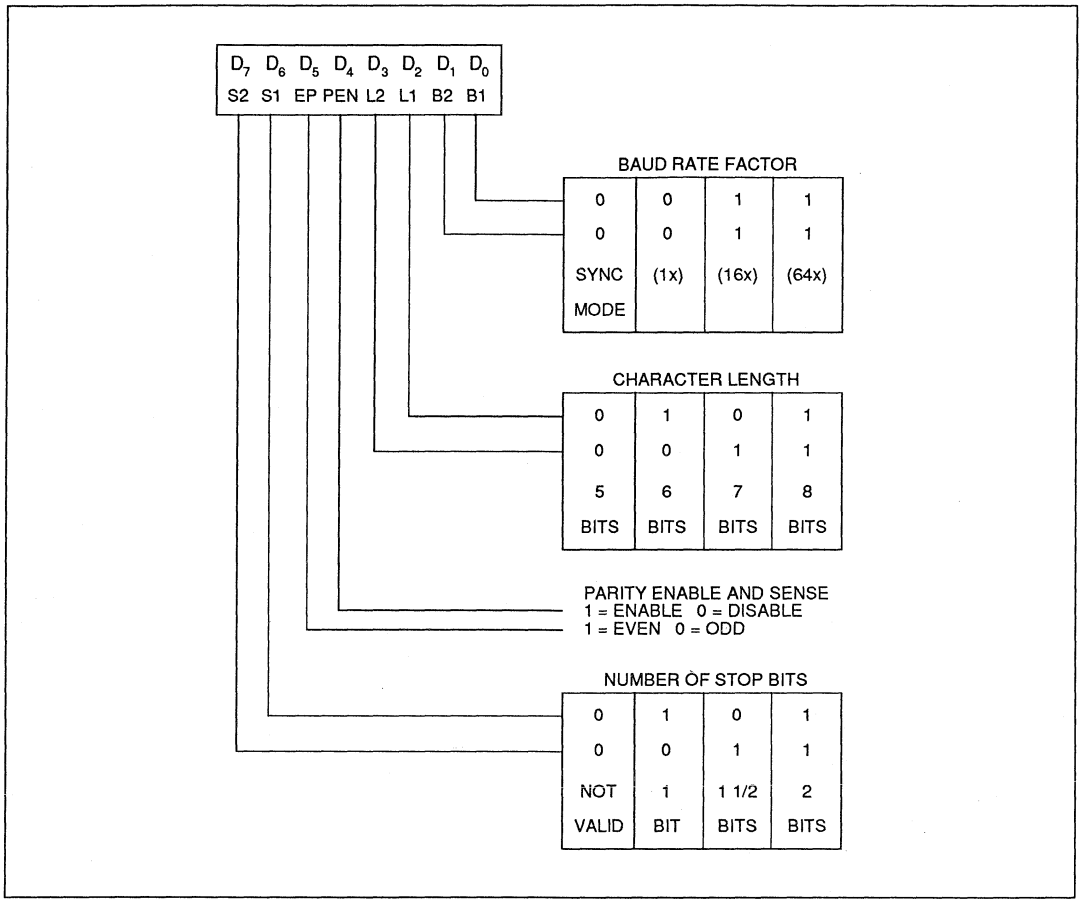


Figure 4: Mode Instruction Format, Asynchronous Mode

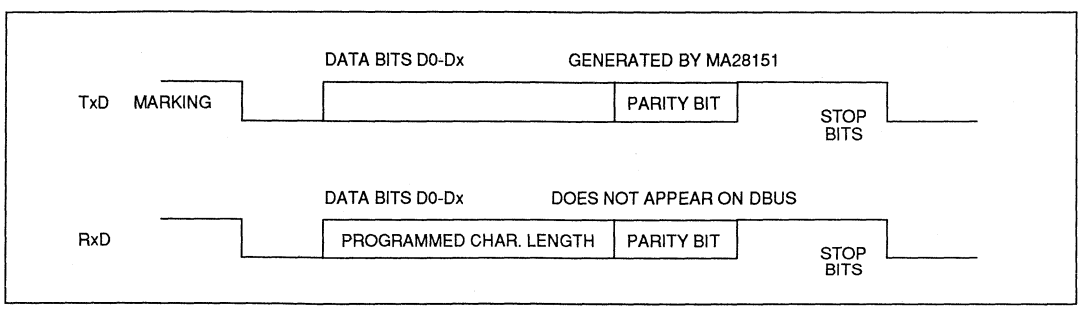


Figure 5: Asynchronous Mode

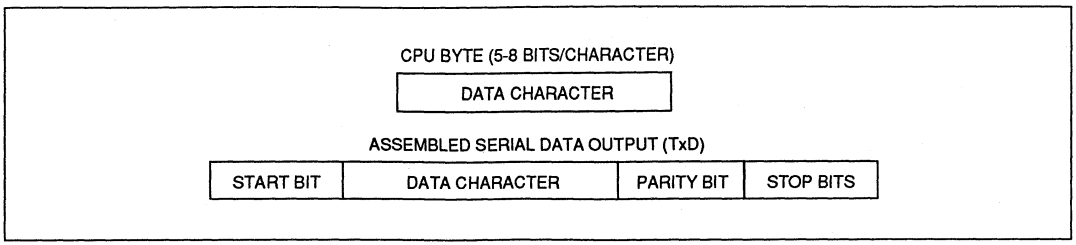


Figure 6: Transmission Format

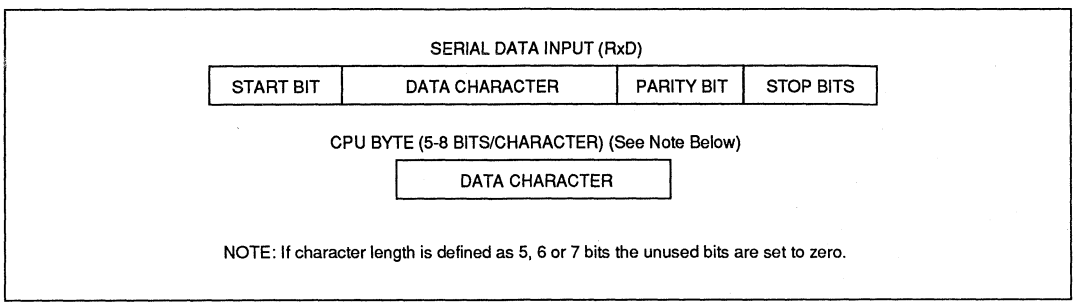


Figure 7: Receive Format

3.6 SYNCHRONOUS MODE (TRANSMISSION)

The TxD output is continuously high until the CPU sends its first character to the MA28151 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the MA28151 with a data character before the MA28151 Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY does not go low when the SYNC is being shifted out (see figure 8). The TxEMPTY pin is internally reset by a data character being written into the MA28151.

3.7 SYNCHRONOUS MODE (RECEIVER)

In this mode character synchronisation can be internally or externally achieved. If the SYNC mode has been programmed, ENTER-HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared to every bit boundary with the first SYNC character until a match occurs.

If the MA28151 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit, instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the MA28151 out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

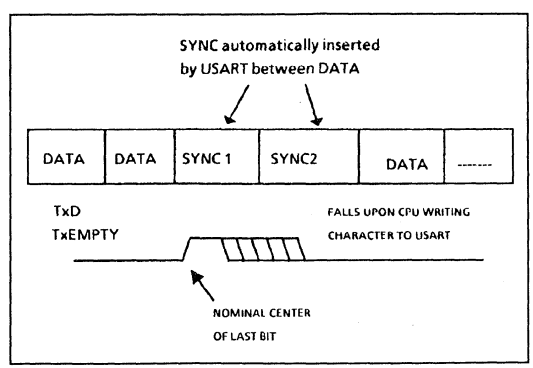


Figure 8: Sync Character Insertion

Parity error and overrun error are both checked in the same way as in the Asynchronous Receive mode. Parity is checked when not in HUNT, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronisation is lost. This will also set all the used character bits in the buffer to a one thus preventing a possible false SYNDET caused by data that happens to be in the Rx buffer at ENTER HUNT time.

Note: the SYNDET flip-flop is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the MA28151 to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the known word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been contiguously received to gate a SYNDET indication). When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET flip-flop may be set at any bit boundary.

3.9 DATA FORMAT, SYNCHRONOUS MODE

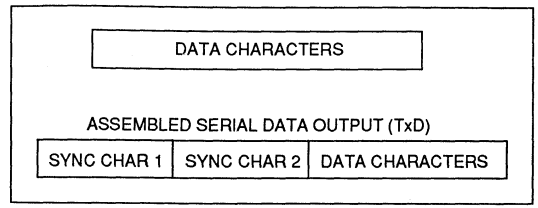


Figure 9: Receive Format, Synchronous Mode

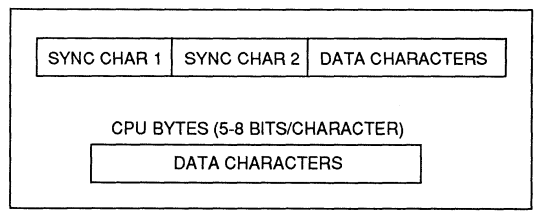


Figure 10: Data Format, Synchronous Mode

3.8 MODE INSTRUCTION FORMAT, SYNCHRONOUS MODE

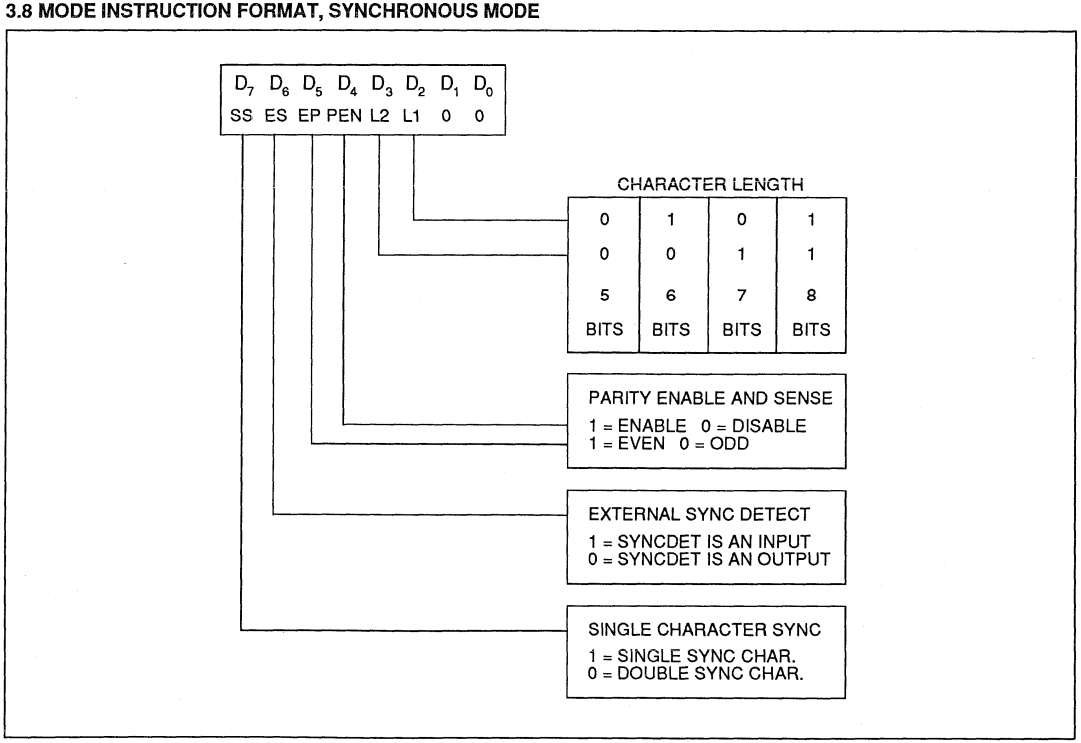


Figure 11: Mode Instruction Format, Synchronous Mode

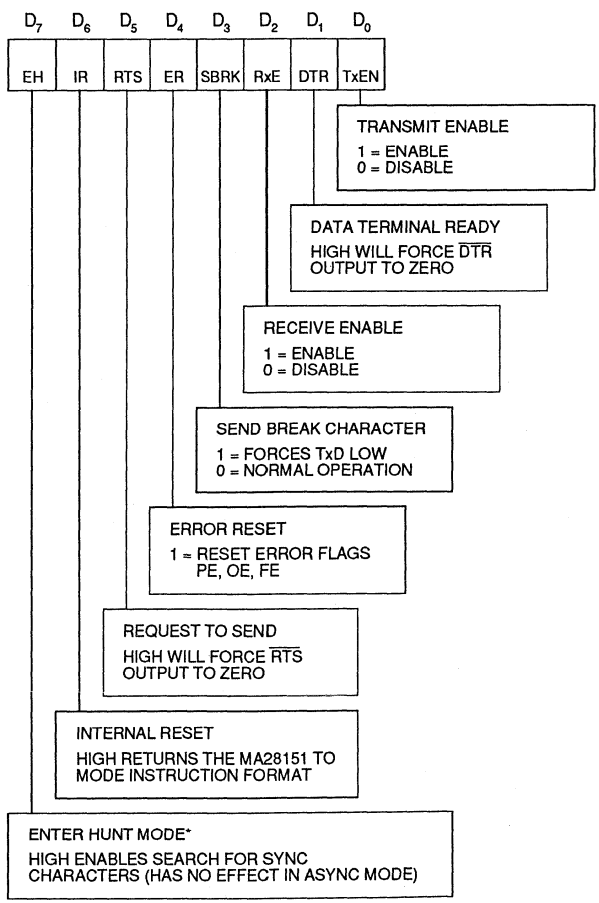
3.10 COMMAND INSTRUCTION DEFINITION

Once the functional definition of the MA28151 has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communications. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the MA28151 and Sync characters inserted, if necessary, then all further "control writes" (CDN=1) will load a Command Instruction. A Reset Operation (internal or external) will return the MA28151 to the Mode instruction format.

Note: Internal Reset on Power-up. When power is first applied, the MA28151 may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00_Hs consecutively into the device with CDN=1 configures sync operation and writes two dummy 00_H sync characters. An internal reset command (40_H) may then be issued to return the device to the idle state.

3.11 COMMAND INSTRUCTION FORMAT



*NOTE: ERROR RESET must be performed whenever RxENABLE and ENTER-HUNT are programmed.

Figure 12: Command Instruction Format

3.12 STATUS READ DEFINITION

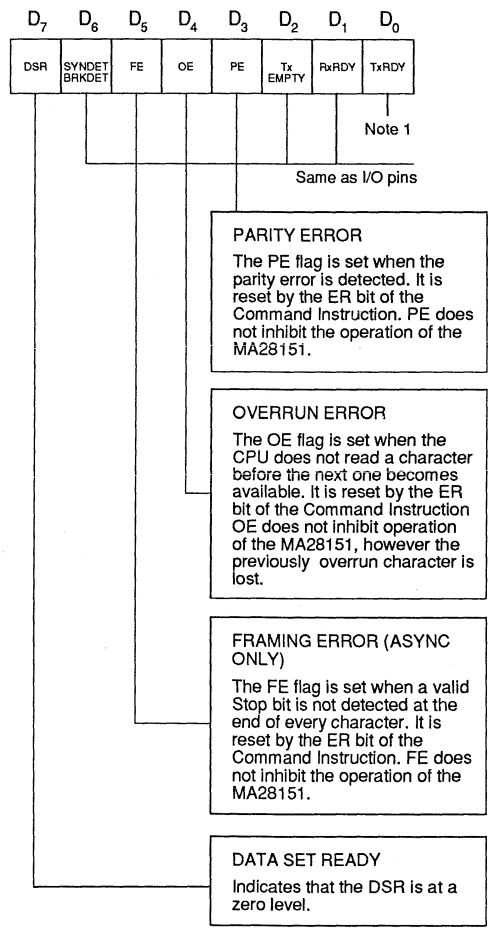
In data communication systems it is often necessary to examine the status of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The MA28151 has facilities that allow the programmer to read the status of the device at any time during the functional operation. (Status update is inhibited during status read).

A normal read command is issued by the CPU with CDN high to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the MA28151 can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

3.13 STATUS READ FORMAT



Note 1: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN, the latter is conditioned by both CTS and $\overline{TxEN}$.
ie. TxRDY status bit 0 DB buffer empty
TxRDY pin out = DB buffer empty OR ($\overline{CTSN}$ = 0) OR (TxEN = 1)

Figure 13: Status Read Format

4. TIMING WAVEFORMS

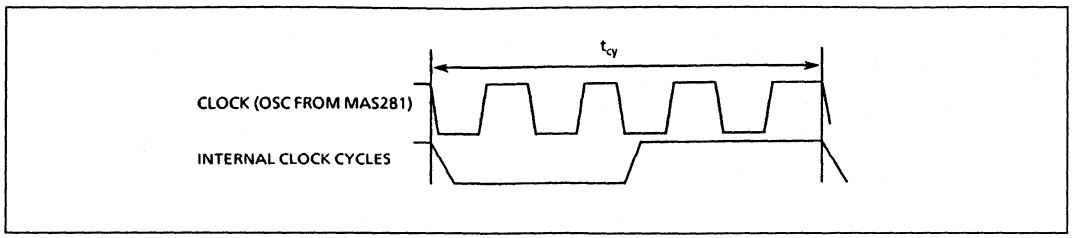


Figure 14: System Clock Input

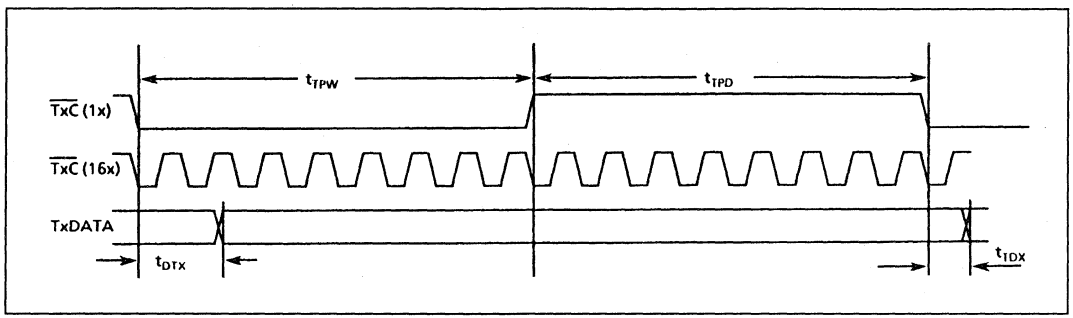


Figure 15: Transmitter Clock and Data

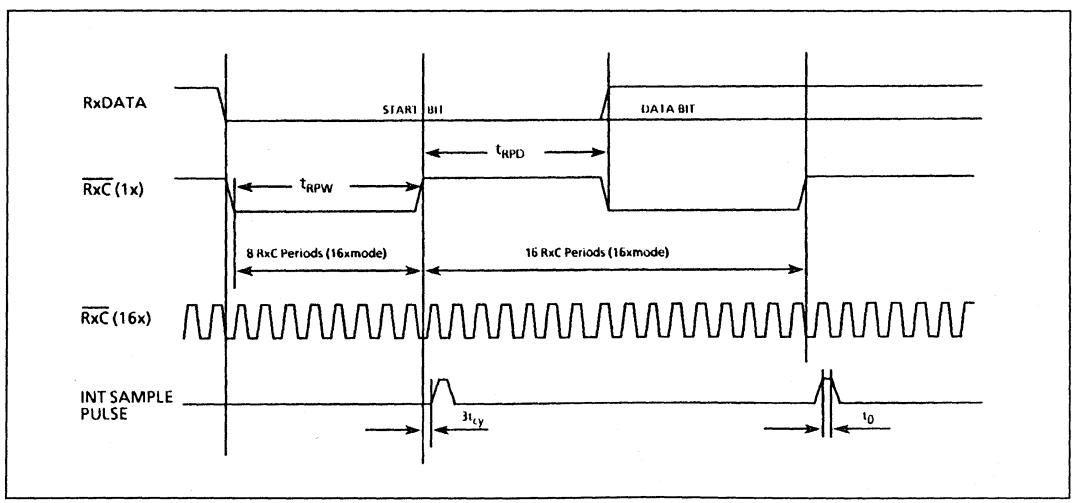


Figure 16: Receive Clock and Data

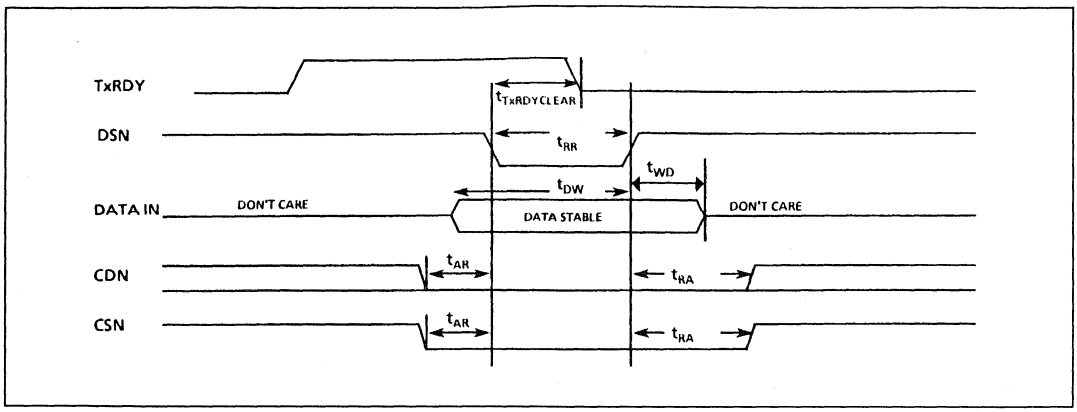


Figure 17: Write Data Cycle (CPU to USART)

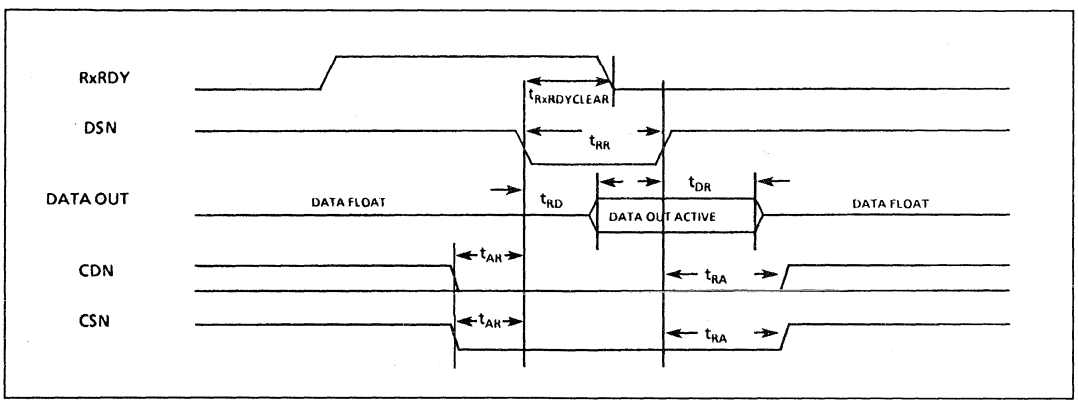


Figure 18: Read Data Cycle (USART to CPU)

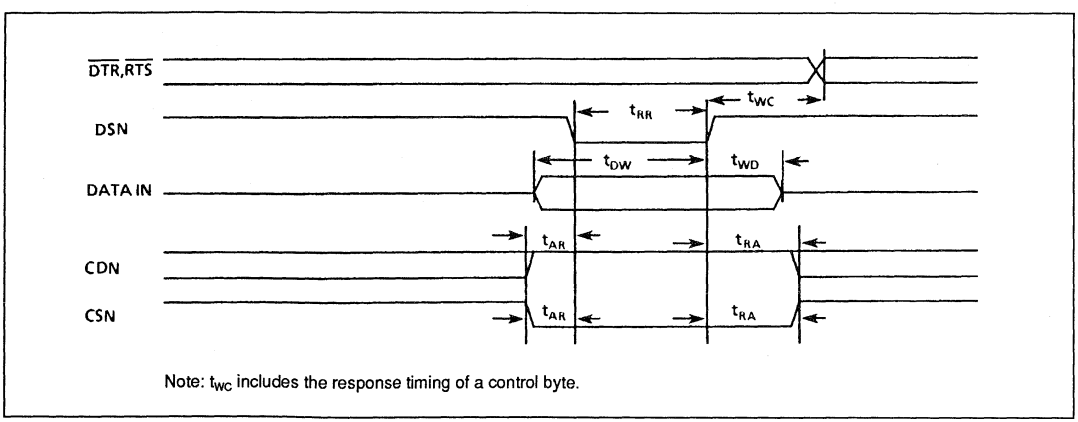


Figure 19: Write Control or Output Port Cycle (CPU to USART)

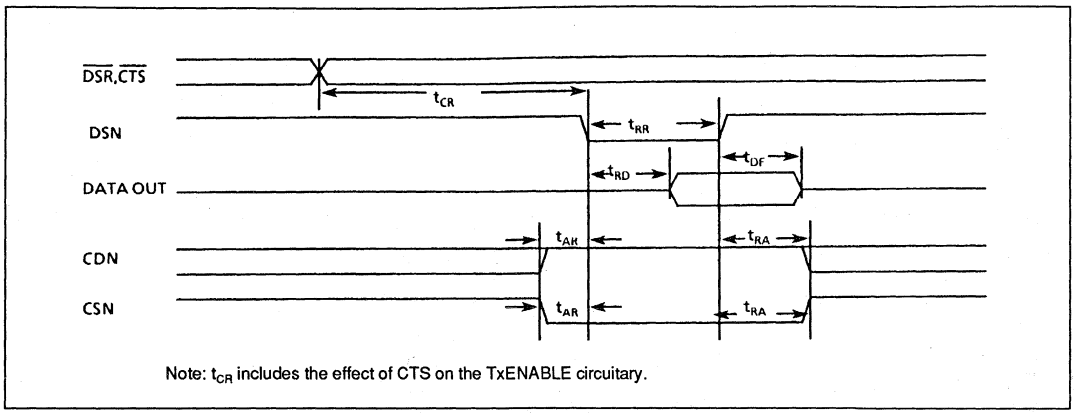


Figure 20: Read Control or Output Port Cycle (USART to CPU)

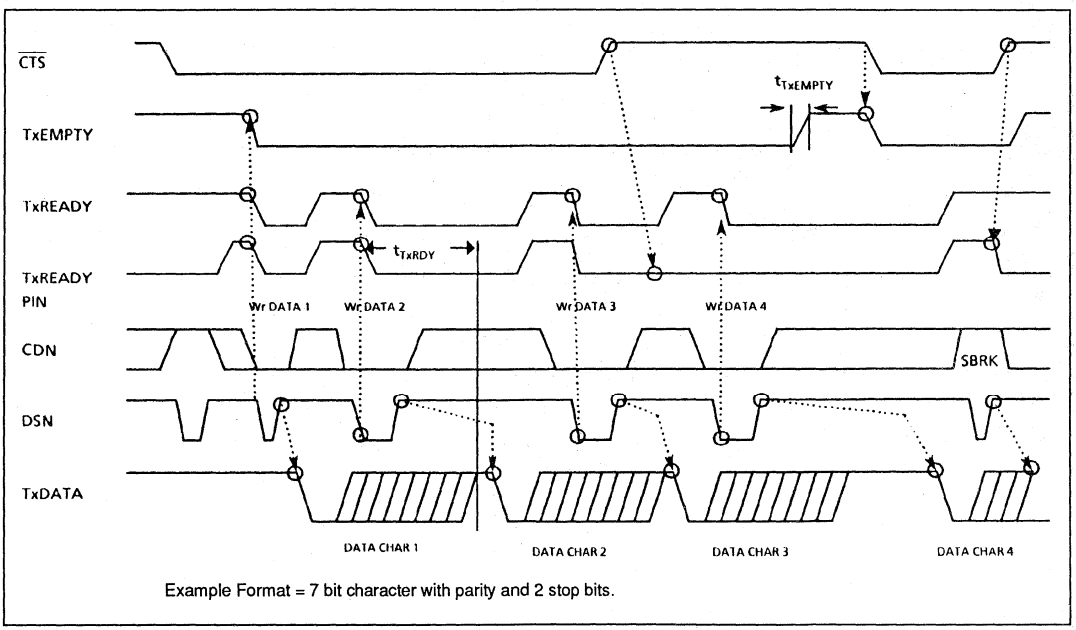


Figure 21: Transmitter Control and Flag Timing (ASYNC Mode)

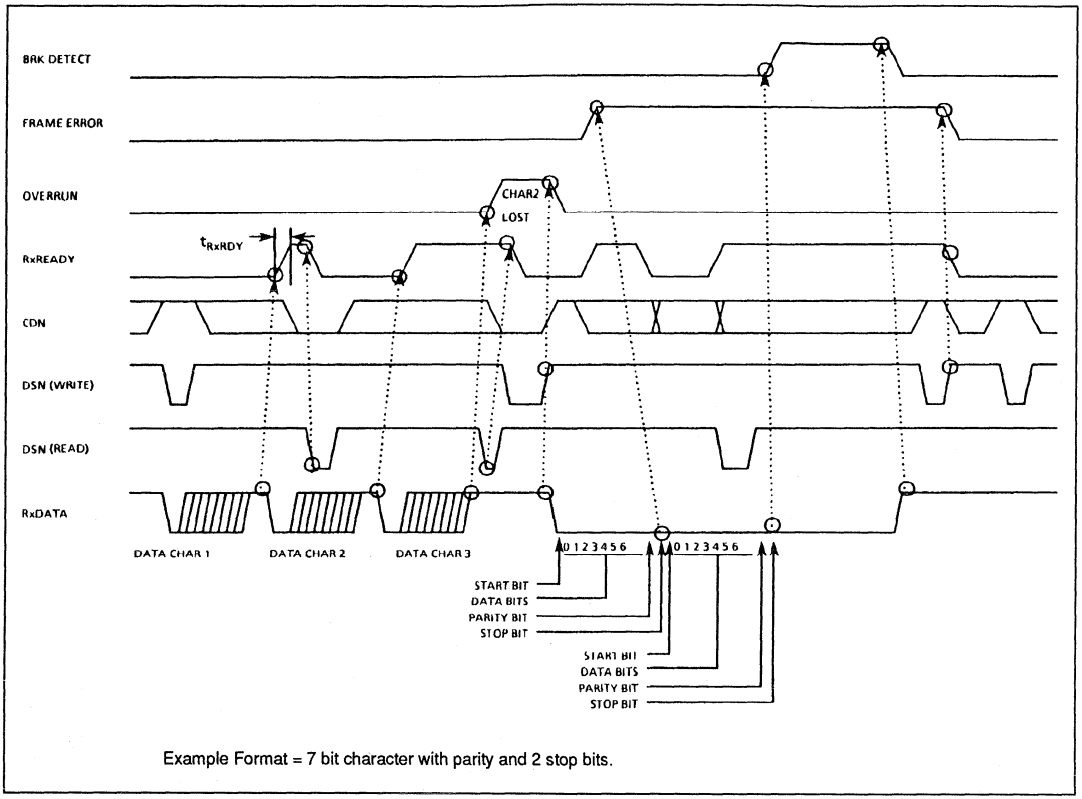


Figure 22: Receiver Control and Flag Timing (ASYNC Mode)

5. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Condition
t_{CY}	Internal clock cycle time	200	1000	nS	Notes 1, 5, 6
t_0	External Clock high pulse width	25	-	nS	-
$t_{\overline{0}}$	External Clock low pulse width	25	-	nS	-
t_R, t_F	Clock rise and fall time	-	10	nS	-
t_{DTX}	TxD delay from falling edge of TxD	-	1	µS	-
t_{TPW}	Transmitter input clock pulse width	$12xt_{CY}$	-	-	1 x baud rate
		$1xt_{CY}$	-	-	16 x and 64 x baud rate
t_{TPD}	Transmitter input clock pulse delay	$15xt_{CY}$	-	-	1 x baud rate
		$3xt_{CY}$	-	-	16 x and 64 x baud rate
t_{RPW}	Receive input clock pulse width	$12xt_{CY}$	-	-	1 x baud rate
		$1xt_{CY}$	-	-	16 x and 64 x baud rate
t_{RPD}	Receive input clock pulse delay	$15xt_{CY}$	-	-	1 x baud rate
		$3xt_{CY}$	-	-	16 x and 64 x baud rate
t_{TxRDY}	TxRDY pin delay from CENTER of last bit	-	$8xt_{CY}$	-	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY fall from falling DSN (WRITE)	-	45	-	Note 7
t_{RxRDY}	RxRDY pin delay from center of last bit	-	$26xt_{CY}$	-	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY fall from falling DSN (READ)	-	45	-	Note 7
$t_{TxEMPTY}$	TxEMPTY from centre of last bit	$20xt_{CY}$	-	-	Note 7
t_{WC}	Control delay from rising edge of WRITE	$8xt_{CY}$	-	-	Note 7
t_{CR}	Control to READ set-up time ($\overline{DSR}$, $\overline{CTS}$)	$20xt_{CY}$	-	-	Note 7
t_{AR}	Address stable before DSN (CSN, CDN)	0	-	ns	Note 2
t_{RA}	Address hold time before DSN (CSN, CDN)	0	-	ns	Note 2
t_{RR}	DSN pulse width	20	-	ns	-
t_{RD}	Data delay from DSN falling (READ)	-	30	ns	Note 3
t_{DF}	DSN rising to data floating (READ)	10	45	ns	Note 8
t_{DW}	Data set-up time to DSN rising (WRITE)	15	-	ns	-
t_{WD}	Data hold time to DSN rising (WRITE)	5	-	ns	-
t_{RV}	Recovery time between writes (not shown)	$6xt_{CY}$	-	-	Note 4

Notes: 1. AC Timings measured V_{OH} = 1.5 V_{OL} = 1.5.
2. CSN and Command/Data are considered as addresses.
3. Assumes that address is valid before DSN goes low.
4. This recovery time is for Mode Initialisation only. Write data is allowed when TxRDY = 1. Recovery time between writes for Asynchronous Mode is $8xt_{CY}$ and for Synchronous Mode is $16xt_{CY}$.
5. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitation with respect to clock: For 1 x baudrate, f_{TX} or $f_{RX} \leq 1/(30t_{CY})$: For 16 x and 64 x baud rate, f_{TX} or $f_{RX} \leq 1/(4.5t_{CY})$.
6. Reset Pulse Width = $6t_{CY}$ minimum; System clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.
8. Data Bus connected to V_{DD} via loads of 680Ω (minimum).

Mil-Std-883, method 5005, subgroups 9, 10, 11

Figure 23: AC Electrical Characteristics

Symbol	Parameter	Min.	Max.	Units	Condition
-	Clock Frequency (osc)	-	20	MHz	-
f_{Tx}	Transmitter input clock frequency	DC	64	kHz	1 x baud rate
		DC	310	kHz	16 x baud rate
		DC	615	kHz	64 x baud rate
f_{Rx}	Receiver input clock frequency	DC	64	kHz	1x baud rate
		DC	310	kHz	16 x baud rate
		DC	615	kHz	64 x baud rate

Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Figure 24: Operating AC Electrical Characteristics

6. DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 25: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	2.2	-	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	V_{DD}-0.5	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA	-	-	V_{SS}+0.4	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Tristate Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	µA
I_{DD}	Power Supply Current	Static, V_{DD} = 5.5V	-	0.1	10	mA

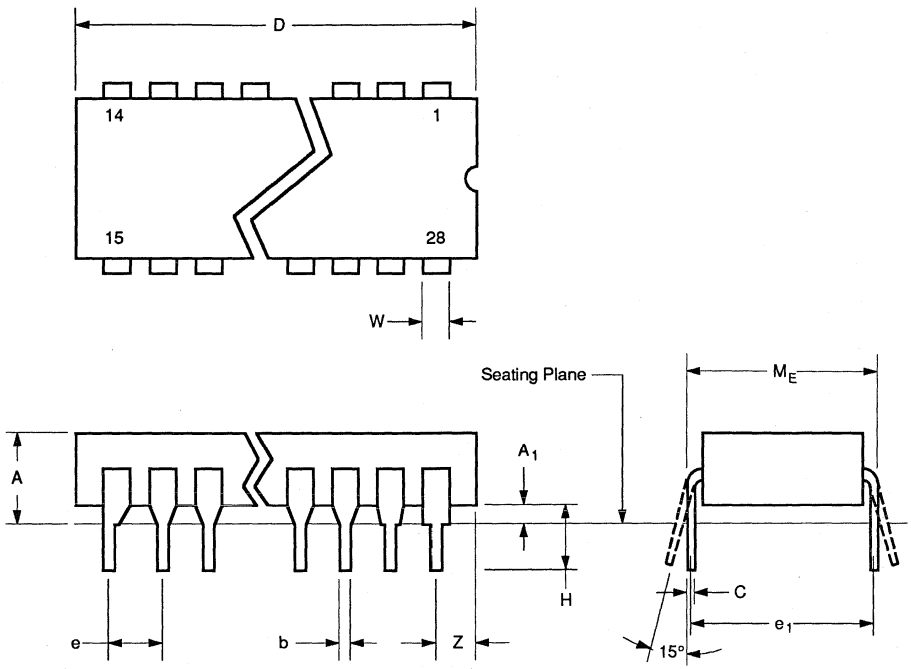
V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not tested at -55°C

Figure 26: Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 26 at +25°C
2	Static characteristics specified in Figure 26 at +125°C
3	Static characteristics specified in Figure 26 at -55°C
7	Functional characteristics specified in Figure 24 at +25°C
8A	Functional characteristics specified in Figure 24 at +125°C
8B	Functional characteristics specified in Figure 24 at -55°C
9	Switching characteristics specified in Figure 23 at +25°C
10	Switching characteristics specified in Figure 23 at +125°C
11	Switching characteristics specified in Figure 23 at -55°C

Figure 27: Definition of Mil-Std-883, Method 5005 Subgroups

7. OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

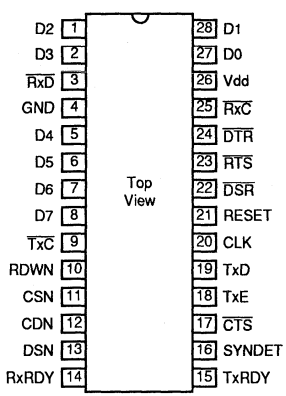
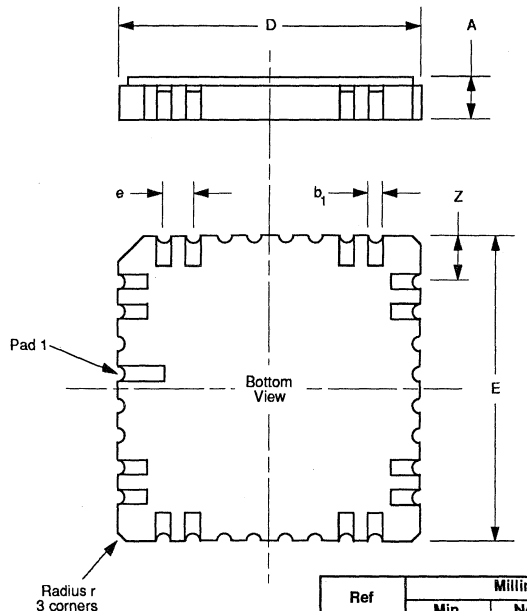


Figure 28: 28-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.29	-	-	0.090
b1	-	0.51	-	-	0.020	-
D	-	-	14.60	-	-	0.575
E	-	-	14.60	-	-	0.575
e	-	1.02	-	-	0.040	-
Z	-	1.52 Typ.	-	-	0.060 Typ.	-

XG431

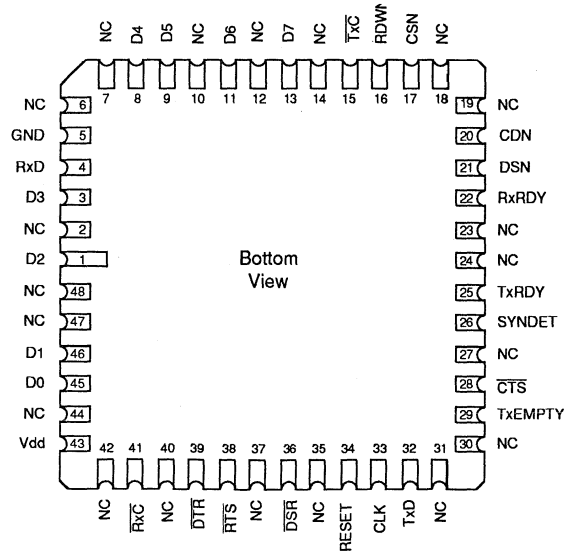
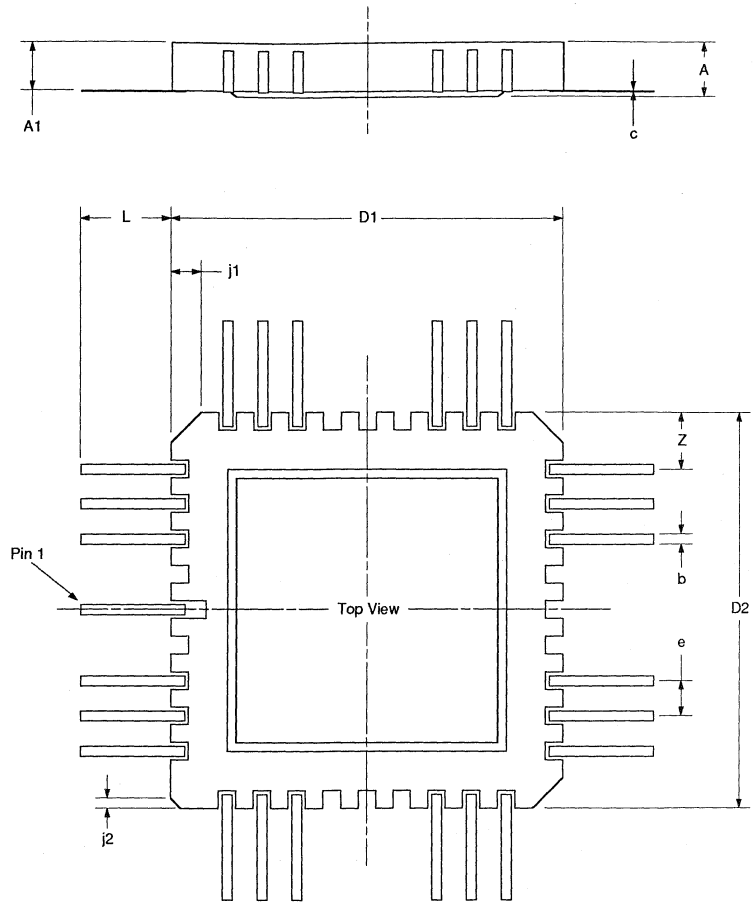


Figure 29: 48-Pad Leadless Chip Carrier - Package Style L



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

Figure 30a: 68-Lead Topbraze Flatpack - Package Style F

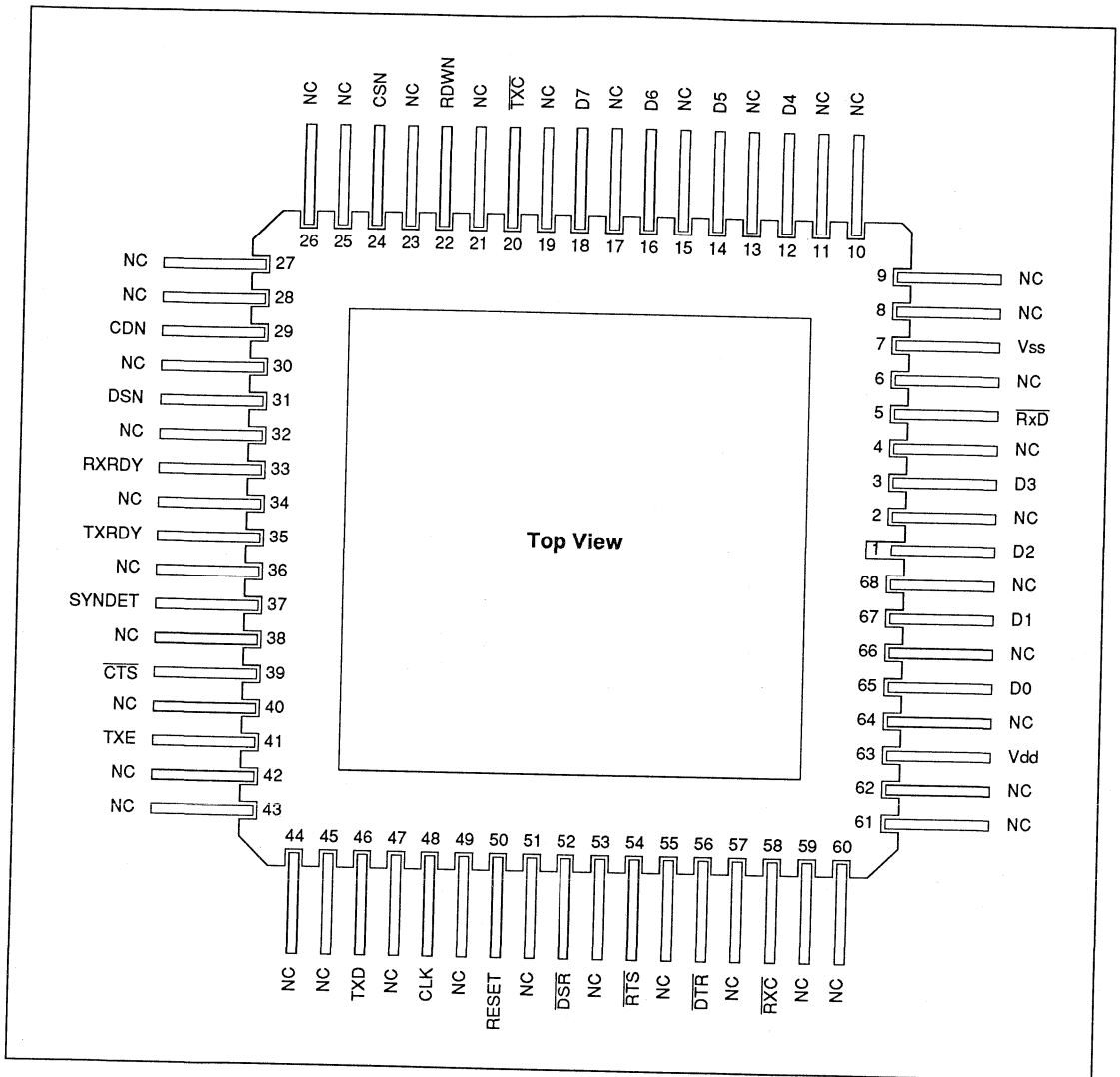


Figure 30b: 68-Lead Topbraze Flatpack - Package Style F

8. RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 Ionizing Radiation (Total Dose) test 1019.

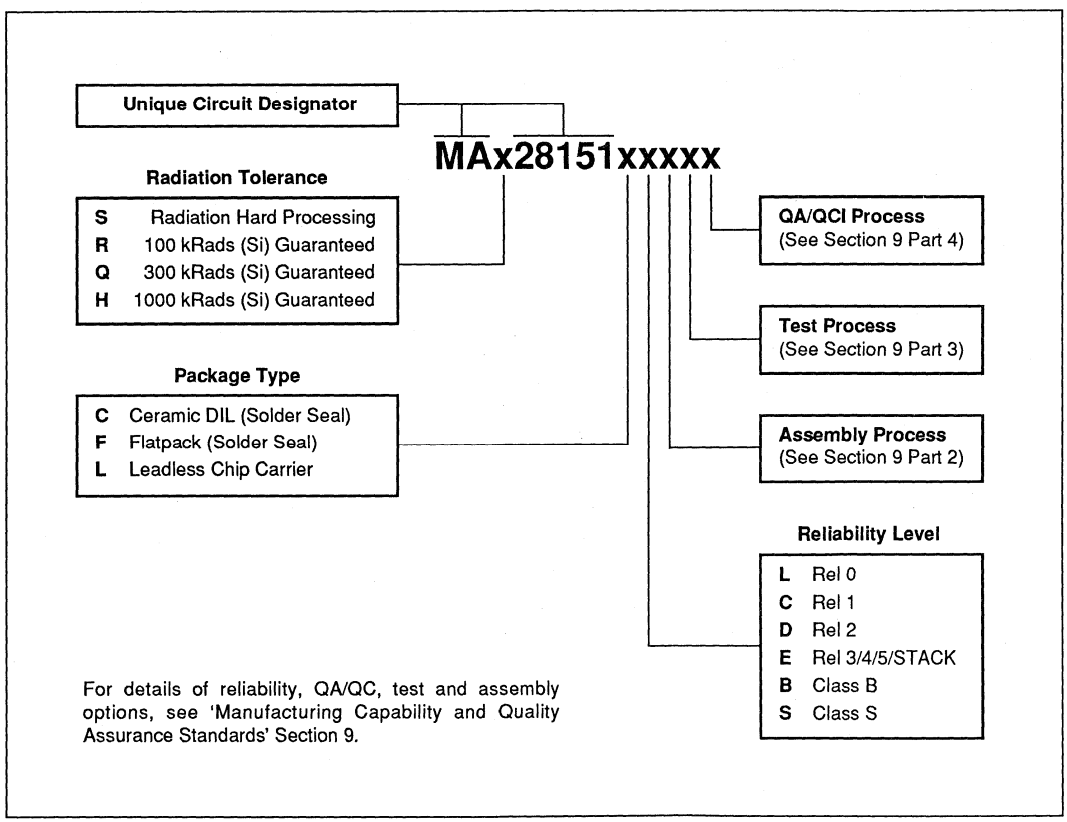
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 31: Radiation Hardness Parameters

9. ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3575-3.5

MA28155

RADIATION HARD PROGRAMMABLE PERIPHERAL INTERFACE

The MA28155 is a general purpose programmable Input/Output device designed for use with the MAS281 microprocessor. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be inputs or outputs. In the second mode (MODE 1), each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for hand-shaking and interrupt control signals. The third mode of operation (MODE 2) is the bidirectional bus mode, which uses 8 lines for a bidirectional bus and 5 lines, borrowing one from the other group, for hand-shaking.

FEATURES

- Radiation Hard to 1MRad (Si)
- High SEU Immunity, Latch Up Free
- Silicon-on-Sapphire Technology
- 24 Programmable I/O Pins
- All Inputs and Outputs are TTL Compatible
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Replaces Several MSI Packages
- Compatible with MAS281 (Mil-Std-1750A) Microprocessor

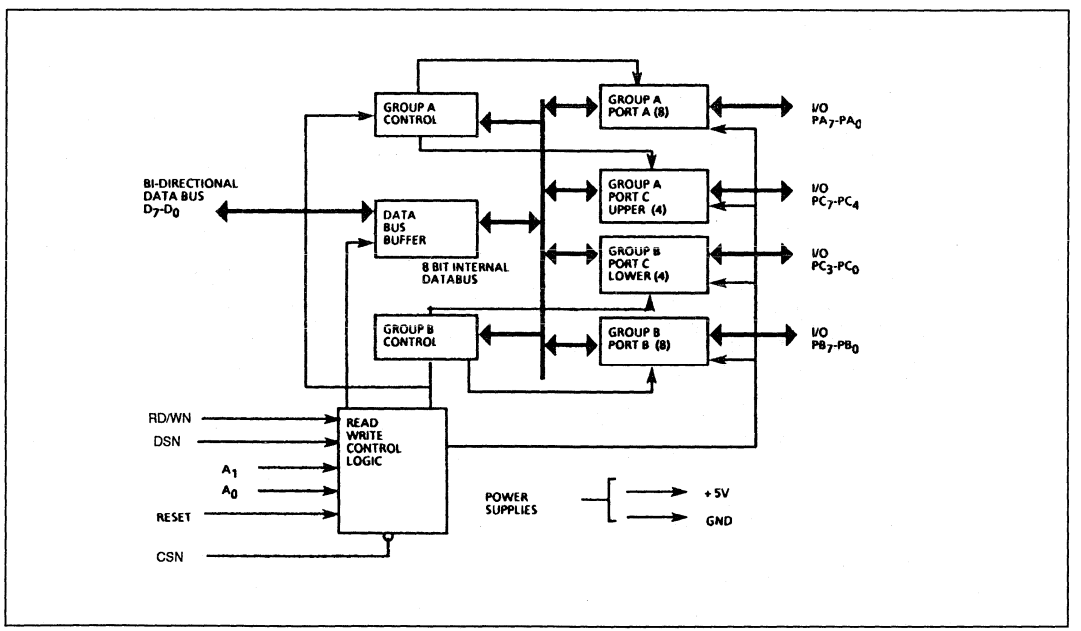


Figure 1: Block Diagram

FUNCTIONAL DESCRIPTION

The MA28155 is a programmable peripheral interface (PPI) device designed for use with MAS281. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the MA28155 is programmed by the system software so that, normally, no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the MA28155 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Reset (RESET)

A high on this input clears the control register and all ports (A,B,C) are set to the input mode.

Chip Select (CSN)

A low on this input pin enables the communication between the MA28155 and the CPU.

Read/Write Select (RD/WN)

A high on RD/WN indicates a CPU read from the MA28155 and a low indicates a CPU data or control word write to the MA28155. The RD/WN line is active only when DSN is low.

Data Strobe (DSN)

This input indicates that a data transfer is taking place. During a CPU write operation the MA28155 reads data from the bus on the rising edge of DSN. During a read operation the MA28155 outputs data to the bus while DSN is low. Data is valid on the rising edge of DSN.

Port Select O and Port Select 1 (AO and A1)

These input signals, in conjunction with the DSN and RD/WN inputs, control the selection of one of the three ports of the control word registers. They are normally connected to the least significant bits of the address bus.

Basic Operation

A1	A0	DSN	RD/WN	CSN	READ
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					WRITE
0	0	0	0	0	DATA BUS → PORT A
0	1	0	0	0	DATA BUS → PORT B
1	0	0	0	1	DATA BUS → PORT C
1	1	0	0	1	DATA BUS → CONTROL
					DISABLE
x	x	x	x	1	DATA BUS → TRI-STATE
1	1	0	1	0	ILLEGAL CONDITION
x	x	1	x	0	DATA BUS → TRI-STATE

Table 1: Basic Operation

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation, which can be selected by the system software:

Mode 0. Basic Input/Output
Mode 1. Strobed Input/Output
Mode 2 Bi-directional Bus

When the reset input goes high all ports will be set to the input mode (i.e. all 24 lines will be in the high impedance state) After the reset is removed the MA28155 can remain in the input mode with no additional initialisation required.

During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single MA28155 to service a variety of peripheral devices with a single software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed.

Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance; Group B can be programmed in Mode 0 whilst Group A could be simultaneously programmed in Mode 1.

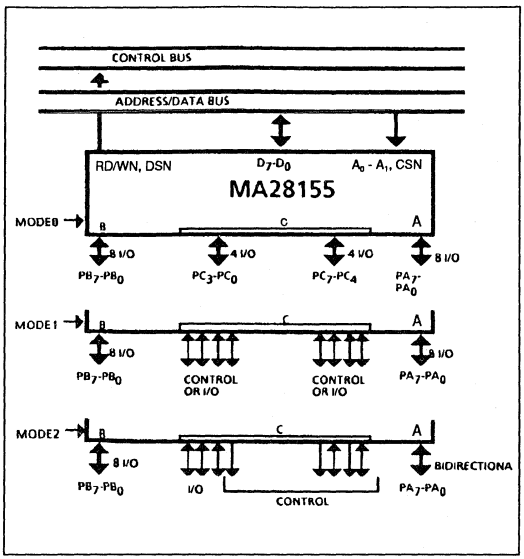


Figure 2: Basic Mode Definitions and Bus Interface

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as Status/Control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the MA28155 is programmed to operate in Mode 1 or 2, control signals are provided that can be used as interrupt request inputs to the CPU (figure 4). The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE register bit, using the Bit Set/Reset function of Port C.

This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU, without affecting any other device in the interrupt structure.

INTE register bit definitions:
(BIT-SET): INTE is SET -Interrupt enable
(BIT-RESET): INTE is RESET -Interrupt disable

Note: All mask register bits are automatically reset during mode selection and device reset.

Mode Definition Format (D_7= 1)

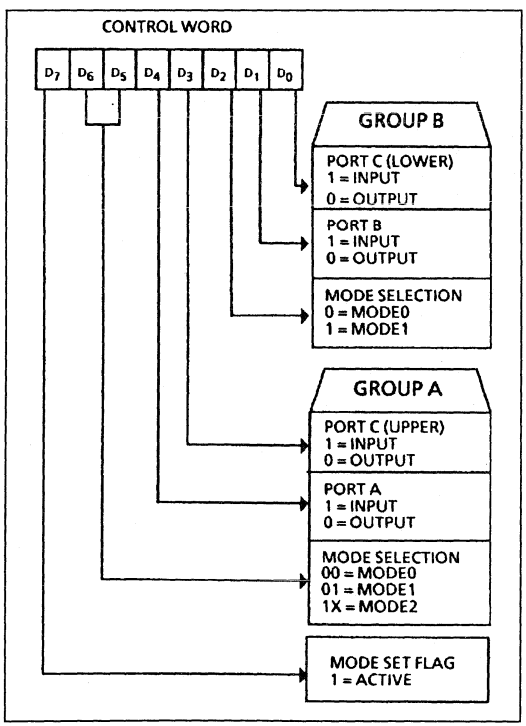


Figure 3: Mode Definition Format (D_7 = 1)

Bit Set/Reset Format (D_7 = 0)

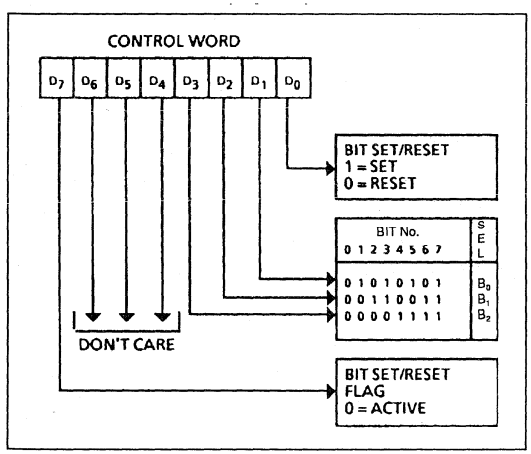


Figure 4: Bit Set/Reset Format (D_7 = 0)

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. In essence, the CPU outputs a control word to the MA28155. The control word contains information such as mode, bit set, bit reset, etc., this initializes the functional configuration of the MA28155.

Each of the Control blocks (Group A and Group B) accept commands from the Read/Write Control Logic, receive control words from the internal data bus and issue the proper commands to its associated ports:

Control Group A - Port A and Port C upper (C7-C4) Control Group B - Port B and Port C lower (C3-C0)

The Control Word Register can only be written into. Therefore reading of the Control Word Register is not allowed .

Ports A, B and C

The MA28155 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features to further enhance the power and flexibility of the MA28155.

Port A.

One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B.

One 8-bit data input/output latch/buffer and one 8-bit input buffer

Port C.

One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input) This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B

OPERATING MODE 0
(Basic Input/Output)

This functional configuration provides simple input and output operation for each of the three ports. No handshaking is required; data is simply written to or read from a specified port.

- Two 8-bit ports and 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

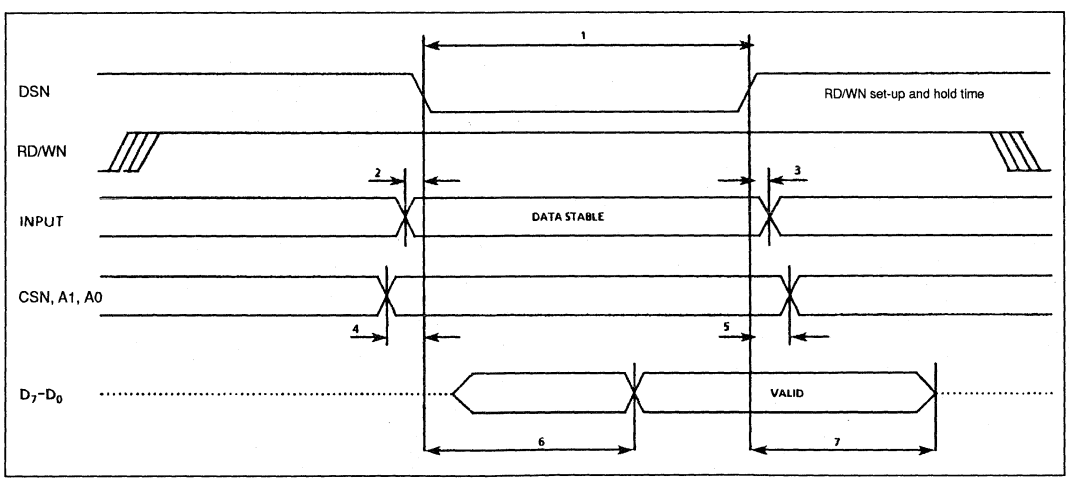


Figure 5: Basic Input (Read) Timing Diagram

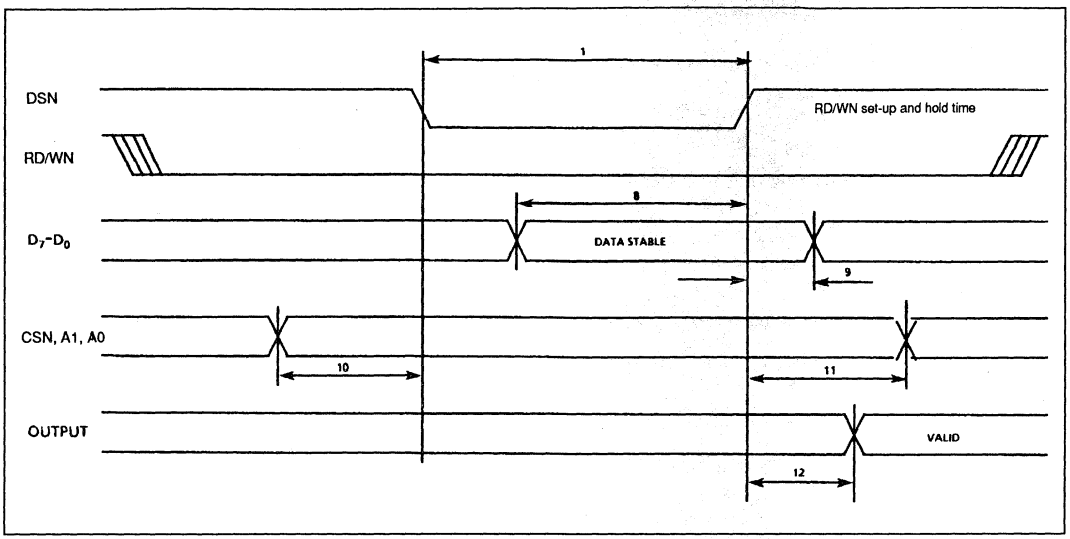


Figure 6: Basic Input (Write) Timing Diagram

Port Definition Mode 0

D_4	D_3	D_1	D_0	PORT A (UPPER)	PORT C	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	INPUT	INPUT
1	1	0	0	INPUT	INPUT	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	INPUT	INPUT

Table 2: Port Definition Mode 0 (See Also Figure 3)

OPERATING MODE 1
(Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or handshaking signals. In mode 1, port A and port B use the lines on port C to generate or accept these handshaking signals

- Two Groups (Group A and Group B) .
- Each Group contains one 8-bit data port and one 4-bit control/data port,
- The 8-bit data port can be either input or output, Both inputs and outputs are latched,
- The 4-bit port is used for control and status of the 8-bit data port.

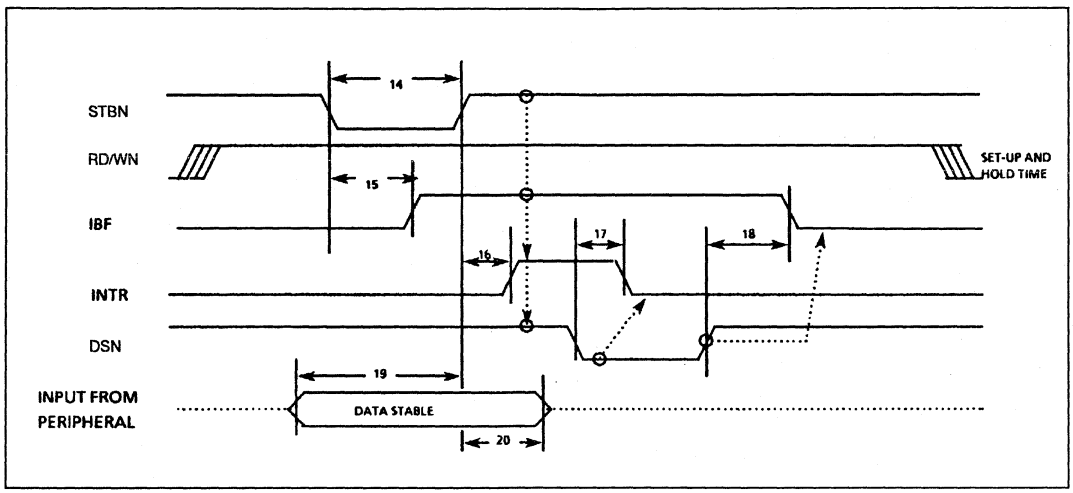


Figure 7: Strobed Input Timing Diagram

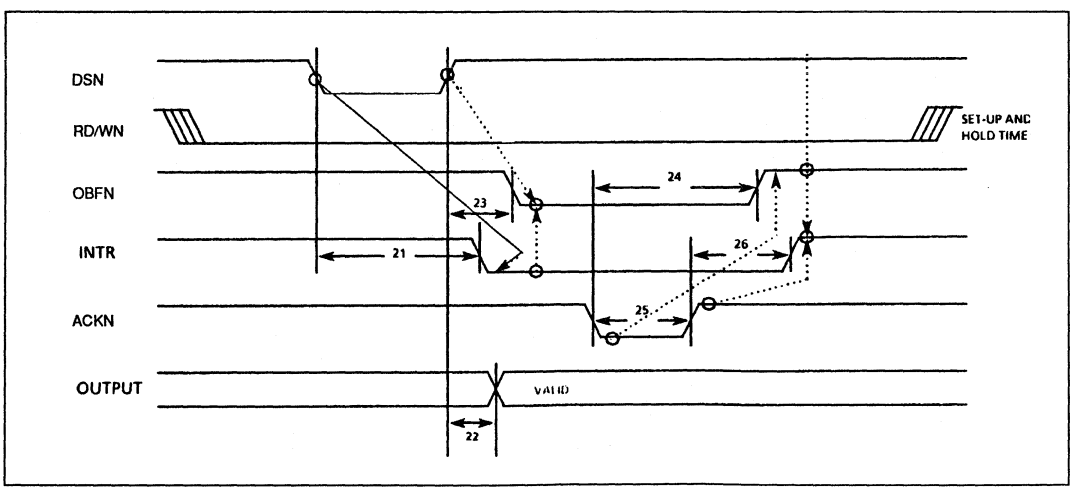


Figure 8: Strobed Output Timing Diagram

Input Control Signal Definition (Mode 1)

STBN (Strobe Input).

A low on this input loads data into the input latch.

IBF (Input Buffer Full Register Bit).

A high on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement.

IBF is set by a STBN active pulse (which strobes data into the device), and is reset by the rising edge of DSN (which reads the latched data out of the device).

INTR (Interrupt Request).

A high on this output can be used to interrupt the CPU when an input device is requesting service, INTR is set by the STBN being high and IBF being high and INTE being enabled, It is reset by the falling edge of DSN, This procedure allows an input device to request service from the CPU by simply strobing its data into the port,

INTE A: Controlled by bit set/reset of PC_4

INTE B: Controlled by bit set/reset of PC_2

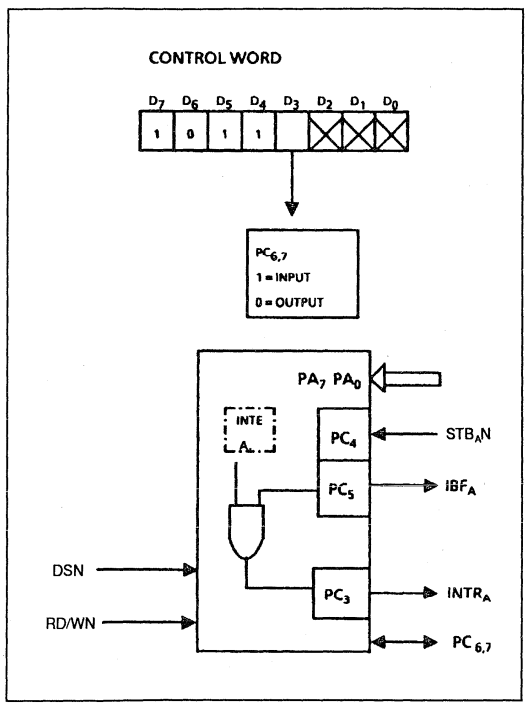


Figure 9: Strobed Input (PORT A)

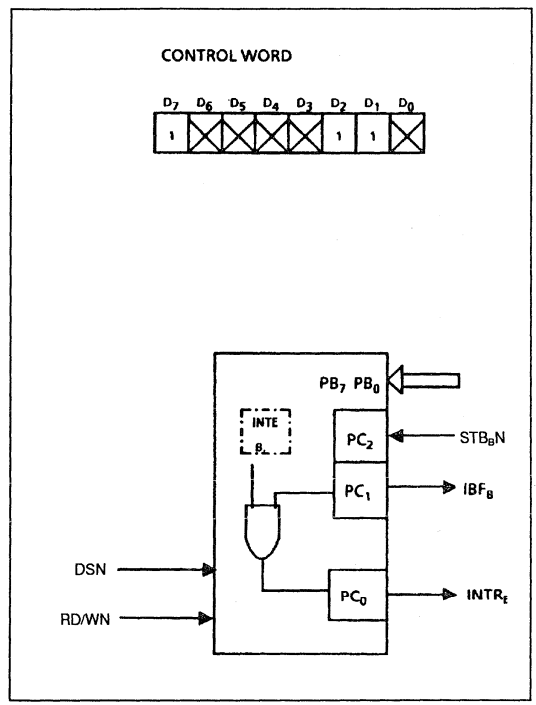


Figure 10: Strobed Input (PORT B)

Output Control Signal Definition (Mode 1)

OBFN (Output Buffer Full Register Bit).

The OBFN output will go low to indicate that the CPU has written data out to the specified port. The OBF register bit will be set by the rising edge of the DSN input and reset by ACKN input being low.

ACKN (Acknowledge Input).

A low on this input informs the 28155 that the data from port A or port B has been accepted; in essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request).

A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACKN is high, OBFN is high and INTE is high. It is reset by the falling edge of DSN.

INTE A: Controlled by bit set/reset of PC_6
INTE B: Controlled by bit set/reset of PC_2

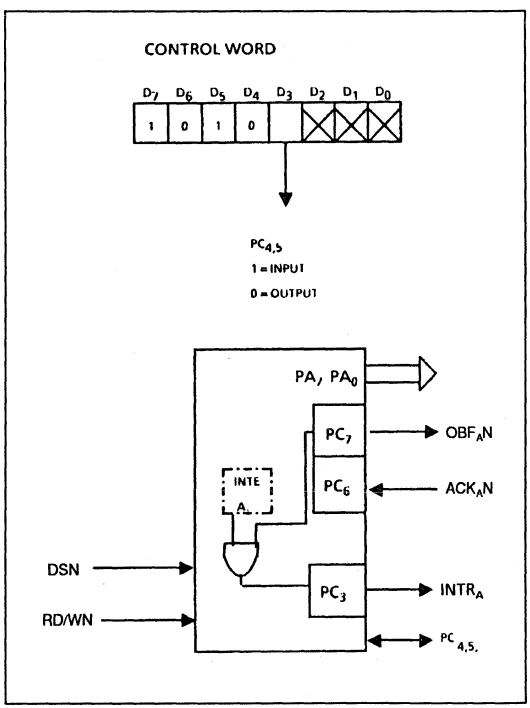


Figure 11: Strobed Output (PORT A)

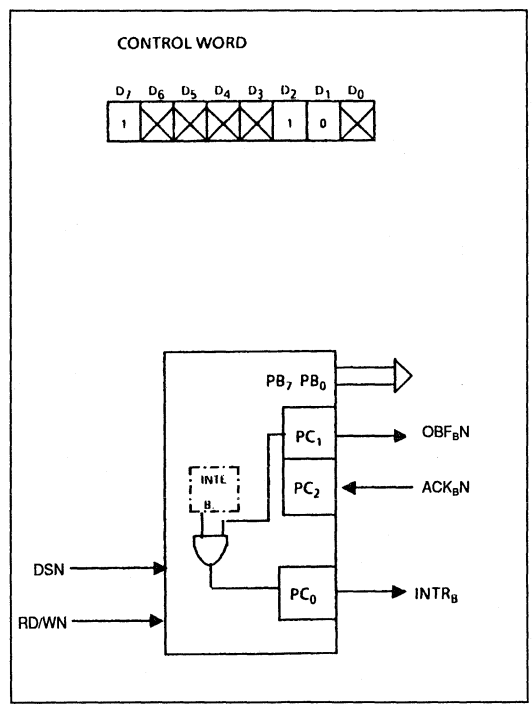


Figure 12: Strobed Output (PORT B)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

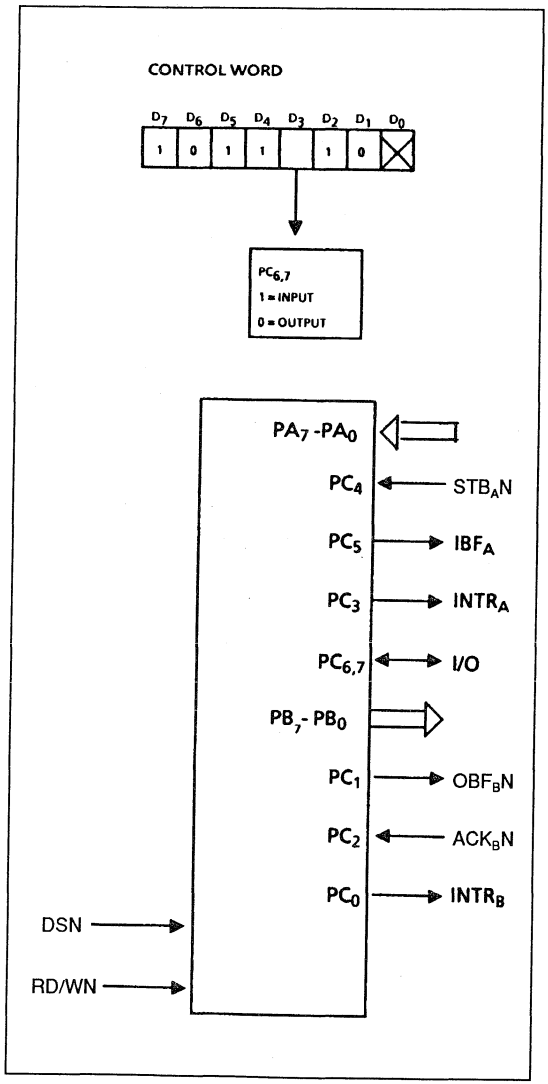


Figure 13: PORT A (STROBED INPUT) PORT B (STROBED OUTPUT)

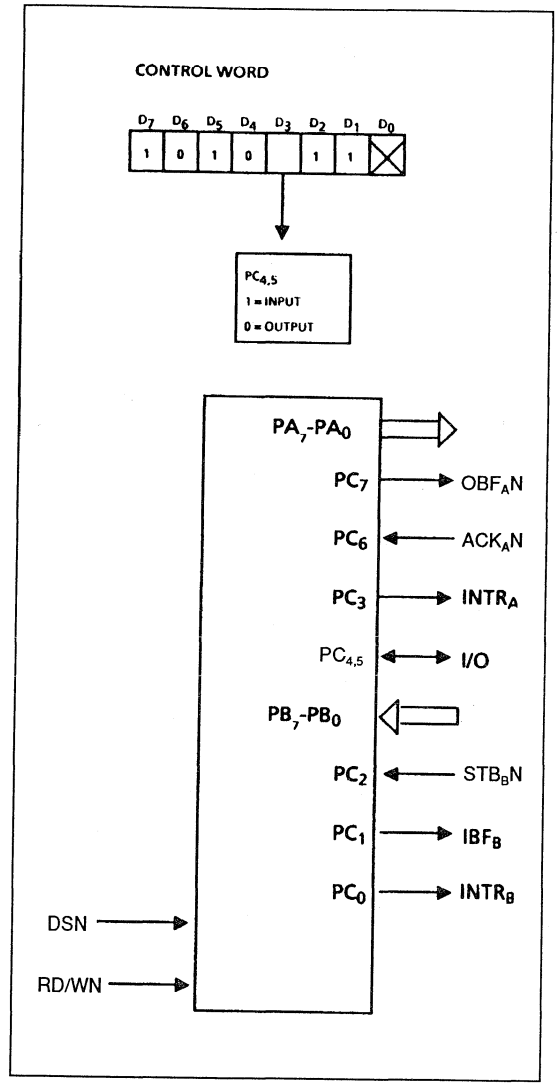
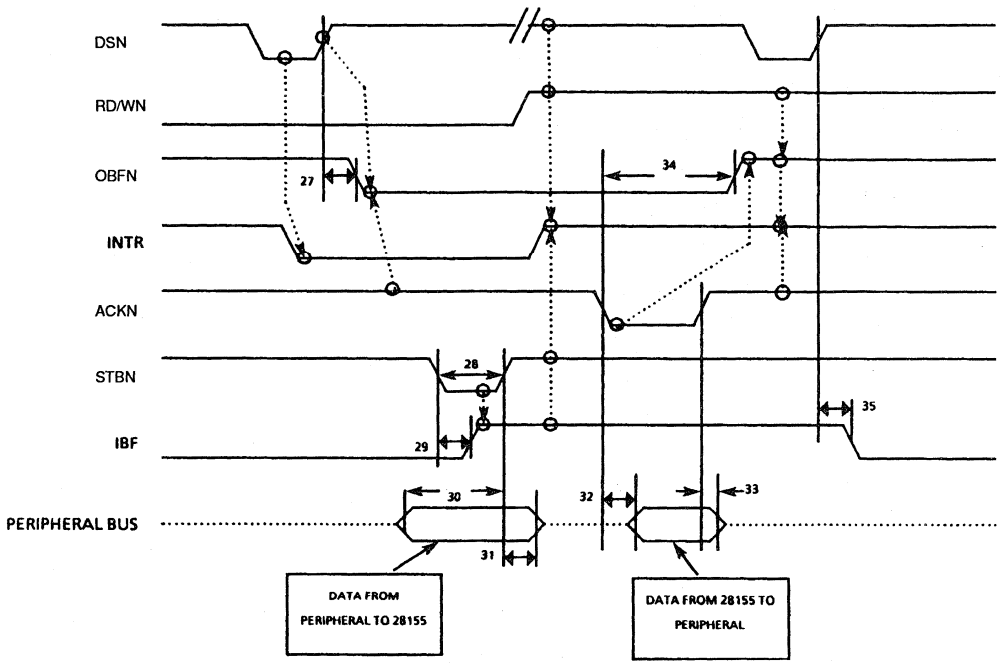


Figure 14: PORT A (STROBED OUTPUT) PORT B (STROBED INPUT)

OPERATING MODE 2
(Strobed Bidirectional Bus I/0)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O) . Handshaking signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1, Interrupt generation and enable/disable functions are also available.

- Used in group A only.
- One 8-bit bidirectional bus port (port A) and 5-bit control port (port C).
- Both inputs and outputs are latched,
- The 5-bit control port (port C) is used for control and status of the 8-bit bidirectional bus port (port A).



NOTE:
Any sequence where RD/WN = 0 coincident with DSN low occurs before ACKN and STBN occurs before RD/WN = 1 coincident with DSN is permissable
(INTR = IBF MASK STBN (RD/WN = 1. DSN = 0) + OBFN MASK ACKN (RD/WN = 0. DSN = 0))

Figure 15: Bidirectional Timing Diagram

BIDIRECTIONAL BUS I/O CONTROL

Signal Definition (Mode 2)

INTR (Interrupt Request):
A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

OBFN (Output Buffer Full):
The OBF output will go low to indicate that the CPU has written data out to port A.

ACKN (Acknowledge):
A low on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state,

INTE 1 (INTE register bit associated with OBFN):
Controlled by Bit Set/Reset of PC_6.

Input Operations

STBN (Strobe input):
A low on this input loads data in to the input latch,

IBF (Input Buffer Full Register Bit):
A high on this output indicates data has been loaded in to the input latch,

INTE 2 (The INTE register bit associated with IBF).
Controlled by Bit Set/Reset of PC_4.

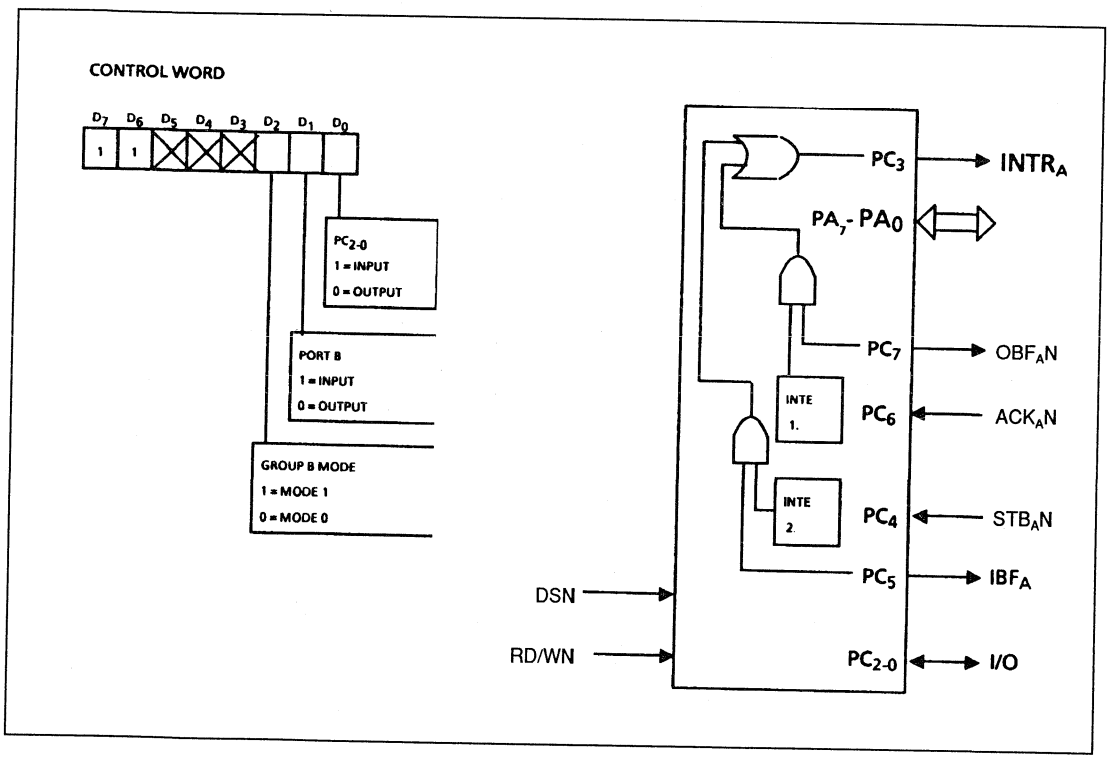


Figure 16: Mode 2 Bidirectional

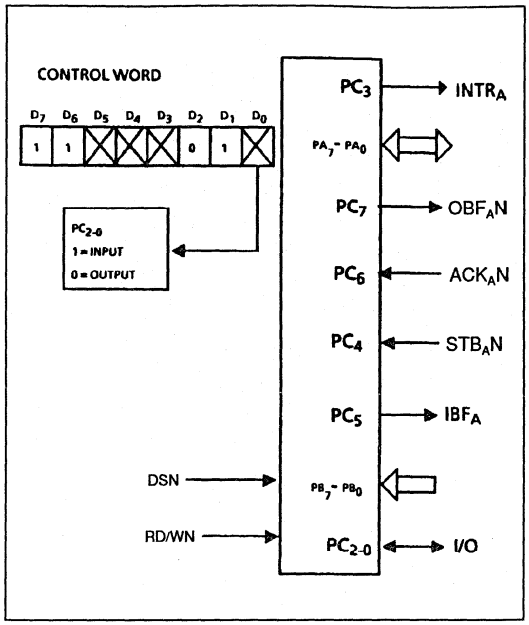


Figure 17a: Mode 2 and Mode 0 (Input)

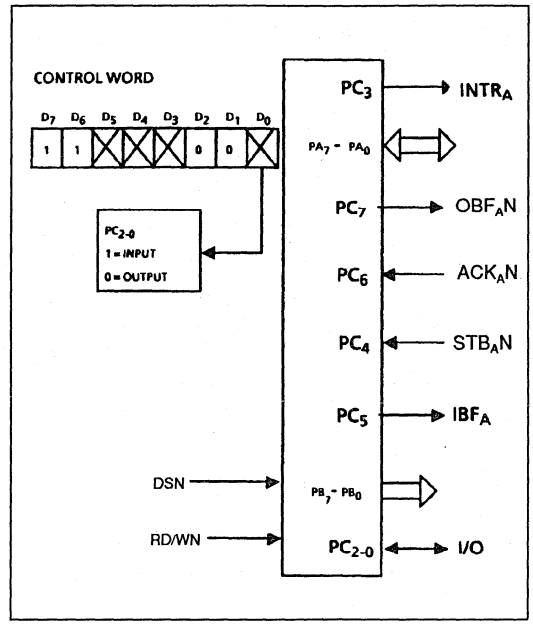


Figure 17b: Mode 2 and Mode 0 (Output)

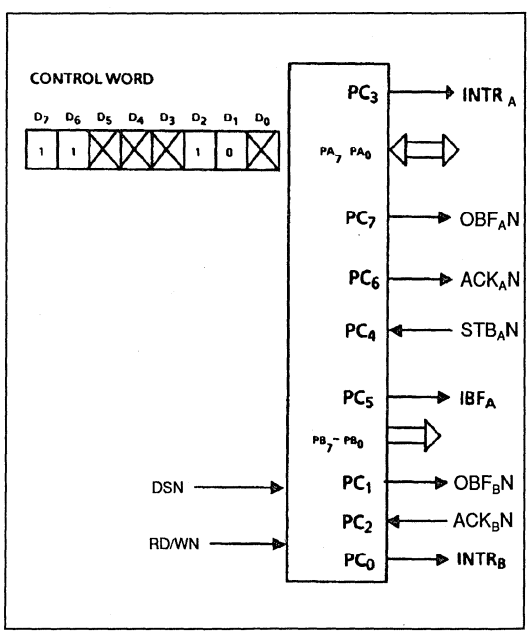


Figure 17c: Mode 2 and Mode 1 (Output)

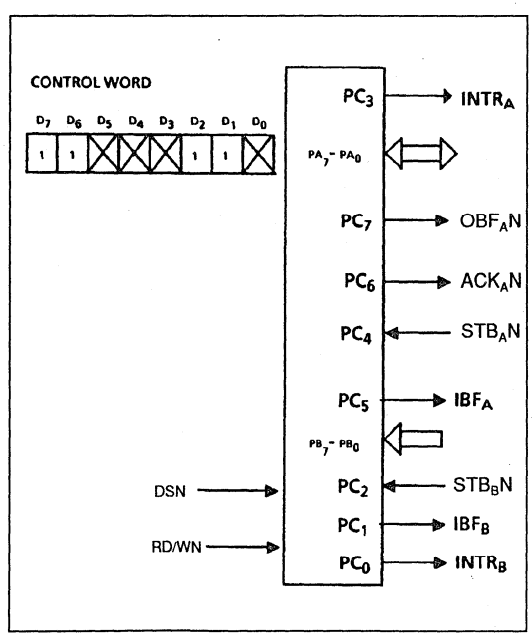


Figure 17d: Mode 2 and Mode 1 (Input)

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	
PA_0	IN	OUT	IN	OUT	⇐ ⇒
PA_1	IN	OUT	IN	OUT	⇐ ⇒
PA_2	IN	OUT	IN	OUT	⇐ ⇒
PA_3	IN	OUT	IN	OUT	⇐ ⇒
PA_4	IN	OUT	IN	OUT	⇐ ⇒
PA_5	IN	OUT	IN	OUT	⇐ ⇒
PA_6	IN	OUT	IN	OUT	⇐ ⇒
PA_7	IN	OUT	IN	OUT	⇐ ⇒
PB_0	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_1	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_2	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_3	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_4	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_5	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_6	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PB_7	IN	OUT	IN	OUT	PORT B MODE 0 or 1
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	OBF_BN	I/O
PC_2	IN	OUT	STB_BN	ACK_BN	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	STB_AN	I/O	STB_AN
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	ACK_AN	ACK_AN
PC_7	IN	OUT	I/O	OBF_AN	OBF_AN

Table 3: Mode Definition Summary

Special Mode Combination Considerations.

There are several combinations of modes when not all of the bits in port C are used for control or status. The remaining bits can be used as follows:

If programmmed as inputs-

All input lines can be accessed during normal port C read.

If programmed as outputs

Bits in C upper (PC7-PC4) must be individually accessed using a bit set/reset function.

Bits in C lower (PC3-PC0) can be accessed using the bit set/reset function or bits PC2-PC0 may also be accessed as a trio by writing into port C.

Reading Port C Status.

In Mode 0 Port C transfers data from or to the peripheral device, When the MA28155 is programmed to function in Modes 1 or 2 Port C generates or accepts handshaking signals with the peripheral device, Reading the contents of Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is no special instruction to read the Status Information from Port C. A normal read operation of Port C is executed to perform this function.

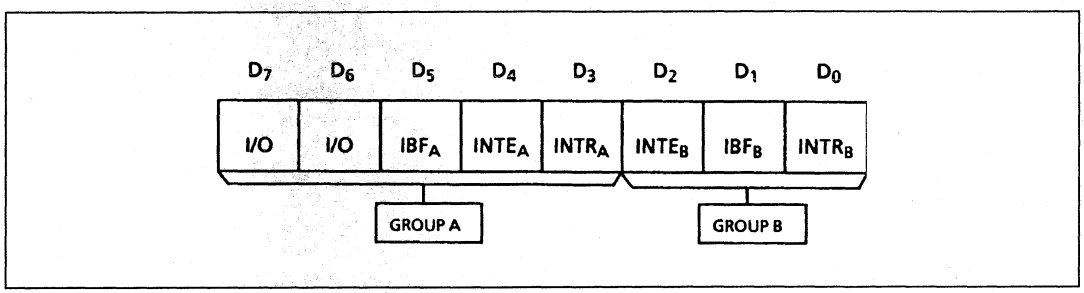


Figure 18a: Mode 1 Input Configuration

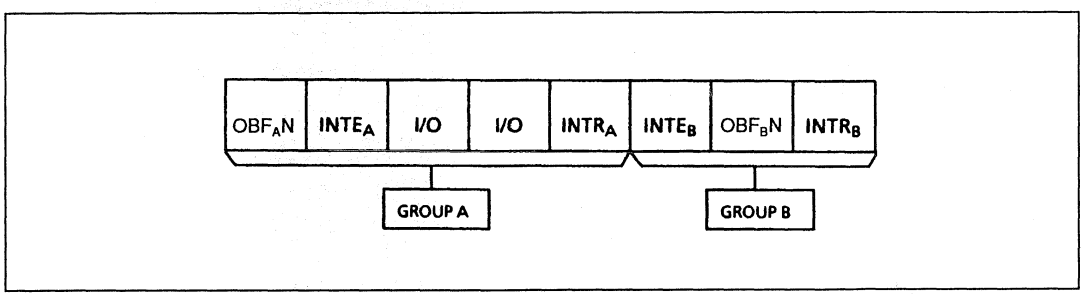


Figure 18b: Mode 1 Output Configuration

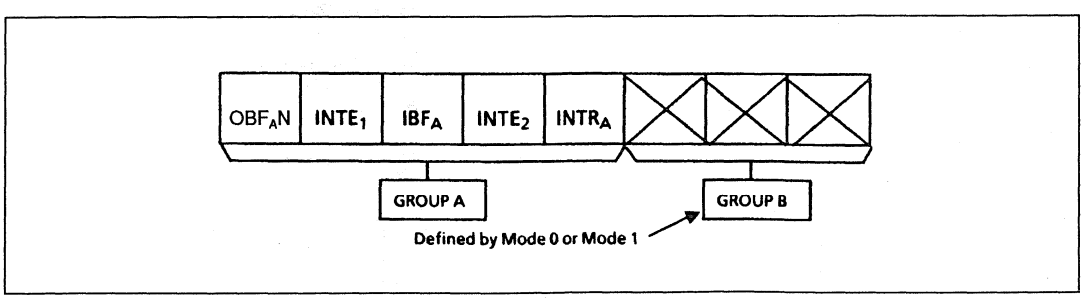


Figure 18c: Mode 2

DEFINITION OF SUBGROUPS

Subgroup	Definition
1	Static characteristics specified in Table 5 at +25°C
2	Static characteristics specified in Table 5 at +125°C
3	Static characteristics specified in Table 5 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Table 6 at +25°C
10	Switching characteristics specified in Table 6 at +125°C
11	Switching characteristics specified in Table 6 at -55°C

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	2.2	-	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -6mA	3.5	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 12mA	-	-	0.5	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Tristate Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	µA
I_{DD}	Power Supply Current	Static,	-	0.1	10	mA

Note 1: Guaranteed but not tested at -55°C
Mil-Std-883, method 5005, subgroups 1, 2, 3.
V_{DD} = 5V±10%, over full operating temperature range.

Table 5: Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

	Parameter	Min.	Max.	Units		Parameter	Min.	Max	Units
					18	DSN ⇑ to IBF ⇑	-	65	ns
					19	Peripheral Data set up to STBN ⇑	0		ns
1	DSN width	65	-	ns	20	Peripheral Data hold after STBN ⇑	100		ns
2	Peripheral Data set up to DSN	0	-	ns	21	DSN ⇓ to INTR ⇓ (note 4)	-	DS+ 100	ns
3	Peripheral Data hold after DSN	10	-	ns	22	Output valid from DSN ⇑	-	100	ns
4	CSN, A1, A0 setup to DSN ⇓	0	-	ns	23	DSN ⇑ to OBFN ⇓	-	105	ns
5	CSN, A1, A0 hold after DSN ⇑	0	-	ns	24	ACKN ⇑ to OBFN ⇓	-	50	ns
6	Data valid from DSN ⇓	-	60	ns	25	ACKN pulse width	100	-	ns
7	Data float from DSN ⇑ (note 5)	10	100	ns	26	ACKN ⇑ INTR ⇑	-	80	ns
8	Data set up to DSN ⇓	20	-	ns	27	DSN ⇑ to OBFN ⇓	-	105	ns
9	Data hold after DSN ⇑	30	-	ns	28	STBN pulse width	100	-	ns
10	CSN, A1, A0 setup to DSN ⇓	0	-	ns	29	STBN ⇓ to IBF ⇑	-	65	ns
11	CSN, A1, A0 hold after DSN ⇑	20	-	ns	30	Peripheral Data set up to STBN ⇑	0	-	ns
12	Output valid from DSN ⇑	-	100	ns	31	Perlpheral Data hold after STBN ⇑	100	-	ns
14	STBN pulse width	100	-	ns	32	Output valid from ACKN ⇓	-	45	ns
15	STBN ⇓ to IBF ⇑	-	65	ns	33	Output float from ACKN ⇑ (Note 5)	10	100	ns
16	STBN ⇑ to INTR ⇑	-	65	ns	34	ACKN ⇓ to OBFN ⇑	-	50	ns
17	DSN ⇓, to INTR ⇓	-	65	ns	35	DSN ⇑ to IBF ⇓	-	65	ns

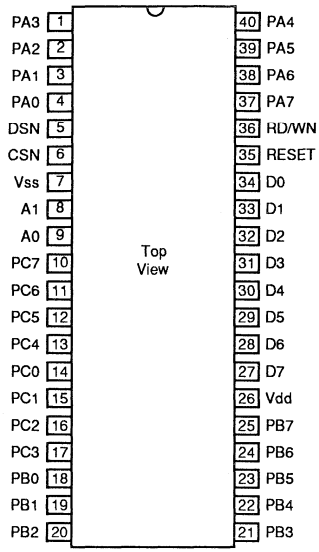
Mil-Std-883, method 5005, subgroup 9, 10, 11.
1. V_{DD} = 5V±10% and C_{CL} = 50pF, over full operating temperature range.
2. Input Pulse V_{SS} to 3.0 Volts.
3. Times Measurement Reference Level 1.5 Volts.
4. DSN = Data Strobe Pulse Width.
5. Measured by a 1.0 Volt change in output voltage. Outputs tied to V_{SS} via 680Ω.

Table 6: AC Electrical Characteristics

PACKAGE OUTLINES & PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	51.31	-	-	2.020
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG405



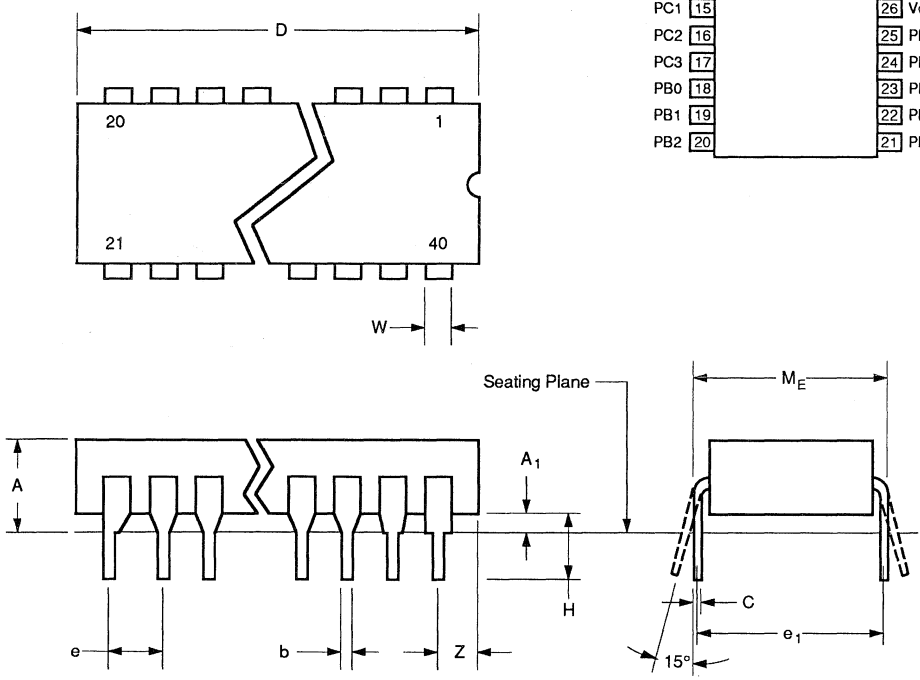


Figure 19: 40-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.41	-	-	0.095
b1	-	0.64	-	-	0.025	-
D	16.33	-	16.81	0.643	-	0.662
E	16.33	-	16.81	0.643	-	0.662
e	-	1.27	-	-	0.050	-
Z	-	1.91 Typ.	-	-	0.075 Typ.	-

XG446

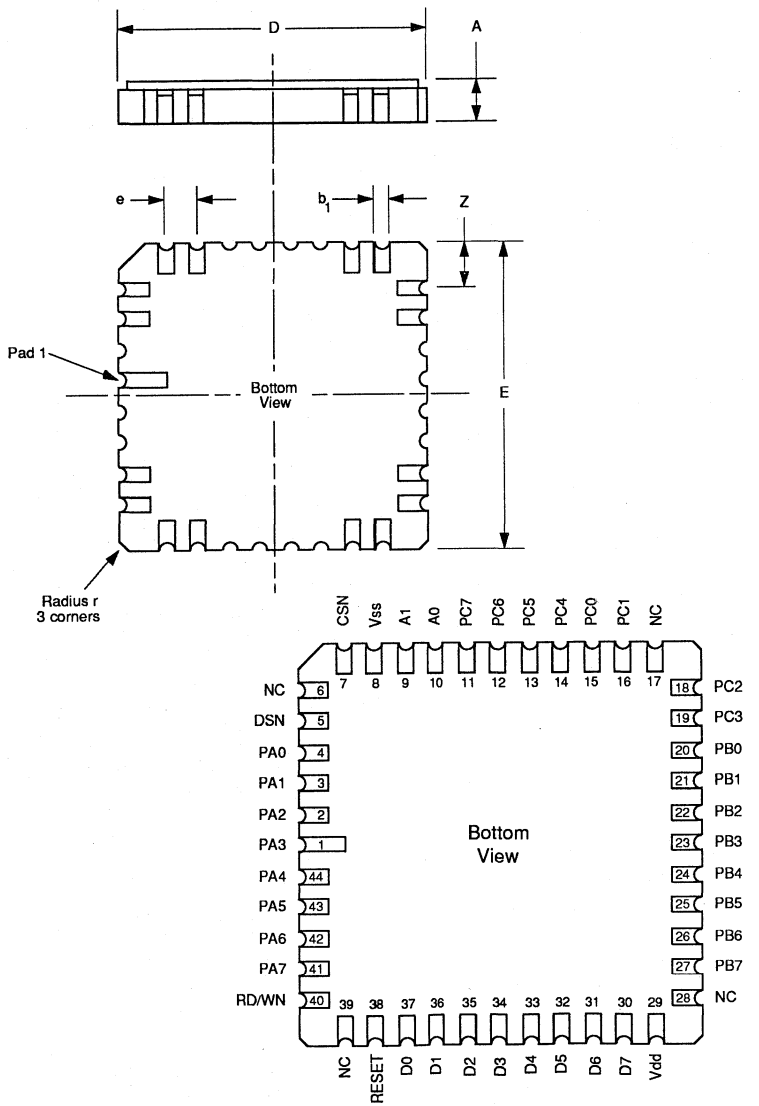


Figure 20: 44-Pad Leadless Chip Carrier (Package Style L)

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

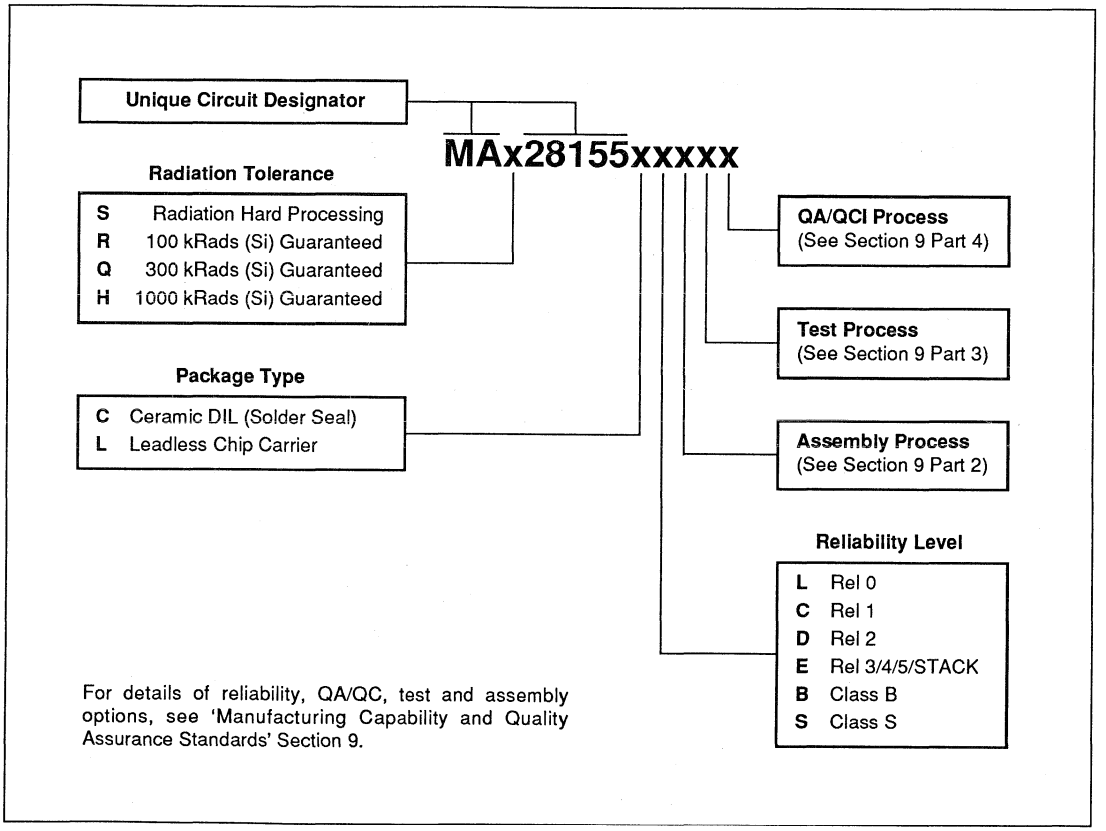
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 21: Radiation Hardness Parameters

ORDERING INFORMATION



DS3810-2.4

MA8251

RADIATION HARD PROGRAMMABLE COMMUNICATION INTERFACE

The MA8251 is based on the industry standard 8251A Universal Synchronous Asynchronous Receiver/Transmitter (USART).

The MA8251 is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission.

Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART signals the CPU whenever it receives a character for transmission or whenever it receives a character for the CPU. The CPU can read the complete status of the USART at any time, including data transmission errors and control signals such as SYNDET and TxEMPTY.

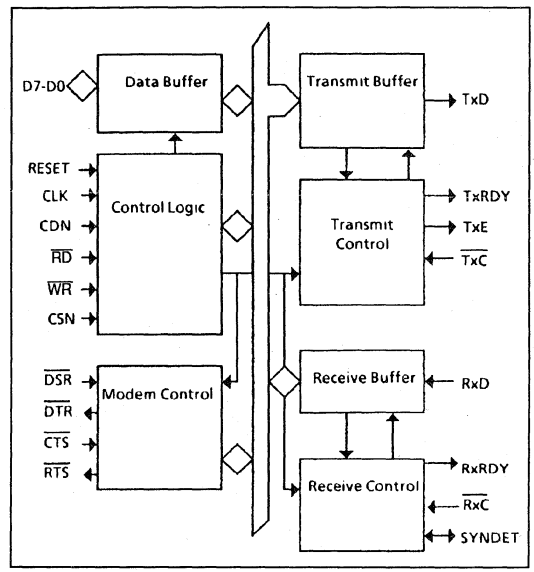


Figure 1: MA8251 Block Diagram

FEATURES

- Radiation Hard to 1MRad(Si)
- Latch Up Free, High SEU Immunity
- Silicon-on-Sapphire Technology
- Synchronous 5 - 8 Bit Characters; Internal or External Character Synchronisation; Automatic Sync Insertion
- Asynchronous 5 - 8 Bit Characters; Clock Rate - 1, 16 or 64 Times Baud Rate; Break Character Generation, 1 ½ or 2 Stop Bits
- All Inputs and Outputs are TTL Compatible
- Compatible with the MA31750 (MIL-STD-1750A & Draft MIL-STD-1750B Option 2) Microprocessor

The MA8251 is based on the industry standard 8251A USART, incorporating the following features:

1. MA8251 has double-buffered data paths with separate I/O registers for control status, data in and data out, which considerably simplifies control programming and minimizes CPU overhead.
2. In synchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
3. A refined Rx initialisation prevents the Receiver from starting when in the "break" state, preventing unwanted interrupts from the disconnected USART.
4. At the conclusion of a transmission, the TxD line will always return to the marking state unless SBRK is programmed.
5. Tx Enable logic enhancement prevents a Tx Disable command from prematurely halting transmission of the previously written data before completion. The logic also prevents the transmitter from turning off in the middle of a word.
6. When external Sync Detect is programmed, Internal Sync Detect is disabled and an External Sync Detect status is provided via a flip-flop, which clears itself upon a status read.
7. The possibility of a false sync detect is minimized in two ways: by ensuring that if double character sync is programmed, the characters will be continuously detected and by clearing the Rx register to all 1's whenever Enter-Hunt command is issued in Sync mode.
8. When the MA8251 is not selected, the RDN and WRN lines do not affect the internal operation of the device.
9. The MA8251 Status can be read at any time but the status update will be inhibited during status read.
10. The MA8251 is free from extraneous glitches, providing higher speed and better operating margins.
11. Synchronous Baud rate is from DC to 64K.
12. Asynchronous Baud rate is from DC to 19.2K.

1. FUNCTIONAL DESCRIPTION

1.1 GENERAL

The MA8251 is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for use with the MA31750 microprocessor. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The MA8251 can support most serial data techniques in use, including IBM bi-sync.

In a communication environment, an interface device must convert parallel format system data into serial format for transmission, and convert incoming serial data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear transparent to the CPU for the simple input or output of byte-oriented system data.

1.2 DATA BUS BUFFER

This 3-state, bidirectional, 8-bit buffer is used to interface the MA8251 to the system data bus. Data is transmitted or received by the buffer upon execution of OUTput or INput instructions from the CPU.

Control word, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-in and Data-out registers are separate 8-bit registers, communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register, which store the various control formats for the device's functional definition.

1.3 RESET

A high on this input forces the MA8251 into idle mode. The MA8251 will remain at idle until its functional definition is programmed with a new set of control words. Minimum RESET pulse width is 6 tcy (clock must be running).

The device can also be put into the idle state by a command reset operation .

1.4 CLOCK (CLK)

The CLK input is used to generate internal device timing and is normally connected to the clock generator (OSC) of the system.

Please note: None of the external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

1.5 READ STROBE (RDN)

A low on this signal line indicates that the CPU is reading data or status information from the MA8251. The MA8251 drives output data onto its data bus whilst this signal remains low.

1.6 WRITE STROBE (WRN)

A low on this signal line indicates that the CPU is writing data or control information to the MA8251. The MA8251 clocks data into its data input buffers on a rising edge of WRN.

1.7 CONTROL/DATA (CDN)

This input, in conjunction with the WRN and RDN inputs, informs the MA8251 that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0= DATA

CDN	RDN	WRN	CSN	ACTION
0	0	1	0	MA8251 to CPU
0	1	0	0	CPU to MA8251
1	0	1	0	Status to CPU
1	1	0	0	CPU to Control
x	1	1	0	Bus Tristate
x	x	x	1	Bus Tristate

Figure 2: Read/Write Control

1.8 CHIP SELECT (CSN)

A low on this input selects the MA8251. No reading or writing will occur unless the device is selected. When CSN is high, the Data Bus is in the float state and the RDN and WRN lines have no effect on the chip.

1.9 MODEM CONTROL

The MA8251 has a set of control inputs and outputs which can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

1.10 DATA SET READY ($\overline{\text{DSR}}$)

The $\overline{\text{DSR}}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{\text{DSR}}$ input is normally used to test modem conditions such as Data Set Ready.

1.11 DATA TERMINAL READY ($\overline{\text{DTR}}$)

The $\overline{\text{DTR}}$ output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{\text{DTR}}$ output signal is normally used for modem control such as Data Terminal Ready.

1.12 REQUEST TO SEND ($\overline{RTS}$)

The $\overline{RTS}$ output signal is a general purpose, 1-bit inverting output port. It can be set low by programming the appropriate bit in the Command instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request To Send.

1.13 CLEAR TO SEND ($\overline{CTS}$)

A low on this input enables the MA8251 to transmit serial data if the Tx Enable bit in the Command byte is set to a high. If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx disable command, before shutting down.

1.14 TRANSMITTER BUFFER

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset, or when Tx Enable or $\overline{CTS}$ = 1, or the transmitter is empty.

1.15 TRANSMITTER CONTROL

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

1.16 TRANSMITTER READY (TxRDY)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the falling edge of WRN when a data character is loaded from the CPU.

Note that when using the polled operation, the TxRDY status bit is not masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data input Register.

1.17 TRANSMITTER EMPTY (TxE)

When the MA8251 has no characters to send, the TxEMPTY output will go high. It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of transmission mode, so that the CPU can turn the line around in the half-duplex operational mode.

In the Synchronous mode, a high on the TxEMPTY output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being automatically transmitted as fillers. TxEMPTY does not go low when the SYNC characters are being shifted out.

1.18 TRANSMITTER CLOCK ($\overline{TxC}$)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1,1/16 or 1/64 the $\overline{TxC}$.

For Example:
If Baud Rate equals 110 Baud
$\overline{TxC}$ equals 110Hz in the 1x mode
$\overline{TxC}$ equals 1.76kHz in the 16x mode
$\overline{TxC}$ equals 7.04kHz in the 64x mode
The falling edge of $\overline{TxC}$ shifts the serial data out of the MA8251.

1.19 RECEIVER BUFFER

The Receiver accepts serial data, converts the data to parallel format, checks for bits or characters that are unique to the communications techniques and sends an assembled character to the CPU. Serial data is input to the RxD pin and is clocked in on the rising edge of RxC.

1.20 RECEIVER CONTROL

This functional block manages all receiver-related activities which consist of the following features:

The RxD initialisation circuit prevents the MA8251 from mistaking an unused input line for an active low data line in the break condition. Before starting to receive serial characters on the RxD line, a valid 1 must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (start bit) is enabled. This feature is only active in the asynchronous mode and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts as the result of a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

1.21 RxRDY (RECEIVER READY)

This output indicates that the MA8251 contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation. RxEnable, when off holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, the overrun error will be set and the old character will be lost.

1.22 $\overline{RxC}$ (RECEIVER CLOCK)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 of the Receiver Clock.

For example:
Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz in the 1 x mode:
$\overline{RxC}$ equals 4.8 kHz in the 16x mode
$\overline{RxC}$ equals 19.2 kHz in the 64x mode.
Baud Rate equals 2400 Baud if
$\overline{RxC}$ equals 2400 Hz in the 1x mode
$\overline{RxC}$ equals 38.4 kHz in the 16x mode;
$\overline{RxC}$ equals 153.6 kHz in the 64x mode.
Data is sampled into the MA8251 on the rising edge of $\overline{RxC}$.

Note: In most communications systems, the MA8251 will be handling both the transmission and reception operations of a single link. Consequently the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

1.23 SYNC/BREAK DETECT (SYNDET/BRKDET)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode, low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go high to indicate that the MA8251 has located the SYNC character in the Receive mode. If the MA8251 is programmed to use double Sync characters (bi-sync), the SYNDET will go high in the middle of the last bit of the second Sync character.

SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the MA8251 to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the high input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

1.24 BREAK (ASYNC MODE ONLY)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences including the start bits, data bits, and parity bits. Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

C/D	ACTION
1	MODE INSTRUCTION
1	SYNC CHARACTER 1 (SYNC ONLY) *
1	SYNC CHARACTER 2 (SYNC ONLY) *
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION
0	DATA
1	COMMAND INSTRUCTION

Note: The second sync character is skipped if mode instruction has programmed the MA8251 to single character mode. Both sync characters are skipped if mode instruction has programmed the MA8251 to async mode

Figure 3: Typical data block

2. OPERATION DESCRIPTION

2.1 GENERAL

The complete functional definition of the MA8251 is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the MA8251 to support the desired communications format. These control words will program the: Baud Rate, Character Length, Number of Stop Bits, Synchronous or Asynchronous Operation, Even/Odd/Off Parity, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the MA8251 is ready to perform its communication functions. The TxRDY output is raised high to signal the CPU that the MA8251 is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the MA8251. Alternatively, the MA8251 receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised high to signal to the CPU that the MA8251 has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The MA8251 cannot begin transmission until the TxEnable (Transmitter Enable) bit is set in the Command instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

3. PROGRAMMING THE MA8251

3.1 MODE AND COMMAND INSTRUCTIONS

Prior to starting data transmission or reception, the MA8251 must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the MA8251 and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:
1. Mode Instruction
2. Command Instruction

3.1.1 Mode Instruction

This instruction defines the general operational characteristics of the MA8251. It must follow a Reset operation (internal or external). Once the Mode instruction has been written into the MA8251 by the CPU, SYNC characters or Command Instructions may be written.

3.1.2 Command Instruction

This instruction defines a word that is used to control the actual operation of the MA8251.

Both the Mode and Command Instruction must conform to a specified sequence for proper device operation. The Mode instruction must be written immediately following a Reset operation, prior to using the MA8251 for data communications.

All control words written into the MA8251 after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the MA8251 at any time in the data block during the operation of the MA8251. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation. This automatically places the MA8251 back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

3.2 MODE INSTRUCTION DEFINITION

The MA8251 can be used for either Asynchronous or Synchronous data communications. To understand how the Mode Instruction defines the functional operation of the MA8251, the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant data bus bits will hold the data; unused bits are 'don't care' when writing data to the MA8251, and will be zeros when reading the data from the MA8251.

3.3 TEST MODE

The Mode Instruction can be used to select a scan path test facility. In this mode a test vector is read in through RxD and read out in TxD. For more information on test mode please contact GEC Plessey Semiconductors.

3.4 ASYNCHRONOUS MODE (TRANSMISSION)

Whenever a data character is sent by the CPU the MA8251 automatically adds a Start bit (low level), followed by the data bits (least significant bit first,) and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The Character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16 or 1/64 times that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the MA8251 the TxD output remains high (marking) unless a Break (continuously low) has been programmed.

3.5 ASYNCHRONOUS MODE (RECEIVE)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16x or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If a parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the receiver requires only one stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the MA8251. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched.

If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the MA8251.

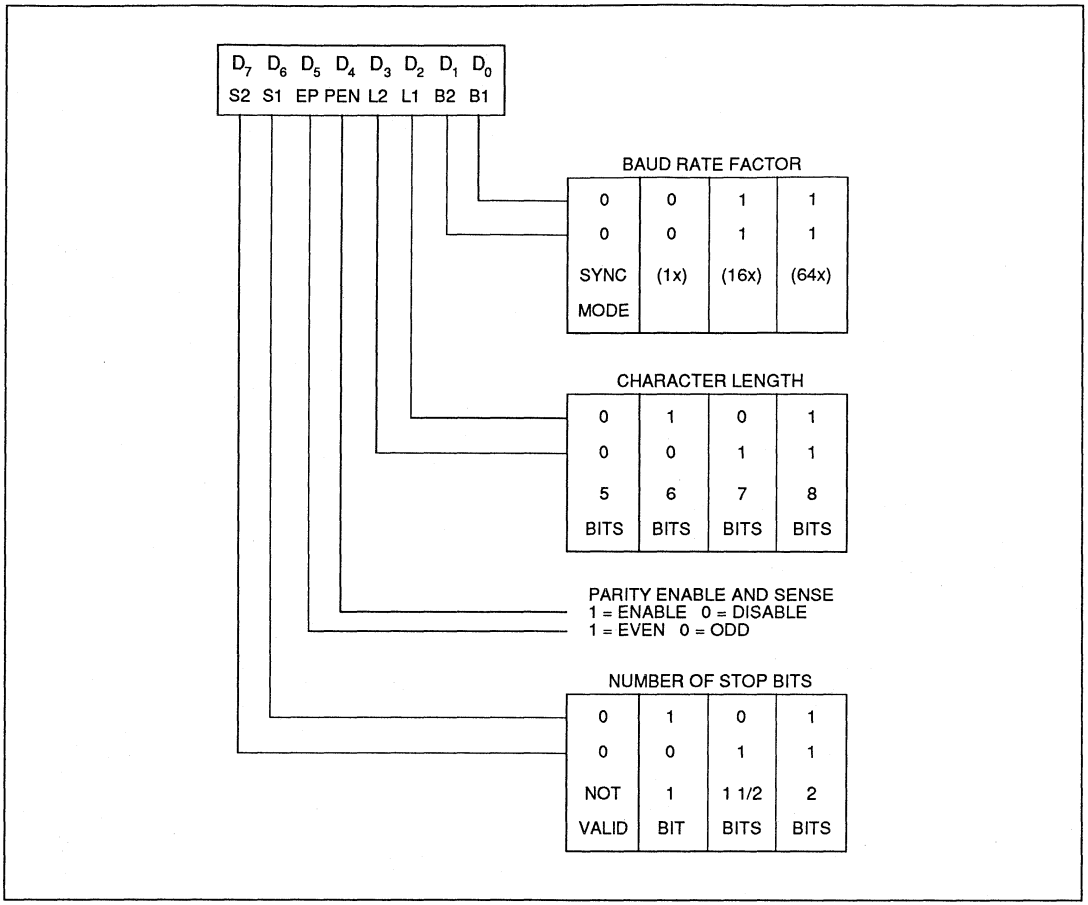


Figure 4: Mode Instruction Format, Asynchronous Mode

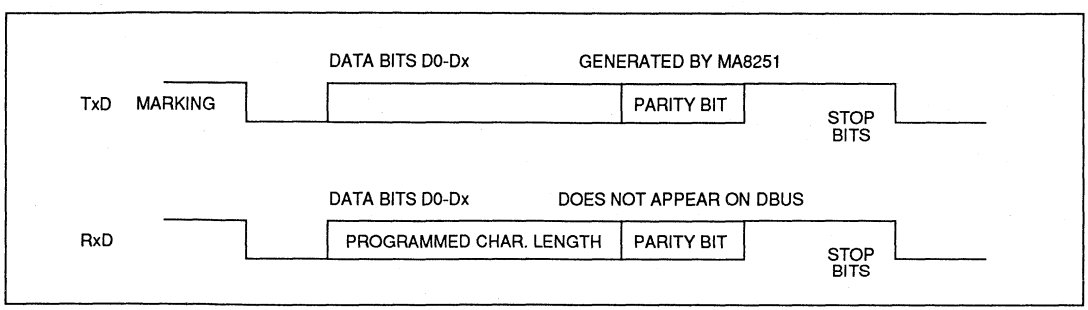


Figure 5: Asynchronous Mode

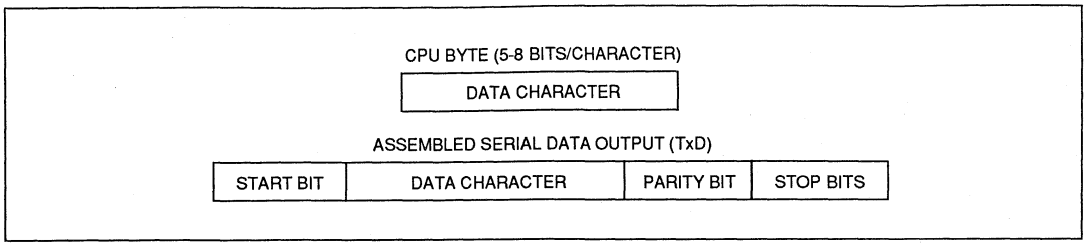


Figure 6: Transmission Format

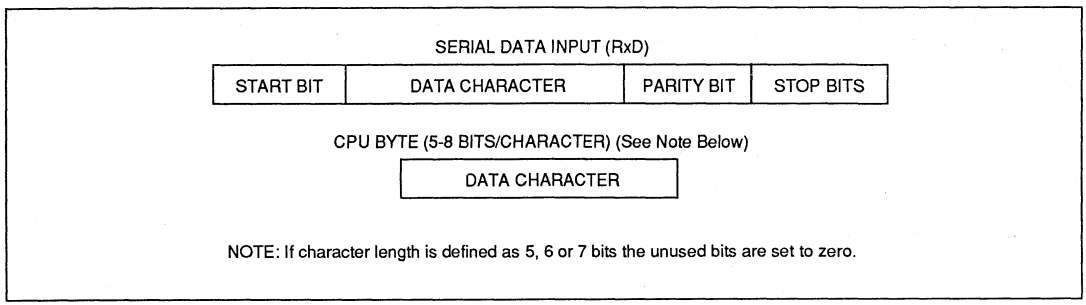


Figure 7: Receive Format

3.6 SYNCHRONOUS MODE (TRANSMISSION)

The TxD output is continuously high until the CPU sends its first character to the MA8251 which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the MA8251 with a data character before the MA8251 Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY does not go low when the SYNC is being shifted out (see figure 8). The TxEMPTY pin is internally reset by a data character being written into the MA8251.

3.7 SYNCHRONOUS MODE (RECEIVER)

In this mode character synchronisation can be internally or externally achieved. If the SYNC mode has been programmed, ENTER-HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared to every bit boundary with the first SYNC character until a match occurs.

If the MA8251 has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit, instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the MA8251 out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

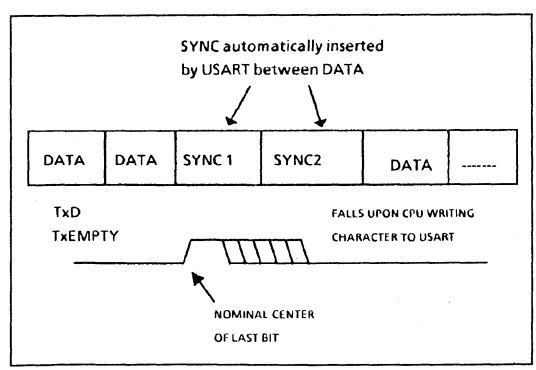


Figure 8: Sync Character Insertion

Parity error and overrun error are both checked in the same way as in the Asynchronous Receive mode. Parity is checked when not in HUNT, regardless of whether the Receiver is enabled or not.

The CPU can command the receiver to enter the HUNT mode if synchronisation is lost. This will also set all the used character bits in the buffer to a one thus preventing a possible false SYNDET caused by data that happens to be in the Rx buffer at ENTER HUNT time.

Note: the SYNDET flip-flop is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the MA8251 to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the known word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been contiguously received to gate a SYNDET indication). When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET flip-flop may be set at any bit boundary.

3.9 DATA FORMAT, SYNCHRONOUS MODE

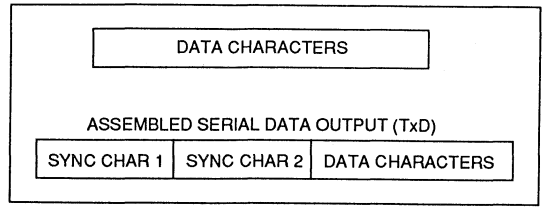


Figure 9: Receive Format, Synchronous Mode

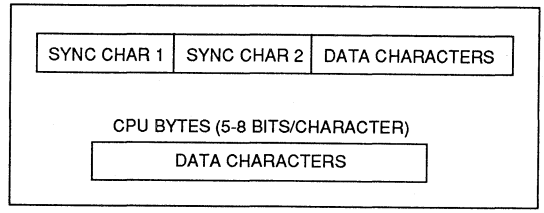


Figure 10: Data Format, Synchronous Mode

3.8 MODE INSTRUCTION FORMAT, SYNCHRONOUS MODE

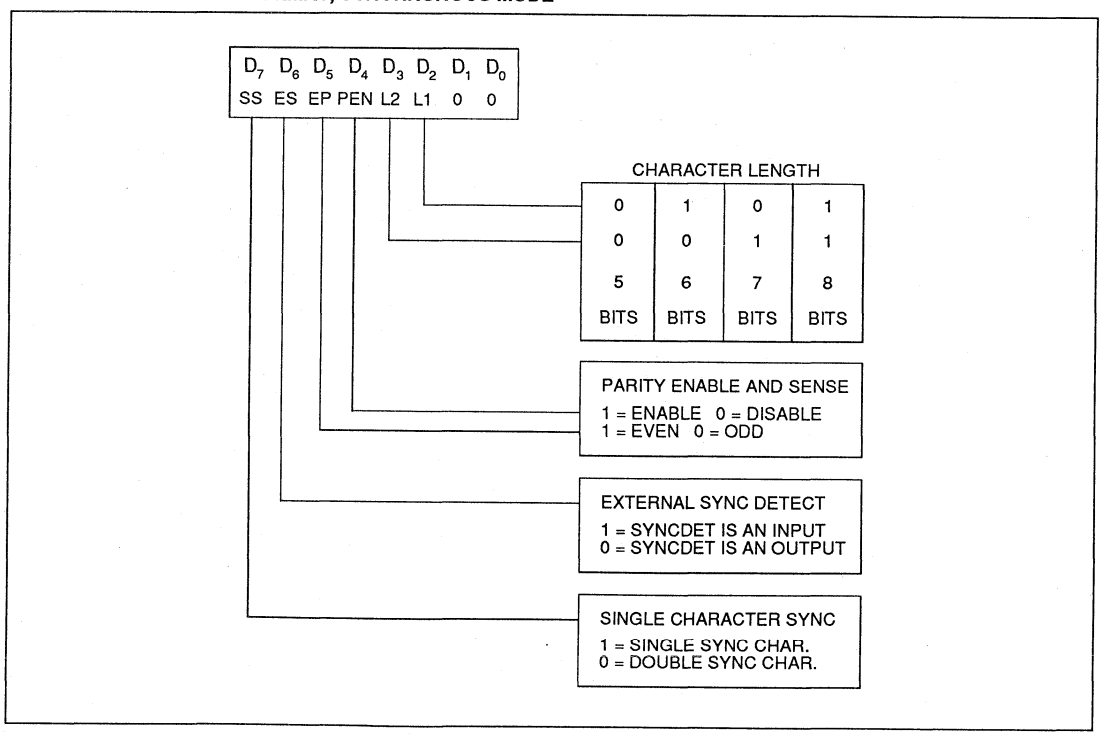


Figure 11: Mode Instruction Format, Synchronous Mode

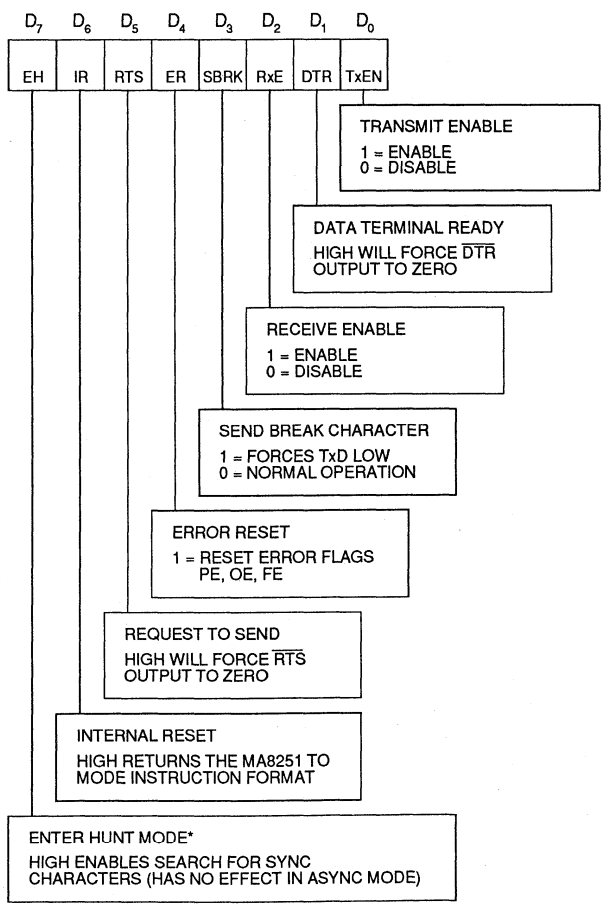
3.10 COMMAND INSTRUCTION DEFINITION

Once the functional definition of the MA8251 has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communications. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the MA8251 and Sync characters inserted, if necessary, then all further "control writes" (CDN=1) will load a Command Instruction. A Reset Operation (internal or external) will return the MA8251 to the Mode instruction format.

Note: Internal Reset on Power-up. When power is first applied, the MA8251 may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00_Hs consecutively into the device with CDN=1 configures sync operation and writes two dummy 00_H sync characters. An internal reset command (40_H) may then be issued to return the device to the idle state.

3.11 COMMAND INSTRUCTION FORMAT



*NOTE: ERROR RESET must be performed whenever RxENABLE and ENTER-HUNT are programmed.

Figure 12: Command Instruction Format

3.12 STATUS READ DEFINITION

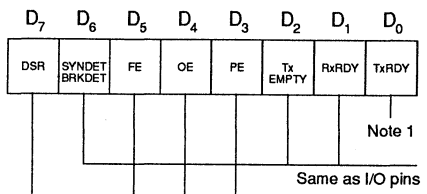
In data communication systems it is often necessary to examine the status of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The MA8251 has facilities that allow the programmer to read the status of the device at any time during the functional operation. (Status update is inhibited during status read).

A normal read command is issued by the CPU with CDN high to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the MA8251 can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

3.13 STATUS READ FORMAT



PARITY ERROR

The PE flag is set when the parity error is detected. It is reset by the ER bit of the Command Instruction. PE does not inhibit the operation of the MA8251.

OVERRUN ERROR

The OE flag is set when the CPU does not read a character before the next one becomes available. It is reset by the ER bit of the Command Instruction OE does not inhibit operation of the MA8251, however the previously overrun character is lost.

FRAMING ERROR (ASYNC ONLY)

The FE flag is set when a valid Stop bit is not detected at the end of every character. It is reset by the ER bit of the Command Instruction. FE does not inhibit the operation of the MA8251.

DATA SET READY

Indicates that the DSR is at a zero level.

Note 1: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN, the latter is conditioned by both CTS and $\overline{TxEN}$.
ie. TxRDY status bit 0 DB buffer empty
TxRDY pin out = DB buffer empty OR ($\overline{CTSN}$ = 0) OR (TxEN = 1)

Figure 13: Status Read Format

4. TIMING WAVEFORMS

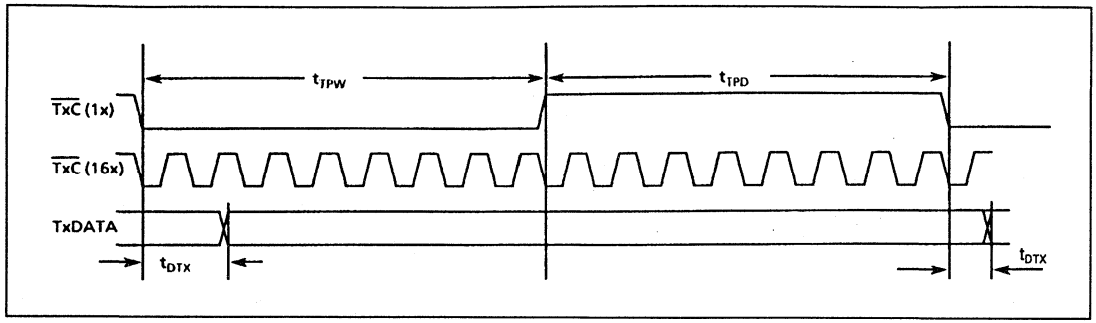


Figure 14: Transmitter Clock and Data

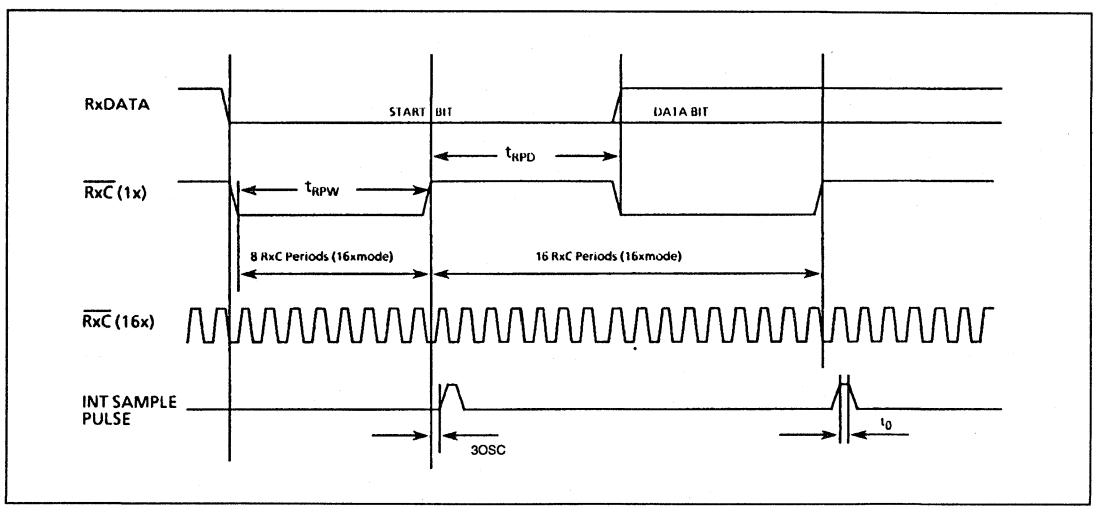


Figure 15: Receive Clock and Data

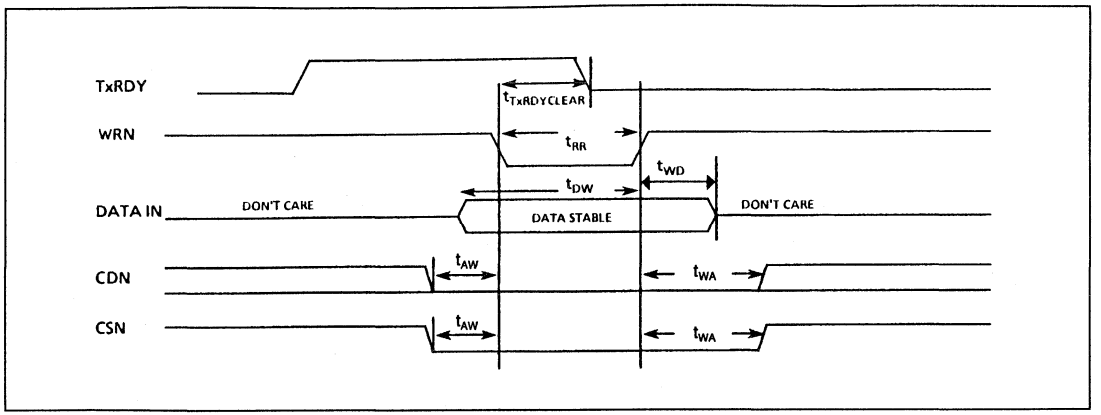


Figure 16: Write Data Cycle (CPU to USART)

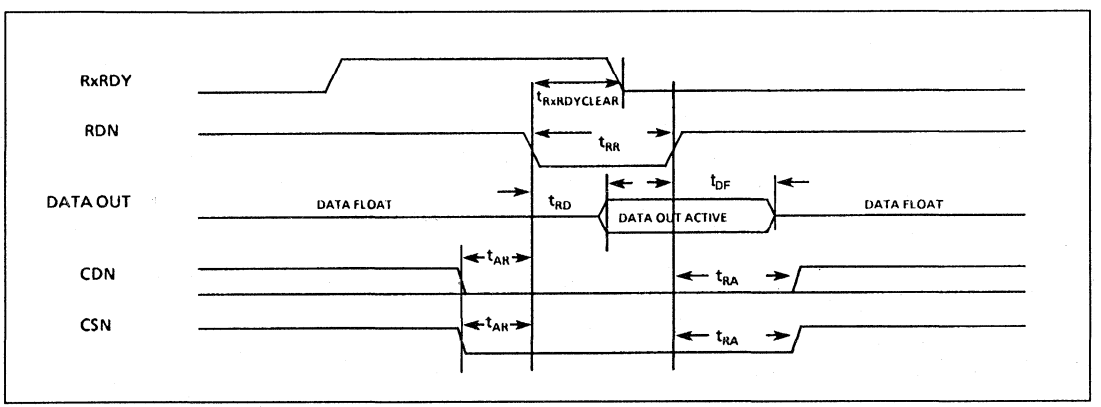
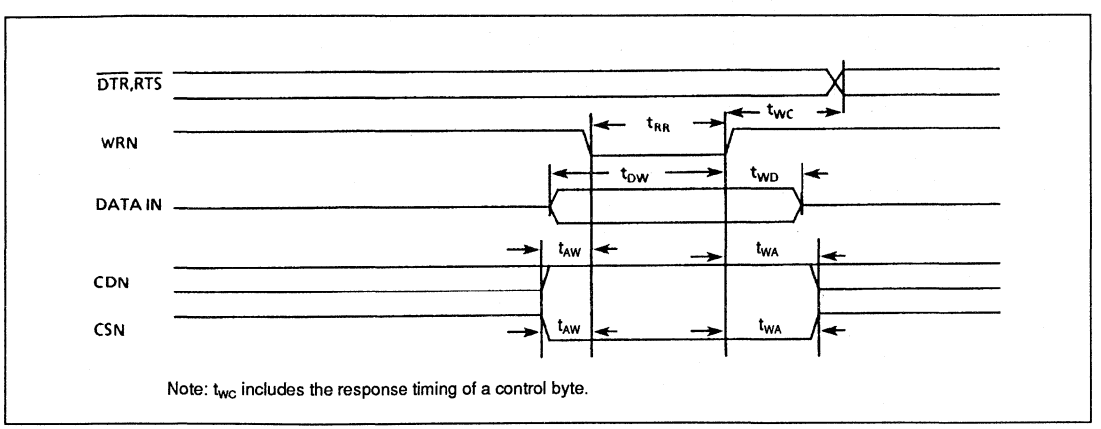
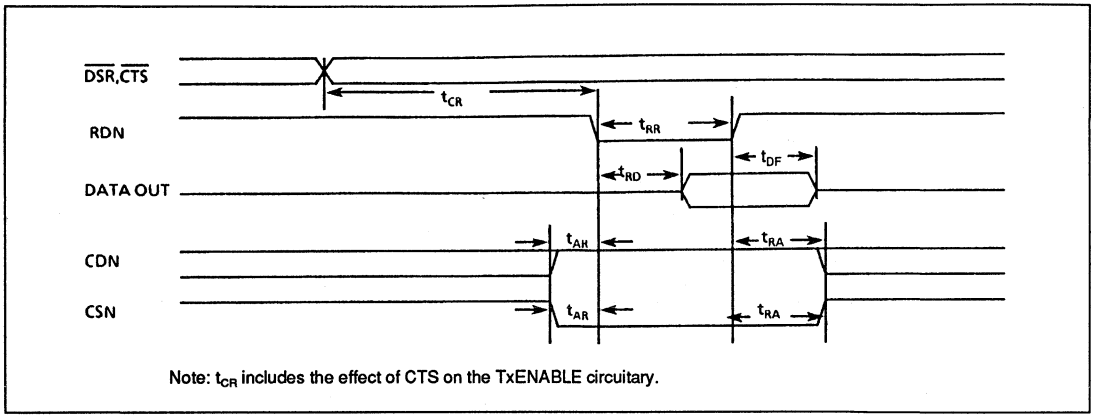


Figure 17: Read Data Cycle (USART to CPU)



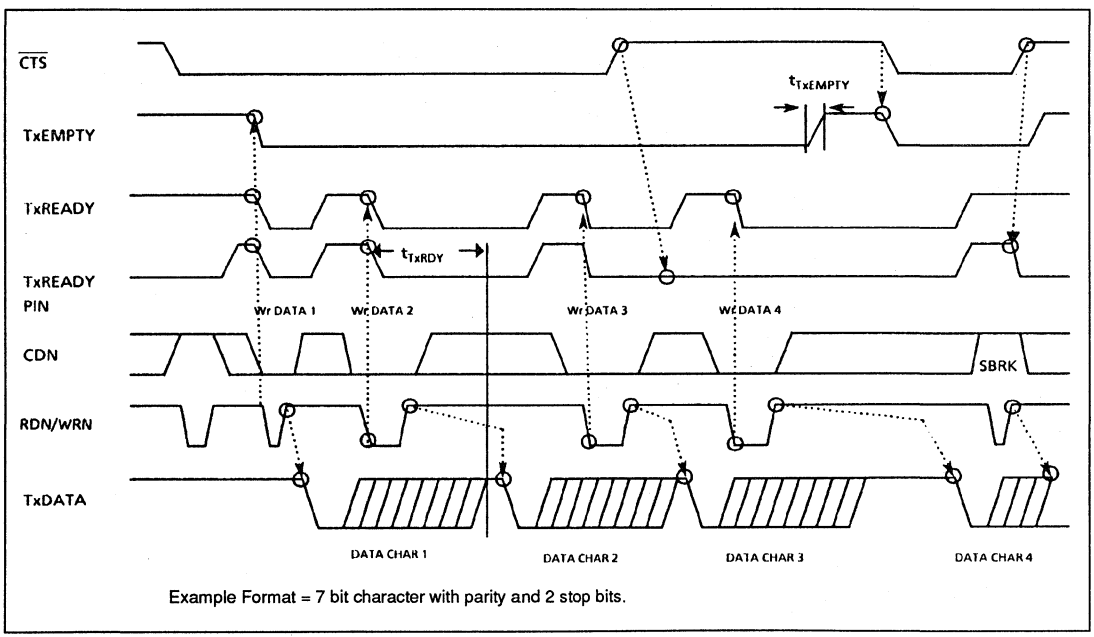
Note: t_{WC} includes the response timing of a control byte.

Figure 18: Write Control or Output Port Cycle (CPU to USART)



Note: t_{CR} includes the effect of CTS on the TxENABLE circuitary.

Figure 19: Read Control or Output Port Cycle (USART to CPU)



Example Format = 7 bit character with parity and 2 stop bits.

Figure 20: Transmitter Control and Flag Timing (ASYNC Mode)

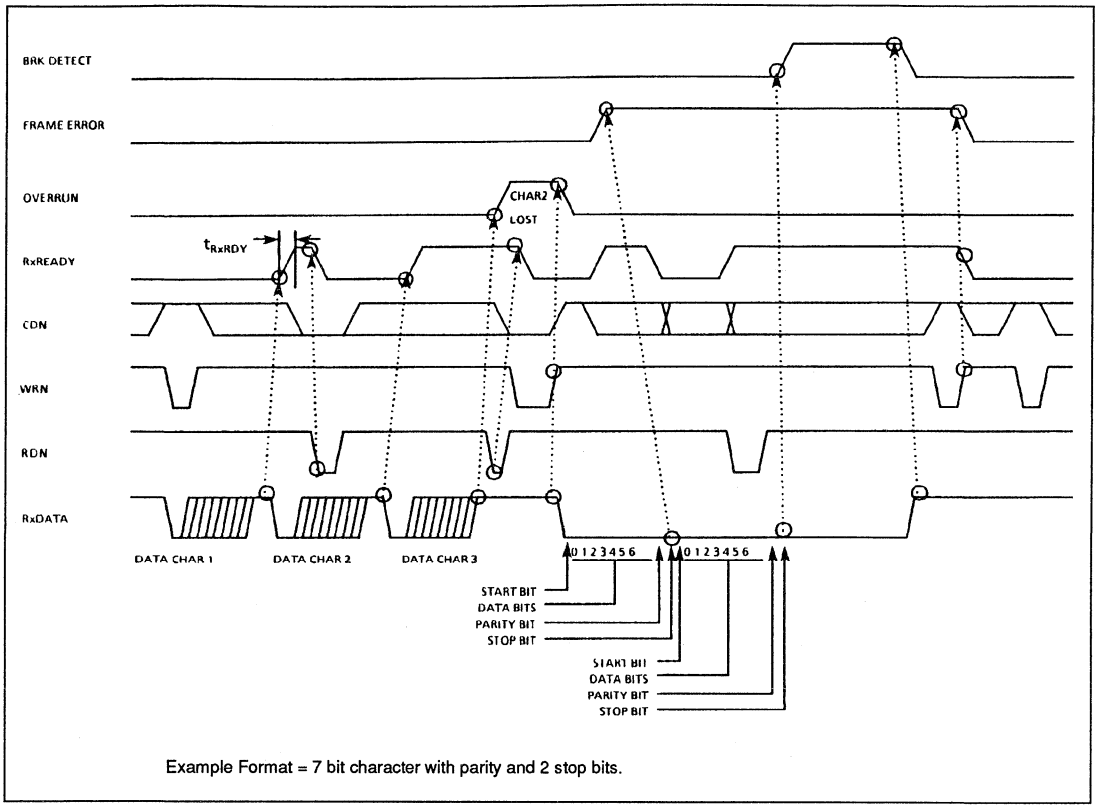


Figure 21: Receiver Control and Flag Timing (ASYNC Mode)

5. AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units	Condition
t_0	Clock high pulse width	100	-	nS	-
$t_{\overline{0}}$	Clock low pulse width	100	-	nS	-
t_R, t_F	Clock rise and fall time	-	20	nS	-
t_{DTX}	TxD delay from falling edge of TxC	-	1	µS	-
t_{TPW}	Transmitter input clock pulse width	12xosc	-	-	1 x baud rate
		1xosc	-	-	16 x and 64 x baud rate
t_{TPD}	Transmitter input clock pulse delay	15xosc	-	-	1 x baud rate
		3xosc	-	-	16 x and 64 x baud rate
t_{RPW}	Receive input clock pulse width	12xosc	-	-	1 x baud rate
		1xosc	-	-	16 x and 64 x baud rate
t_{RPD}	Receive input clock pulse delay	15xosc	-	-	1 x baud rate
		3xosc	-	-	16 x and 64 x baud rate
t_{TxRDY}	TxRDY pin delay from CENTER of last bit	-	8xosc	-	Note 6
$t_{TxRDY\ CLEAR}$	TxRDY fall from falling WRN	-	50	ns	Note 6
t_{RxRDY}	RxRDY pin delay from center of last bit	-	26xosc	-	Note 6
$t_{RxRDY\ CLEAR}$	RxRDY fall from falling RDN	-	50	ns	Note 6
$t_{TxEMPTY}$	TxEMPTY from centre of last bit	20xosc	-	-	Note 6
t_{WC}	Control delay from rising edge of WRN	8xosc	-	-	Note 6
t_{CR}	Control to RDN set-up time ($\overline{DSR}$, $\overline{CTS}$)	20xosc	-	-	Note 6
t_{AR}	Address stable before RDN (CSN, CDN)	0	-	ns	Note 1
t_{RA}	Address hold time from RDN (CSN, CDN)	0	-	ns	Note 1
t_{AW}	Address stable before WRN	0	-	ns	-
t_{WA}	Address hold time from WRN	0	-	ns	-
t_{RR}	RDN/WRN pulse width	20	-	ns	-
t_{RD}	Data delay fromRDN falling	-	30	ns	Note 2
t_{DF}	RDN rising to data floating	10	45	ns	Note 7
t_{DW}	Data set-up time to WRN rising	15	-	ns	-
t_{WD}	Data hold time from WRN rising	5	-	ns	-
t_{RV}	Recovery time between writes (not shown)	6xosc	-	-	Note 3

Notes: 1. CSN and Command/Data are considered as addresses.
2. Assumes that address is valid before RDN goes low.
3. This recovery time is for Mode Initialisation only. Write data is allowed when TxRDY = 1. Recovery time between writes for Asynchronous Mode is 8xosc and for Synchronous Mode is 16xosc.
4. The $\overline{TxC}$ and $\overline{RxC}$ frequencies have the following limitation with respect to clock: For 1 x baudrate, f_{TX} or $f_{RX} \leq 1/(30osc)$: For 16 x and 64 x baud rate, f_{TX} or $f_{RX} \leq 1/(4.5osc)$.
5. Reset Pulse Width = 6osc minimum; System clock must be running during Reset.
6. Status update can have a maximum delay of 28 clock periods from the event affecting the status.
7. Data Bus connected to V_{DD} via loads of 680Ω (minimum).

Mil-Std-883, method 5005, subgroups 9, 10, 11

Figure 22: AC Electrical Characteristics

Parameter	Min.	Max.	Units	Conditions
Clock Frequency (osc)	-	5	MHz	-
Transmitter input clock frequency	DC	64	kHz	1 x baud rate
	DC	310	kHz	16 x baud rate
	DC	615	kHz	64 x baud rate
Receiver input clock frequency	DC	64	kHz	1x baud rate
	DC	310	kHz	16 x baud rate
	DC	615	kHz	64 x baud rate

Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Figure 23: Operating AC Electrical Characteristics

6. DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 24: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding 3x10^5 Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	2.2	-	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	V_{DD}-0.5	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 5mA	-	-	V_{SS}+0.4	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Tristate Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	µA
I_{DD}	Power Supply Current	Static, V_{DD} = 5.5V	-	0.1	10	mA

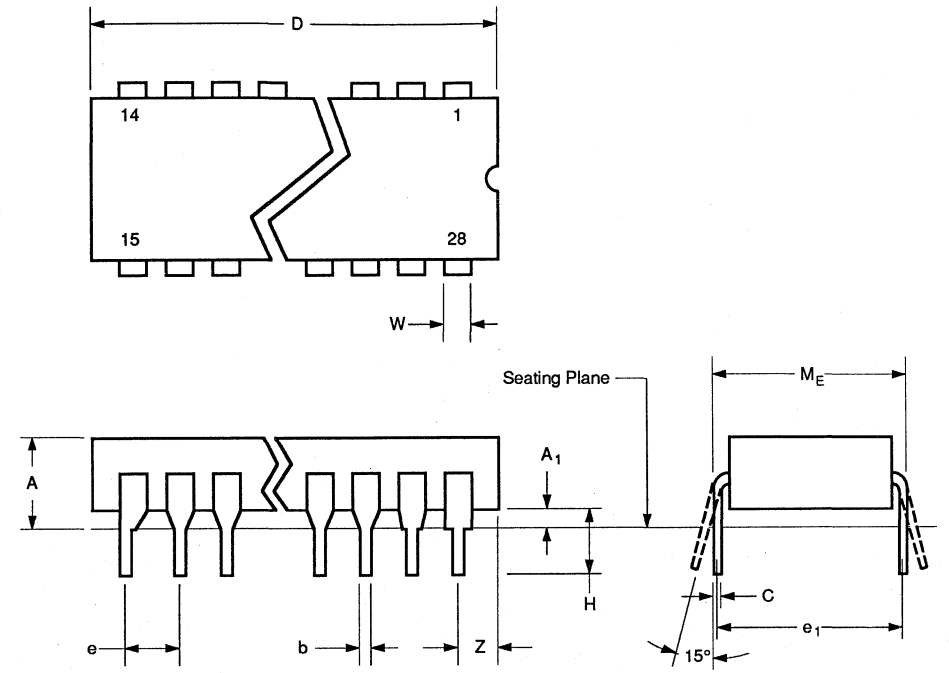
V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Note 1: Guaranteed but not tested at -55°C.

Figure 25: Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 25 at +25°C
2	Static characteristics specified in Figure 25 at +125°C
3	Static characteristics specified in Figure 25 at -55°C
7	Functional characteristics specified in Figure 23 at +25°C
8A	Functional characteristics specified in Figure 23 at +125°C
8B	Functional characteristics specified in Figure 23 at -55°C
9	Switching characteristics specified in Figure 22 at +25°C
10	Switching characteristics specified in Figure 22 at +125°C
11	Switching characteristics specified in Figure 22 at -55°C

Figure 26: Definition of Mil-Std-883, Method 5005 Subgroups

7. OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

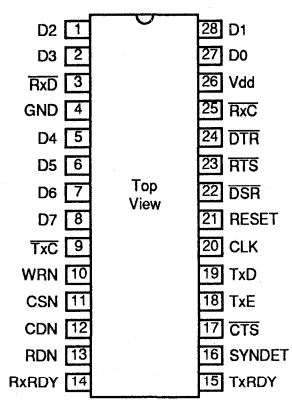
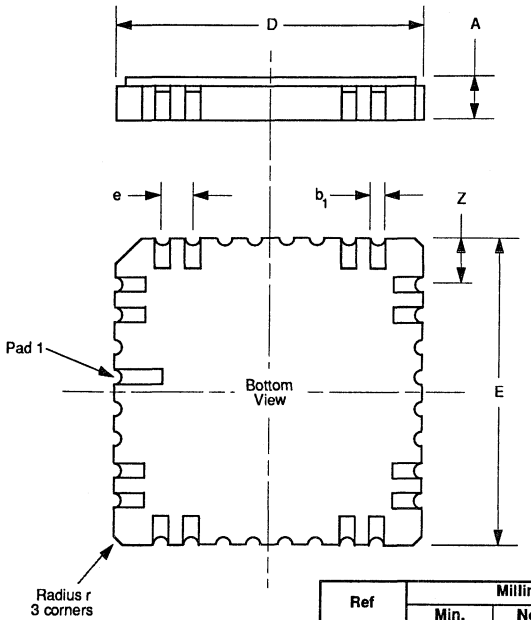


Figure 27: 28-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.29	-	-	0.090
b1	-	0.51	-	-	0.020	-
D	-	-	14.60	-	-	0.575
E	-	-	14.60	-	-	0.575
e	-	1.02	-	-	0.040	-
Z	-	1.52 Typ.	-	-	0.060 Typ.	-

XG431

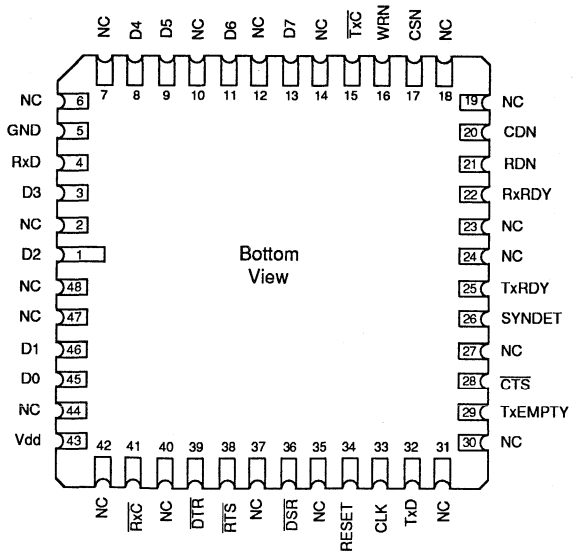
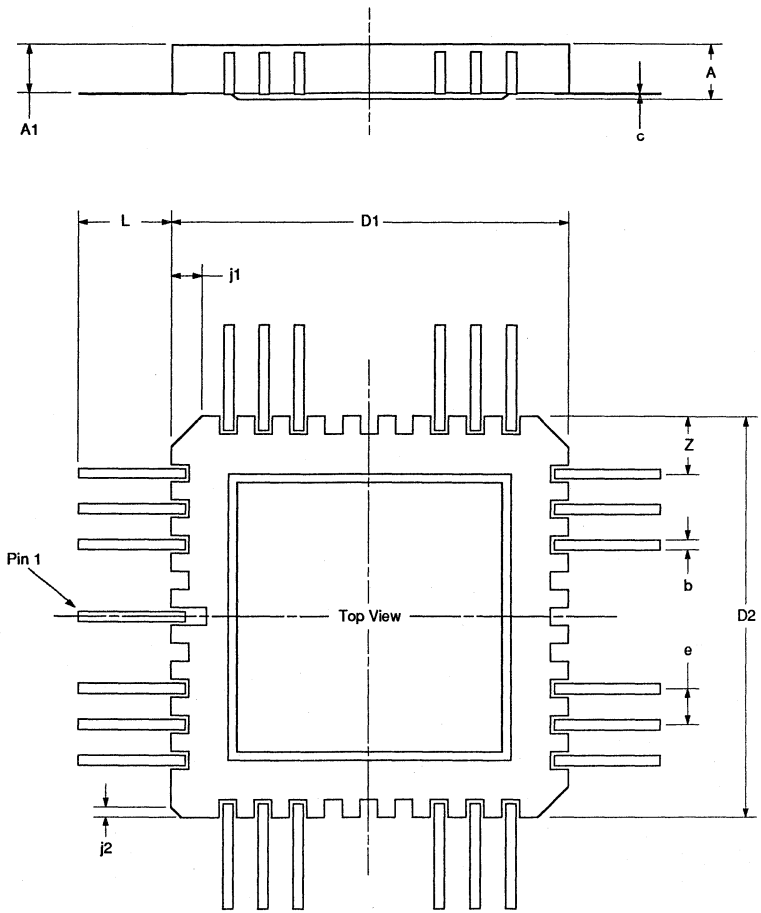


Figure 28: 48-Pad Leadless Chip Carrier - Package Style L



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.72	-	-	0.107
A1	1.83	-	2.24	0.072	-	0.088
b	0.41	-	0.51	0.016	-	0.020
c	0.20	-	0.30	0.008	-	0.012
D1, D2	23.88	-	24.51	0.940	-	0.960
e	-	2.54	-	-	0.050	-
j1	-	1.02	-	-	0.040	-
j2	-	0.51	-	-	0.020	-
L	10.16	-	10.54	0.400	-	0.415
Z	1.65	-	2.16	0.065	-	0.085

XG540

Figure 29a: 68-Lead Topbraze Flatpack - Package Style F

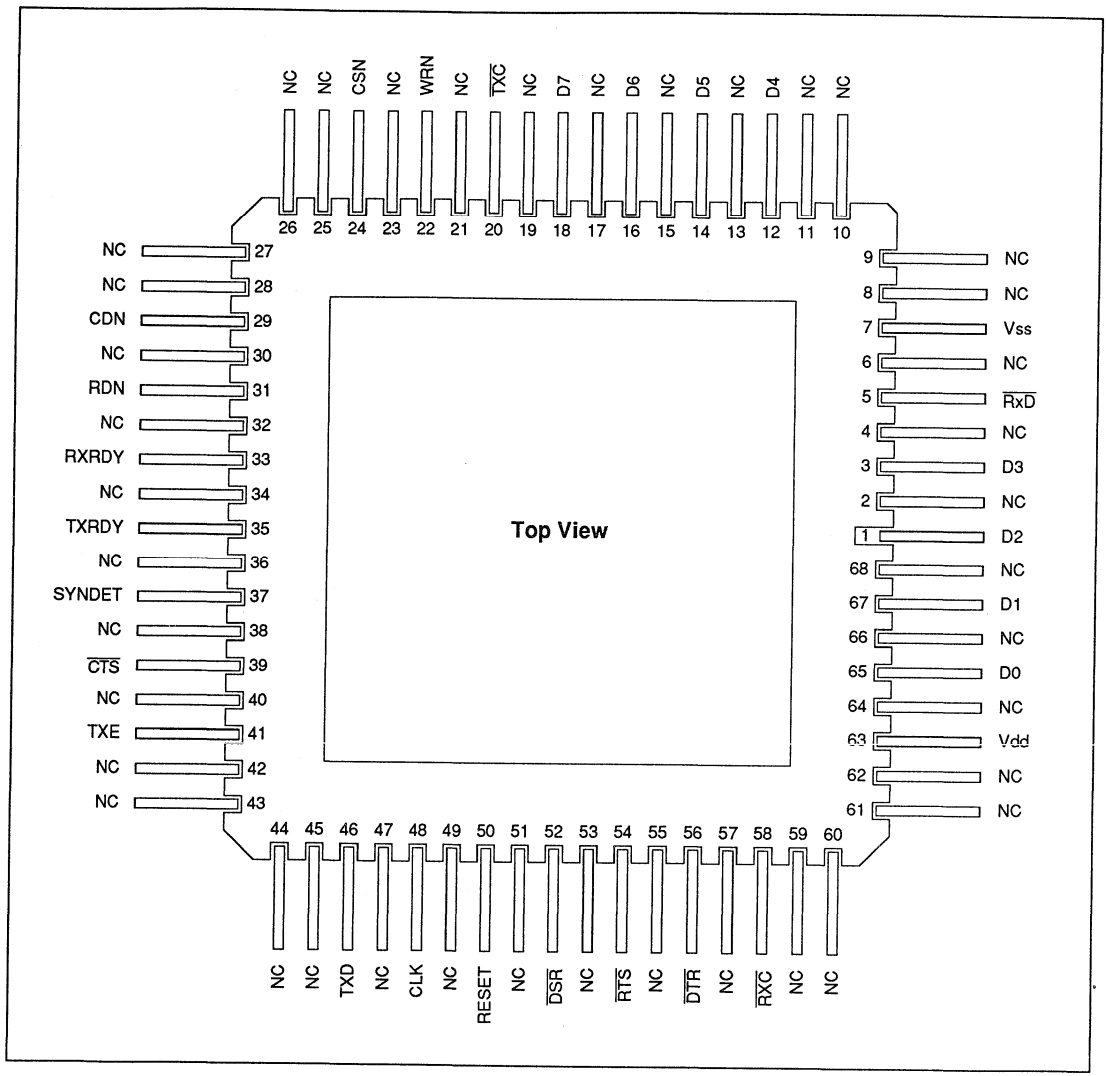


Figure 29b: 68-Lead Topbraze Flatpack - Package Style F

8. RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

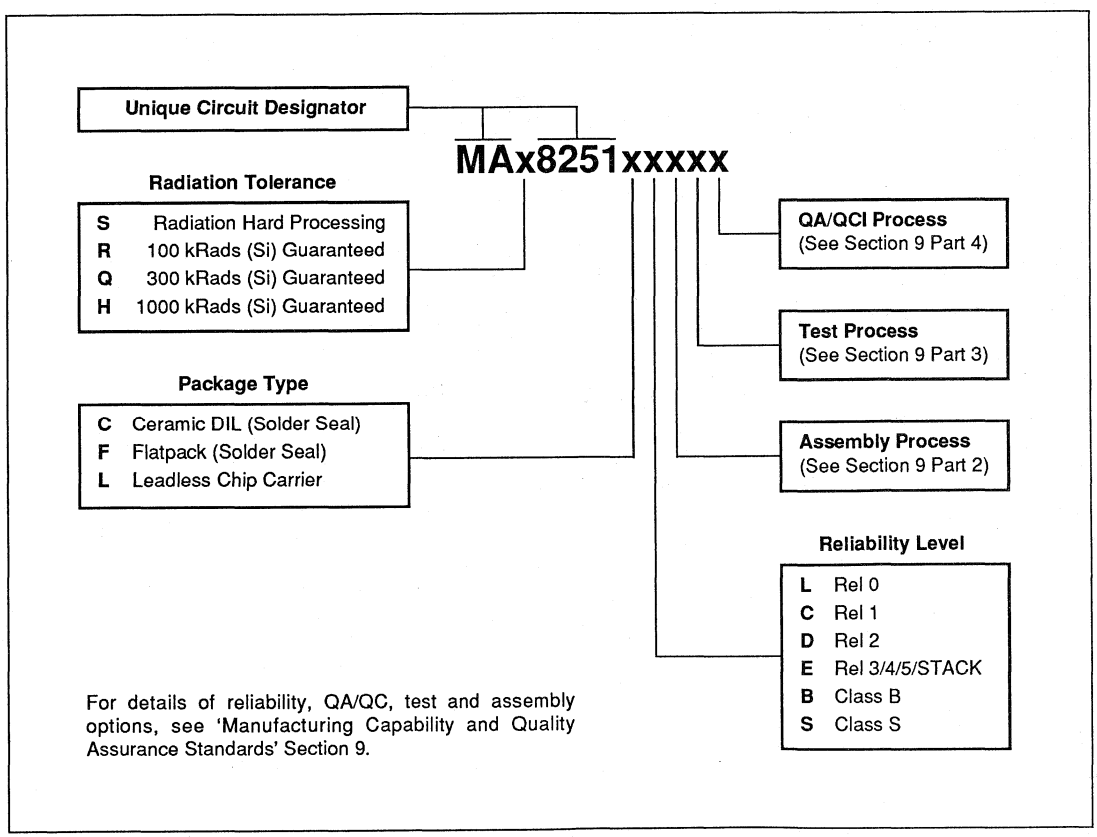
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 30: Radiation Hardness Parameters

9. ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3815-1.4

MA8255

RADIATION HARD PROGRAMMABLE PERIPHERAL INTERFACE

The MA8255 is a general purpose programmable Input/Output device designed for use with the MA31750 microprocessor. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be inputs or outputs. In the second mode (MODE 1), each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for hand-shaking and interrupt control signals. The third mode of operation (MODE 2) is the bidirectional bus mode, which uses 8 lines for a bidirectional bus and 5 lines, borrowing one from the other group, for hand-shaking.

FEATURES

- Radiation Hard to 1MRad (Si)
- High SEU Immunity, Latch Up Free
- Silicon-on-Sapphire Technology
- 24 Programmable I/O Pins
- All Inputs and Outputs are TTL Compatible
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Replaces Several MSI Packages
- Compatible with MA31750 (Mil-Std-1750A) Microprocessor

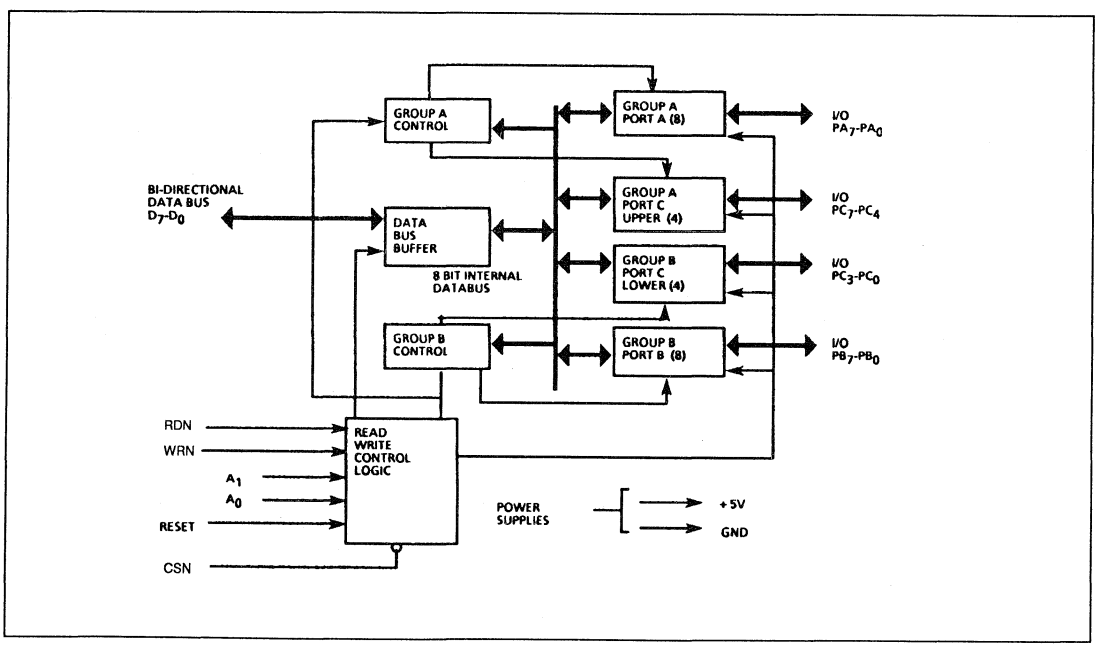


Figure 1: Block Diagram

FUNCTIONAL DESCRIPTION

The MA8255 is a programmable peripheral interface (PPI) device designed for use with MA31750. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the MA8255 is programmed by the system software so that, normally, no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the MA8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Reset (RESET)

A high on this input clears the control register and all ports (A,B,C) are set to the input mode.

Chip Select (CSN)

A low on this input pin enables the communication between the MA8255 and the CPU.

Read Select (RDN)

A low pulse on RDN indicates a CPU read from the MA8255.

Write Select (WRN)

A low pulse on WRN indicates a write from the CPU to the MA8255.

Port Select O and Port Select 1 (AO and A1)

These input signals, in conjunction with the RDN and WRN inputs, control the selection of one of the three ports of the control word registers. They are normally connected to the least significant bits of the address bus.

Basic Operation

A1	A0	RDN	WRN	CSN	READ
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					WRITE
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE
x	x	x	x	1	DATA BUS → TRI-STATE
1	1	0	1	0	ILLEGAL CONDITION
x	x	1	1	0	DATA BUS → TRI-STATE

Table 1: Basic Operation

OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation, which can be selected by the system software:

Mode 0. Basic Input/Output
Mode 1. Strobed Input/Output
Mode 2 Bi-directional Bus

When the reset input goes high all ports will be set to the input mode (i.e. all 24 lines will be in the high impedance state) After the reset is removed the MA8255 can remain in the input mode with no additional initialisation required.

During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single MA8255 to service a variety of peripheral devices with a single software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status register, will be reset whenever the mode is changed.

Modes may be combined so that their functional definition can be tailored to almost any I/O structure. For instance; Group B can be programmed in Mode 0 whilst simultaneously Group A could be programmed in Mode 1.

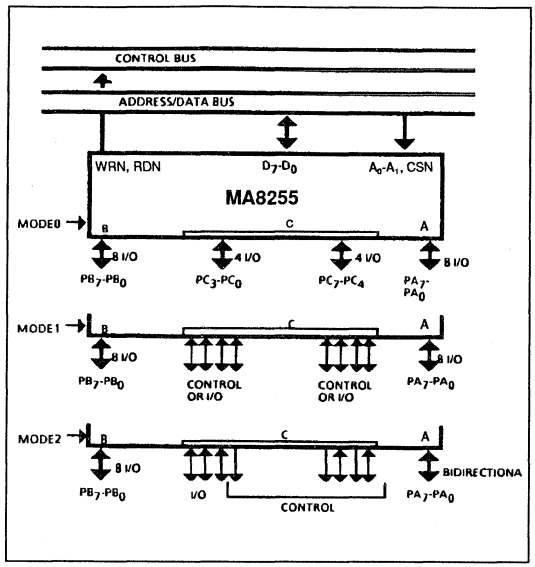


Figure 2: Basic Mode Definitions and Bus Interface

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single output instruction. This feature reduces software requirements in control-based applications.

When Port C is being used as Status/Control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the MA8255 is programmed to operate in Mode 1 or 2, control signals are provided that can be used as interrupt request inputs to the CPU (figure 4). The interrupt request signals, generated from Port C, can be inhibited or enabled by setting or resetting the associated INTE register bit, using the Bit Set/Reset function of Port C.

This function allows the programmer to disallow or allow a specific I/O device to interrupt the CPU, without affecting any other device in the interrupt structure.

INTE register bit definitions:
(BIT-SET): INTE is SET -Interrupt enable
(BIT-RESET): INTE is RESET -Interrupt disable

Note: All mask register bits are automatically reset during mode selection and device reset.

Mode Definition Format (D_7= 1)

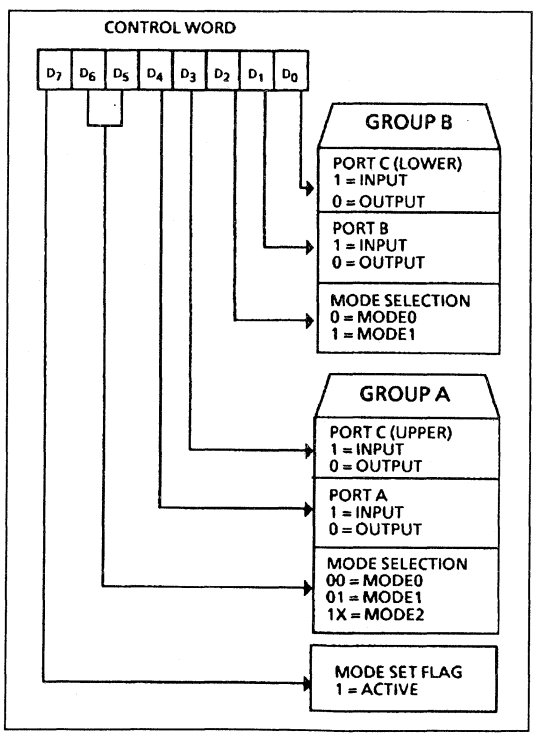


Figure 3: Mode Definition Format (D_7 = 1)

Bit Set/Reset Format (D_7 = 0)

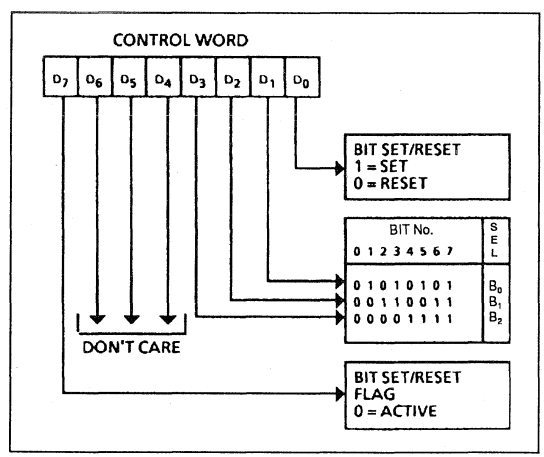


Figure 4: Bit Set/Reset Format (D_7 = 0)

Group A and Group B Controls

The functional configuration of each port is programmed by the system software. In essence, the CPU outputs a control word to the MA8255. The control word contains information such as mode, bit set, bit reset, etc., this initializes the functional configuration of the MA8255.

Each of the Control blocks (Group A and Group B) accept commands from the Read/Write Control Logic, receive control words from the internal data bus and issue the proper commands to its associated ports:

Control Group A - Port A and Port C upper (C7-C4) Control Group B - Port B and Port C lower (C3-C0)

The Control Word Register can only be written into. Therefore reading of the Control Word Register is not allowed.

Ports A, B and C

The MA8255 contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features to further enhance the power and flexibility of the MA8255.

Port A.

One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B.

One 8-bit data input/output latch/buffer and one 8-bit input buffer

Port C.

One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B

OPERATING MODE 0
(Basic Input/Output)

This functional configuration provides simple input and output operation for each of the three ports. No handshaking is required; data is simply written to or read from a specified port.

- Two 8-bit ports and 4-bit ports
- Any port can be input or output
- Outputs are latched
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

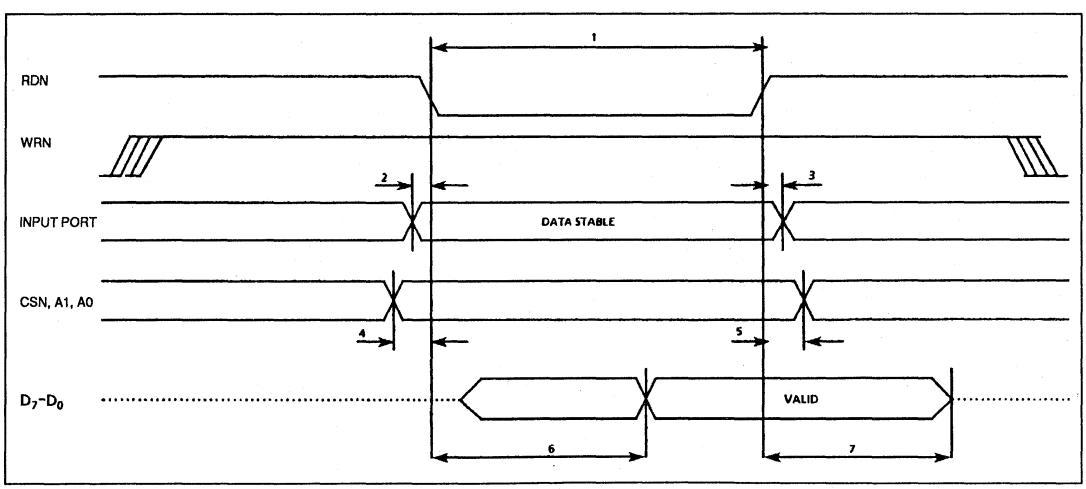


Figure 5: Basic Input (Read) Timing Diagram

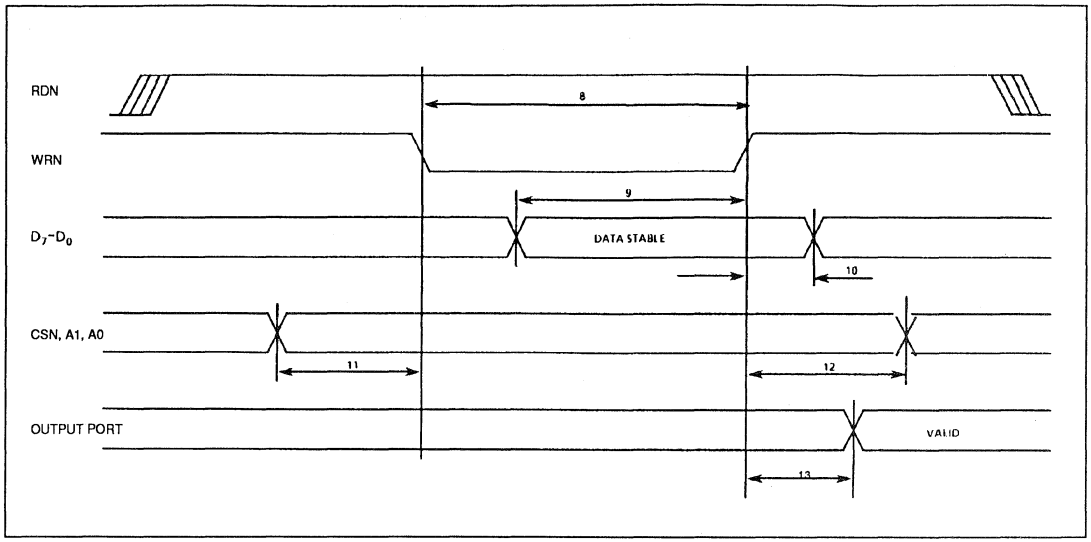


Figure 6: Basic Input (Write) Timing Diagram

Port Definition Mode 0

D_4	D_3	D_1	D_0	PORT A (UPPER)	PORT C	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	INPUT	INPUT
1	1	0	0	INPUT	INPUT	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	INPUT	INPUT

Table 2: Port Definition Mode 0 (See Also Figure 3)

OPERATING MODE 1
(Strobed Input/Output)

This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or handshaking signals. In mode 1, port A and port B use the lines on port C to generate or accept these handshaking signals

- Two Groups (Group A and Group B) .
- Each Group contains one 8-bit data port and one 4-bit control/data port,
- The 8-bit data port can be either input or output, Both inputs and outputs are latched,
- The 4-bit port is used for control and status of the 8-bit data port.

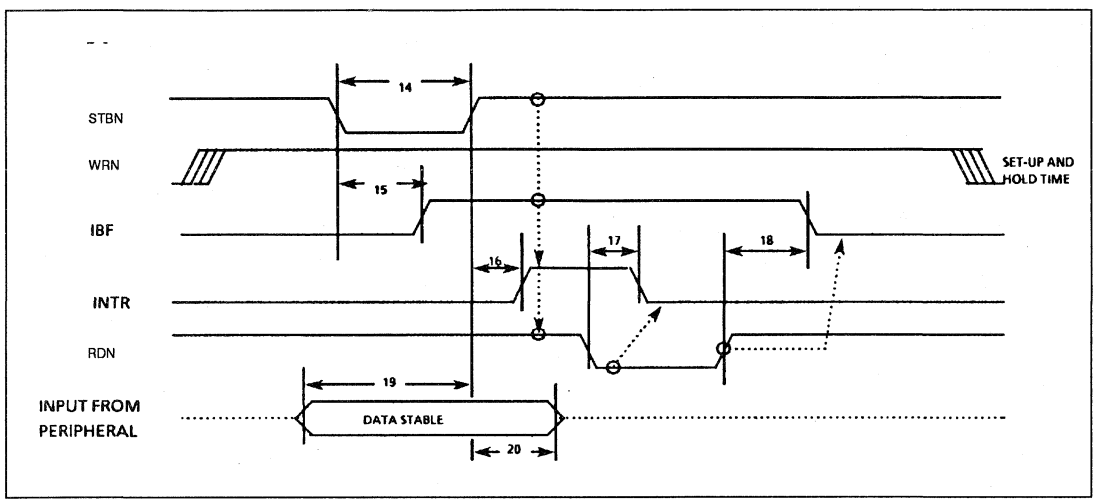


Figure 7: Strobed Input Timing Diagram

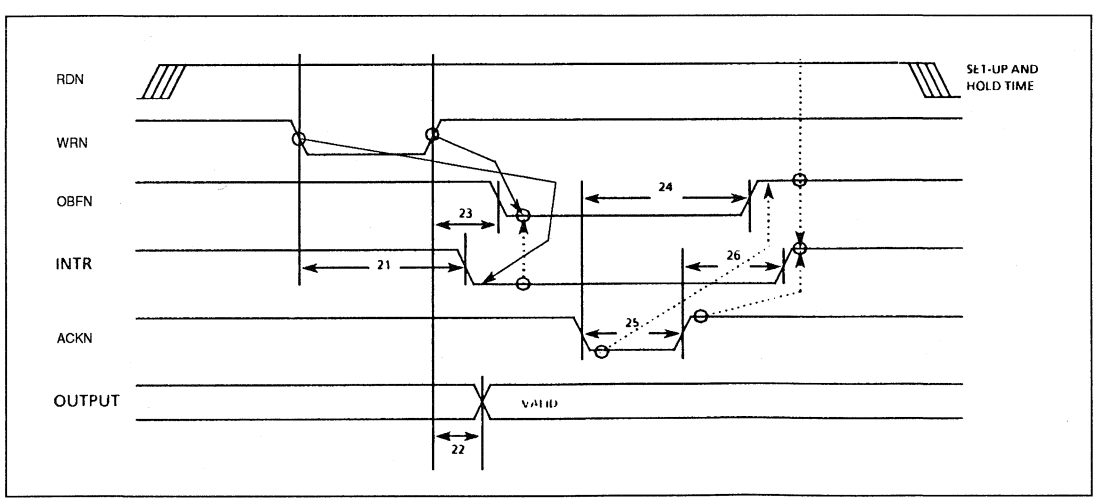


Figure 8: Strobed Output Timing Diagram

Input Control Signal Definition (Mode 1)

STBN (Strobe Input).

A low on this input loads data into the input latch.

IBF (Input Buffer Register Bit).

A high on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement.

IBF is set by STBN active pulse (which strobes data into the device) and is reset by the rising edge of RDN (which reads the latched data out of the device).

INTR (Interrupt Request).

A high on this output can be used to interrupt the CPU when an input device is requesting service, INTR is set by the STBN being high and IBF being high and INTE being enabled, It is reset by the falling edge of RDN, This procedure allows an input device to request service from the CPU by simply strobing its data into the port,

INTE A: Controlled by bit set/reset of PC_4

INTE B: Controlled by bit set/reset of PC_2

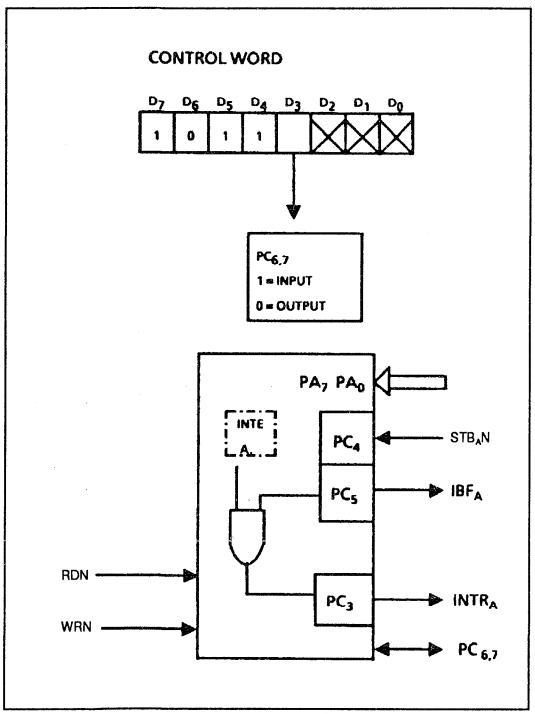


Figure 9: Strobed Input (PORT A)

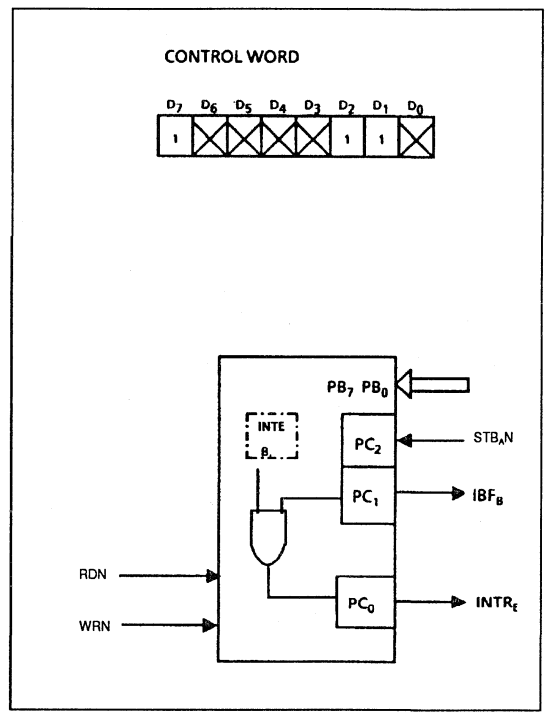


Figure 10: Strobed Input (PORT B)

Output Control Signal Definition (Mode 1)

OBFN (Output Buffer Full Register Bit).

The OBFN output will go low to indicate that the CPU has written data out to the specified port. The OBF register bit will be set by the rising edge of the WRN input and reset by ACKN input being low.

ACKN (Acknowledge Input).

A low on this input informs the 8255 that the data from port A or port B has been accepted; in essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request).

A high on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU, INTR is set when ACKN is high, OBF is high and INTE is high. It is reset by the falling edge of WRN.

INTE A: Controlled by bit set/reset of PC_6
INTE B: Controlled by bit set/reset of PC_2

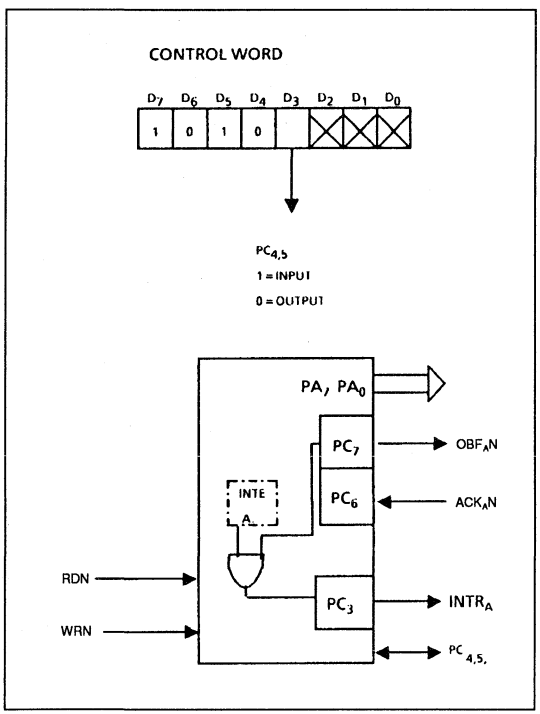


Figure 11: Strobed Output (PORT A)

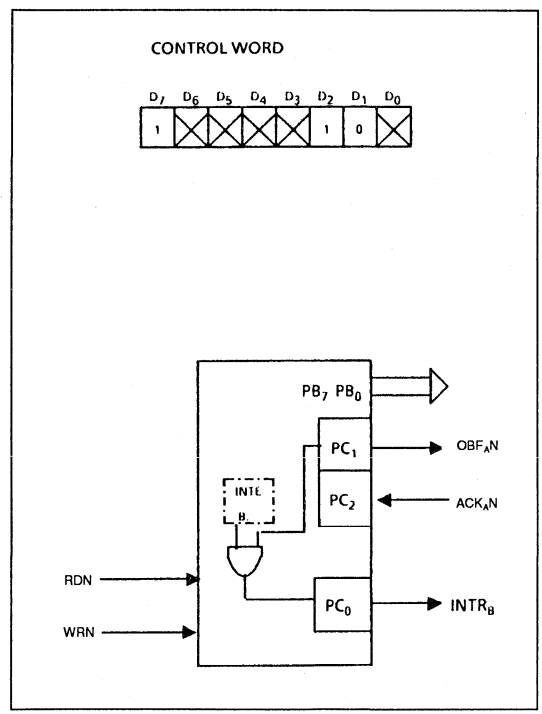


Figure 12: Strobed Output (PORT B)

Combinations of Mode 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

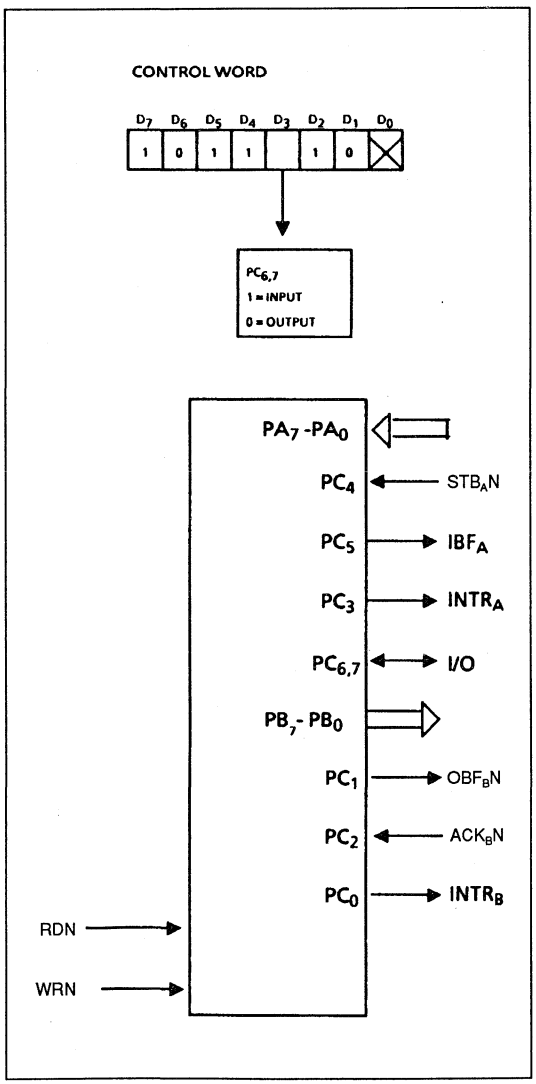


Figure 13: PORT A (STROBED INPUT) PORT B (STROBED OUTPUT)

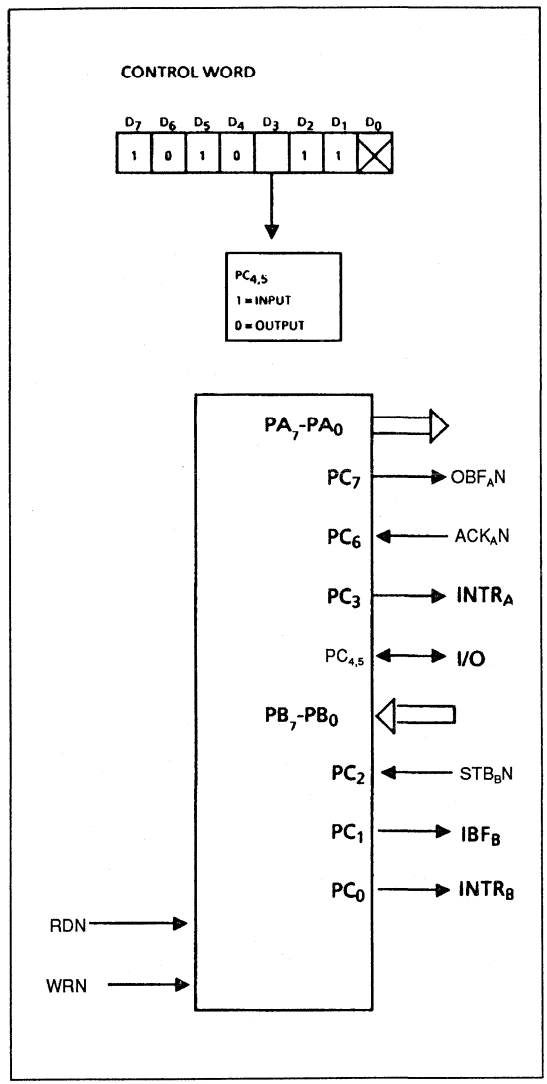
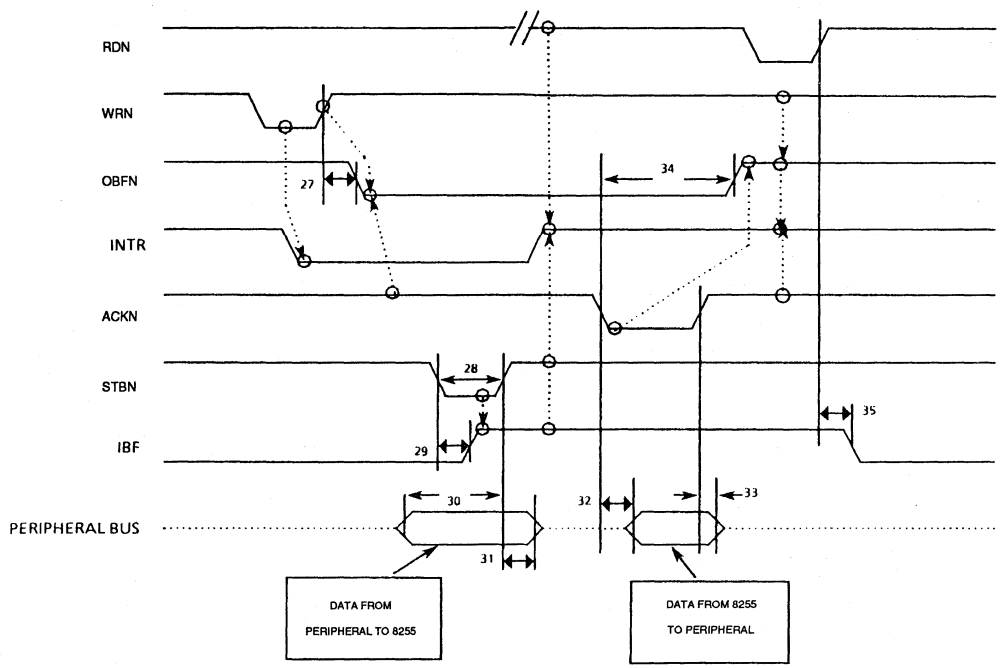


Figure 14: PORT A (STROBED OUTPUT) PORT B (STROBED INPUT)

OPERATING MODE 2
(Strobed Bidirectional Bus I/0)

This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O) . Handshaking signals are provided to maintain proper bus flow discipline in a similar manner to Mode 1, Interrupt generation and enable/disable functions are also available.

- Used in group A only.
- One 8-bit bidirectional bus port (port A) and 5-bit control port (port C).
- Both inputs and outputs are latched,
- The 5-bit control port (port C) is used for control and status of the 8-bit bidirectional bus port (port A).



The sequence of events to output information is:
WRN strobes data into the device on the rising edge of WRN. This in turn causes OBFN to go low. The ACKN pulse reads the data out, and also resets OBFN. An interrupt to obtain more data is generated when INTE1 (PC_6) = 1, WRN = 1, ACKN = 1, OBFN = 1. The next WRN will clear INTR.
The sequence of events to input information is: STBN strobes data into the device. This causes IBF to be set. An interrupt to forward the data is generated when INTE2 (PC_4) = 1, RDN = 1, STBN = 1, IBF = 1. INTR is reset by RDN.

Figure 15: Bidirectional Timing Diagram

BIDIRECTIONAL BUS L/O CONTROL

Signal Definition (Mode 2)

INTR (Interrupt Request):
A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

OBFN (Output Buffer Full):
The OBFN output will go low to indicate that the CPU has written data out to port A.

ACKN (Acknowledge):
A low on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state,

INTE 1 (INTE register bit associated with OBFN):
Controlled by Bit Set/Reset of PC_6.

Input Operations

STBN (Strobe input):
A low on this input loads data in to the input latch,

IBF (Input Buffer Full Register Bit):
A high on this output indicates data has been loaded in to the input latch,

INTE 2 (The INTE register bit associated with IBF).
Controlled by Bit Set/Reset of PC_4.

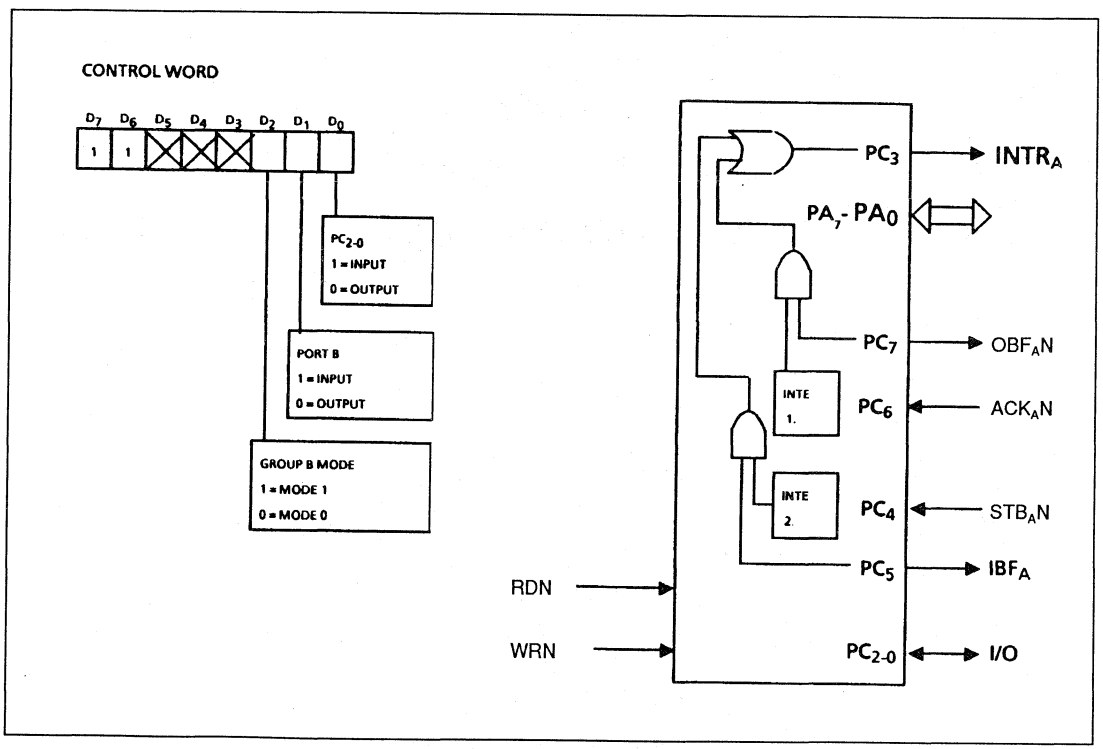


Figure 16: Mode 2 Bidirectional

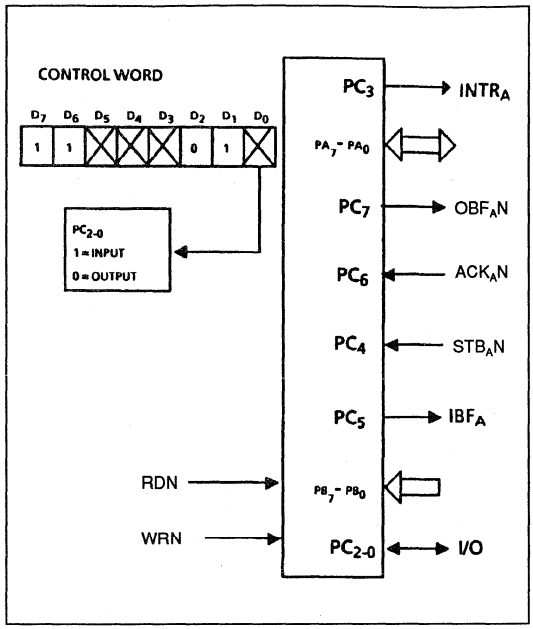


Figure 17a: Mode 2 and Mode 0 (Input)

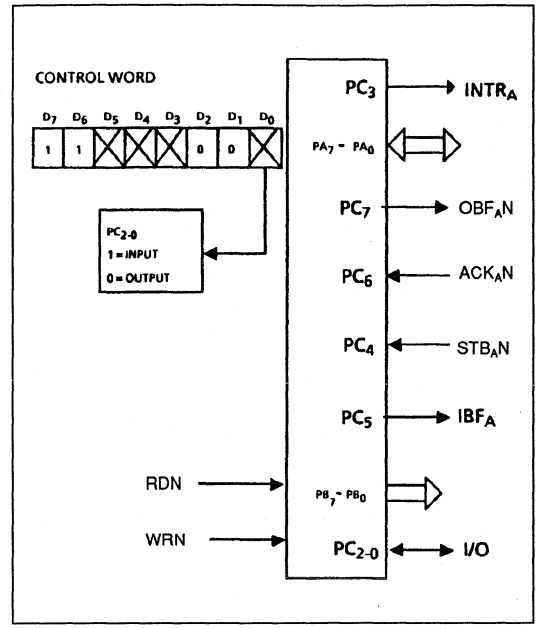


Figure 17b: Mode 2 and Mode 0 (Output)

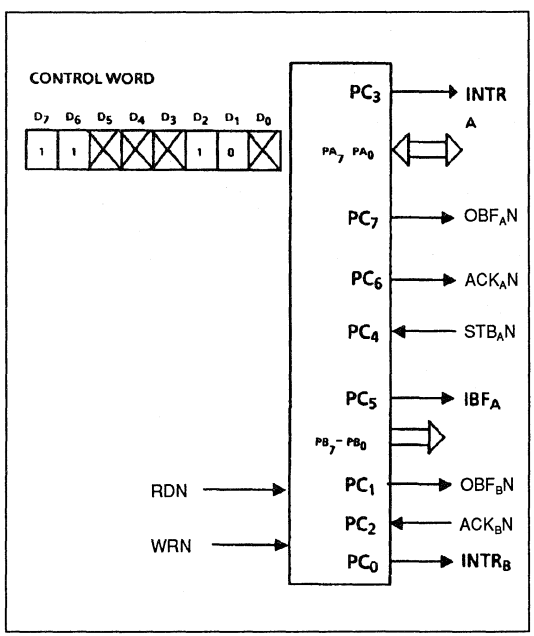


Figure 17c: Mode 2 and Mode 1 (Output)

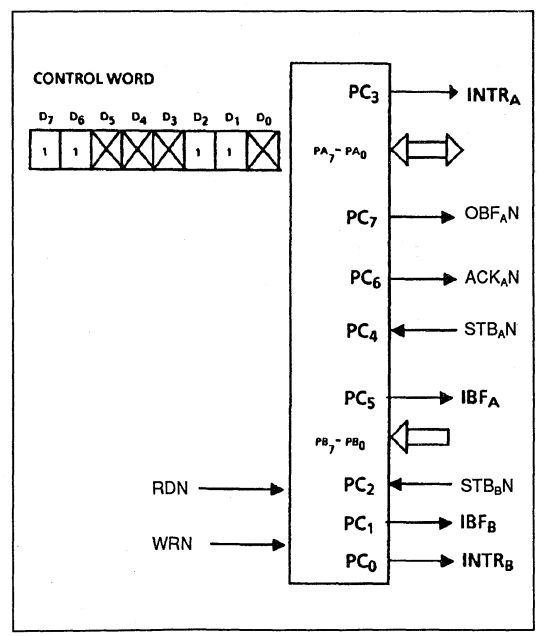


Figure 17d: Mode 2 and Mode 1 (Input)

Mode Definition Summary

	MODE 0		MODE 1		MODE 2
	IN	OUT	IN	OUT	
PA_0	IN	OUT	IN	OUT	⇐ ⇒
PA_1	IN	OUT	IN	OUT	⇐ ⇒
PA_2	IN	OUT	IN	OUT	⇐ ⇒
PA_3	IN	OUT	IN	OUT	⇐ ⇒
PA_4	IN	OUT	IN	OUT	⇐ ⇒
PA_5	IN	OUT	IN	OUT	⇐ ⇒
PA_6	IN	OUT	IN	OUT	⇐ ⇒
PA_7	IN	OUT	IN	OUT	⇐ ⇒
PB_0	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_1	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_2	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_3	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_4	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_5	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_6	IN	OUT	IN	OUT	Port B mode 0 or 1
PB_7	IN	OUT	IN	OUT	Port B mode 0 or 1
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O
PC_1	IN	OUT	IBF_B	OBF_BN	I/O
PC_2	IN	OUT	STB_BN	ACK_BN	I/O
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$
PC_4	IN	OUT	STB_AN	I/O	STB_AN
PC_5	IN	OUT	IBF_A	I/O	IBF_A
PC_6	IN	OUT	I/O	ACK_AN	ACK_AN
PC_7	IN	OUT	I/O	OBF_AN	OBF_AN

Table 3: Mode Definition Summary

Special Mode Combination Considerations.

There are several combinations of modes when not all of the bits in port C are used for control or status. The remaining bits can be used as follows:

If programmmed as inputs-

All input lines can be accessed during normal port C read.

If programmed as outputs

Bits in C upper (PC7-PC4) must be individually accessed using a bit set/reset function.

Bits in C lower (PC3-PC0) can be accessed using the bit set/reset function or bits PC2-PC0 may also be accessed as a trio by writing into port C.

Reading Port C Status.

In Mode 0 Port C transfers data from or to the peripheral device, When the MA8255 is programmed to function in Modes 1 or 2 Port C generates or accepts handshaking signals with the peripheral device, Reading the contents of Port C allows the programmer to test or verify the status of each peripheral device and change the program flow accordingly.

There is no special instruction to read the Status Information from Port C. A normal read operation of Port C is executed to perform this function.

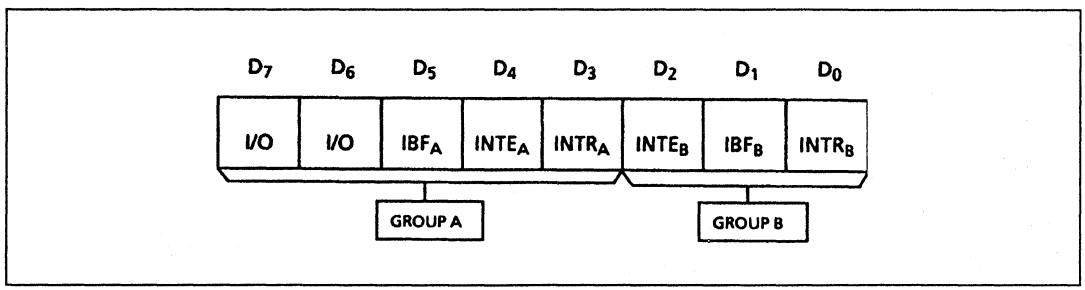


Figure 18a: Mode 1 Input Configuration

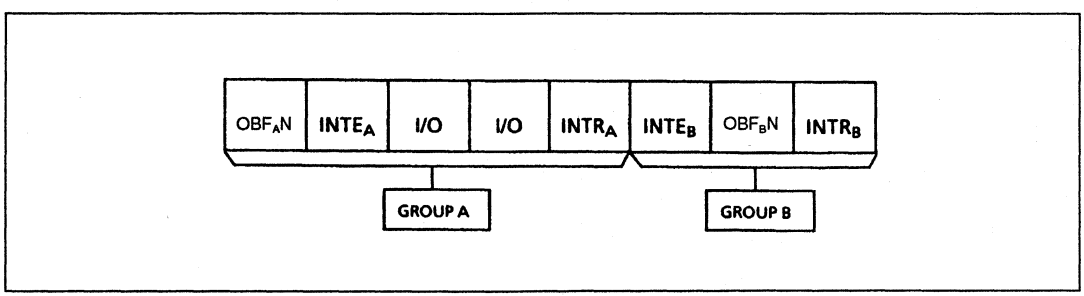


Figure 18b: Mode 1 Output Configuration

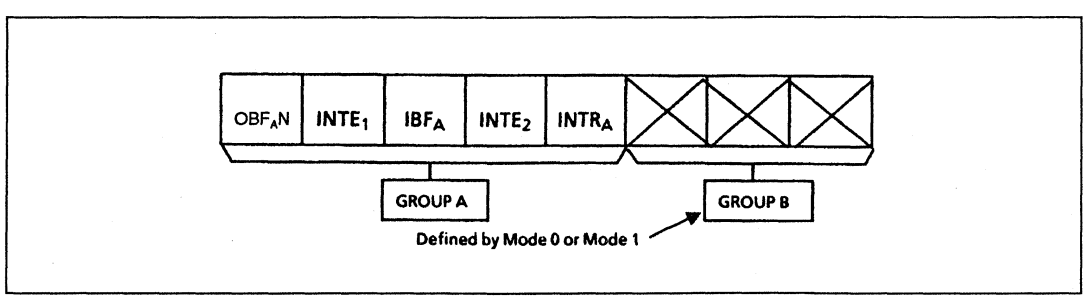


Figure 18c: Mode 2

Subgroup	Definition
1	Static characteristics specified in Table 6 at +25°C
2	Static characteristics specified in Table 6 at +125°C
3	Static characteristics specified in Table 6 at -55°C
7	Functional characteristics specified in Table 7 at +25°C
8A	Functional characteristics specified in Table 7 at +125°C
8B	Functional characteristics specified in Table 7 at -55°C
9	Switching characteristics specified in Table 7 at +25°C
10	Switching characteristics specified in Table 7 at +125°C
11	Switching characteristics specified in Table 7 at -55°C

Table 4: Definition of Subgroups

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	2.2	-	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -5mA	3.5	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 10mA	-	-	V_{SS}+0.4	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Tristate Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	µA
I_{DD}	Power Supply Current	Static,	-	0.1	10	mA

Note 1: Guaranteed but not tested at -55C.
V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3

Table 6: Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

	Parameter	Min.	Max.	Units		Parameter	Min.	Max	Units
					18	RDN ⇑ to IBF ⇑	-	65	ns
					19	Peripheral Data set up to STBN ⇑	100		ns
1	RDN pulse width	65	-	ns	20	Peripheral Data hold after STBN ⇑	100		ns
2	Peripheral Data set up to RDN	0	-	ns	21	WRN ⇓ to INTR ⇓ (note 4)	-	WRN +100	ns
3	Peripheral Data hold after RDN	10	-	ns	22	Output valid from WRN ⇑	-	100	ns
4	CSN, A1, AO setup to RDN ⇓	0	-	ns	23	WRN ⇑ to OBFN ⇓	-	105	ns
5	CSN, A1, AO hold after RDN ⇑	0	-	ns	24	ACKN ⇓ to OBFN ⇑	-	50	ns
6	Data valid from RDN ⇓	-	60	ns	25	ACKN pulse width	100	-	ns
7	Data float from RDN ⇑ (note 5)	10	100	ns	26	ACKN ⇑ INTR ⇑	-	80	ns
8	WRN pulse width	65	-	ns	27	WRN ⇑ to OBFN ⇓	-	105	ns
9	Data Set up to WRN ⇑	25	-	ns	28	STBN pulse width	100	-	ns
10	Data hold after WRN ⇑	30	-	ns	29	STBN ⇓ to IBF ⇑	-	65	ns
11	CSN, A1, AO setup to WRN ⇓	5	-	ns	30	Peripheral Data set up to STBN ⇑	0	-	ns
12	CSN, A1, AO hold after WRN ⇑	20	-	ns	31	Perlpheral Data hold after STBN ⇑	100	-	ns
13	Output valid from WRN ⇑	-	100	ns	32	Output valid from ACKN ⇓	-	45	ns
14	STBN pulse width	100	-	ns	33	Output float from ACKN ⇑ (note 5)	10	100	ns
15	STBN ⇓ to IBF ⇑	-	65	ns	34	ACKN ⇓ to OBFN ⇑	-	50	ns
16	STBN ⇑ to INTR ⇑	-	65	ns	35	RDN ⇑ to IBF ⇓	-	65	ns
17	RDN ⇓, to INTR ⇓	-	65	ns					

1. V_{DD} = 5V±10% and C_{CL} = 50pF, over full operating temperature range.
2. Input Pulse V_{SS} to 3.0 Volts.
3. Times Measurement Reference Level 1.5 Volts.
4. WRN = WRN Pulse Width.
5. Measured by a 1.0 Volt change in output voltage. Outputs tied to V_{SS} via 680Ω.

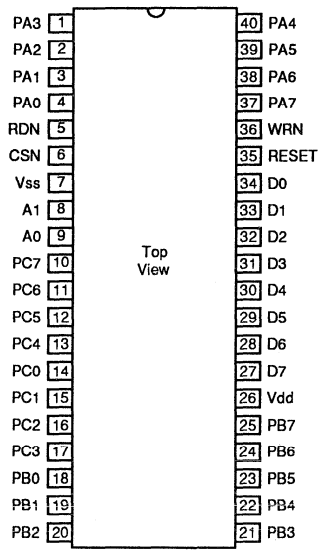
Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Table 7: AC Electrical Characteristics

PACKAGE OUTLINES & PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	51.31	-	-	2.020
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG405



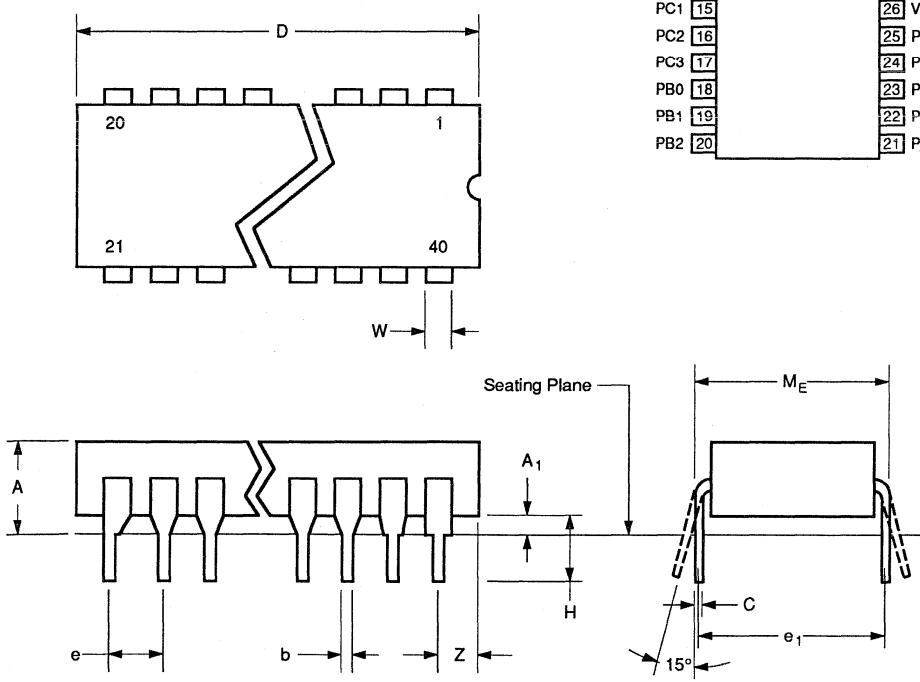


Figure 19: 40-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.41	-	-	0.095
b1	-	0.64	-	-	0.025	-
D	16.33	-	16.81	0.643	-	0.662
E	16.33	-	16.81	0.643	-	0.662
e	-	1.27	-	-	0.050	-
Z	-	1.91 Typ.	-	-	0.075 Typ.	-

XG446

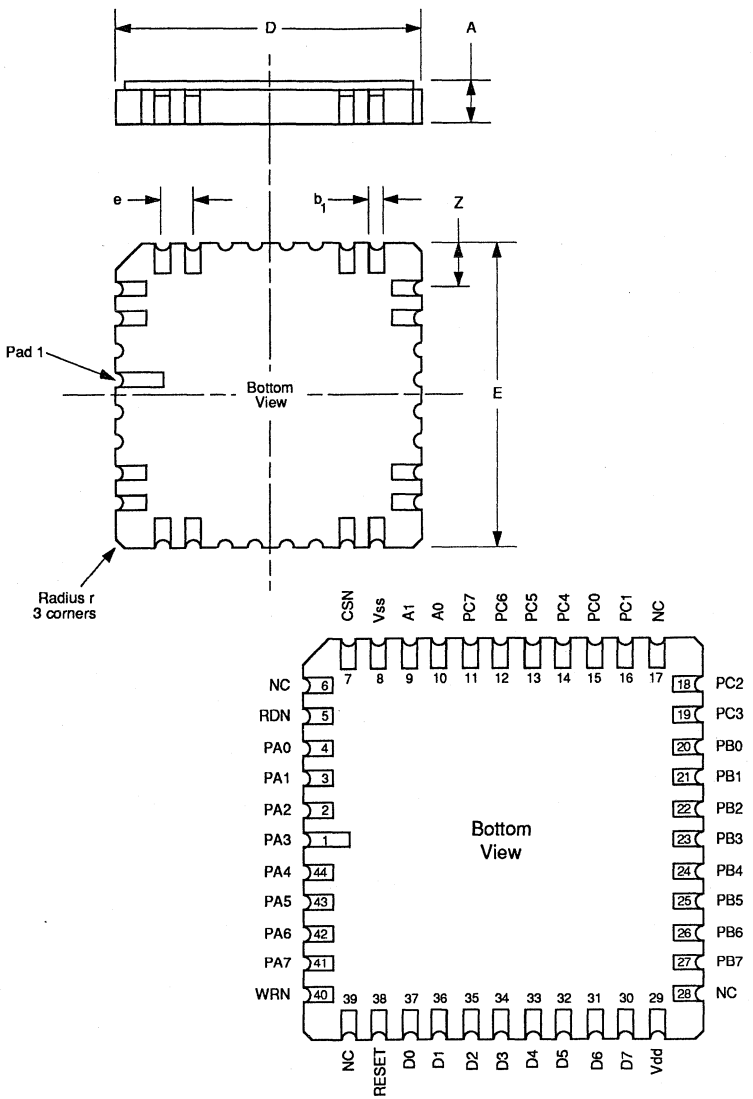


Figure 20: 44-Pad Leadless Chip Carrier (Package Style L)

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

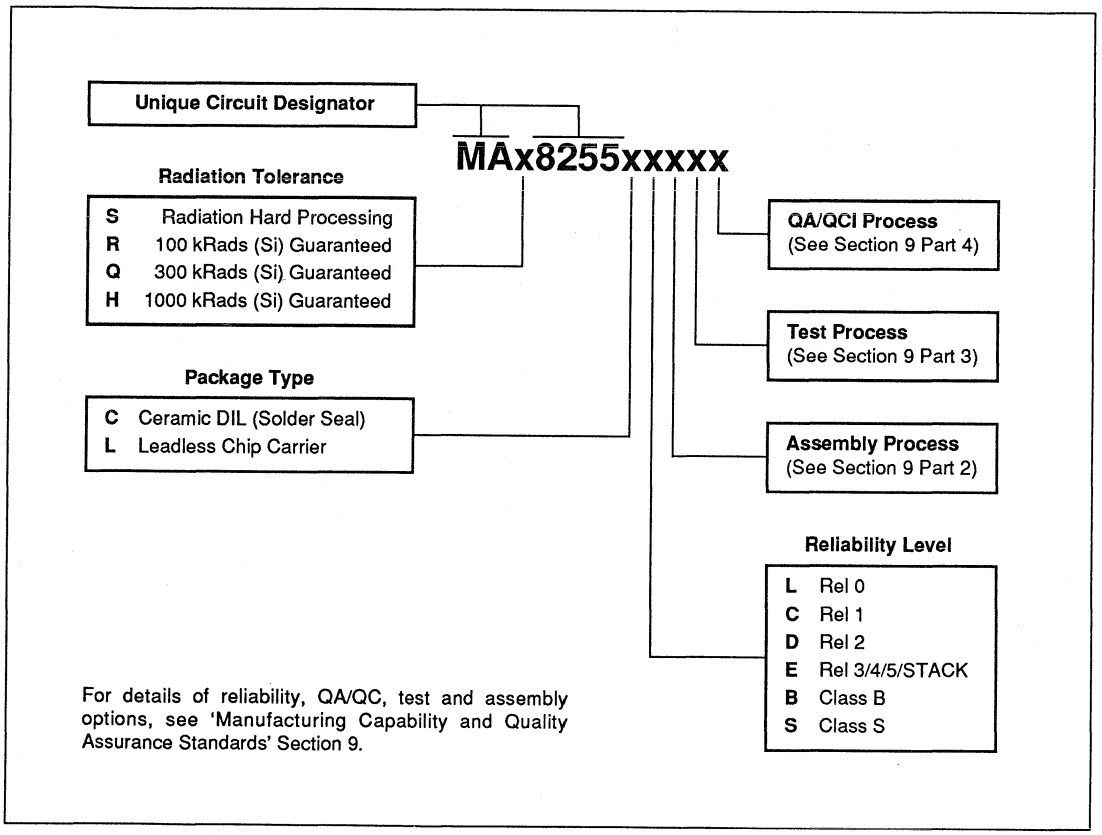
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 21: Radiation Hardness Parameters

ORDERING INFORMATION



Section 3

Bit Slice & Arithmetic Circuits

GEC PLESSEY
SEMICONDUCTORS

MA2901

RADIATION HARD 4-BIT MICROPROCESSOR SLICE

The MA2901 is an industry standard 4-bit microprocessor slice It provides a set of ALU functions selected by microcode data applied to the inputs. The device is cascadable to handle any word length. It can be used as a building block in the construction of microcomputers and controllers tailored to meet specialised applications.

Dual Address Architecture
Machine cycles are saved by simultaneous, independent access to two working registers.

ALU has Eight Functions
Operations performed are addition, two subtractions and five logic functions on two source operands.

Four State Flags
Zero, negative, carry and overflow.

Left / Right Shift is Independent of ALU
Only one cycle taken for add and shift operations.

Expandable
Any number of MA2901 units can be connected together to achieve longer word lengths.

Micro Programmable
Three groups, each of three bits, for ALU function, source operand and destination control.

FEATURES

- Fully Compatible with Industry Standard 2901
- CMOS SOS Technology
- High SEU Immunity and Latch-up Free
- High Speed
- Low Power

OPERATION

A detailed block diagram of the microprogrammable microprocessor structure is shown in figure 1. The circuit is a four-bit slice, cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the figure 1 are the 16-word by 4-bit 2-port RAM and the high speed ALU.

Data from any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A-address field input. Likewise, data from any of the 16 words of the RAM as defined by the B-address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A-select field and B-select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B-address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

The ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

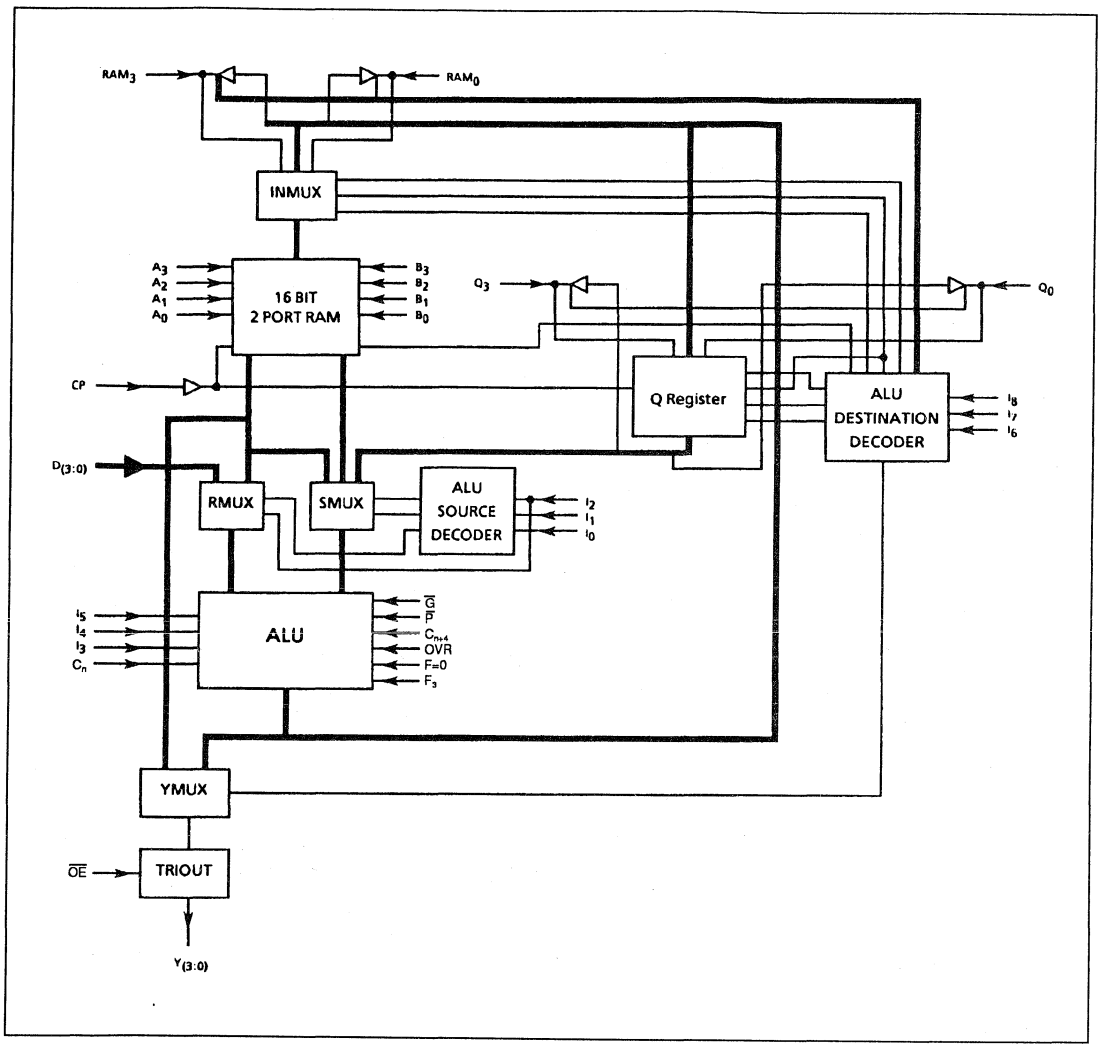


Figure 1: Block Diagram

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent the AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant sourced operand pairs for the ALU. The MA2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading ALU of several devices is in a look-ahead carry mode. Carry generate, GN, and carry propagate, PN, are outputs of the device for use with a carry-look-ahead-generator. A carry-out Cn + 4, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (Cn) and carry-out (Cn+4) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F=0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is when Cn + 3 and Cn + 4 are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organised. An output control (OEN) is used to enable the three-state outputs. When OEN is HIGH, the Y outputs are in the high impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (x 2) or shifted down one position (÷ 2). The shifter has two ports; labeled RAM_0 and RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer.

Microcode				ALU Source Operands	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	C
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

Figure 2: ALU Source Operand Control

Microcode				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R plus S	R + S
L	L	H	1	S minus R	S - R
L	H	L	2	R minus S	R - S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	RN AND S	RN ∧ S
H	L	H	5	R AND S	R ∧ S
H	H	L	6	R EX-OR S	R ∇ S
H	H	H	7	R EX-NOR S	RN ∇ SN

+ = plus; - = minus; ∨ = OR; ∧ = AND; ∇ = EX-OR

Figure 2: ALU Function Control

In the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. The shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the non-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7 and I_8 as shown in Figure 4.

The clock input shown in Figure 1 controls the RAM, the Q resister and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

SOURCE OPERANDS & ALU FUNCTION

Any one of eight source operand pairs can be selected by instruction inputs Io, I_1 and I_2 for use by the ALU; instruction inputs I_3, I_4, and I_5 then control function selection for the ALU - five logic and three arithmetic functions. In the arithmetic mode, the carry input (Cn) also affects the ALU functions; the carry input has no effect on the 'F' result in the logic mode. These control parameters (I_6 - I_0 and Cn) are summarised in Figure 5 to completely define the ALU/source operand functions.

The ALU functions can also be examined on a task basis: that is, add, subtract, AND, OR, and so on. Again, in the arithmetic mode, the carry input still affects the result, whereas in the logic mode it will not. Figures 6 and 7, respectively, define the various logic and arithmetic functions of the ALU; both carry states (Cn = 0 / Cn = 1) are defined in the function matrices.

Microcode				RAM Function		Q-Reg Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F→Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F→B	X	None	A	X	X	X	X
L	H	H	3	None	F→B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2→B	Q/2→Q	F	-	F0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2→B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F→B	Up	2Q→Q	F	IN_0	F_3	IN_3	Q_3
H	H	H	7	Up	2F→B	X	None	F	IN_0	F_3	X	Q_3

X = Don't Care. Electrically, the shift pin is a TTL input internally connected to a TRI-STATE output which is in the high-impedance state.
B = Register addressed by 8 inputs. Up is towards MSB, Down is towards LSB.

Figure 4: ALU Destination Control

	$I_{2,1,0}$ Octal	0	1	2	3	4	5	6	7
Octal $I_{5,4,3}$	ALU Source /ALU Function	A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n=L R plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n=H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	Cn=L S minus R	Q-A-1	B-A-1	Q-1	B-1	A-1	A-D1	Q-D-1	-D-1
	C_n=H	Q-A	B-A	Q	B	A	A-D	Q-D	-D
2	C_n=L R minus S	A-Q-1	A-B-1	-Q-1	-B-1	-A-1	D-A-1	D-Q-1	D-1
	C_n=H	A-Q	A-B	-Q	-B	-A	D-A	D-Q	D
3	R or S	A∨Q	A∨B	Q	B	A	D∨A	D∨Q	D
4	R and S	A∧Q	A∧B	0	0	0	D∧A	D∧Q	0
5	RN and S	AN∧Q	AN∧B	Q	B	A	DN∧A	DN∧Q	0
6	R EX-OR S	A∇Q	A∇B	Q	B	A	D∇A	D∇Q	D
7	R EX NOR S	AN∇QN	AN∇BN	Q	B	A	DN∇AN	DN∇QN	DN

+ = plus; - = minus; ∨ = OR; ∧ = AND; ∇ = EX-OR

Figure 5: Source Operand and ALU Function Matrix

Octal $I_{5,4,3}$ /$I_{2,1,0}$	Group	Function
40	AND	A ∧ Q
41		A ∧ B
45		D ∧ A
46		D ∧ Q
30	OR	A ∨ Q
31		A ∨ B
35		D ∨ A
36		D ∨ Q
60	EX-OR	A ∇ Q
61		A ∇ B
65		D ∇ A
66		D ∇ Q
70	EX-NOR	AN ∇ QN
71		AN ∇ BN
75		DN ∇ AN
76		DN ∇ QN
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
40	'ZERO'	0
43		0
44		0
47		0
50	AND	AN ∧ Q
51		AN ∧ B
55		DN ∧ A
56		DN ∧ Q

+ = plus; - = minus; ∨ = OR; ∧ = AND; ∇ = EX-OR

Figure 6: ALU Logic Mode Functions (C_n Irrelevant)

Octal	Cn=0(Low)		Cn = 1 (High)	
$I_{5,4,3}$/$I_{2,1,0}$	Group	Function	Group	Function
00	ADD	A+Q	ADD plus one	A+Q+1
01		A+B		A+B+1
05		D+A		D+A+1
06		D+Q		D+Q+1
02	PASS	Q	Increment	Q+1
03		B		B+1
04		A		A+1
07		D		D+1
12	Decrement	Q-1	PASS	Q
13		B-1		B
14		A-1		A
27		D-1		D
22	1s comp	-Q-1	2s comp (negate)	-Q
23		-B-1		-B
24		-A-1		-A
17		-D-1		-D
10	SUBTRACT (1s comp)	Q-A-1	SUBTRACT (2s comp)	Q-A
11		B-A-1		B-A
15		A-D-1		A-D
16		Q-D-1		Q-D
20		A-Q-1		A-Q
21		A-B-1		A-B
25		D-A-1		D-A
26		D-Q-1		D-Q

Figure 7: ALU Arithmetic Mode Functions

PIN DESCRIPTION

Name	I/O	Description
A_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the A port
B_{0-3}	I	The four address inputs to the register stack used to select one register whose contents are displayed through the B port and into which new data can be written when the clock goes LOW
I_{0-8}	I	The nine instruction control lines. Used to determine what data sources will be applied to the ALU($I_{0,1,2}$), what function the ALU will perform ($I_{3,4,5}$), and what data is to be deposited in the Q-register or the register stack ($I_{6,7,8}$)
Q_3 RAM_3	I/O	The shift line at the MSB of the Q-register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on $I_{6,7,8}$ indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the Q-register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three state outputs are electrically OFF (high impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q-register (Octal 4) and RAM (Octal 4 or 5)
Q_0 RAM_0	I/O	Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q-register and ALU data.
D_{0-3}	I	Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device D_0 is the LSB
Y_{0-3}	O	The four data outputs. These are three-state output lines. When they are enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code $I_{6,7,8}$.
OEN	I	Output enable. When OEN is HIGH, the Y outputs are OFF; when OEN is LOW, the Y outputs are active (HIGH or LOW)
GN,PN	O	The carry generate and propagate outputs of the internal ALU. These signals are used with the MA2901 for carry lookahead.
OVR	O	Overflow. This pin is logically the Exclusive OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit
F = 0	O	This is an open collector output which goes HIGH(OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates that the result of the ALU operation is zero
F_3	O	The most significant ALU output bit.
C_n	I	The carry-in to the internal ALU.
$C_n + 4$	O	The carry-out of the ALU internal ALU.
CP	I	The clock input. The Q-register and register stack outputs change on the clock LOW - to HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

Figure 8: Pin Description

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 9: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Subgroup	Definition
1	Static characteristics specified in Figure 11 at +25°C
2	Static characteristics specified in Figure 11 at +125°C
3	Static characteristics specified in Figure 11 at -55°C
7	Functional characteristics at +25°C
8A	Functional characteristics at +125°C
8B	Functional characteristics at -55°C
9	Switching characteristics specified in Figures 12, 13 and 14 at +25°C
10	Switching characteristics specified in Figures 12, 13 and 14 at +125°C
11	Switching characteristics specified in Figures 12, 13 and 14 at -55°C

Figure 10: Definition of Subgroups

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	2.4	-	-	V
V_{IL}	Input Low Voltage	-	-	-	0.8	V
V_{OH}	Output High Voltage	I_{OH} = -6mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 10mA	-	-	0.4	V
I_{IN}	Input Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Output Leakage Current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±50	µA
I_{DD}	Power Supply Current	Static, V_{DD} = 5.5V	-	0.1	10	mA

V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Notes: 1. Guaranteed but not measured at -55°C

Figure 11: Operating Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

Read-Modify-Write Cycle (from selection of A,B registers to end of a cycle	40ns
Maximum Clock Frequency to shift Q(50% duty cycle, I = 432 or 632)	25MHz
Minimum Clock LOW time	20ns
Minimum Clock HIGH time	20ns
Minimum Clock Period	40ns

Note: 1. These timings are applied during functional tests and are not routinely measured.

Figure 12: Cycle Time and Clock Characteristics

From Input	To Output							
	Y	F_3	$C_n + 4$	G,P	F = 0	OVR	RAM_0 RAM_3	Q_0 Q_3
A,B Address	65	55	60	55	70	65	65	-
D	55	40	50	50	65	55	55	-
C_n	60	40	35	-	55	35	50	-
$I_{0,1,2}$	70	50	55	55	70	55	65	-
$I_{3,4,5}$	60	45	50	45	65	50	65	-
$I_{6,7,8}$	45	-	-	-	-	-	30	30
A Bypass ALU(I=2xx)	45	-	-	-	-	-	-	-
Clock	55	50	55	50	50	55	55	35

Note: All timings in ns

Figure 13: Combinational Propagation Delays

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A,B Source Address	25	5	30	-
B Destination Address	25	No change	No change	5
D	-	-	40	0
C_n	-	-	40	0
$I_{0,1,2}$	-	-	45	0
$I_{3,4,5}$	-	-	45	0
$I_{6,7,8}$	10	No change	No change	10
$RAM_{0,3}$, $Q_{0,3}$	-	-	15	10

MIL-STD-883, method 5005, subgroups 9, 10, 11

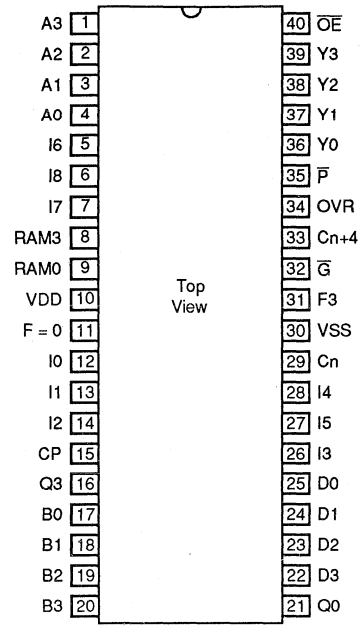
Note: 1. V_{DD} = 5V ±10%, over full operational temperature range
2. CL = 50 pF

Figure 14: Set-up and Hold Times Relative to Clock (CP) Input

OUTLINES AND PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	51.31	-	-	2.020
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG405



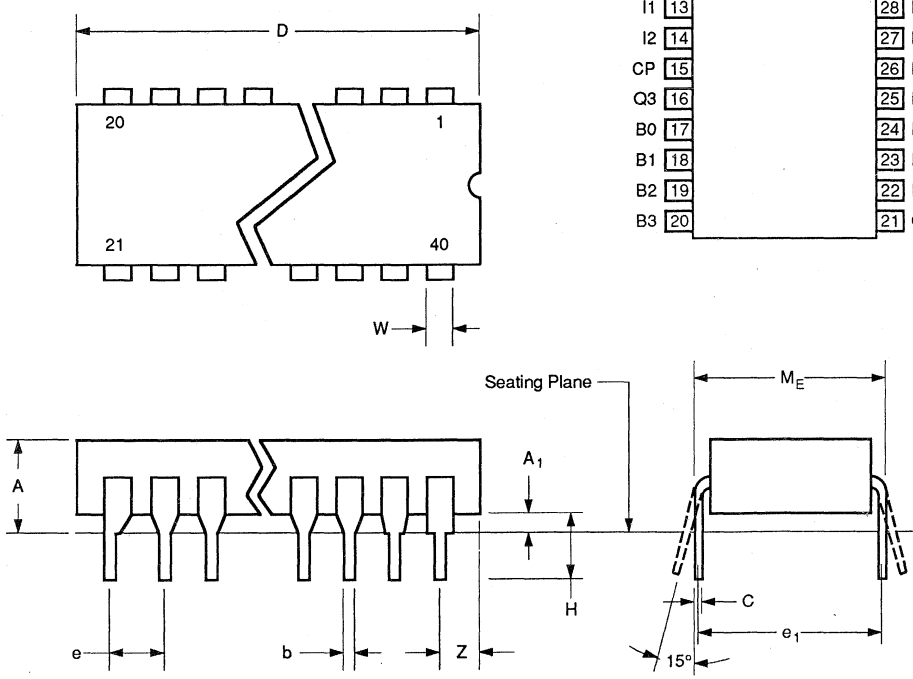
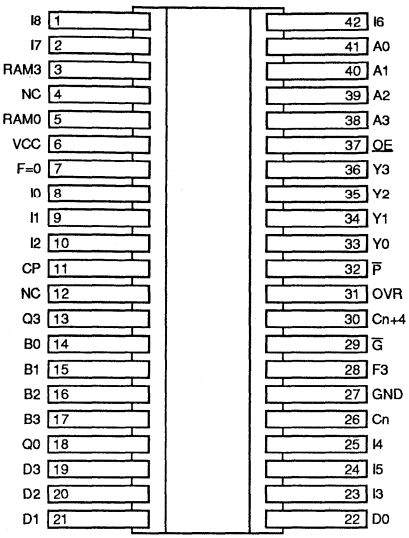


Figure 15: 40-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres		Inches	
	Min.	Max.	Min.	Max.
A	1.75	2.49	0.070	0.098
b	0.43	0.53	0.017	0.023
c	0.15	0.25	0.006	0.010
D	26.67	27.69	1.050	1.080
E	15.75	16.76	0.620	0.660
E1	-	17.27	-	0.630
E2	13.21	-	0.520	-
E3	0.76	-	0.030	-
e	1.14	1.40	0.045	0.055
L	7.87	9.40	0.310	0.370
L1	32.51	34.54	1.250	1.360
Q	0.76	1.52	0.030	0.060
S	-	1.14	-	0.045
S1	0.13	-	0.005	-

XG136



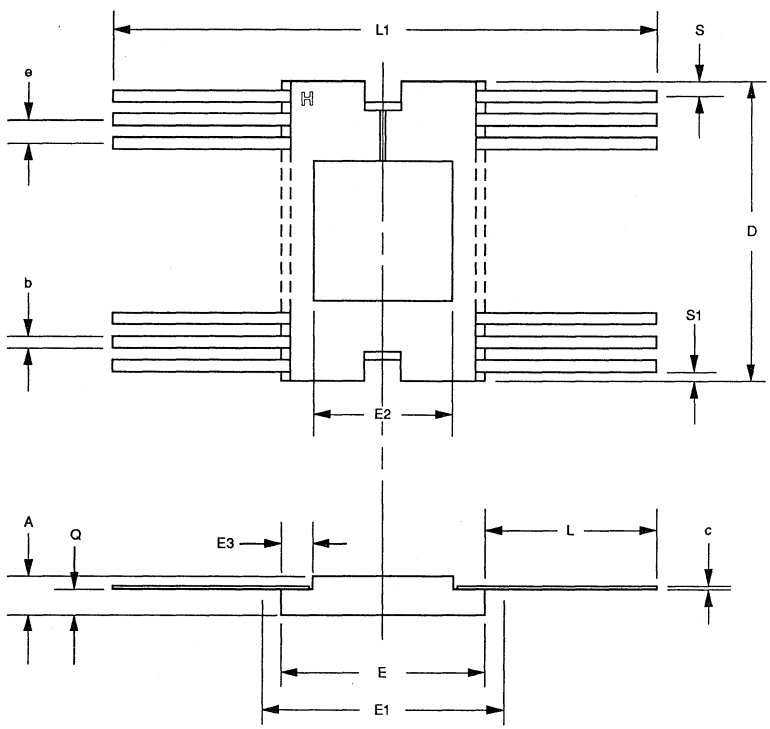


Figure 16: 42-Lead Flatpack (Solder Seal)

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

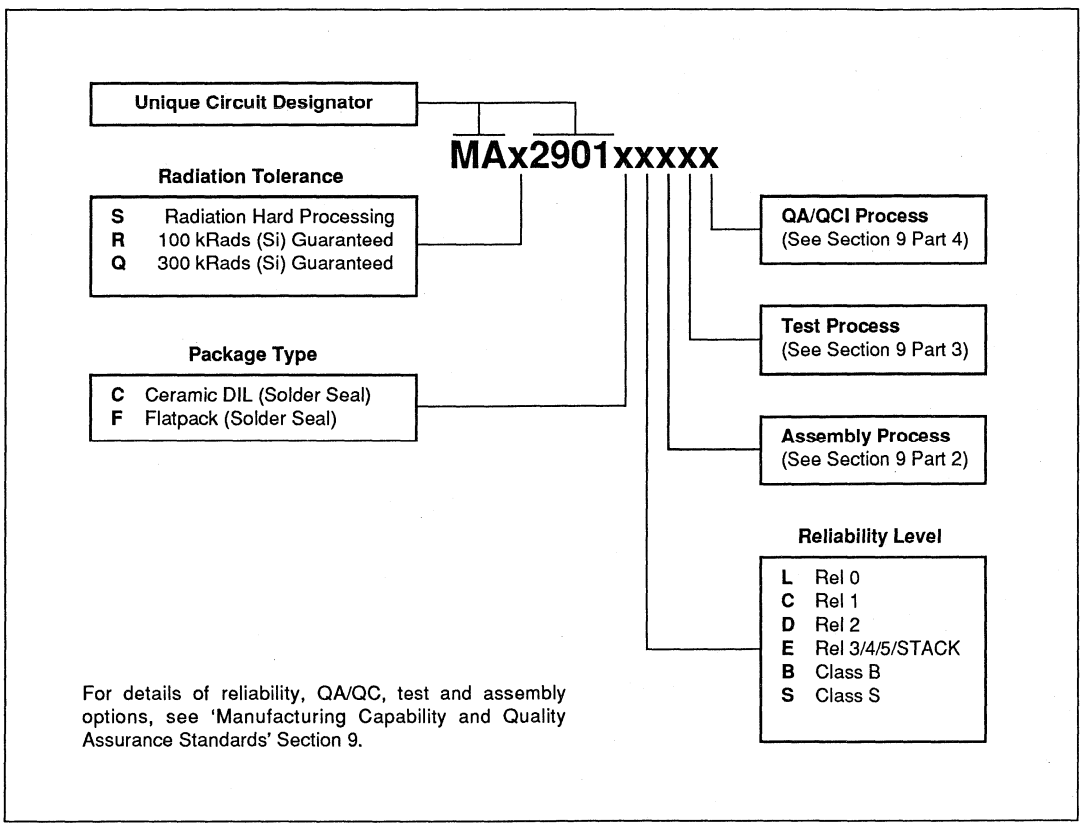
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 17: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA2909/11

RADIATION HARD MICROPROGRAM SEQUENCER

The MA2909/11 Microprogram Sequencer is fully compatible with the industry standard 2909A and 2911A components, and forms part of the GPS 2900 Series of devices. The series offers a building block approach to microcomputer and controller design, with each device in the range being expandable to permit efficient emulation of any microcode machine.

The devices have tristate outputs and have an internal address register, with all internal registers changing state on LOW to HIGH clock transition.

The 4-bit slice can cascade to any number of microwords. Branch input for N-way branches is supported. Additional features include:

- 4-bit cascadable microprogram counter.
- 4 x 4 file with stack counter supporting nesting microsubroutines.
- Zero input for returning to the zero microcode word.
- Individual OR input for each bit for branching to higher microinstructions (2909 only).

The 2909 is a 4-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two 2909s may be interconnected to generate an 8-bit address (256 words), and three may be used to generate a 12-bit address (4K words).

The 2909 can select an address from any of four sources:

1) A set of external direct inputs (D);

2) External data from the R inputs, stored in an internal register;

3) A four-word push/pop stack; or

4) A program counter register (which usually contains the last address plus one).

The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The 2911 is an identical circuit to the 2909 except the four OR inputs are removed and the D and R inputs are tied together.

FEATURES

- Fully Compatible with Industry Standard 2909A and 2911A Components
- Radiation Hard CMOS SOS Technology
- High SEU Immunity
- High Speed / Low Power
- Fully TTL Compatible

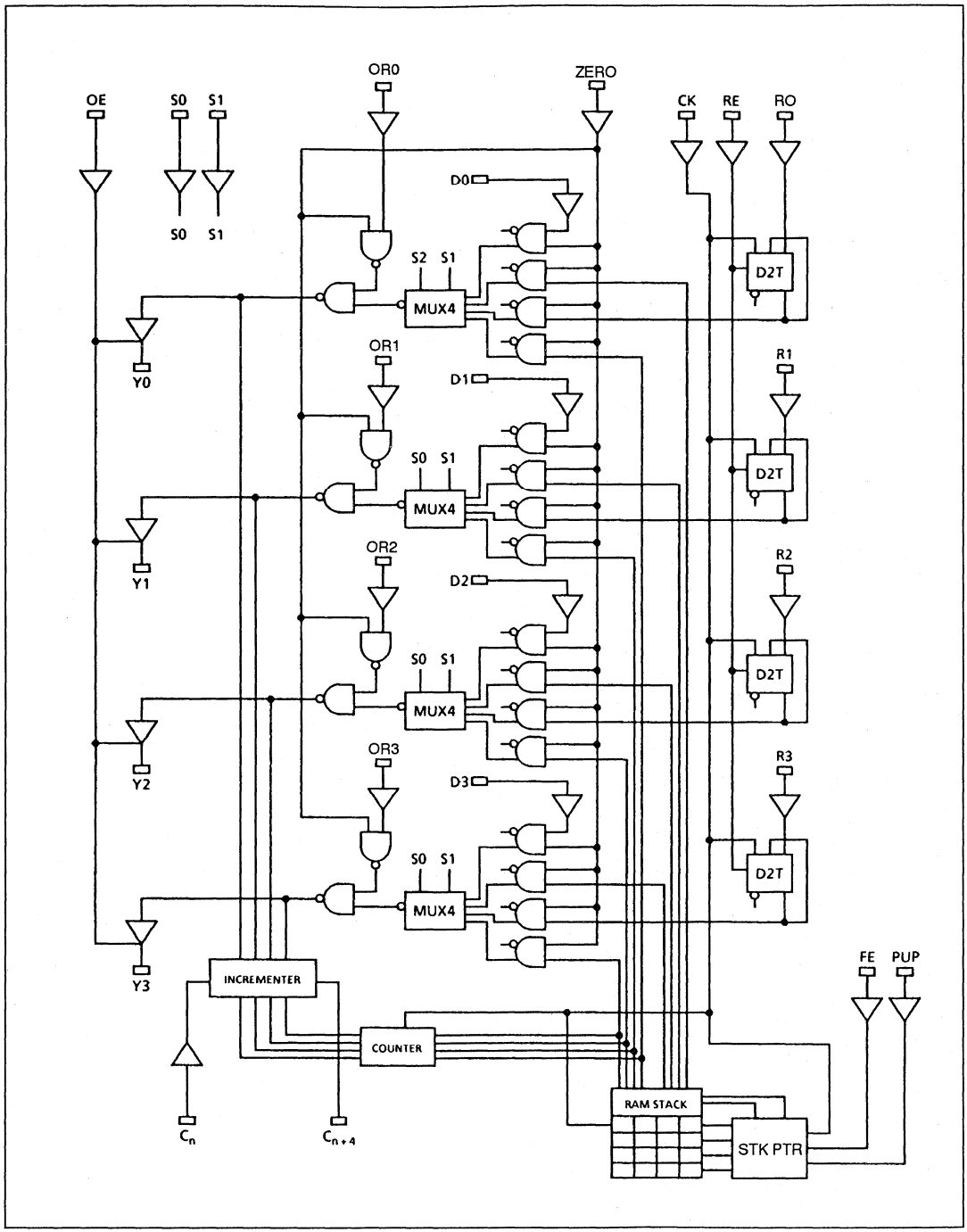


Figure 1: Microprogram Sequencer Block Diagram

The 2909/2911 are CMOS SOS microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256 words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in figure 1.

The device contains a four input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S0 and S1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address The direct input is a 4-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the 2911 the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The 2909/2911 contains a microprogram counter (µPC) that is composed of a 4-bit incrementer followed by a 4bit register. The incrementer has carry-in (C_n) and carry-out (C_n + 4) such that cascading to larger word lengths is straight forward. The µPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y + 1 ➔ µPC). Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprgram register is loaded with the same Y word on the next clock cycle (Y ➔ µPC). Thus, the same microinstruction can be executed any number of times by using the 4x4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage - the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of push, pop or stack references can be achieved. One microinstruction subroutine can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW all Y outputs are LOW regardless of any other inputs (except OE). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The 2909/2911 feature three-state Y outputs. These can be particularly useful in designs requiring external equipment to provide automatic checkout of the microprocessor. The internal control can be placed in the high impedance state and preprogrammed.

MULTIPLEXER SELECT CODES

Table 1 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Table 1 also shows the truth table for the output control and for the control of the push/pop stack. Table 2 shows in detail the effect of S_0, S_1, FE and PUP on the 2909. These four signals define the address that apears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

OR1	ZERO	OE	Y1
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0S_1

H = High, L = Low, Z = High Impedance

Table 1a: Output Control

FE	ZERO	PUSH-POP stack change
H	X	No change
L	H	Increment stack pointer, then push current PC on to STK0
L	L	Pop stack (decrement stack pointer)

H = High, L = Low, X = Irrelevant

Table 1b: Synchronous Stack Control

S_1 S_2	Source for Y outputs	Symbol
L L	Microprogram counter	µPC
L H	Address/Holding register	AR
H L	Push-Pop stack	STKO
H H	Direct inputs	D_1

Table 1c: Address Selection

Cycle	S1	S0	FE	PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	Comment	Principal Use
N	L	L	L	L	J	K	R_a	R_b	R_c	R_d	J	Pop Stack	End Loop
N + 1		-			J + 1	K	R_b	R_c	R_d	R_a	-		
N	L	L	L	H	J	K	R_a	R_b	R_c	R_d	J	Push μPC	Set-up Loop
N + 1		-			J + 1	K	J	R_a	R_b	R_c	-		
N	L	L	H	X	J	K	R_a	R_b	R_c	R_d	J	Continue	Continue
N + 1		-			J + 1	K	R_a	R_b	R_c	R_d	-		
N	L	H	L	L	J	K	R_a	R_b	R_c	R_d	K	Pop Stack;	End Loop
N + 1		-			K + 1	K	R_b	R_c	R_d	R_a	-	Use AR for Address	
N	L	H	L	H	J	K	R_a	R_b	R_c	R_d	K	Push μPC;	JSR AR
N + 1		-			K + 1	K	J	R_a	R_b	R_c	-	Jump to Address in AR	
N	L	H	H	X	J	K	R_a	R_b	R_c	R_d	K	Jump to Address in AR	JMP AR
N + 1		-			K + 1	K	R_a	R_b	R_c	R_d	-		
N	H	L	L	L	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in	RTS
N + 1		-			R_a + 1	K	R_b	R_c	R_d	R_a	-	STK0; Pop Stack	
N	H	L	L	H	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in	
N + 1		-			R_a + 1	K	J	R_a	R_b	R_c	-	STK0; Push μPC	
N	H	L	H	X	J	K	R_a	R_b	R_c	R_d	R_a	Jump to Address in	Stack Ref
N + 1		-			R_a + 1	K	R_a	R_b	R_c	R_d	-	STK0	(Loop)
N	H	H	L	L	J	K	R_a	R_b	R_c	R_d	D	Pop Stack;	End Loop
N + 1		-			D + 1	K	R_b	R_c	R_d	R_a	-	Jump to Address on D	
N	H	H	L	H	J	K	R_a	R_b	R_c	R_d	D	Jump to Address on D;	JSR D
N + 1		-			D + 1	K	J	R_a	R_b	R_c	-	Push μPC	
N	H	H	H	X	J	K	R_a	R_b	R_c	R_d	D	Jump to Address on D	JMP D
N + 1		-			D + 1	K	R_a	R_b	R_c	R_d	-		

1 = High, 0 = Low, X = Irrelevant, Assume C_n = High
Note: STK0 is the location addressed by the stack pointer

Table 2: Output and Internal Next-Cycle Register States for 2909/2911

Table 3 (Page 5) illustrates the execution of a subroutine using the 2909. The configuration of Figure 2 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also control (indirectly, perhaps) the four signals S0, S1, FE, and PUP. The starting address of the subroutine is applied to the D inputs of the 2909 at the appropriate time.

In the column on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the command "Jump to subroutine at A".

At the time T_2, this instruction is in the μWR, and the 2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J + 3 is pushed on to the stack. The return instruction is executed at T_5. Table 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
2909 inputs (from µWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	FE	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	µPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	-	-	-	J + 3	J + 3	J + 3	-	-		
	STK1	-	-	-	-	-	-	-	-		
	STK2	-	-	-	-	-	-	-	-		
	STK3	-	-	-	-	-	-	-	-		
2909 Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)	I(J + 5)		
Contents of µWR (instruction being executed)	µWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	RTS	I(J + 3)	I(J + 4)		

Table 3: Subroutine Execution

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J - 1	-
T_0	J	-
T_1	J + 1	-
T_2	J + 2	JSR A
T_6	J + 3	-
T_7	J + 4	-
	-	-
	-	-
	-	-
	-	-
	-	-
T_3	A	I(A)
T_4	A + 1	-
T_5	A + 2	RTS
	-	-
	-	-
	-	-
	-	-
	-	-
	-	-

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
2909 inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0	2	0
	FE	H	H	L	H	H	L	H	H	L	H
	PUP	X	X	H	X	X	L	X	X	L	X
	D	X	X	A	X	X	X	X	X	X	X
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	-	-	-	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	-
	STK1	-	-	-	-	-	-	J + 3	-	-	-
	STK2	-	-	-	-	-	-	-	-	-	-
	STK3	-	-	-	-	-	-	-	-	-	-
2909 Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A+ 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)	I(J + 4)
Contents of μWR (instruction being executed)	μWR	I(J)	I(J + 1)	JSR A	I(A)	I(A + 1)	JRS B	RTS	I(A + 3)	RTS	I(J + 3)

Table 4: Two Nested Subroutines

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J - 1	-
T_0	J	-
T_1	J + 1	-
T_2	J + 2	JSR A
T_9	J + 3	-
	-	-
	-	-
	-	-
	-	-
T_3	A	-
T_4	A + 1	-
T_5	A + 2	JSR B
T_7	A + 3	-
T_8	A + 4	RTS
	-	-
	-	-
	-	-
	-	-
T_6	B	RTS
	-	-

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-	20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Subgroup	Definition
1	Static characteristics specified in Table 7 at +25°C
2	Static characteristics specified in Table 7 at +125°C
3	Static characteristics specified in Table 7 at -55°C
7	Functional characteristics at +25°C
8a	Functional characteristics at +125°C
8b	Functional characteristics at -55°C
9	Switching characteristics specified in Tables 8, 9 and 10 at +25°C
10	Switching characteristics specified in Tables 8, 9 and 10 at +125°C
11	Switching characteristics specified in Tables 8, 9 and 10 at -55°C

Table 6: Definition of Subgroups

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{OH}	Output high voltage	V_{DD} = Min., I_{OH} = -2.6mA, V_{IN} = V_{IH} or V_{IL}	V_{DD} -0.5	-	V
V_{OL}	Output low voltage	V_{DD} = Max., I_{OL} = 16 mA, V_{IN} = V_{IH} or V_{IL}	-	0.5	V
V_{IH}	Input high level (Note 1)	Guaranteed input logical high voltage for all inputs	V_{DD}/2	-	V
V_{IL}	Input low level (Note 1)	Guaranteed input logical low voltage for all inputs	-	0.8	V
I_{IH}	Input high current	V_{IN} = V_{DD} (Note 3)	-	10	µA
I_{IL}	Input low current	V_{IN} = V_{SS} (Note 3)	-	-10	µA
I_{OZH}	Tristate high current	V_O = V_{DD} (Note 3)	-	50	µA
I_{OZL}	Tristate low current	V_O = V_{SS} (Note 3)	-	-50	µA
I_{DD}	Power supply current		-	10	mA

NOTES:
Mil-Std-883, Method 5005, Subgroups 1, 2, 3.
1. These input levels provide no guaranteed noise immunity and should only be static tested in a noise-free environment.
2. V_{DD} = 5V ±10%, over full operating temperature range.
3. Guaranteed but not tested at low temperatures.

Table 7: DC Operating Characteristics

Time	
Minimum clock low time	15
Minimum clock high time	15

Table 8: Cycle Time and Clock Charcteristics

From input	Y	$C_n + 4$
D_1	35	40
S_0, S_1	30	35
OR_I	20	30
C_n	-	25
ZERO	35	40
OE LOW (enable) (Note 2)	25	-
OE HIGH (disable) (Note 3)	25	-
Clock: S_1S_0 = LH	40	45
Clock: S_1S_0 = LL	40	45
Clock: S_1S_0 = HL	50	45

Notes:
1. CL < 50pF
2. RL ≥ 680Ω
3. RL ≥ 680Ω, measured 0.5V change in output level

Table 9: Maximum Combinational Propogation Delays

From input	Set-up time	Hold Time
RE	10	10
R_I	10	7
PUP	20	5
FE	20	10
C_n	15	5
D_I	20	0
OR_I	20	0
S_0, S_1	20	0
ZERO	25	0

Table 10: Guaranteed Set-up and Hold Times (all in ns)

All times in ns across full voltage and temperature range.
MIL-STD-883, method 5005, subgroups 9, 10 and 11.

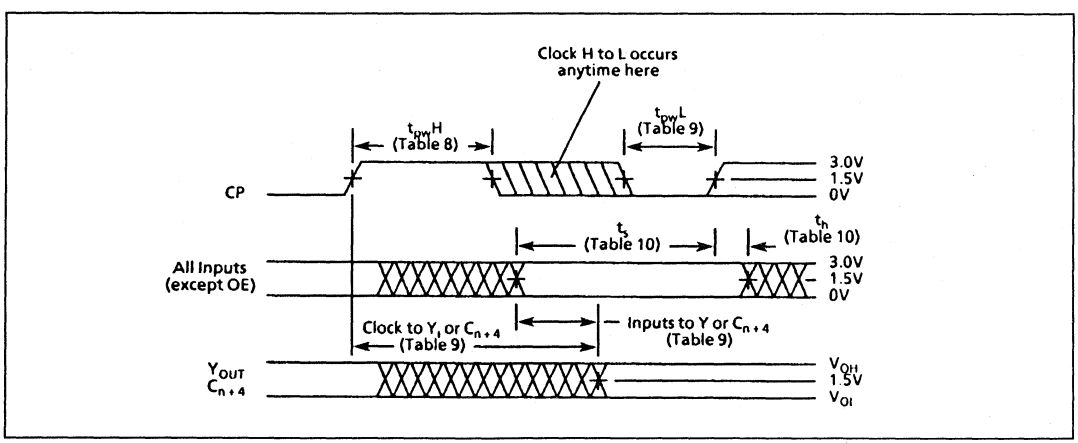


Figure 2

PACKAGE OUTLINES

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

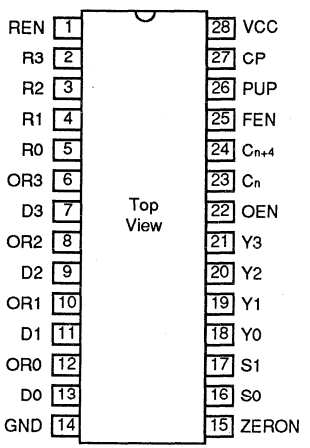


Figure 3: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.97	-	-	0.117
b	0.381	-	0.482	0.015	-	0.019
c	0.076	-	0.152	0.003	-	0.006
D	18.08	-	18.49	0.712	-	0.728
E	12.50	-	12.9	0.492	-	0.508
E2	9.45	-	9.85	0.372	-	0.388
e	1.143	-	1.40	0.045	-	0.055
L	8.00	-	9.27	0.315	-	0.365
Q	0.66	-	-	0.026	-	-
S	-	-	1.14	-	-	0.045

XG543

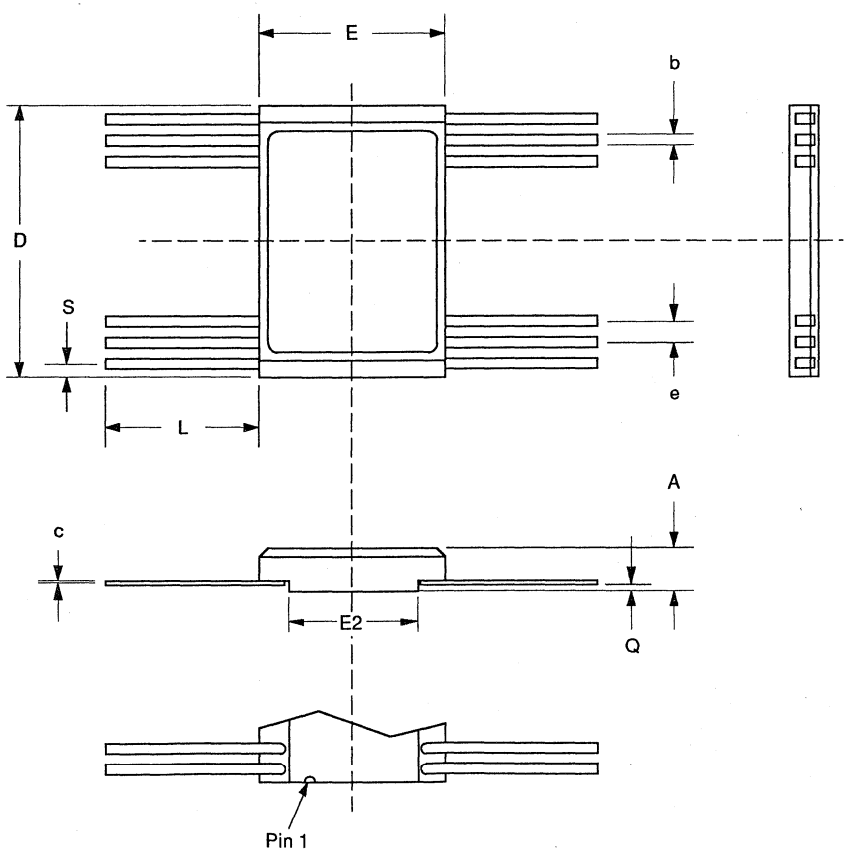


Figure 3: 28-Lead Dual Flatpack (Solder Seal) - Package Style C

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

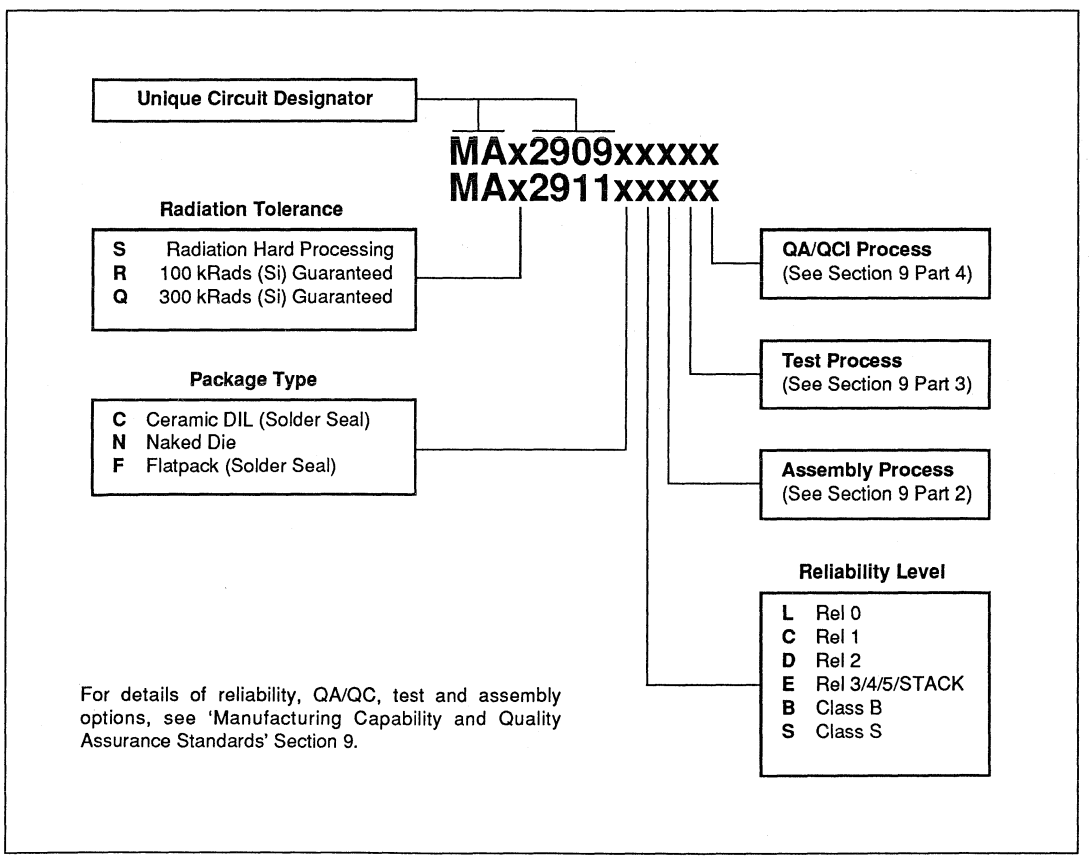
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 11: Radiation Hardness Parameters

ORDERING INFORMATION



MA2910

RADIATION HARD MICROPROGRAM CONTROLLER

The industry standard MA2910 Microprogram Controller forms part of the MA2900 family of devices.

Offering a building block approach to microcomputer and controller design, each device in the range is expandable permitting efficient emulation of any microcode-controlled machine. The family has been designed for operation in severe environments such as space, and is qualified to the highest levels of reliability.

The MA2910 Micro-program Controller is an address sequencer intended for sequence control of microinstructions stored in microprogram memory in high speed micro-processor applications.

All internal elements are full 12 bits wide and address up to 4096 words with one chip. The device has an integral settable 12 bit internal loop counter for repeating instructions and counting loop iterations.

The MA2910 has four address sources which allow Microprogram Address to be selected from the microgram counter, branch address bus, 9 level push/pop stack, or internal holding register.

The MA2910 supports 100ns cycle times and has an integral decoder function to enable external devices onto branch address bus which eliminates the requirement for an external decoder.

FEATURES

- Fully Compatible with Industry Standard 2910A
- CMOS SOS Technology
- Radiation Hard and High SEU Immunity
- High Speed / Low Power
- Fully TTL Compatible

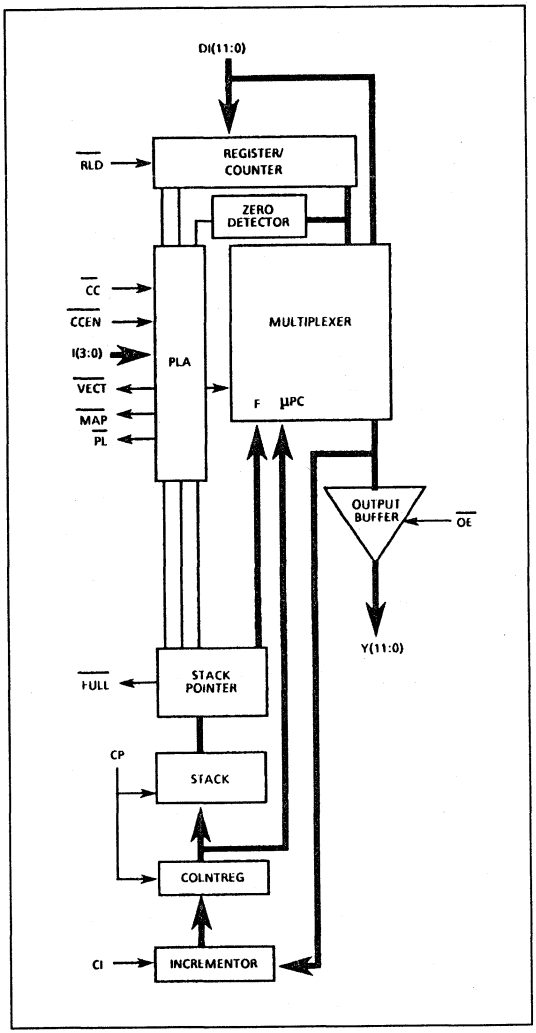


Figure 1: Block Diagram

OPERATION

The MA2910 is a SOS microprogram controller intended for use in high speed microprocessor applications. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range.

A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are nine nesting levels of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

The device is controlled by 16, 4-bit microinstructions. The PLA decodes the microinstructions on I(3:P) and produces select control codes for the multiplexer, register/counter, microprogram counter register, and stack. The 4-bit microinstructions also generate three active low enable signals ($\overline{PL}$, $\overline{VECT}$, and $\overline{MAP}$) for external use. The operation of each device block is detailed below:

MULTIPLEXER

The MA2910 contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

REGISTER/COUNTER

The register/counter consists of 12 D-type, edgetriggered flip-flops, with a common clock enable. It is operated during microinstructions (8,9,15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions.

The register/ counter is arranged such that if it is preloaded with a number N and is then used as a loop termination counter, the sequence will be executed exactly N+1 times. During instruction 15, a three way branch under combined control of the loop counter and the condition code is available. When its load control, RLD, is LOW, new data is loaded on the next positive control transition.

The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register /counter.

MICROPROGRAM COUNTER-REGISTER

The Microprogram Counter Register (μPC) is composed of a 12-bit incrementer followed by a 12-bit register. The (μPC) can be used in one of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded onto the next clock cycle with the current Y output word plus one (Y + 1 → μPC). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output unmodified so that the μPC is reloaded with the same Y word on the next clock cycle (Y → μPC). The same microinstruction is thus executed any number of times.

STACK AND STACK POINTER

The third source available at the multiplexer input is a 9-word by 12-bit stack. The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a POP.

Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever the stack is empty, the contents of the top of the stack are undefined until a push occurs. Any POPs performed while the stack is empty put undefined data on the outputs and leave the stack at zero.

The stack pointer operates as an up/down counter. During microinstructions 1,4, and 5, the PUSH operation may occur. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one.

PIN DESCRIPTIONS

VDD and GND (Power and Ground)

The MA2910 operates from a single supply voltage of 5V + 10%

D (0 to 11) (Direct input)

These connections provide direct input to the register/ counter, and the multiplexer. D0 is the least significant bit and D1 the most significant

I (0 to 3) (instruction bus)

The data on these inputs is read on the rising edge of CP. It determlnes the instruction to be executed in accordance with table 1.

$\overline{CC}$ (Condition Code)

This active low input is used to determine the result of conditional instructlon. LOW indicates a TRUE conditlon.

$\overline{CCEN}$ (Condition code enable)

This active low input enables the CC input. When CCEN is HIGH, CC is ignored and a conditional operation executed as though CC were LOW (TRUE).

$\overline{CI}$ (Carry input)

When HIGH this input causes the microprogramme counter register to increment on the rising edge of CP. When LOW the counter remains unchanged.

$\overline{RLD}$ (Register load)

This active low input loads the register/counter from the D bus on the rising edge of CP. It will override any HOLD or DEC instruction specified by data on the I bus.

Y (0 to 11) (Microcode address)

This is a 12 bit wide tristate output bus. It carries the microcode address generated according to the instruction read in from the I bus. OE can be used to put the bus in a high impedance state. This allows another to take control of the microcode address bus.

$\overline{OE}$ (Output enable)

This active low input is used to enable the 12 lines of the Y bus.

CP (Clock Pulse)

A LOW-to-HIGH transition on this input is used to trigger all state changes within the device.

$\overline{FULL}$ (stack full)

The active low output FULL indicates that 9 items have been loaded onto the stack .

$\overline{PL}$, $\overline{MAP}$ & $\overline{VECT}$ (pipeline, map and vector)

These active low outputs are set according to the instruction being executed. At any time only one is active.

They may be used to select from one of three possible external sources for microprogramme jumps, being used directly as three-state enables for these sources.

Typically: $\overline{PL}$ enables the primary source of microprogramme jumps, usually part of a pipeline register; $\overline{MAP}$ enables a PROM which maps an instruction to a microcode starting location; $\overline{VECT}$ enables an optional third source, after a vector from DMA or interrupt source.

I_3 - I_0	MNEMONIC	NAME	REGISTER /CONTROL	FAIL CCEN = LOW & CC = HIGH		PASS CCEN = HIGH & CC = LOW		REGISTER/ CONTROL	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	O	CLEAR	HOLD	PL
1	CJS	COND JS P PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL VECTOR	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP CNTR ≠ 0	≠ 0 = 0	F PC	HOLD POP	F PC	HOLD POP	DEC HOLD	PL PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠ 0 = 0	D PC	HOLD HOLD	D PC	HOLD HOLD	DEC HOLD	PL PL
10	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
11	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
12	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
13	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
14	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
15	TWB	THREE-WAY BRANCH	≠ 0 = 0	F D	HOLD PO P	PC PC	POP POP	DEC HOLD	PL P L

Note 1: If $\overline{CCEN}$ = LOW & $\overline{CC}$ = HIGH, hold, else load.

Figure 2: Table of Instructions

INSTRUCTION SET

The MA2910 provides 16 instructions which select the address of the next microinstruction to be executed. 4 of the instructions are unconditional and their effect depends only on the instruction. 10 of the instructions have an effect which is partially controlled by external conditions. 3 of the instructions have an effect which is partially controlled by the contents of the internal register/counter. In this discussion it is assumed the CI is tied HIGH.

In the 10 conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is it forces a pass.Other ways of using $\overline{CCEN}$ include; (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of MA2910 instruction bit I_0, which leaves instructions 4,6 and 10 as data-dependent but leaves others unconditional. All of these tricks save one bit of microcode width

The effect of three instructions depend upon the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected.These instructions are useful for executing a microinstruction loop a finite number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

The most effective technique for understanding the MA2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, examples of all 16 instructions are included.

The examples given should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed.

For example, the CONTINUE instruction (number 14) simply means that the contents of the microprogram memory word 50 are executed, then the contents of word 51 are executed. This is followed by the contents of 52 and 53 The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the following text will explain what the conditional choices are in each example.

Instruction 0: JZ (Jump to Zero, or Reset).

This instruction unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

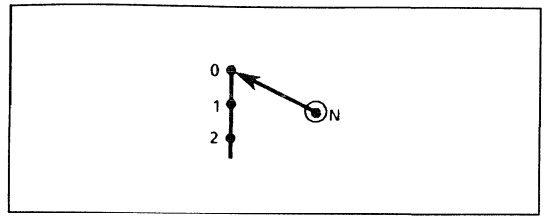


Figure 3: 0 JUMP ZERO (JZ)

Instruction 1: Conditional Jump-to-Subroutine.

This instruction is a conditional Jump-to-Subroutine via the address provided in the pipeline register. As shown in figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead.

Thus, the Conditional Jump-to-Subroutine instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the test input is such that the location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

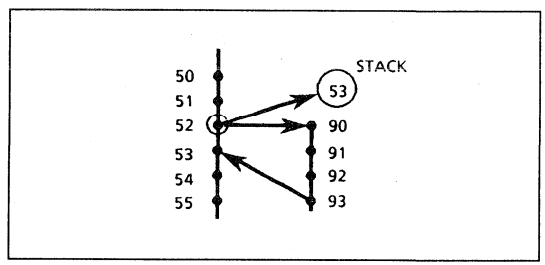


Figure 4: COND JSB PL (CJS)

Instruction 2: Jump-Map.

This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine.

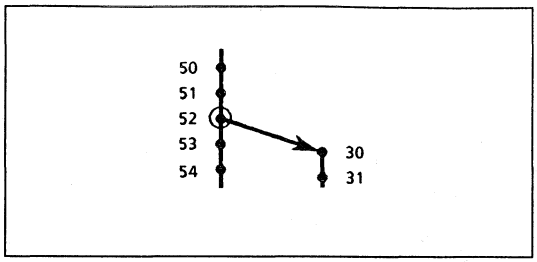


Figure 5: 2 JUMP MAP (JMAP)

In the example of Figure 5, microinstructions at locations 50,51, 52 and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed

Instruction 3: Conditional Jump Pipeline.

This instruction derives its branch address from the pipeline register branch address value (BR_0-BR_{11}). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some functions. This usually has the effect of resetting the input under test until some point in the future.

The example shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or 30, in this example. If the test is passed, the value currently in the pipeline register (30) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is location 53.

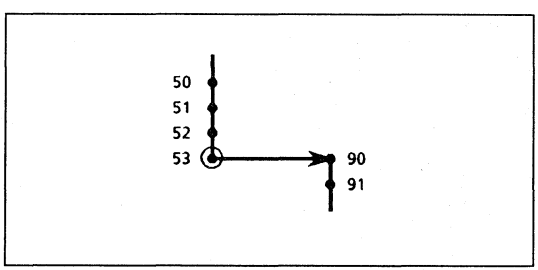


Figure 6: 3 COND JUMP PL (CLP)

Instruction 4: Push/Conditional, Load Counter.

This instruction is used primarily for setting up loops in microprogram firmware. In this example, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field.

Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will describe how to use the pushed value and the register/ counter for looping.

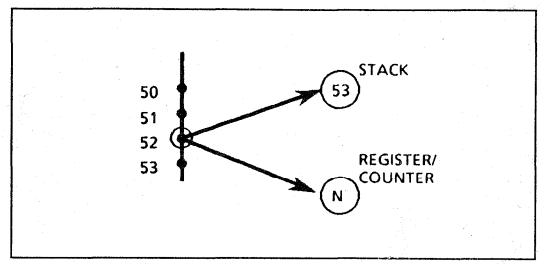


Figure 7: 4 PUSH/COND LD CNTR (PUSH)

Instruction 5: Conditional Jump-to-Subroutine.

This instruction is a Conditional Jump-to-Subroutine via the register/counter of the contents of the PIPELINE register. A PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A RETURN-FROM-SUBROUTINE (instruction number 10) returns the microprogram flow to address 55.

In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Lets assume that the branch address

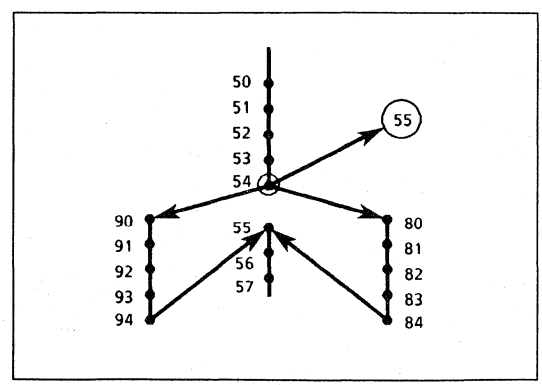


Figure 8: 5 COND JSB R/PL (JSRP)

fields of instruction 53 contain the value 90 so that it will be in the MA2910 register/counter when the contents of the address 54 are in the pipeline register.

This requires that the instruction at address 53 loads the register/counter. Now,during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value=90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value=80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6: Conditional Jump Vector.

This instruction provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the MA2910 output $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter.

In the example, if the Conditional Jump Vector instruction is contained at location 52, execution will continue at vector address 20 if the $\overline{CC}$ input is LOW and the microinstruction at address 53 will be executed if the $\overline{CC}$ input is HIGH.

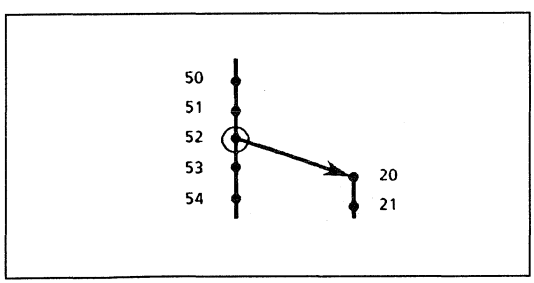


Figure 9: 6 COND JUMP VECTOR (CJV)

Instruction 7: Conditional Jump.

Conditional Jump via the contents of the MA2910 Register/ Counter or the contents of the Pipeline register. This instruction is very similar to instruction 5; the Conditional Jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7.

The example depicts this instruction as a branch to one of the two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 are being executed. As the contents of address 53 are clocked into the pipeline register, the value 70 is loaded into the register/counter in the MA2910. The value 80 is available when the contents of the address 53 are in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

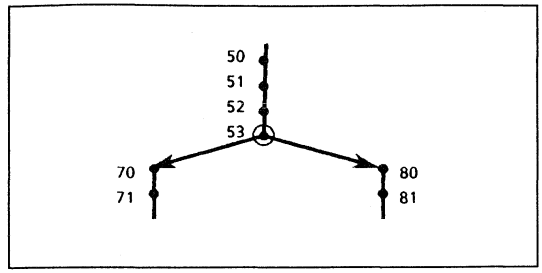


Figure 10: 7 COND JUMP R/PL (JRP)

Instruction 8: Repeat Loop, Counter ≠ Zero.

This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/ counter is decremented, and the address of the next microinstruction is taken from the top of the stack.

If the register/counter contains zero, the loop exit condition is occurring; control falls through to the next sequential microinstruction by selecting μPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

In this example, location 50 is most likely to have contained a Push/Conditional Load Counter instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop .

This method allows a loop to be executed 1 to 4096 times. If it desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

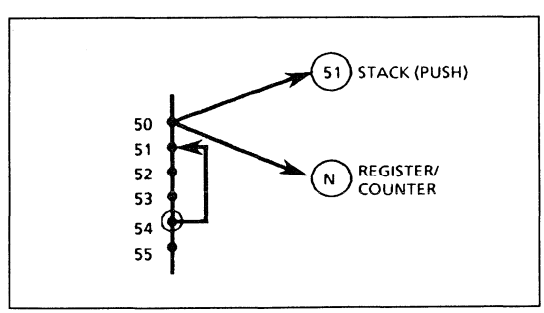


Figure 11: 8 ERPEAT LOOP, CNTR ≠ 0 (RFCT)

Instruction 9: Repeat Pipeline Register, Counter ≠ Zero

This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested nine deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In this example, the REPEAT PIPELINE, COUNTER J ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

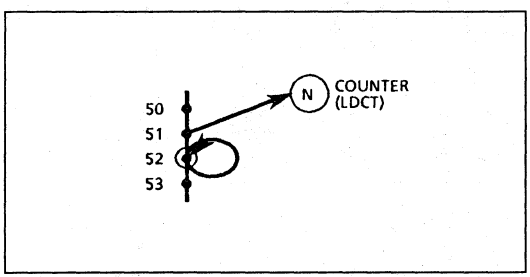


Figure 12: 9 REPEAT PL, CNTR ≠ 0 (RPCT)

Instruction 10: Conditional return form Subroutine.

As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed.

If the test is failed, the next sequential microinstruction is performed. This example depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes.

This example first shows a JUMP-TO-ROUTINE at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed, the program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force $\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

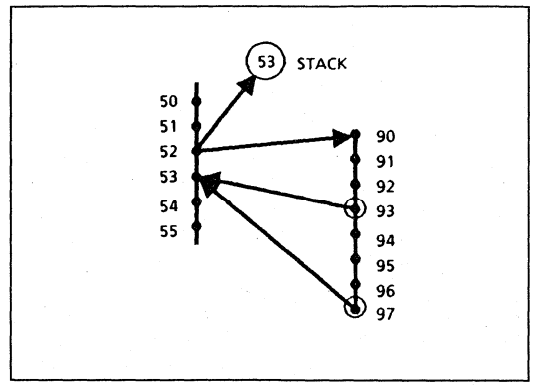


Figure 13: 10 COND RETURN (CRTN)

Instruction 11: Conditional Jump Pipeline register address and POP stack.

This instruction provides another technique for loop termination and stack maintenance. The example shows a loop being performed from address 55 back to address 51. The instructions at locations 52,53, and 54 are all conditional JUMP and POP instructions. At address 52, if the $\overline{CC}$ input is LOW, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55.

An instruction sequence as described here, using the Conditional Jump Pipeline and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level .

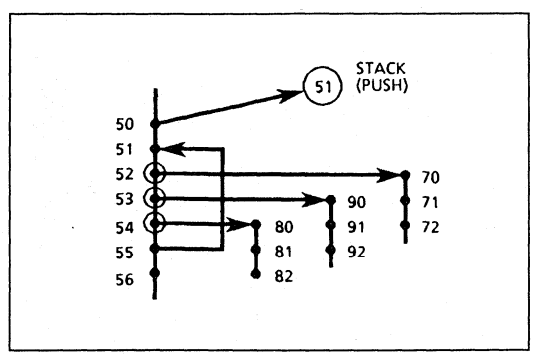


Figure 12: 9 REPEAT PL, CNTR ≠ 0 (RPCT)

Instruction 12: Load Counter and Continue.

This instruction simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed.

Altogether there are three ways of loading the counter: the explicit load by this instruction 12; the conditional load included as part of instruction 4; and use of $\overline{RLD}$ input along with any instructions.

The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width

Instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

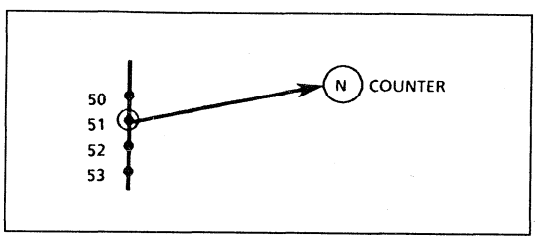


Figure 15: 12 LD CNTR & CONTINUE (LDCT)

Instruction 13: Test End-of-Loop.

This instruction provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop via the file if the test is failed, else to continue to the next sequential instruction.

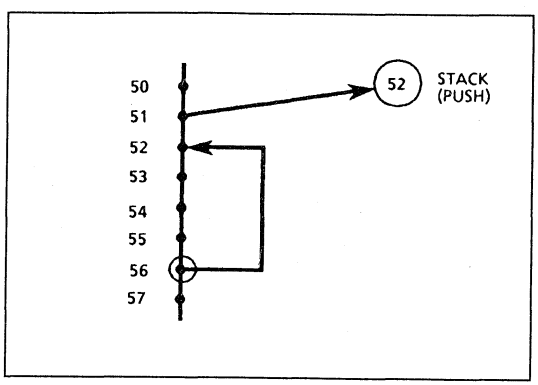


Figure 16: 13 TEST END LOOP (LOOP)

The example shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed which also causes the stack to be POP'd; thus accomplishing the required stack maintenance.

Instruction 14: CONTINUE.

This simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

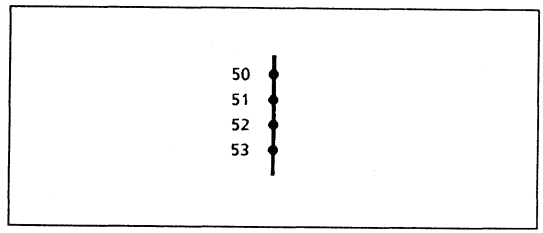


Figure 17: 14 CONTINUE (CONT)

Instruction 15: Three-Way-Branch.

This instruction is the most complex and provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack.

Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero. When the counter reaches zero the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken and the microprogram counter register furnishes the next address. When the loop is ended, either by a count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance: (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

As one example, consider the case of a memory search instruction. As shown, the instruction at microprogram address 63 can be instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before ending the search. Location 64 contains a microinstruction which fetches the next operand from the memory area being searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address.

When the count becomes zero, the microprogram branches to location 72, and carries out the instruction at location 72, if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles the case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once thus removing the value 64 from the top of the stack.

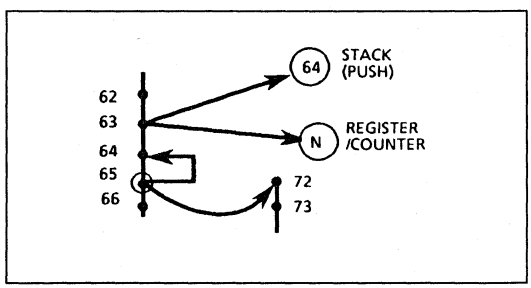


Figure 18: 15 THREE-WAY BRANCH (TWB)

ARCHITECTURE

ONE LEVEL PIPELINE BASED (RECOMMENDED)

One level pipeline provides better speed than most other architectures as the Microprogram Memory and the MA2901 array are in parallel paths.

This is the recommended architecture for all MA2900 designs.

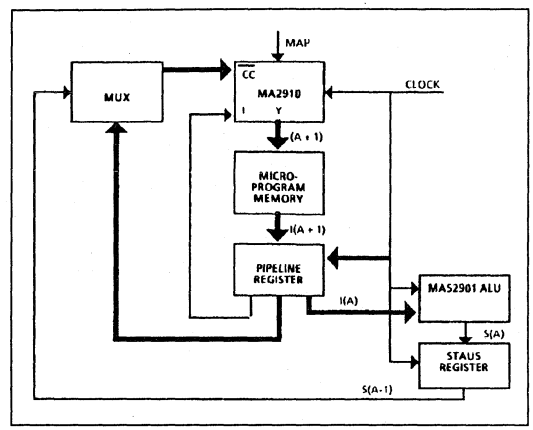


Figure 19a: One level Pipeline Based

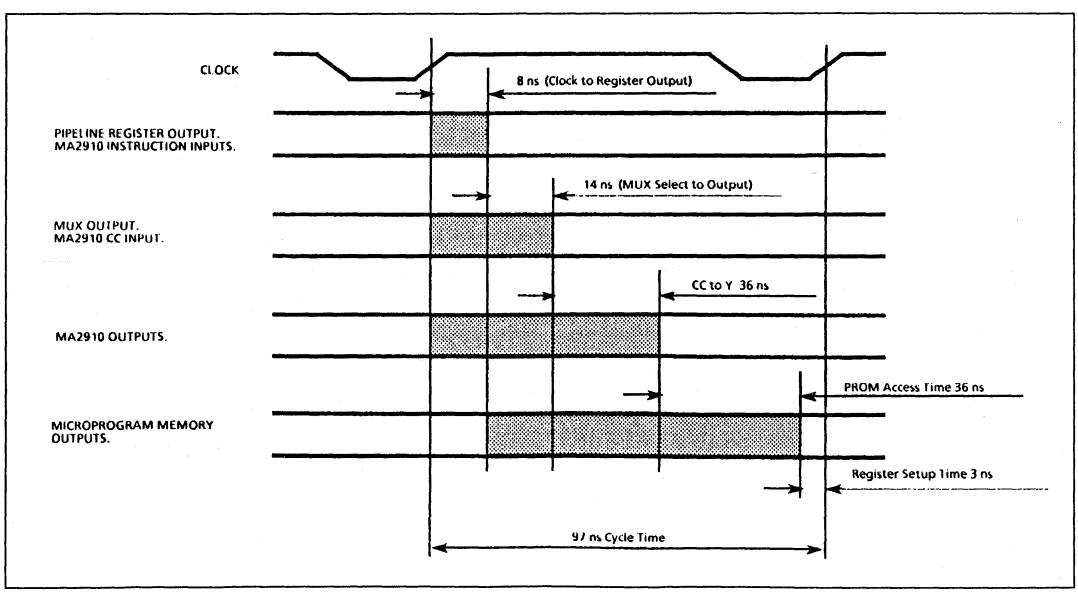


Figure 19b: Timing relationship in the CCU

Instruction Based

A Register at the Microprogram Memory output contains the microinstruction being executed. The Microprogram Memory and MA2901 delay are in series. Conditional branches are executed on the same cycle as the ALU operation generating the condition.

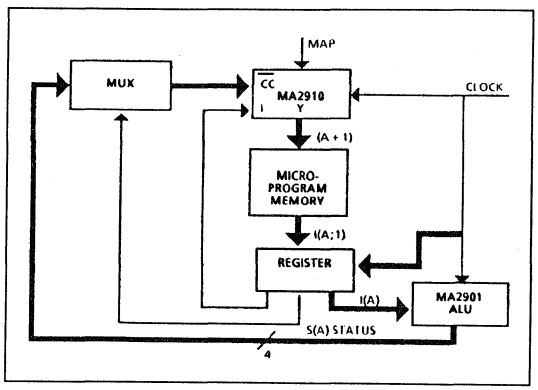


Figure 20: Instruction Based

Data Based

The Status Register provides conditional branch control based on results of the previous ALU cycle. The Microprogram memory and the MA2901 are in series within the critical path.

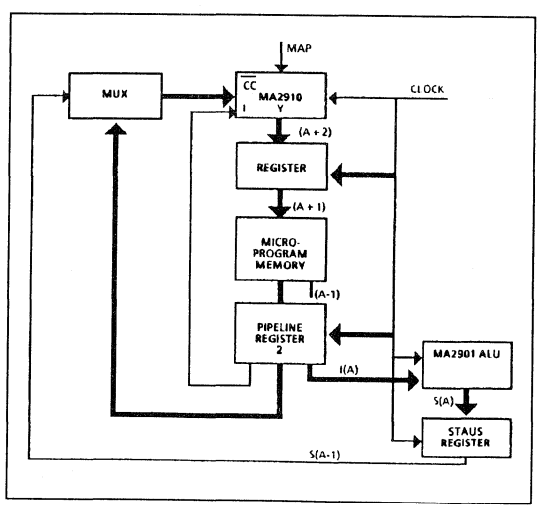


Figure 21: Data Based

Address Based

The Register at the MA2910 output contains the microinstruction being executed. The Microprogram Memory and MA2901 are in series within the critical path. This architecture is of comparable speed to the Instruction Based architecture, but requires fewer register bits, since only the address (typically 10 to 12 bits) is stored instead of the instruction.

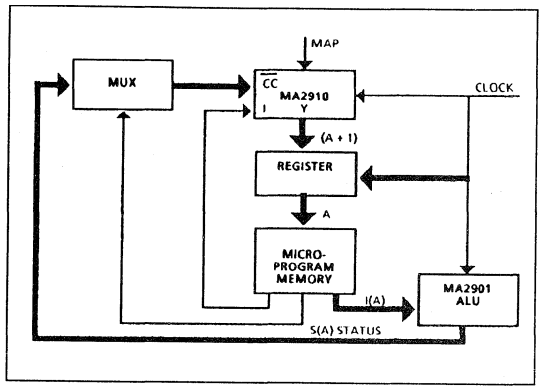


Figure 22: Address Based

Two Level pipeline Based

This architecture provides the highest possible speed. It is, however, more difficult to program as the selection of a microinstruction occurs two instructions ahead of its execution.

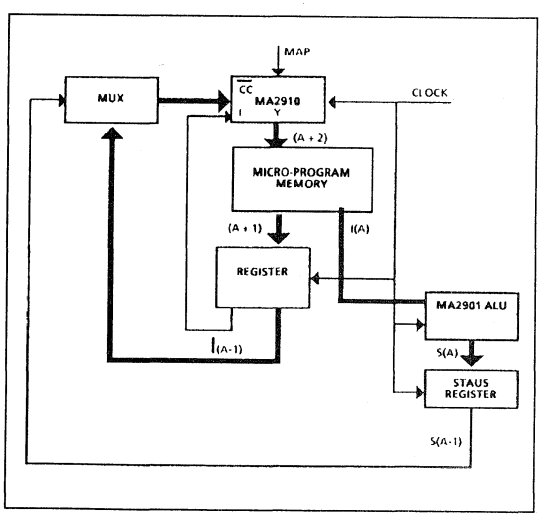


Figure 23: Two Level Pipeline Based

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 24: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Subgroup	Definition
1	Static characteristics specified in Figure 26 at +25°C
2	Static characteristics specified in Figure 26 at +125°C
3	Static characteristics specified in Figure 26 at -55°C
9	Switching characteristics specified in Figures 27 to 29 at +25°C
10	Switching characteristics specified in Figures 27 to 29 at +125°C
11	Switching characteristics specified in Figures 27 to 29 at -55°C

Figure 25: Definition of Subgroups

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad (Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply voltage	-	4 5	5.0	5 5	V
V_{IH}	Input high voltage	-	2.0	-	-	V
V_{IL}	Input low voltage	-	-	-	0 8	V
V_{OH}	Output high voltage	I_{OH} = -2mA	2.4	-	-	V
V_{OL}	Output low voltage	I_{OL} = 5mA	-	-	0.4	V
I_{IN}	Input leakage current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-	-	±10	µA
I_{OZ}	Tristate leakage current (Note 1)	V_{DD} = 5.5V, V_{IN} = V_{SS} Or V_{DD}	-	-	±50	µA
I_{DD}	Power supply current	Static, V_{DD} = 5.5V	-	0.1	10	mA

Mil-Std-883, method 5005, subgroups 1, 2, 3
V_{DD} = 5V ±10%, over full operating temperature range.
Note 1: Worst case at T_A = +125°C, guaranteed at T_A = -55°C. 300K Rad(Si) values at higher radiation levels are available on request.

Figure 26: Operating Electrical Characteristics

AC ELECTRICAL PARAMETERS

1. V_{DD} = 5V ±10%. C_{CL} = 50pF
2. Operating temperature is specified when ordering (see ordering information section on last page).
3. Enable/Disable times measured to 0.5V change on output voltage level with C_L = 50pF.
4. Time measurement Reference Level = 1.5 Volts.
5. Input Pulse = V_{SS} to 3.0 Volts.
6. Set-up and hold times measured relative to CP.

Input	t_s	t_h
Di → R	16	5
Di → PC	20	5
I_0-I_3	30	5
CC	35	0
CCEN	35	0
CI	15	5
RLD	15	5

Figure 27: Set-up and Hold Times

Minimum Clock LOW Time	20ns
Minimum Clock HIGH Time	35ns
Minimum Clock Period	55ns

Figure 28: Clock Requirements

Input	Y	PL, VECT, MAP	FULL
D_0-D_{11}	30	-	-
I_0-I_3	45	30	-
CC	45	-	-
CCEN	45	-	-
CP	60	-	32
OE Enable (Note 1)	25	-	-
OE Disable (Note 1)	25	-	-

Figure 29: Combinational Delays

Mil-Std-883, method 5005, subgroups 9, 10, 11

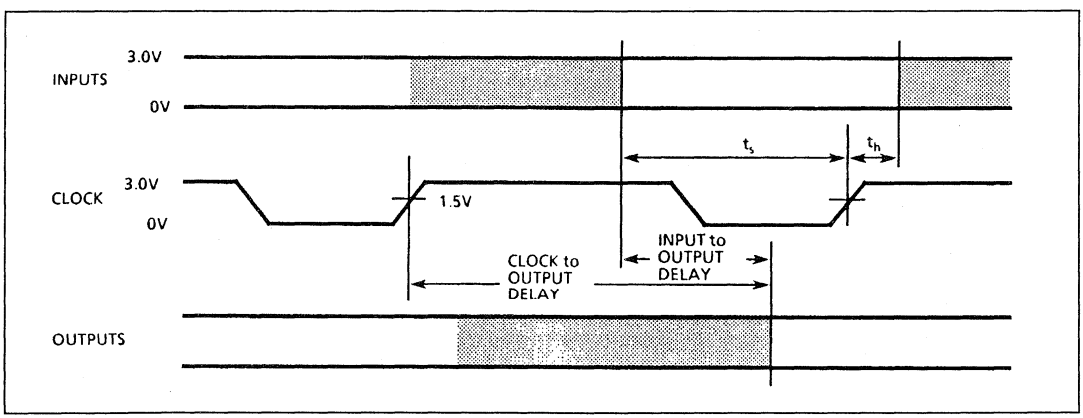
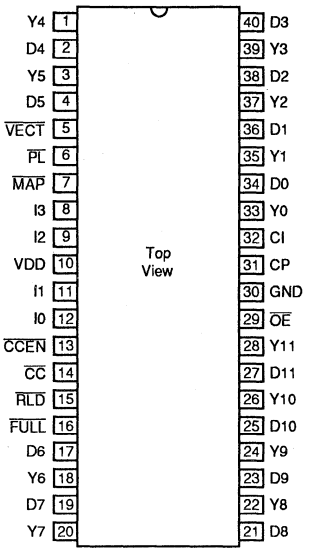


Figure 30: AC Timings

OUTLINES & PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	51.31	-	-	2.020
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG405



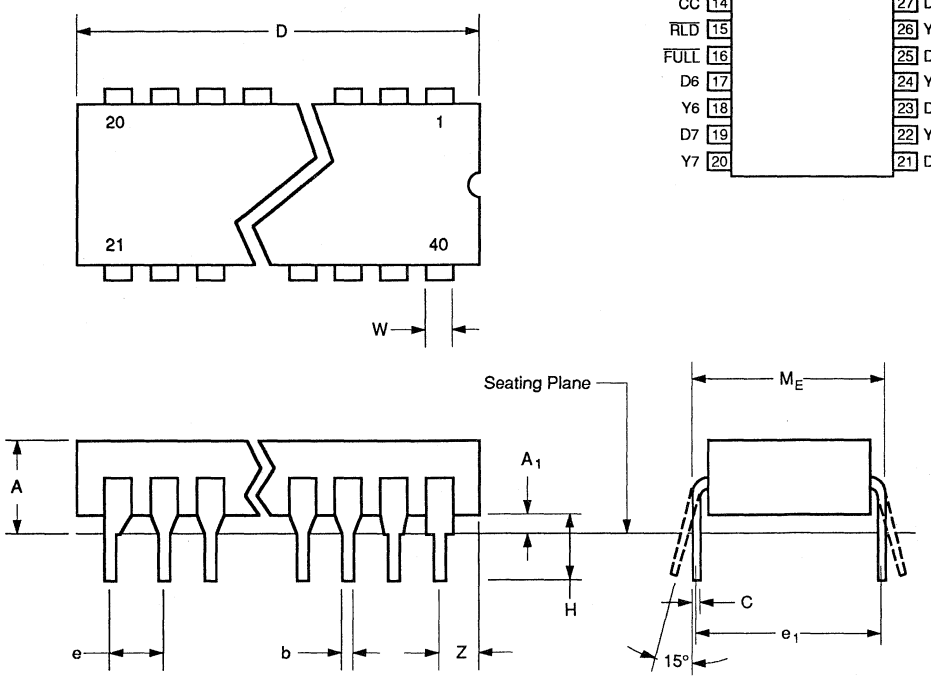


Figure 31: 40-Lead Ceramic DIL (Solder Seal) - Package Style C

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

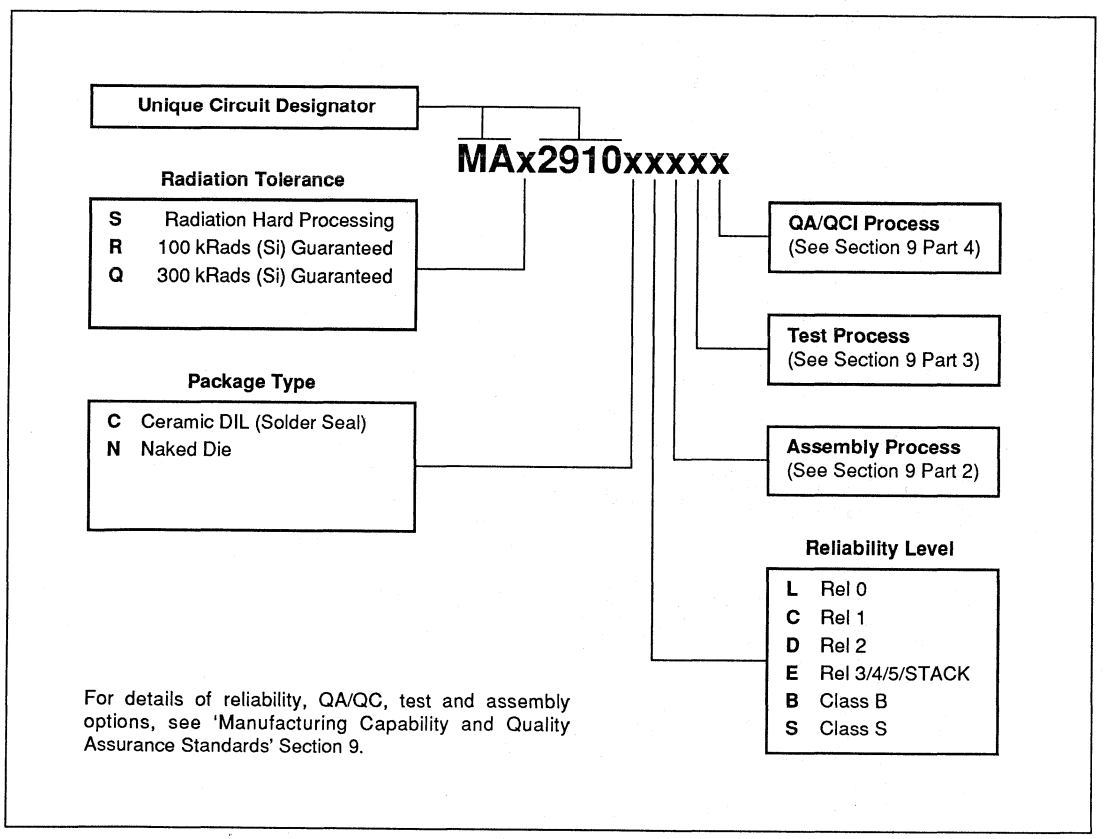
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 32: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

Section 4
Memories

GEC PLESSEY
SEMICONDUCTORS

OVERVIEW OF THE GPS RADIATION HARD 1.5μm CMOS/SOS SRAM RANGE

This product range represents the latest generation of radiation hard SRAMs from GEC Plessey Semiconductors offering very low operating power in conjunction with fast access times. The devices are fabricated in GPS's proven 1.5μm CMOS/SOS DLM process, which in conjunction with specialised circuit techniques gives the parts excellent radiation hardness.

This application note is intended to give users a better understanding of the internal workings of these devices, thus enabling them to obtain the optimum performance for any given application.

ARCHITECTURAL OVERVIEW

The GPS S1.5 SRAM range, in common with most modern SRAMs, is based on a self timed architecture with internal timing circuits triggered by transitions on the address or control lines. This architecture allows the device to offer the very low dynamic operating power necessary for many space applications whilst retaining a fast access time for the technology. A direct consequence of this architecture is that the device does not present a transparent route from the address inputs to the data outputs as was the case with earlier SRAM architectures. Although from a datasheet viewpoint the two architectures behave identically, it is useful to have a working knowledge of how an access sequence is timed internally in order to optimise the performance that can be obtained in any given system application. In addition this knowledge will allow the user to maximise their safety margins during the design phase.

OVERVIEW OF INTERNAL CONTROL CIRCUITRY

The generic block diagram for all the current S1.5 SRAM product range is illustrated in Figure 1. The architecture is essentially an asynchronous design, self timed from active transitions on the address or control lines. The basic functional elements are as follows. The address buffers generate A(n) and A(n) bar signals for each address input. Each buffer is enabled only when CS is active. In addition to the address signals an ATD(n) signal is also generated for each address input. This signal is pulsed active for a short period when any transition is detected on the buffer input. The CS buffer is similar but the transition detection pulse is only produced for high-to-low (active going) transitions. The transition detect summation block sums all the individual transition detect signals to produce a master transition detect signal (ATDSUM). Both row and column addresses are pre-decoded to minimise the address buffer loading and the number of series devices in the main decoders. The timing control block determines whether the device is in the precharge (equalised) or evaluation state. The device is set to the equalisation state by either an active transition or the cycle complete signal (PDBSAB) from the schmitt trigger. The cycle request latch is set by any active transition and reset when the cycle actually starts. The row decoder is a NAND based circuit which drives the selected wordline active. The dummy bitline is identical to the real bitline with each wordline being able to pull it low at approximately twice the rate of the normal ones. The dummy bitline voltage is monitored by the schmitt trigger to detect both valid read data and the equalisation completion time. The schmitt output is used to fire the senseamp and initiate equalisation ready for the next cycle. Once the senseamp has fired no further cycle requests are allowed to proceed until the equalisation is complete.

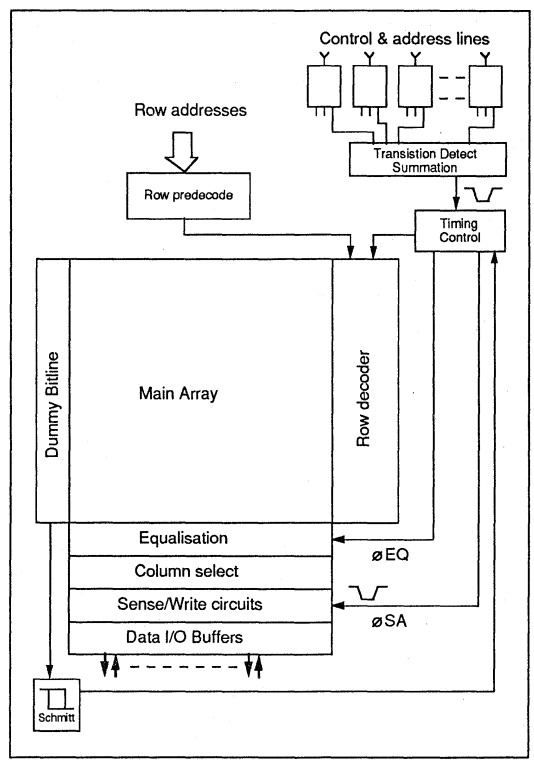


Figure 1: Block Diagram of Self Timed ATD Architecture

OPERATIONAL BENEFITS OF A SELF TIMED, ATD BASED ARCHITECTURE

By only activating circuitry on demand, the GPS architecture is able to offer very low power consumption even when active. This is because, much of the power consuming circuitry is only turned on for a very short period of time during each cycle. Thus even when the device is active during an extended cycle period (ie greater than the access time), power is only consumed during the short time when valid data is being accessed and latched into the output buffer. Once valid data has been latched the device automatically reverts to standby mode until the next active transition is detected. This obviates the need for any external power reduction circuitry to de-select the device once the data has been acknowledged by the rest of the system. This can be very useful in the many applications where the device is actually running at a cycle time significantly greater than the datasheet value for safety margin reasons.

An additional benefit of the self timed architecture is the ability to place the precharge time at the back end of the previous cycle. This is achieved by starting the precharge period as soon as the sense-amplifier has been fired. Thus in the period between the sense amplifier being fired and the valid data appearing on the D_{OUT} pin(s) the device internal nodes are being returned to their precharge state ready for the next cycle. This will result in a faster access time for cycles where the pre-charge has been allowed to complete before the next cycle starts. Because the specification places no limitation on the arrival times of the address and control signals this condition cannot be guaranteed in all possible system applications and therefore the datasheet timings are based on the assumption that precharge is not complete. However by ensuring that each cycle starts with pre-charge complete a 20% reduction in access time can be obtained.

CONSEQUENCES OF USING A SELF TIMED ARCHITECTURE

Whilst this architecture retains the same ease of use traditionally associated with fully asynchronous SRAMs there are some basic guide-lines that should be followed to ensure correct operation.

When an active transition is detected the evaluate phase is entered and the device begins to access the data requested. If another transition is detected before the cycle has run to completion then the device must take account of the change in input signals. How this is achieved depends on the actual separation in time of the received transitions.

Because most systems will have some small amount of address skew there is a short period provided, typically 5nS, before a transition detected will be allowed to start the evaluation cycle. Thus any further transitions received during that period merely have the effect of extending the master summation detect (ATDSUMB) pulse until all address and control signals have been stable for about 5nS. In this case only one cycle is produced and it starts about 5nS after the last transition detected. The access time achieved will still be that associated with pre-charge being complete at cycle start.

If however the separation between the transitions is greater than about 5nS then the evaluate cycle will have started when the second transition is detected. The first cycle is aborted and the circuit returns to the pre-charge state before starting again with the new address. In this case the access time measured will now include the amount of time required to return the internal nodes to their pre-charged state before allowing the second cycle to start. This extra period will be at a maximum when the first cycle is aborted just prior to the internal cycle being terminated by the dummy bitline reaching the schmitt threshold. This is the case when the internal nodes have the greatest voltage differential with the pre-charge state. If the transition is detected close to this point then the sense-amplifier may still be fired and therefore the D_{OUT} value will go invalid until the second cycle completes. This is indicated on the datasheet.

Finally there is the case where the transitions are separated by so long a period that the sense-amplifier has already been fired from the first cycle but valid data has not yet appeared on the D_{OUT} pin. In this case the pre-charge period has already been started by the first cycle and the second cycle is simply held until pre-charge has completed and data from the first cycle latched out onto the D_{OUT} pin.

By being aware of these factors the system designer can ensure that their application operates with the greatest possible safety margin.

MA5104

RADIATION HARD 4096 x 1 BIT STATIC RAM

The MA5104 4k Static RAM is configured as 4096 x 1 bits and manufactured using CMOS-SOS high performance, radiation hard, 3μm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the HIGH state.

Operation Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Read	L	H	D OUT	ISB1
Write	L	L	D IN	
Standby	H	X	High Z	ISB2

Figure 1: Truth Table

FEATURES

- 3μm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 90ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{10}$ Rad(Si)/sec
- SEU $<10^{-10}$ Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 10μA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation

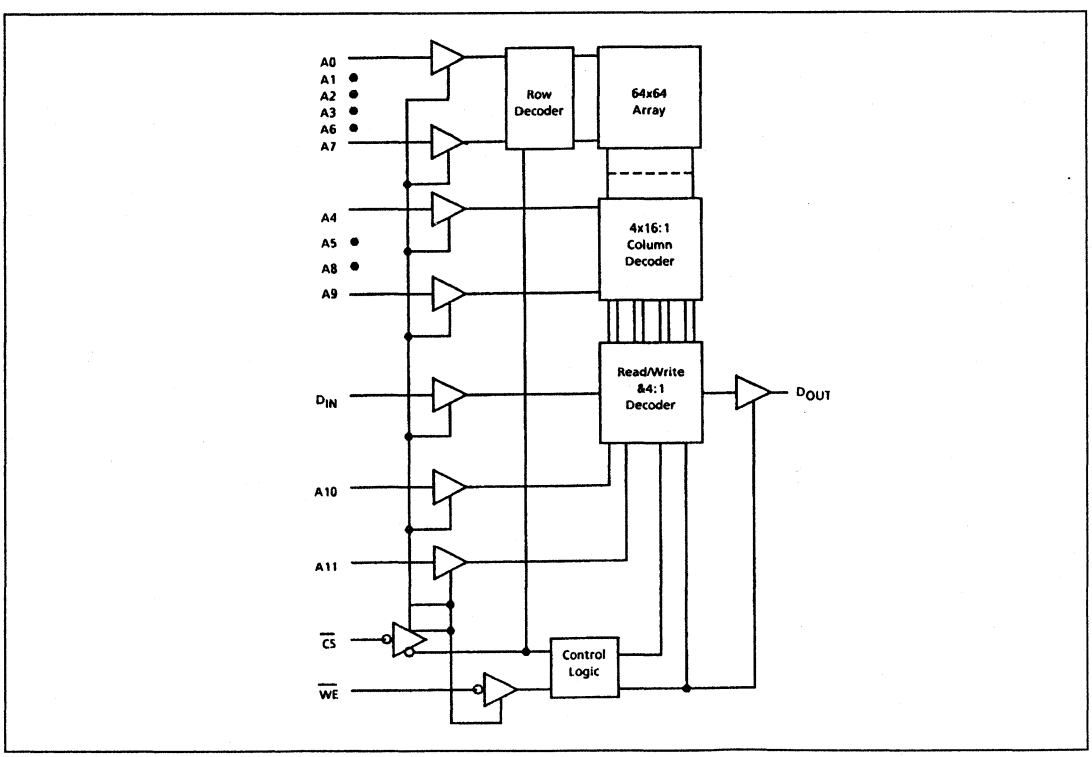


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
1. Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request).
2. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	V_{DD}/2	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output High Voltage	I_{OH1} = -1mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input Leakage Current (note 2)	All inputs except $\overline{CS}$	-	-	±10	µA
I_{LO}	Output Leakage Current (note 2)	Output disabled, V_{OUT} = V_{SS} or V_{DD}	-	-	±20	µA
I_{PUI}	Input Pull-Up Current	V_{IN} = V_{SS} on $\overline{CS}$ input only	-	-	-100	µA
I_{PDI}	Input Leakage Current	V_{IN} = V_{SS} on $\overline{CS}$ input only	-	-	5	µA
I_{DD}	Power Supply Current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	12	16	mA
I_{SB1}	Selected Supply Current	$\overline{CS}$ = V_{SS}	-	25	35	mA
I_{SB2}	Standby Supply Current	Chip disabled	-	50	3000	µA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	30	2000	µA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Transition is measured at ±500mV from steady state.
4. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
T_{AVAVR}	Read Cycle Time	135	-	ns
T_{AVQV}	Address Access Time	-	135	ns
T_{ELQV}	Chip Select to Output Valid	-	135	ns
T_{ELQX} (4)	Chip Select to Output Active	10	-	ns
T_{ELQZ} (4)	Chip Select to Output Tri State	10	50	ns
T_{AXQX}	Output Hold from Address Change	10	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVAVW}	Write Cycle TIme	135	-	ns
T_{AVWL}	Address Set Up Time	10	-	ns
T_{WLWH}	Write Pulse Width	50	-	ns
T_{WHAV}	Write Recovery Time	5	-	ns
T_{DVWH}	Data Set Up Time	35	-	ns
T_{NHDX}	Data Hold Time	5	-	ns
T_{WLQZ} (4)	Write Enable to Output Tri State	10	50	ns
T_{ELWL}	Chip Selection to Write Low	25	-	ns
T_{ELWH}	Chip Selection to End of Write	85	-	ns
T_{AVWH}	Address Valid to End of Write	80	-	ns
T_{WHQX} (4)	Output Active from End to Write	5	-	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

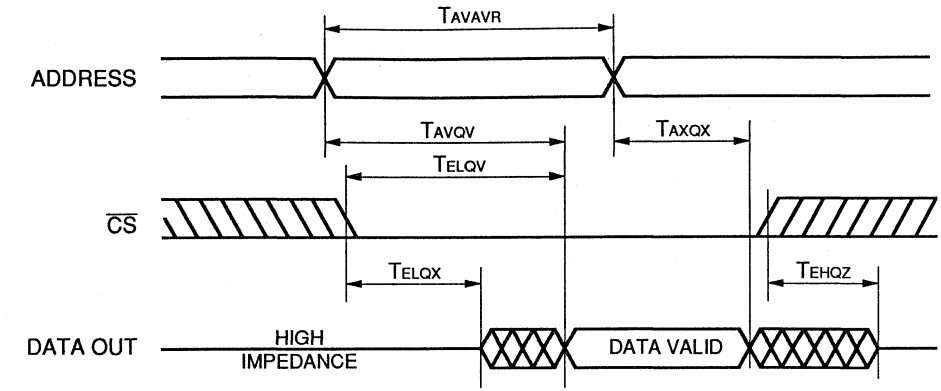
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

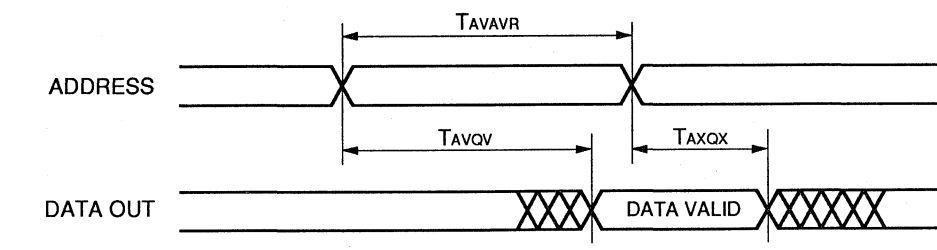
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



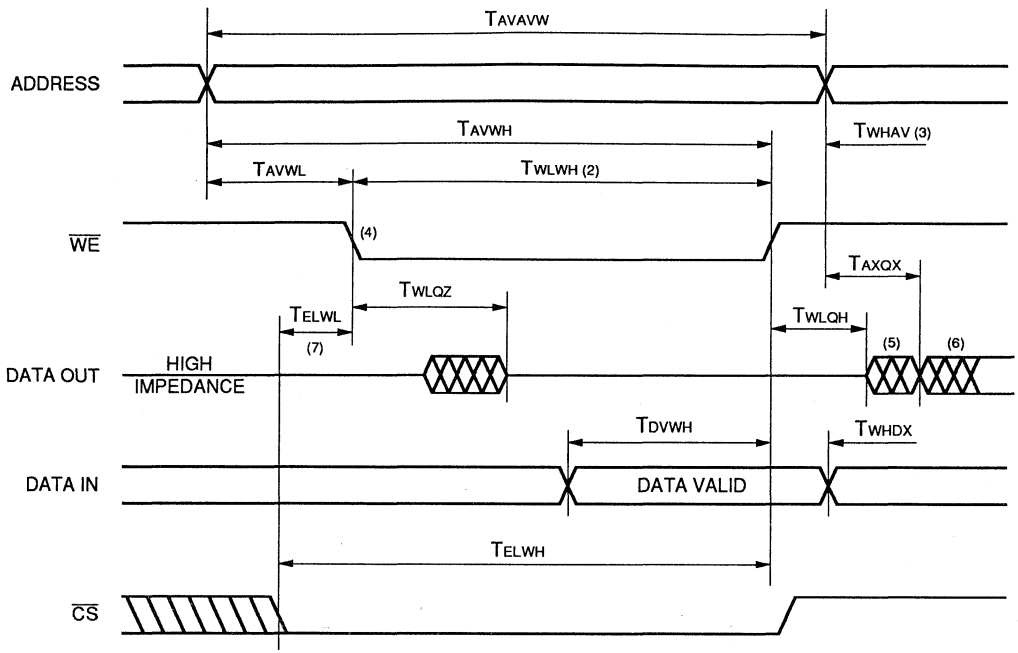
1. $\overline{WE}$ is high for Read Cycle.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.

Figure 11a: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$ low.

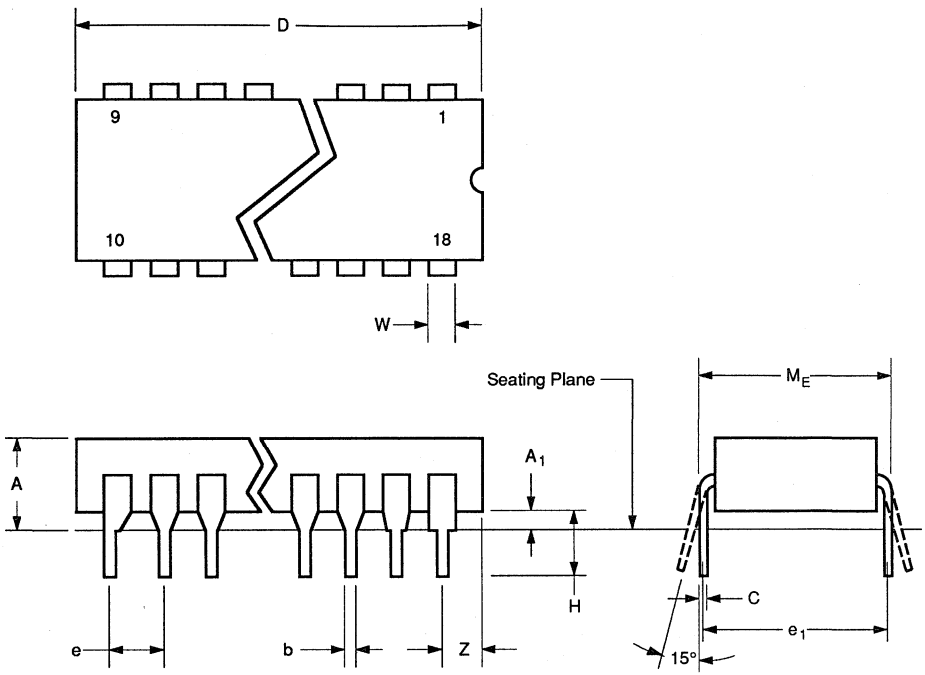
Figure 11b: Read Cycle 2



1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$, a high CE and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high or CE going low, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is the write data of the current cycle, if selected.
6. DATA OUT is the read data of the next address,if selected.
7. T_{ELWL} must be met to prevent memory corruption.

Figure 12: Write Cycle

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	23.11	-	-	0.910
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	8.13 Typ.	-	-	0.300 Typ.	-
H	4.44	-	5.38	0.175	-	0.212
Me	-	-	8.28	-	-	0.326
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG406

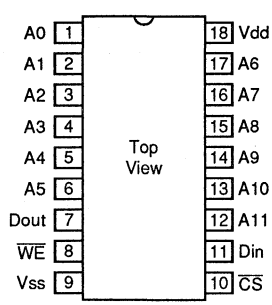
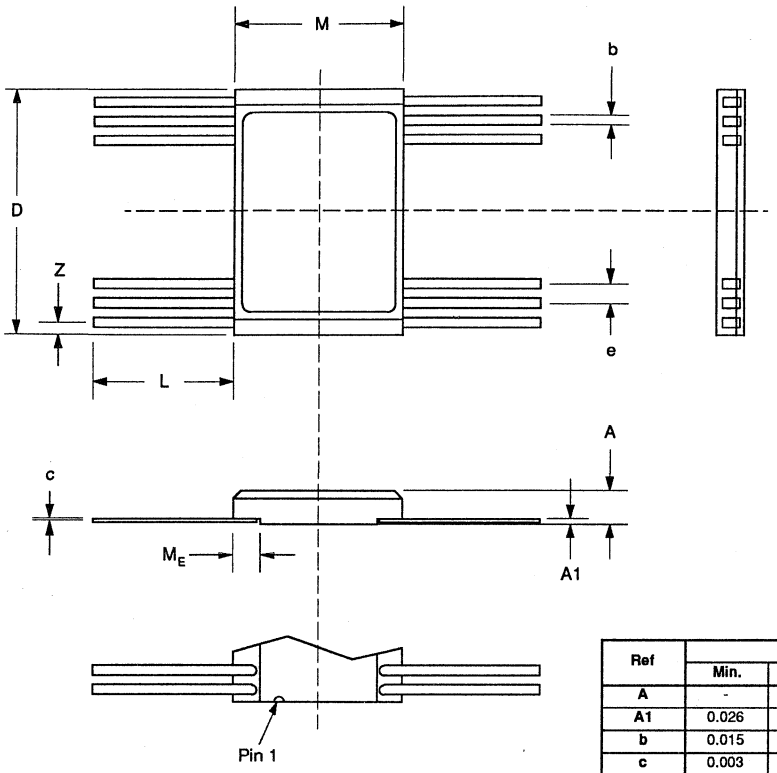


Figure 13: 18-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Inches		
	Min.	Nom.	Max.
A	-	-	0.105
A1	0.026	-	-
b	0.015	-	0.019
c	0.003	-	0.006
D	0.590	-	0.610
e	-	0.050	-
L	0.265	-	0.305
M	0.395	-	0.405
Me	0.30	-	-
Z	0.005	-	0.045

XG537

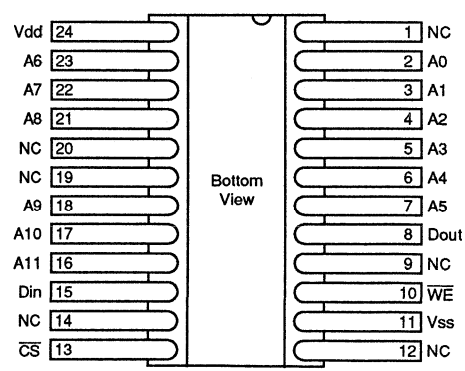


Figure 14: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F

Function	Package Option		Via	Burnin			Radiation
	F	C		Static 1	Static 2	Dynamic	
A0	2	1	R	0V	5V	F0	5V
A1	3	2	R	0V	5V	F1	5V
A2	4	3	R	0V	5V	F2	5V
A3	5	4	R	0V	5V	F3	5V
A4	6	5	R	0V	5V	F4	5V
A5	7	6	R	0V	5V	F5	5V
DOUT	8	7	R	0V	5V	LOAD	5V
WEB	10	8	R	0V	5V	F12	5V
VSS	11	9	Direct	0V	0V	0V	0V
CSB	13	10	R	0V	5V	0V	5V
DIN	15	11	R	0V	5V	F13	5V
A11	16	12	R	0V	5V	F11	5V
A10	17	13	R	0V	5V	F10	5V
A9	18	14	R	0V	5V	F9	5V
A8	21	15	R	0V	5V	F8	5V
A7	22	16	R	0V	5V	F7	5V
A6	23	17	R	0V	5V	F6	5V
VDD	24	18	Direct	5V	5V	5V	5V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Burnin R=1k
3. Radiation R=10k

Figure 15: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$3.4x10^{-9}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 16: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

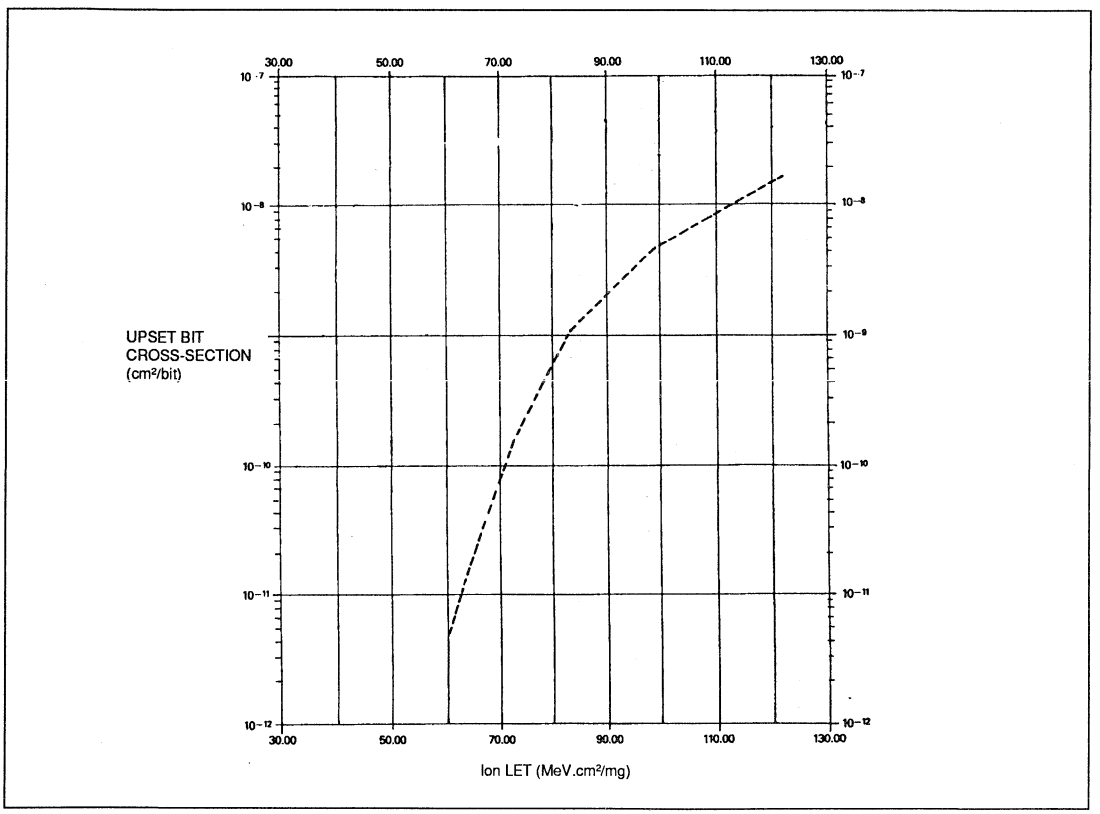
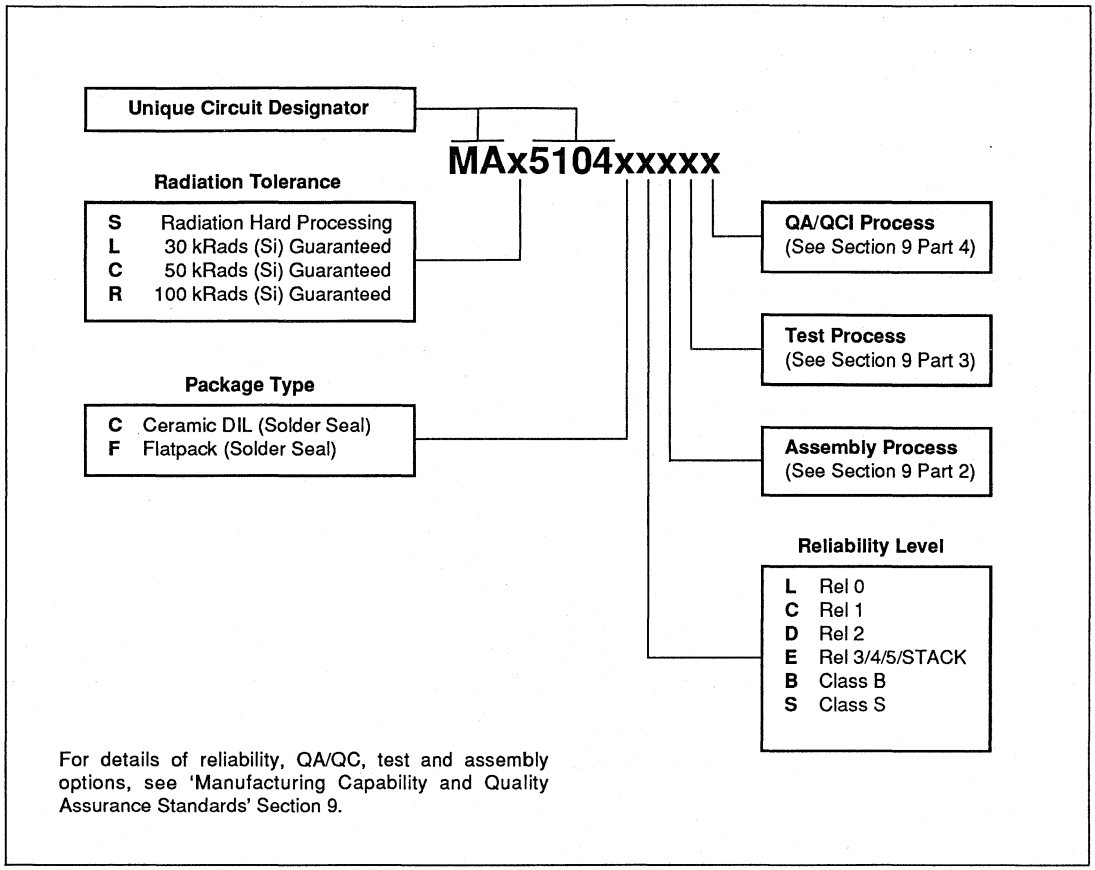


Figure 17: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3581-3.1

MA5114

RADIATION HARD 1024 x 4 BIT STATIC RAM

The MA5114 4k Static RAM is configured as 1024 x 4 bits and manufactured using CMOS-SOS high performance, radiation hard, 3μm technology.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the HIGH state.

Operation Mode	$\overline{CS}$	$\overline{WE}$	I/O	Power
Read	L	H	D OUT	ISB1
Write	L	L	D IN	
Standby	H	X	High Z	ISB2

Figure 1: Truth Table

FEATURES

- 3μm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 90ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{10}$ Rad(Si)/sec
- SEU $<10^{-10}$ Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 50μA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Data Retention at 2V Supply

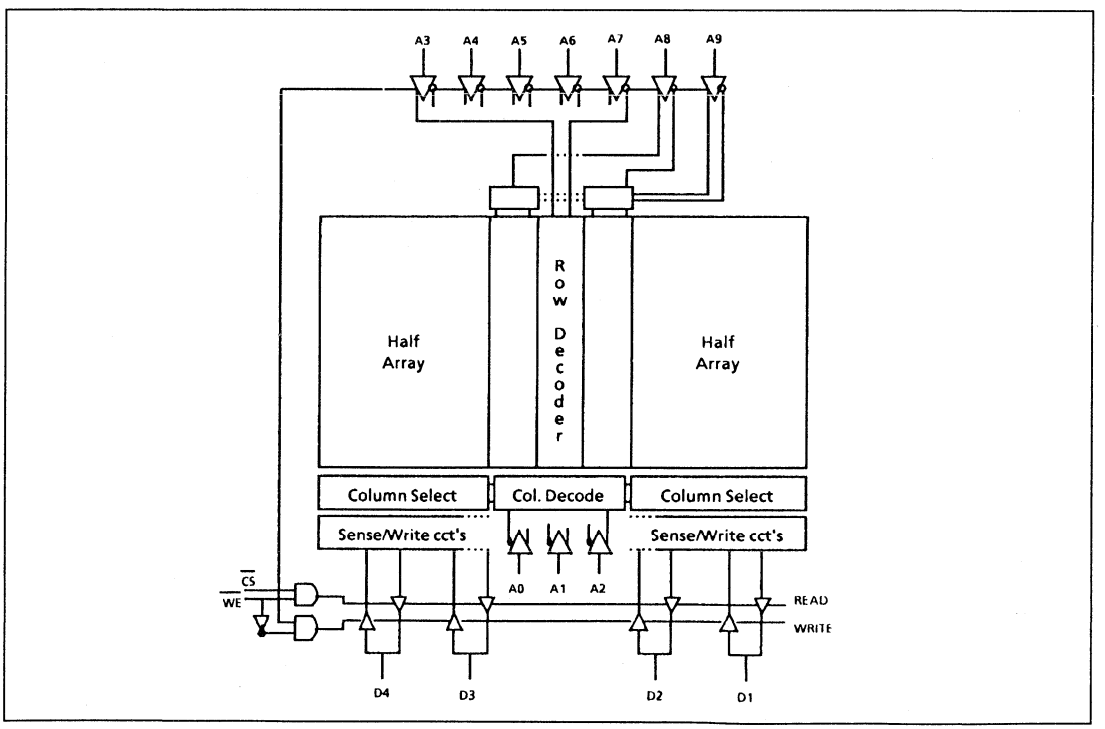


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functlonal operation of the device at these condltions, or at any other condition above those indicated in the operations section of this specification, is not Implied Exposure to absolute maxlmum rating conditions for extended perlods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
1. Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request).
2. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	$V_{DD}/2$	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output High Voltage	I_{OH1} = -1mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 2mA	-	-	0.4	V
I_{LI}	Input Leakage Current (note 2)	All inputs except $\overline{CS}$	-	-	±10	µA
I_{LO}	Output Leakage Current (note 2)	Output disabled, V_{OUT} = V_{SS} or V_{DD}	-	-	±20	µA
I_{PUI}	Input Pull-Up Current	V_{IN} = V_{SS} on $\overline{CS}$ input only	-	-	-100	µA
I_{PDI}	Input Leakage Current	V_{IN} = V_{SS} on $\overline{CS}$ input only	-	-	5	µA
I_{DD}	Power Supply Current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space-	12	16	mA	
I_{SB1}	Selected Supply Current	$\overline{CS}$ = V_{SS}	-	25	35	mA
I_{SB2}	Standby Supply Current	Chip disabled	-	50	3000	µA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	30	2000	µA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Transition is measured at ±500mV from steady state.
4. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
T_{AVAVR}	Read Cycle Time	135	-	ns
T_{AVQV}	Address Access Time	-	135	ns
T_{ELQV}	Chip Select to Output Valid	-	135	ns
T_{ELQX} (3,4)	Chip Select to Output Active	10	-	ns
T_{ELQZ} (3,4)	Chip Select to Output Tri State	10	50	ns
T_{AXQX}	Output Hold from Address Change	10	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
T_{AVAVW}	Write Cycle Time	135	-	ns
T_{AVWL}	Address Set Up Time	10	-	ns
T_{WLWH}	Write Pulse Width	50	-	ns
$T_{\overline{WH}AV}$	Write Recovery Time	5	-	ns
T_{DVWH}	Data Set Up Time	35	-	ns
T_{NHDX}	Data Hold Time	5	-	ns
T_{WLQZ} (3,4)	Write Enable to Output Tri State	10	50	ns
T_{ELWL}	Chip Selection to Write Low	25	-	ns
T_{ELWH}	Chip Selection to End of Write	85	-	ns
T_{AVWH}	Address Valid to End of Write	80	-	ns
T_{WHQX} (3,4)	Output Active from End to Write	5	-	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	8	12	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

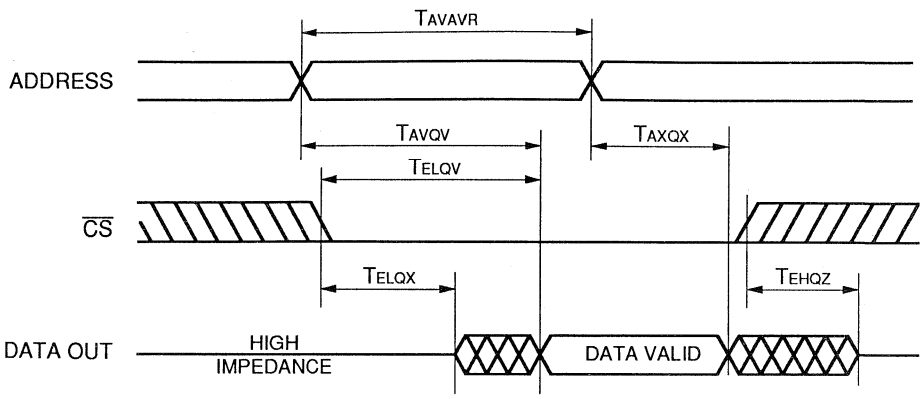
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

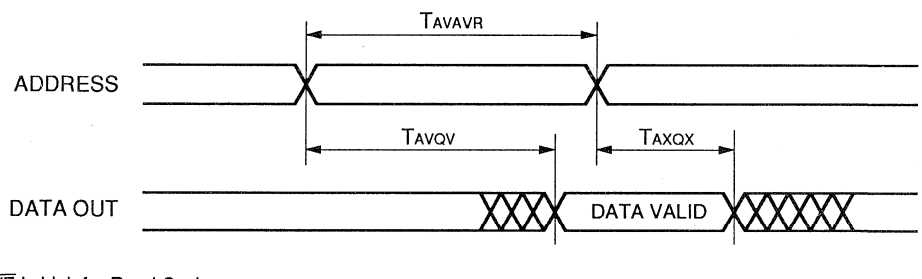
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



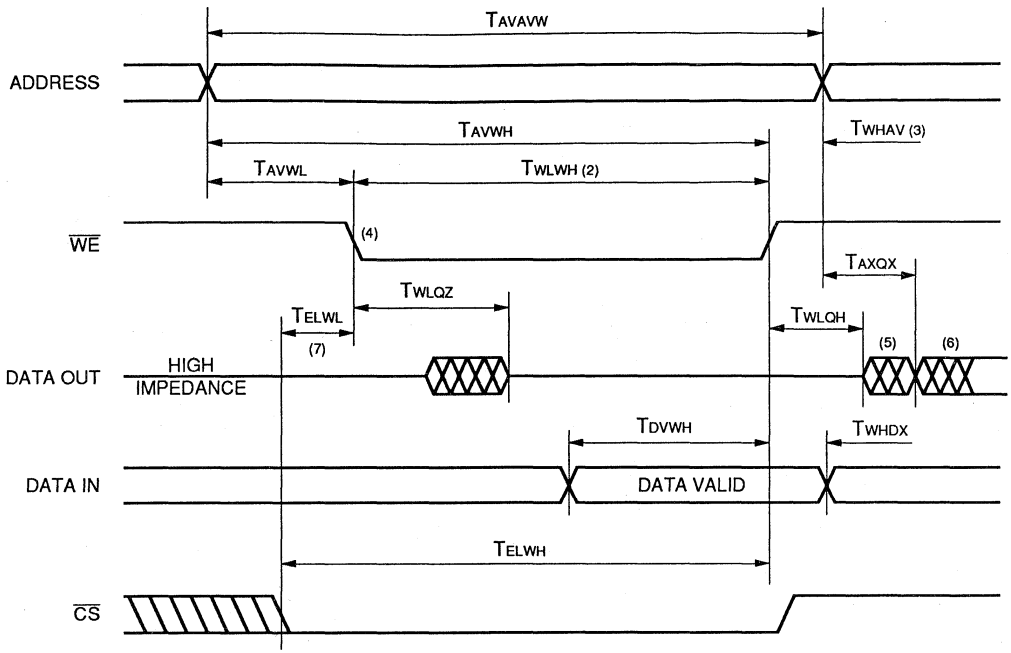
1. $\overline{WE}$ is high for Read Cycle.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.

Figure 11a: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$ low.

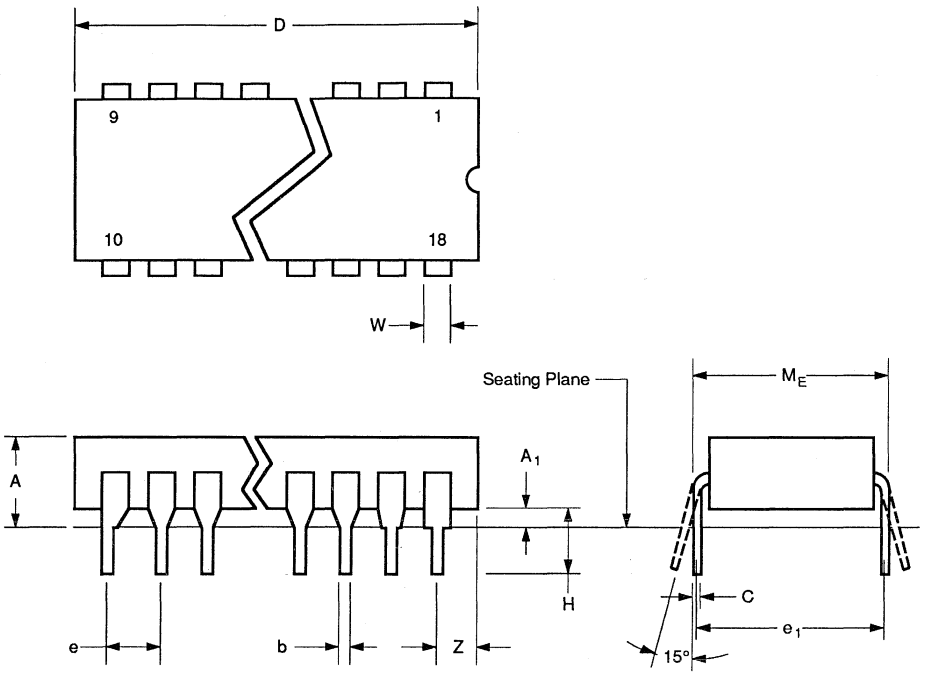
Figure 11b: Read Cycle 2



1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is in the active state, so DATA IN must not be in opposing state.
6. DATA OUT is the write data of the current cycle, if selected.
7. DATA OUT is the read data of the next address, if selected.
8. T_{ELWL} must be met to prevent memory corruption.

Figure 12: Write Cycle

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	23.11	-	-	0.910
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	8.13 Typ.	-	-	0.300 Typ.	-
H	4.44	-	5.38	0.175	-	0.212
Me	-	-	8.28	-	-	0.326
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG406

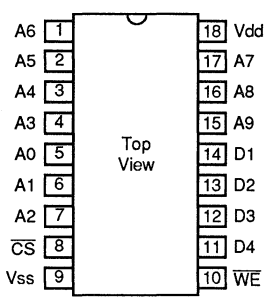
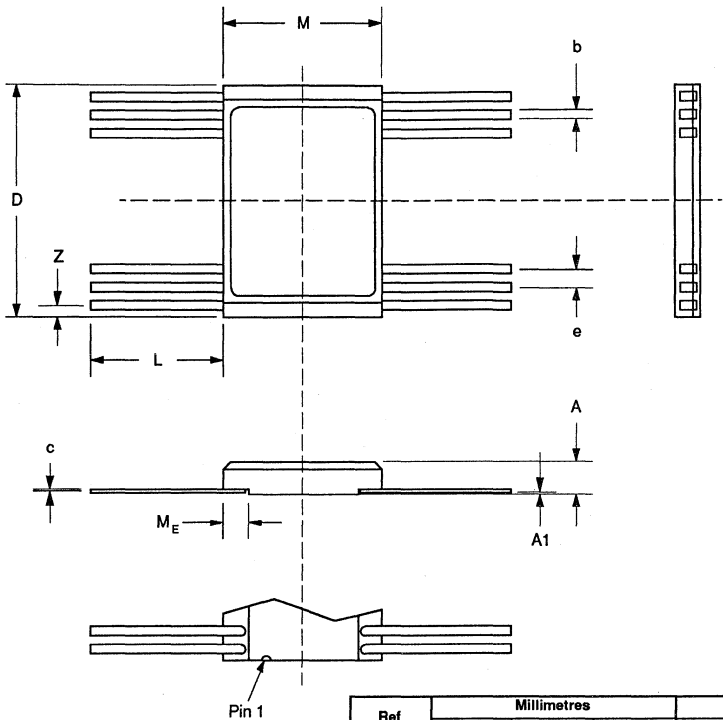


Figure 13: 18-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.07	-	-	0.121
A1	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.08	-	0.152	0.003	-	0.006
D	14.99	-	15.50	0.590	-	0.610
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.96	-	10.36	0.392	-	0.408
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

XG544

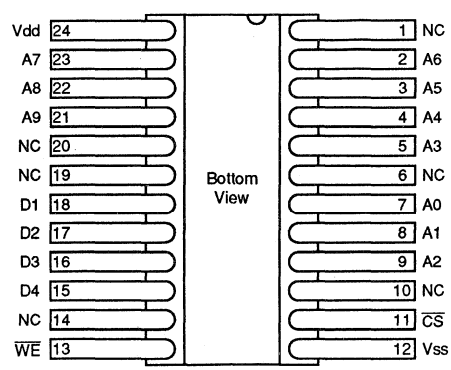
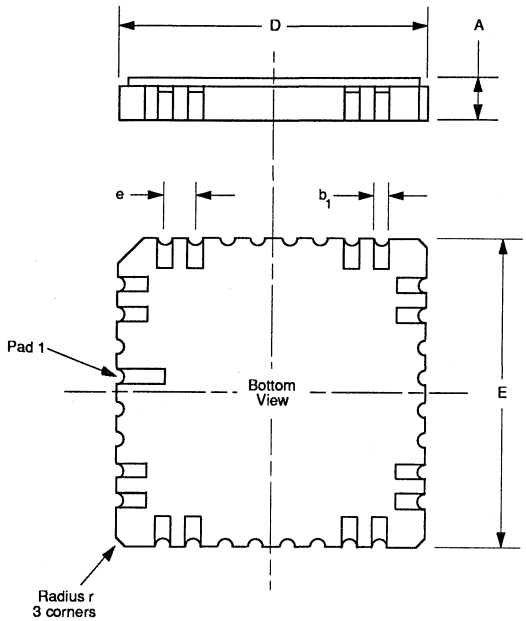
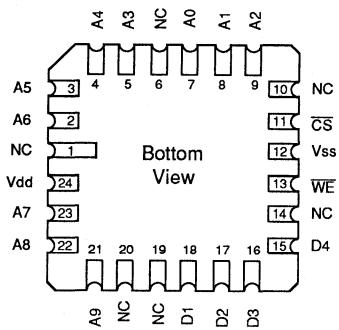


Figure 14: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F





Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.16	-	-	0.096
b1	-	0.51	-	-	0.020	-
D	8.76	-	9.14	0.345	-	0.360
E	8.76	-	9.14	0.345	-	0.360
e	-	1.02	-	-	0.040	-
r	-	0.19	-	-	0.0075	-

XG470

Figure 15: 24-Pad Leadless Chip Carrier - Package Style L

Function	Package Option			Via	Burnin			Radiation
	F	C	L		Static 1	Static 2	Dynamic	
A6	2	1	2	R	0V	5V	F6	5V
A5	3	2	3	R	0V	5V	F5	5V
A4	4	3	4	R	0V	5V	F4	5V
A3	5	4	5	R	0V	5V	F3	5V
A0	7	5	7	R	0V	5V	F0	5V
A1	8	6	8	R	0V	5V	F1	5V
A2	9	7	9	R	0V	5V	F2	5V
NCS	11	8	11	R	0V	5V	0V	5V
VSS	12	9	12	Direct	0V	0V	0V	0V
NWE	13	10	13	R	0V	5V	5V	5V
D4	15	11	15	R	0V	5V	LOAD	5V
D3	16	12	16	R	0V	5V	LOAD	5V
D2	17	13	17	R	0V	5V	LOAD	5V
D1	18	14	18	R	0V	5V	LOAD	5V
A9	21	15	21	R	0V	5V	F9	5V
A8	22	16	22	R	0V	5V	F8	5V
A7	23	17	23	R	0V	5V	F7	5V
VDD	24	18	24	Direct	5V	5V	5V	5V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Burnin R=1k
3. Radiation R=10k

Figure 16: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$3.4x10^{-9}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 17: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

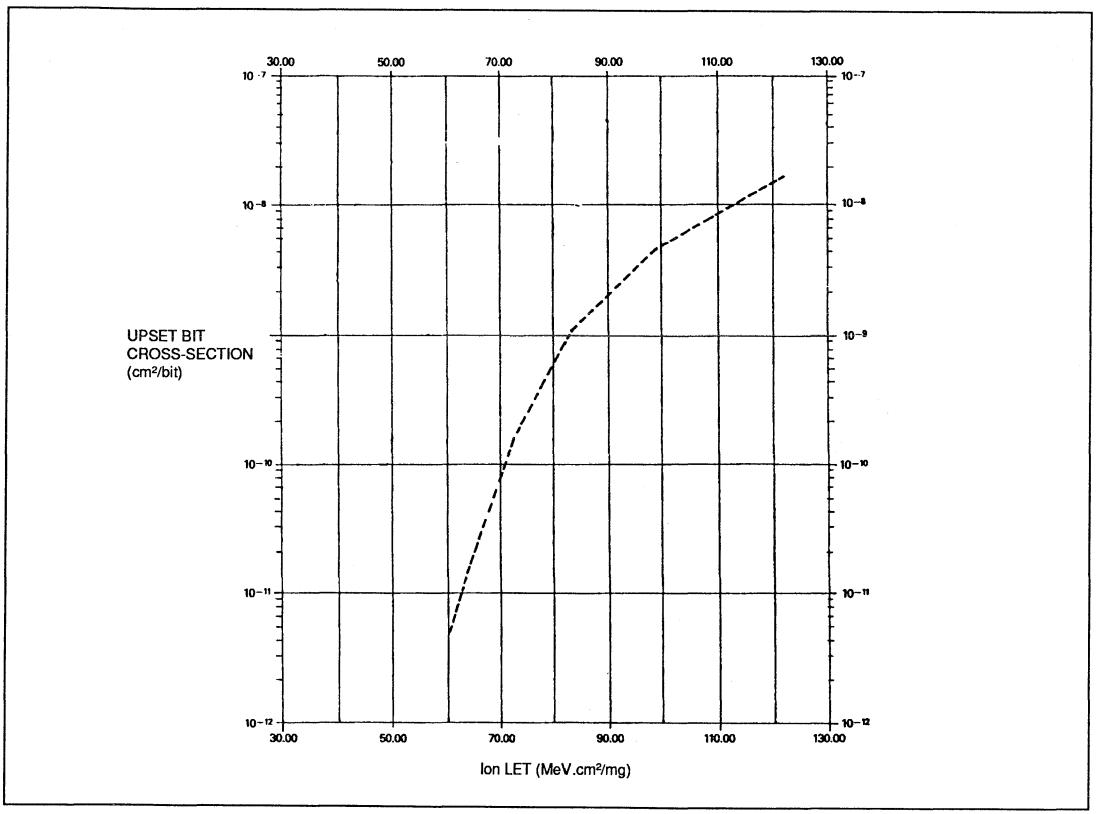
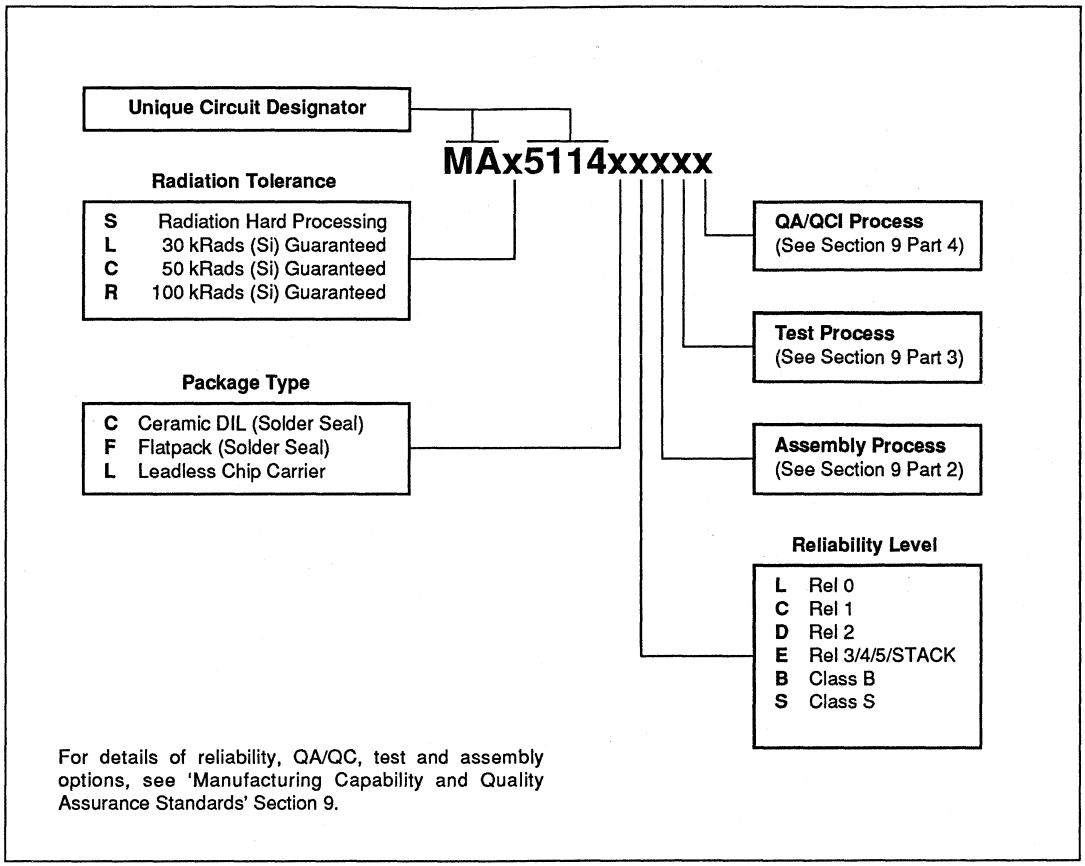


Figure 18: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3582-3.1

MA6116 & MA6216

RADIATION HARD 2048 x 8 BIT STATIC RAM

The MA6116 16k Static RAM is configured as 2048 x 8 bits and manufactured using CMOS-SOS high performance, radiation hard, 3μm technology. The MA6216 is manufactured using 2.5μm technology resulting in faster performance.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

Operation Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Power
Read	L	L	H	D OUT	
Write	L	H	L	D IN	ISB1
Write	L	L	L	D IN	
Standby	H	X	X	High Z	ISB2

Figure 1: Truth Table

FEATURES

- 3μm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 110ns (MA6116) and 85ns (MA6216) Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{10}$ Rad(Si)/sec
- SEU $<10^{-10}$ Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 100μA Typical
- -55°C to +125°C Operation
- TTL and CMOS Compatible Inputs
- Fully Static Operation

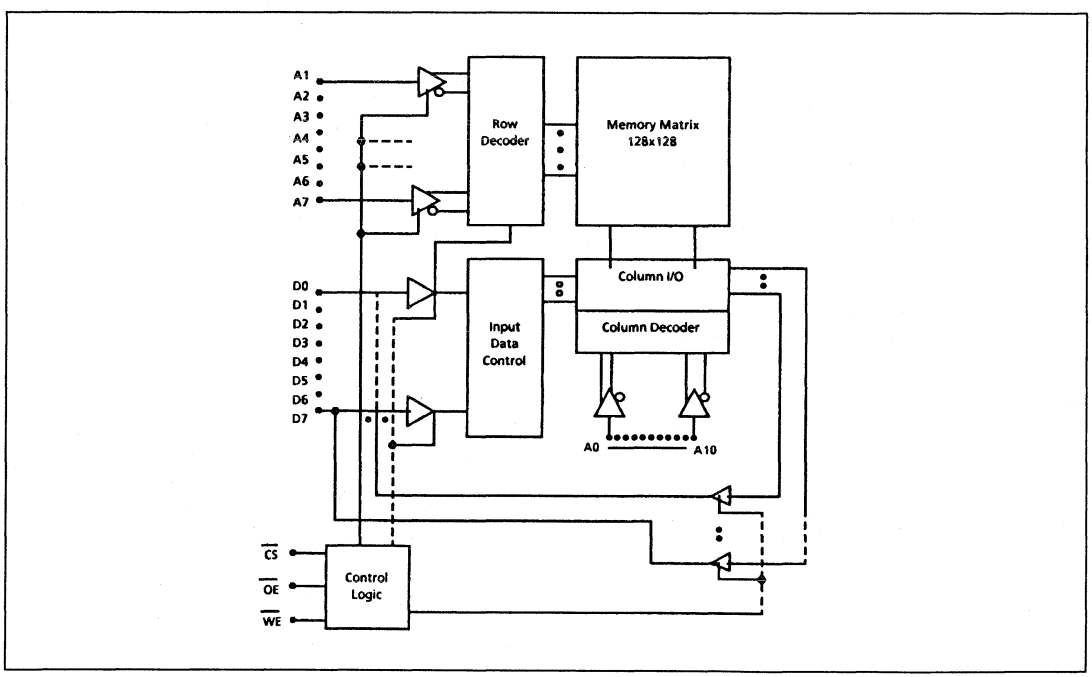


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Figure 3: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for Tables 4 and 5:
1. Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request).
2. Worst case at T_A = +125°C, guaranteed but not tested at T_A = -55°C.
3. GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	-	V_{DD}/2	-	V_{DD}	V
V_{IL}	Input Low Voltage	-	V_{SS}	-	0.8	V
V_{OH}	Output High Voltage	I_{OH1} = -1mA	2.4	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA	-	-	0.4	V
I_{LI}	Input Leakage Current (note 2)	All inputs except $\overline{CS}$	-	-	±10	µA
I_{LO}	Output Leakage Current (note 2)	Output disabled, V_{OUT} = V_{SS} or V_{DD}	-	-	±20	µA
I_{DD}	Power Supply Current	f_{RC} = 1MHz, $\overline{CS}$ = 50% mark:space	-	20	40	mA
I_{SB1}	Selected Supply Current	All inputs = V_{DD}-0.2V except $\overline{CS}$ = V_{SS}+0.2V	-	50	70	mA
I_{SB2}	Standby Supply Current	Chip disabled, $\overline{CS}$ = V_{DD}-0.2V	-	0.1	5	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	50	3000	µA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V.
2. Times measurement reference level = 1.5V.
3. Output load 1TTL gate and C_L = 60pF.
4. Transition is measured at ±500mV from steady state.
5. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MA6116 Min	MA6116 Max	MA6216 Min	MA6216 Max	Units
T_{AVAVR}	Read Cycle Time	150	-	100	-	ns
T_{AVQV}	Address Access Time	-	130	-	95	ns
T_{ELQV}	Chip Select Access Time	-	140	-	100	ns
T_{ELQX} (4,5)	Chip Select to Output in Low Z	10	-	10	-	ns
T_{GLQV}	Output Enable to Output Valid	-	80	-	60	ns
T_{GLQX} (4,5)	Output Enable to Output in Low Z	10	-	10	-	ns
T_{EHQZ} (4,5)	Chip Deselect to Output in High Z	0	60	0	50	ns
T_{GHQZ} (4,5)	Chip Disable to Output in High Z	0	60	0	50	ns
T_{AXQX}	Output Hold from Address Change	10	-	10	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MA6116 Min	MA6116 Max	MA6216 Min	MA6216 Max	Units
T_{AVAVW}	Write Cycle Time	150	-	100	-	ns
T_{ELWH}	Chip Selection to End of Write	85	-	75	-	ns
T_{AVWH}	Address Valid to End of Write	80	-	70	-	ns
T_{AVWL}	Address Set Up Time	20	-	10	-	ns
T_{WLWH}	Write Pulse Width	50	-	40	-	ns
T_{WHAV}	Write Recovery Time	5	-	5	-	ns
T_{WLQZ} (4,5)	Write to Output in High Z	0	60	0	50	ns
T_{DVWH}	Data to Write Time Overlap	30	-	25	-	ns
T_{WHDX}	Data Hold from Write Time	10	-	10	-	ns
T_{WHQX} (4,5)	Output Active from End to Write	5	-	5	-	ns
T_{ELWL}	Chip Selection to Write Low	25	-	25	-	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	6	10	pF
C_{OUT}	Output Capacitance	V_O = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

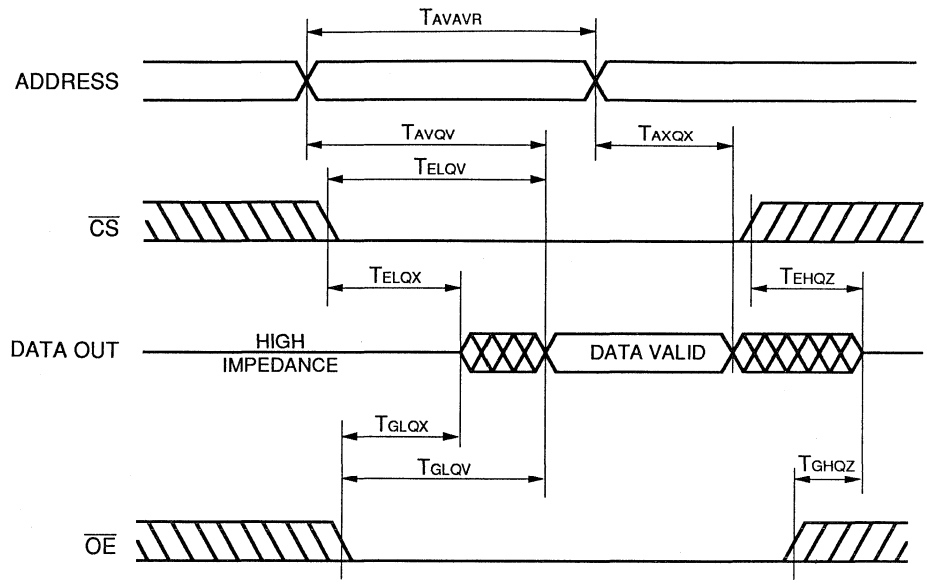
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

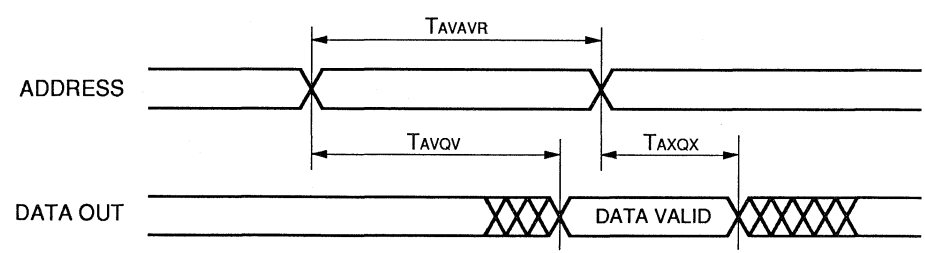
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



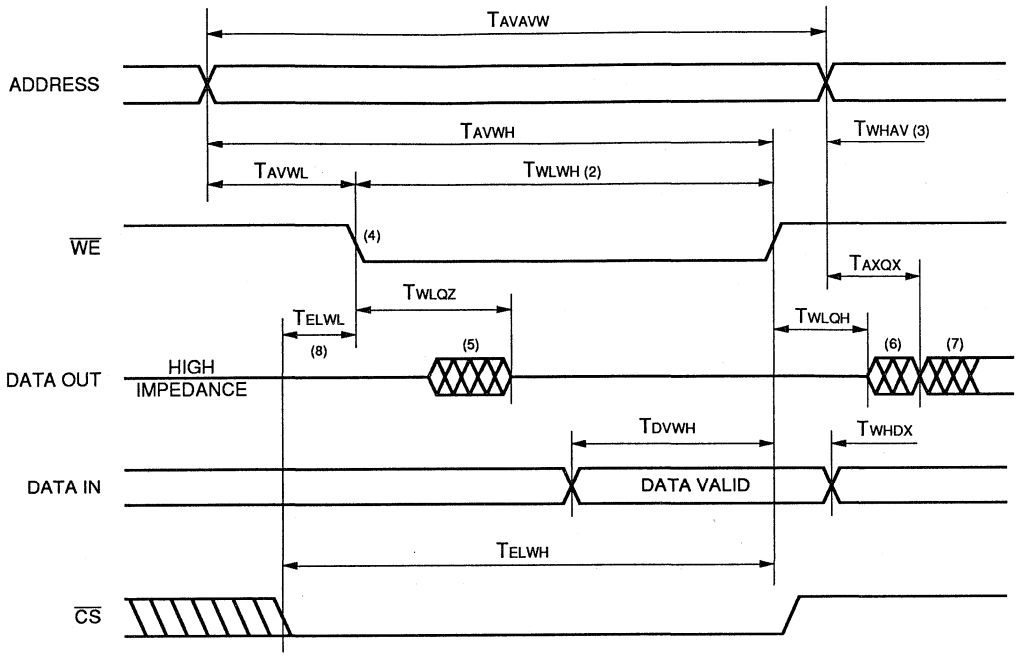
1. $\overline{WE}$ is high for Read Cycle.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.

Figure 11a: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$ is high.

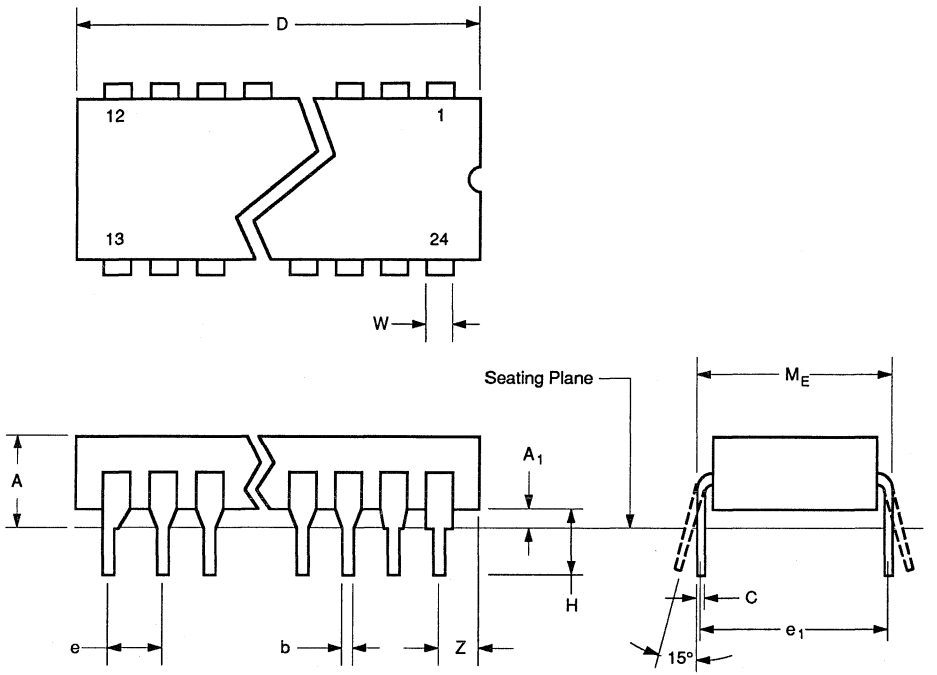
Figure 11b: Read Cycle 2



1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is in the active state, so DATA IN must not be in opposing state.
6. DATA OUT is the write data of the current cycle, if selected.
7. DATA OUT is the read data of the next address, if selected.
8. T_{ELWL} must be met to prevent memory corruption.
9. $\overline{OE}$ is low. (If $\overline{OE}$ is high then DATA OUT remains in the high impedance state throughout the cycle).

Figure 12: Write Cycle

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	30.79	-	-	1.212
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG403

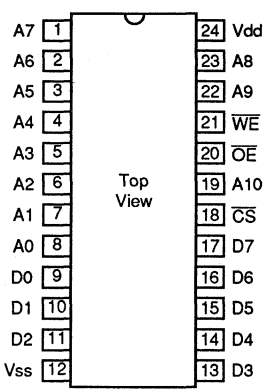
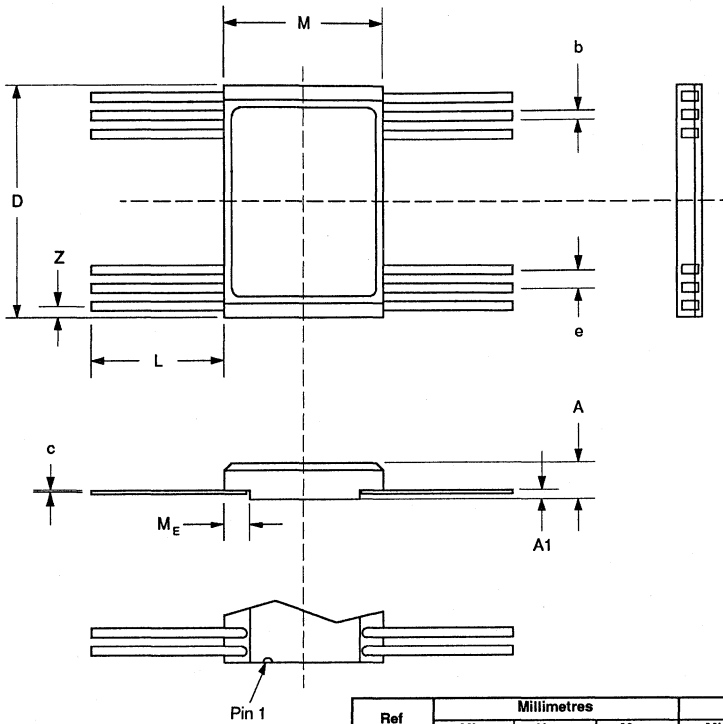


Figure 13: 24-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.07	-	-	0.121
A1	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.08	-	0.152	0.003	-	0.006
D	14.99	-	15.50	0.590	-	0.610
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.96	-	10.36	0.392	-	0.408
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

XG544

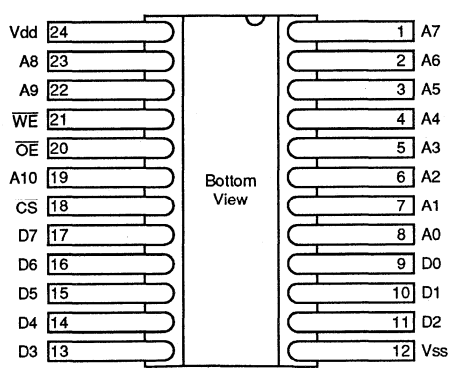
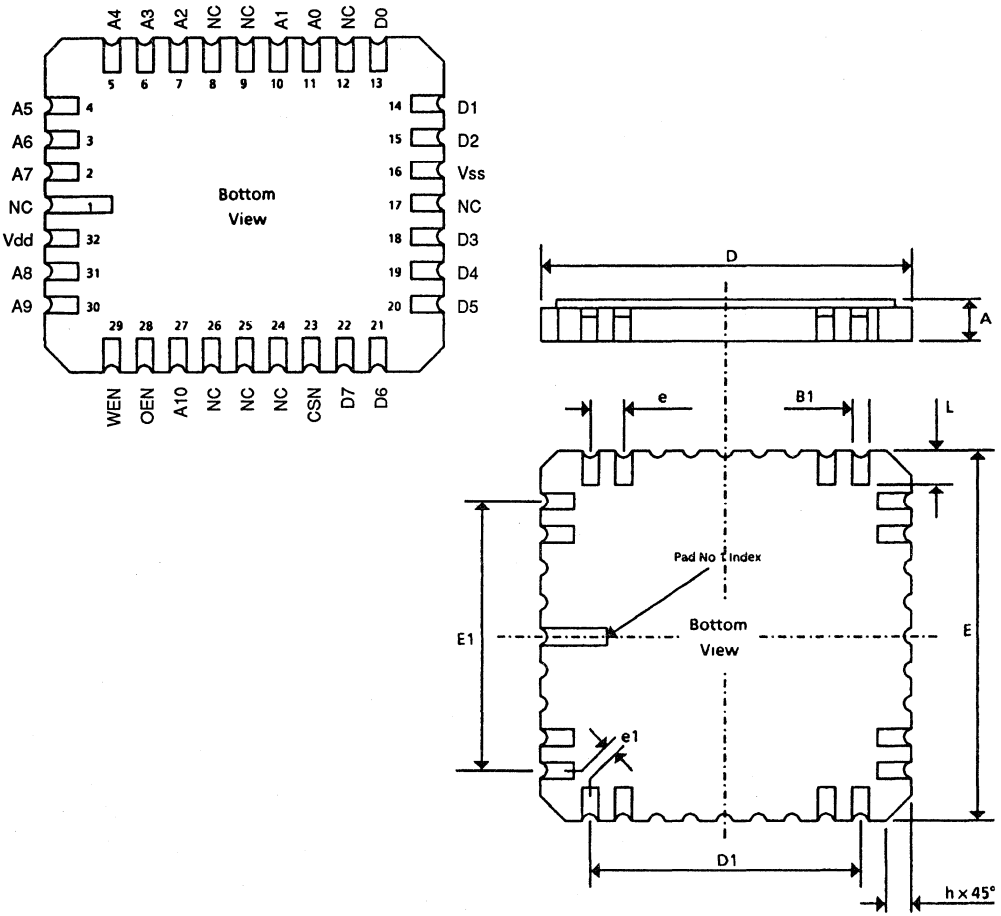


Figure 14: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.83	-	2.28	0.072	-	0.090
B1	0.56	-	0.71	0.022	-	0.028
D	11.30	-	11.63	0.445	-	0.458
D1	-	7.62	-	-	0.300	-
E	13.84	-	14.22	0.545	-	0.560
E1	-	10.61	-	-	0.400	-
e	-	1.27	-	-	0.050	-
e1	0.38	-	-	0.015	-	-
h	-	1.016	-	-	0.040	-
i	-	0.51	-	-	0.020	-
L	-	1.27	-	-	0.050	-
L2	1.96	-	2.36	0.077	-	0.093

XG520

Figure 15: 32-Pad Leadless Chip Carrier - Package Style L

Function	Package Options		Via	Burnin			Radiation
	L	C&F		Static1	Static 2	Dynamic	
A7	2	1	R	0V	5V	F7	5V
A6	3	2	R	0V	5V	F6	5V
A5	4	3	R	0V	5V	F5	5V
A4	5	4	R	0V	5V	F4	5V
A3	6	5	R	0V	5V	F3	5V
A2	7	6	R	0V	5V	F2	5V
A1	10	7	R	0V	5V	F1	5V
A0	11	8	R	0V	5V	F0	5V
D0	13	9	R	0V	5V	LOAD	5V
D1	14	10	R	0V	5V	LOAD	5V
D2	15	11	R	0V	5V	LOAD	5V
VSS	16	12	Direct	0V	0V	0V	0V
D3	18	13	R	0V	5V	LOAD	5V
D4	19	14	R	0V	5V	LOAD	5V
D5	20	15	R	0V	5V	LOAD	5V
D6	21	16	R	0V	5V	LOAD	5V
D7	22	17	R	0V	5V	LOAD	5V
CSB	23	18	R	0V	5V	0V	5V
A10	27	19	R	0V	5V	F10	5V
OEB	28	20	R	0V	5V	5V	5V
WEB	29	21	R	0V	5V	5V	5V
A9	30	22	R	0V	5V	F9	5V
A8	31	23	R	0V	5V	F8	5V
VDD	32	24	Direct	5V	5V	5V	5V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Burnin R=1k
3. Radiation R=10k

Figure 16: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$3.4x10^{-9}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 17: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

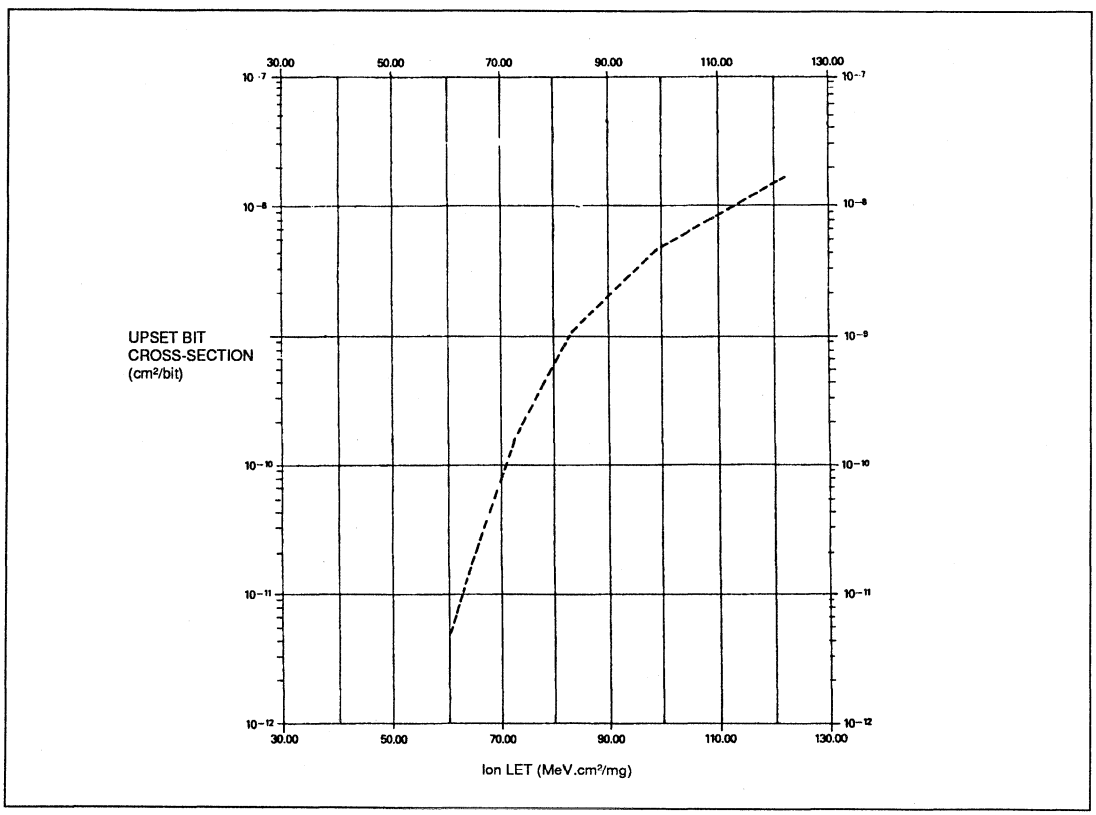
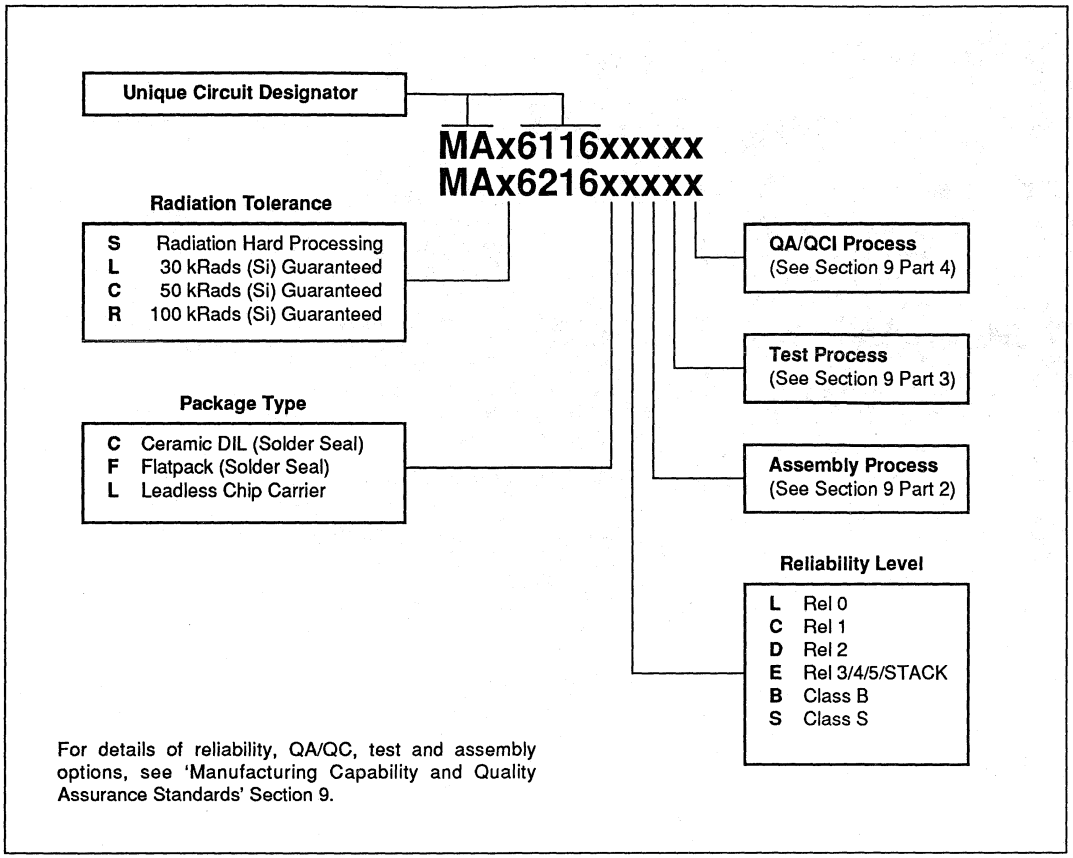


Figure 18: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3585-5.2

MA9167

RADIATION HARD 16384 x 1 BIT STATIC RAM

The MA9167 16k Static RAM is configured as 16384 x 1 bits and manufactured using GPS's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the high state.

See Application Note "Overview of the GPS Radiation Hard 1.5µm CMOS/SOS SRAM Range".

$\overline{CS}$	$\overline{WE}$	Mode	V_{DD} Current	Output Pin
H	X	Deselected	I_{SB2}	High Z
L	H	Read	I_{SB1}	D_{OUT}
L	L	Write	I_{SB1}	High Z

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{11}$ Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Single 5V Supply
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation

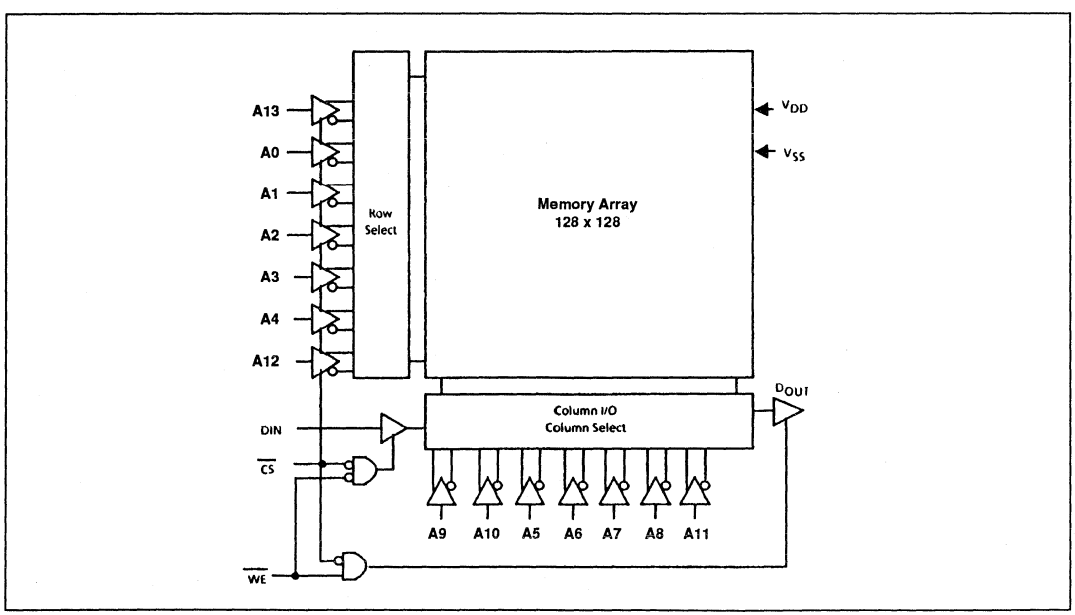


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Figure 3: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Notes for Tables 4 and 5:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{CS}$ = V_{SS} +0.2V	-	0.1	5	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	-	3	8	mA
I_{SB2}	Standby Supply Current	$\overline{CS}$ = V_{DD} -0.2V	-	0.1	5	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	-	0.05	2	mA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V (TTL).
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MAX9167X70 Min	Max	Units
T_{AVAVR}	Read Cycle Time	70	-	ns
T_{AVQV}	Address Access Time	-	70	ns
T_{ELQV}	Chip select Access time	-	70	ns
T_{ELQX} (5,6)	Chip Selection to Output in Low Z	15	-	ns
T_{EHQZ} (5,6)	Chip Deselection to Output in High Z	0	20	ns
T_{AXQX}	Output Hold from Address change	30	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MAX9167X70 Min	Max	Units
T_{AVAVW}	Write Cycle Tlme	50	-	ns
T_{ELWH}	Chip Selection to End of Write	50	-	ns
T_{AVWH}	Address Valid to End of Write	50	-	ns
T_{AVWL}	Address Set Up Time	0	-	ns
T_{WLWH}	Write Pulse Width	35	-	ns
T_{WHAV}	Write Recovery Time	0	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	20	ns
T_{DVWH}	Data to Write Time Overlap	25	-	ns
T_{WHDX}	Data Hold from Write	0	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

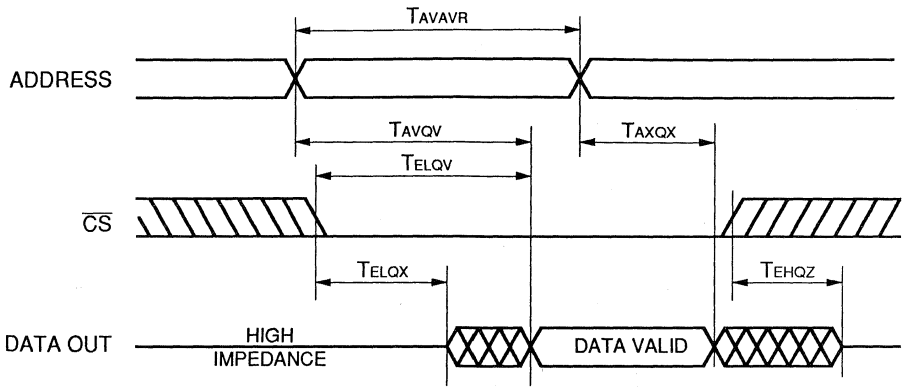
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

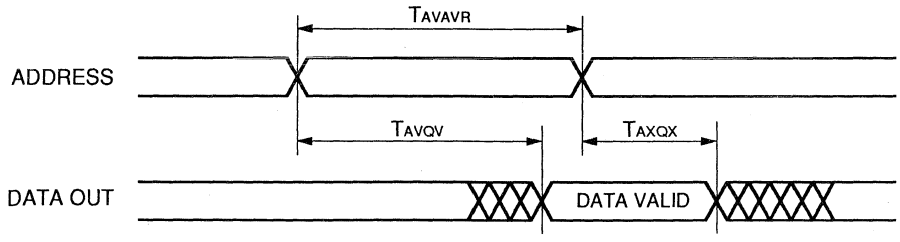
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



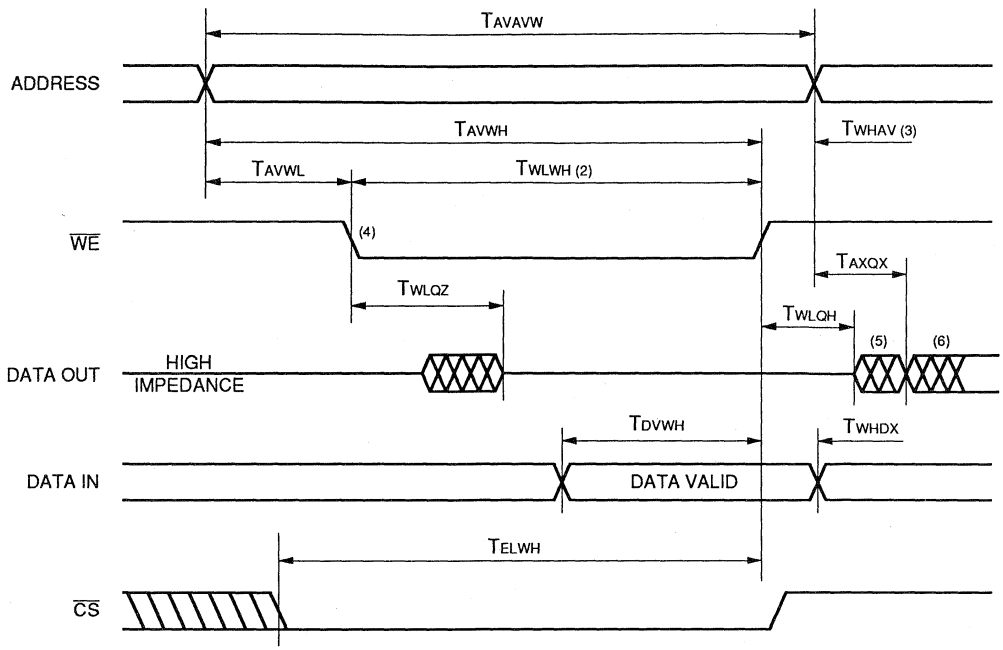
1. $\overline{WE}$ is high for Read Cycle.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.

Figure 11: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$ low.

Figure 12: Read Cycle 2

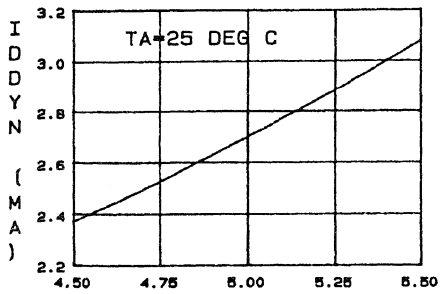


1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is the write data of the current cycle, if selected.
6. DATA OUT is the read data of the next address, if selected.

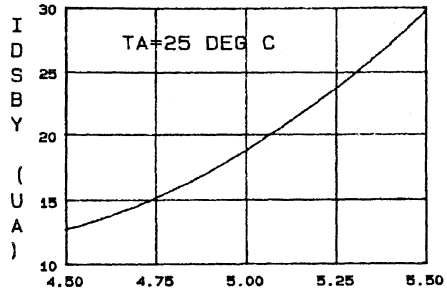
Figure 13: Write Cycle

TYPICAL PERFORMANCE CHARACTERISTICS MAx9167x70

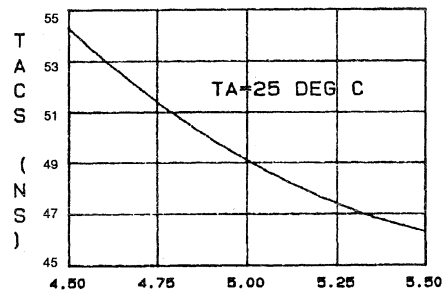
DYNAMIC CURRENT VS SUPPLY VOLTAGE



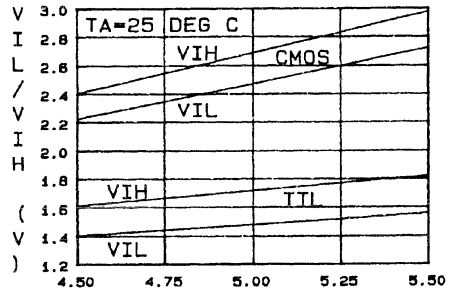
STANDBY CURRENT VS SUPPLY VOLTAGE



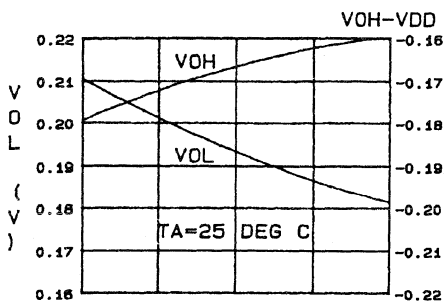
CS ACCESS TIME VS SUPPLY VOLTAGE



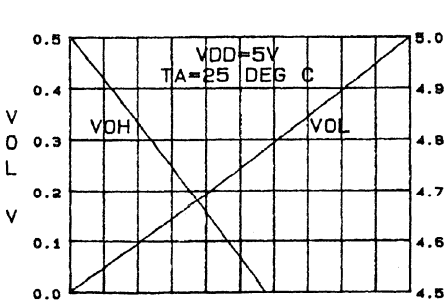
INPUT LEVELS VS SUPPLY VOLTAGE



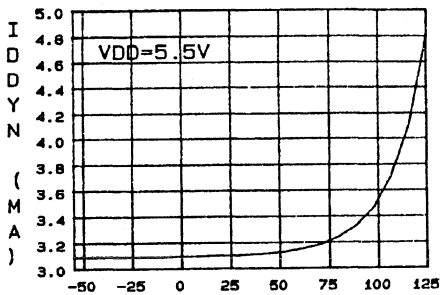
OUTPUT LEVELS VS SUPPLY VOLTAGE



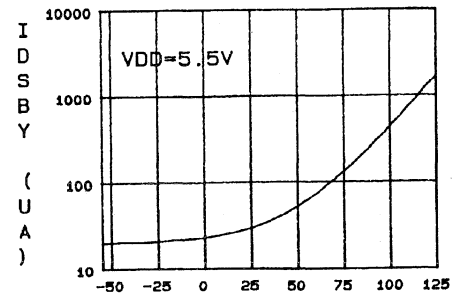
OUTPUT VOLTAGE VS CURRENT



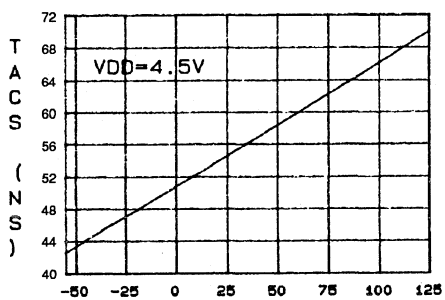
DYNAMIC CURRENT VS TEMPERATURE



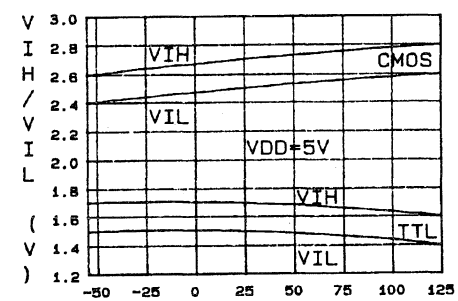
STANDBY CURRENT VS TEMPERATURE



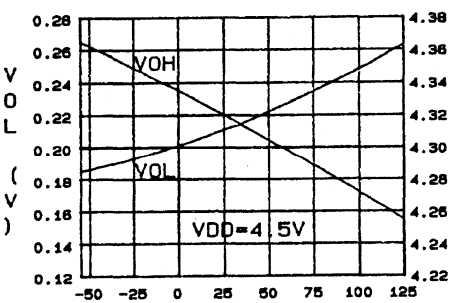
CS ACCESS TIME VS TEMPERATURE



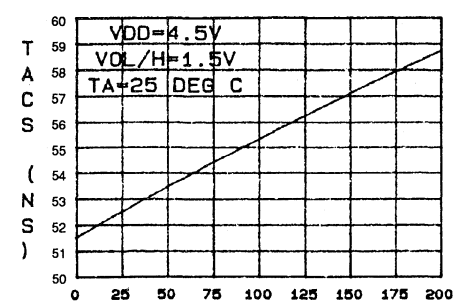
INPUT LEVELS VS TEMPERATURE



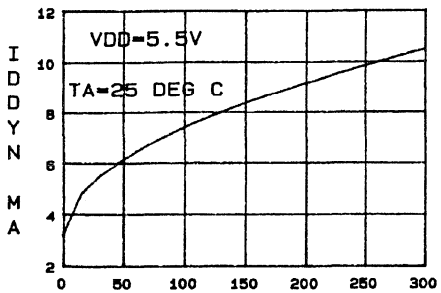
OUTPUT LEVELS VS TEMPERATURE



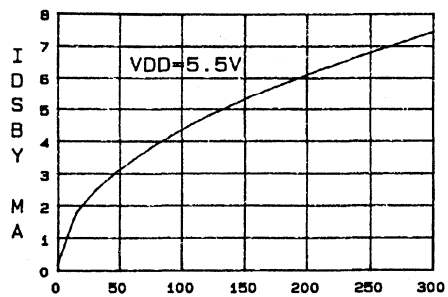
CS ACCESS TIME VS OUTPUT LOAD



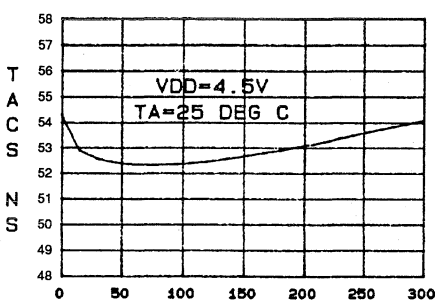
DYNAMIC CURRENT VS RADIATION



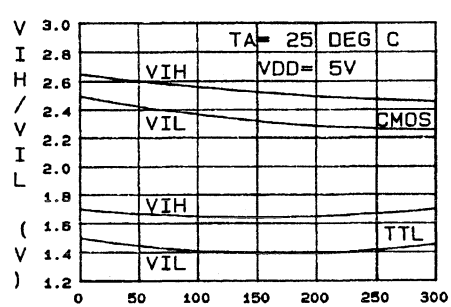
STANDBY CURRENT VS RADIATION



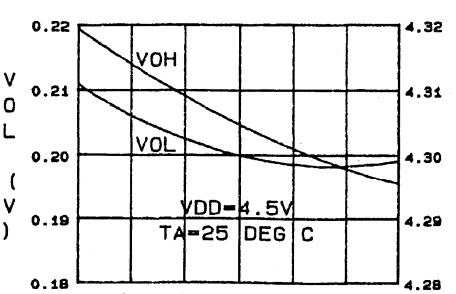
CS ACCESS TIME VS RADIATION



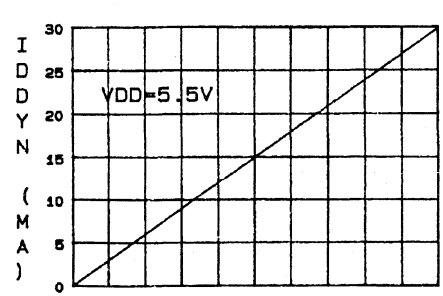
INPUT LEVELS VS RADIATION



OUTPUT LEVELS VS RADIATION



DYNAMIC CURRENT VS FREQUENCY



PIN ASSIGNMENTS

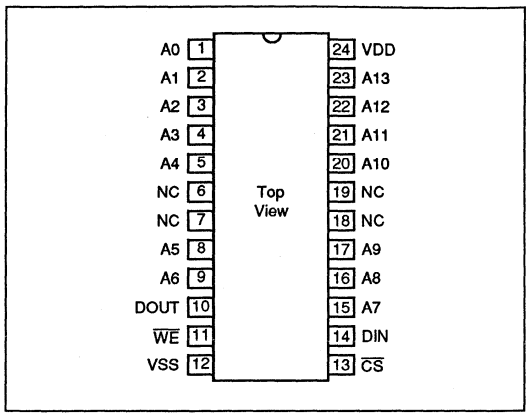


Figure 14: 24-Pin Ceramic DIL (Solder Seal) - Package Style C (Pin Assignment Option 1)

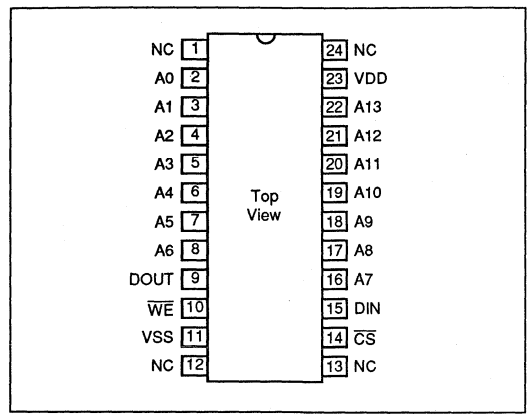


Figure 15: 24-Pin Ceramic DIL (Solder Seal) - Package Style D (Pin Assignment Option 2)

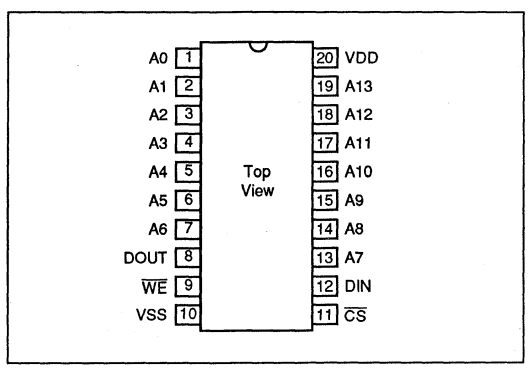


Figure 16: 20-Pin Ceramic DIL(Solder Seal) - Package Style X

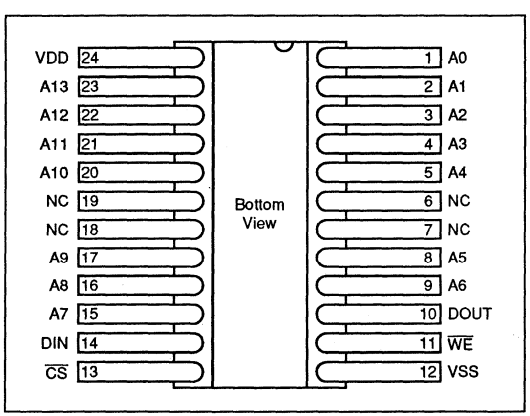


Figure 17: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F (Pin Assignment Option 1)

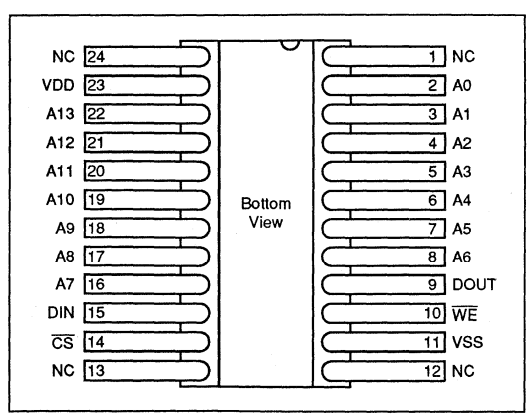
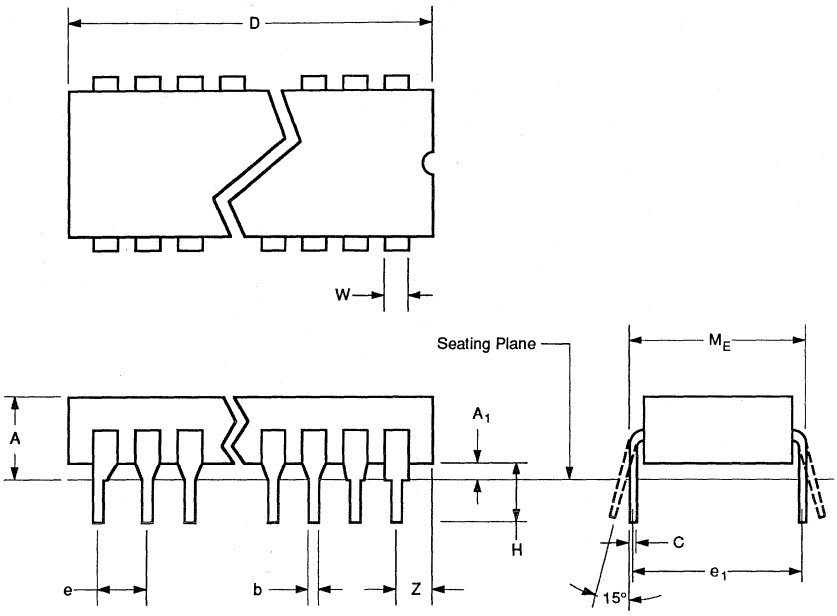


Figure 18: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style Y (Pin Assignment Option 2)

PACKAGE OUTLINES



20-Lead

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	23.11	-	25.65	0.910	-	1.010
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	8.13 Typ.	-	-	0.300 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	7.95	-	-	0.313
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

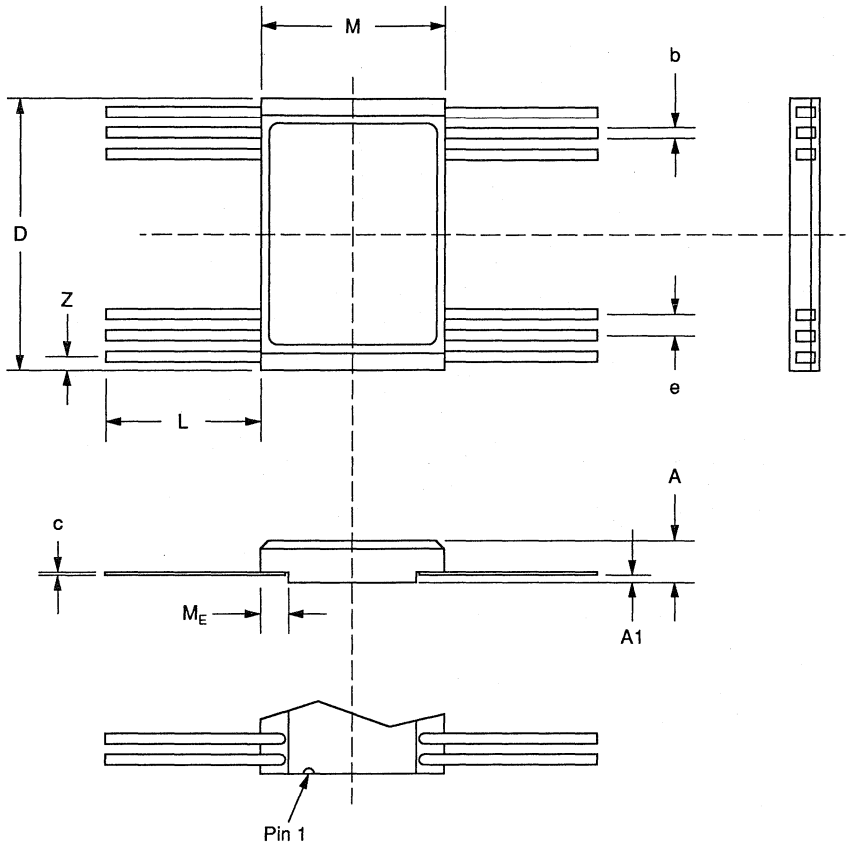
XG483

24-Lead

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	30.79	-	-	1.212
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG403

Figure 19: 20/24-Lead Ceramic DIL (Solder Seal) - Package Styles C, D and X



Package Style F

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.07	-	-	0.121
A1	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.08	-	0.152	0.003	-	0.006
D	14.99	-	15.50	0.590	-	0.610
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.96	-	10.36	0.392	-	0.408
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

XG544

Package Style Y

Ref.	Min.	Nom.	Max.
A	-	-	0.115
A_1	0.026	-	0.035
b	0.015	-	0.019
c	0.003	-	0.006
D	-	-	0.600
e	-	0.050 Typ.	-
L	0.330	-	-
M	0.392	-	0.408
M_E	0.030	-	-
Z	0.005	-	0.045
Dimensions in inches			

XG146

Figure 20: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F and Y

Function	Pin Number			Via	Static 1	Static 2	Dynamic	Radiation
	D and F (24 pin)		D (20 pin)					
	Option 1	Option 2						
A0	1	2	1	R	5V	0V	F0	5V
A1	2	3	2	R	5V	0V	F1	5V
A2	3	4	3	R	5V	0V	F2	5V
A3	4	5	4	R	5V	0V	F3	5V
A4	5	6	5	R	5V	0V	F4	5V
A5	8	7	6	R	5V	0V	F5	5V
A6	9	8	7	R	5V	0V	F6	5V
DOUT	10	9	8	R	5V	0V	LOAD	5V
WEB	11	10	9	R	5V	0V	F14	5V
VSS	12	11	10	Direct	0V	0V	0V	0V
CSB	13	14	11	R	5V	0V	0V	5V
DIN	14	15	12	R	5V	0V	F15	5V
A7	15	16	13	R	5V	0V	F7	5V
A8	16	17	14	R	5V	0V	F8	5V
A9	17	18	15	R	5V	0V	F9	5V
A10	20	19	16	R	5V	0V	F10	5V
A11	21	20	17	R	5V	0V	F11	5V
A12	22	21	18	R	5V	0V	F12	5V
A13	23	22	19	R	5V	0V	F13	5V
VDD	24	23	20	Direct	5V	5V	5V	5V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Burnin R=1k
3. Radiation R=10k

Figure 21: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$4.3x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 22: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

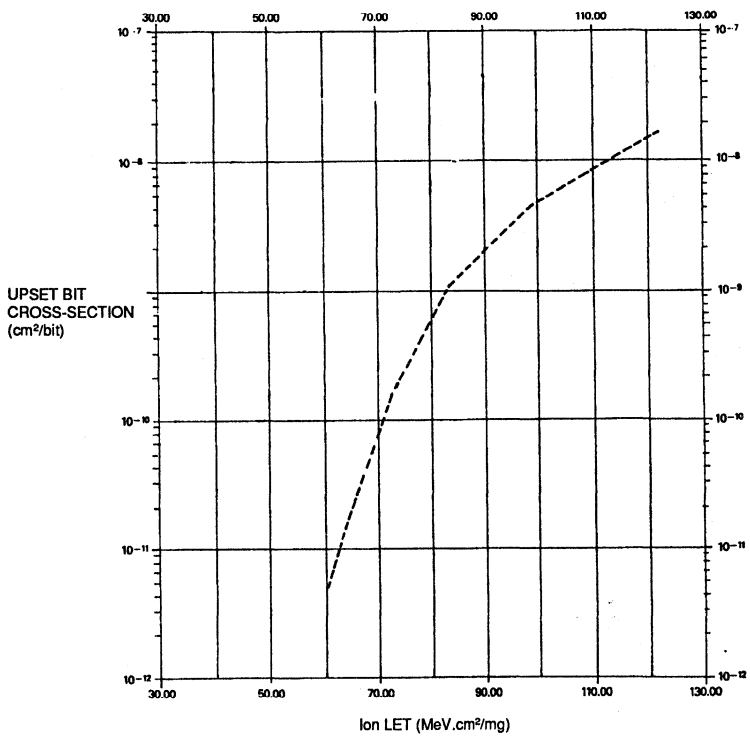
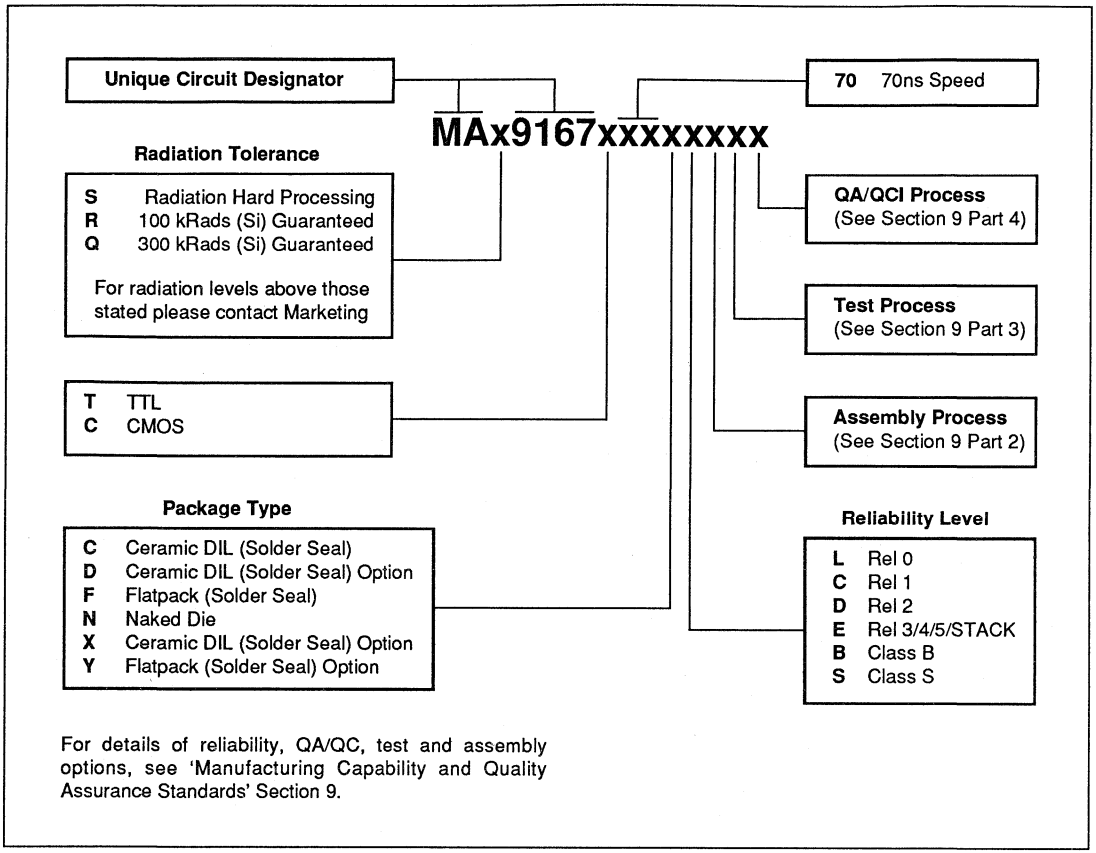


Figure 23: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA9187

RADIATION HARD 65536 x 1 BIT STATIC RAM

The MA9187 64k Static RAM is configured as 65536 x 1 bits and manufactured using GPS's CMOS-SOS high performance, radiation hard, 1.5µm technology.

The device has separate input and output terminals controlled by Chip Select and Write Enable. The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when Chip Select is in the high state.

See Application Note "Overview of the GPS Radiation Hard 1.5µm CMOS/SOS SRAM Range".

$\overline{CS}$	$\overline{WE}$	Mode	V_{DD} Current	Output Pin
H	X	Deselected	I_{SB2}	High Z
L	H	Read	I_{SB1}	D_{OUT}
L	L	Write	I_{SB1}	High Z

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 45ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{11} Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Single 5V Supply
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation

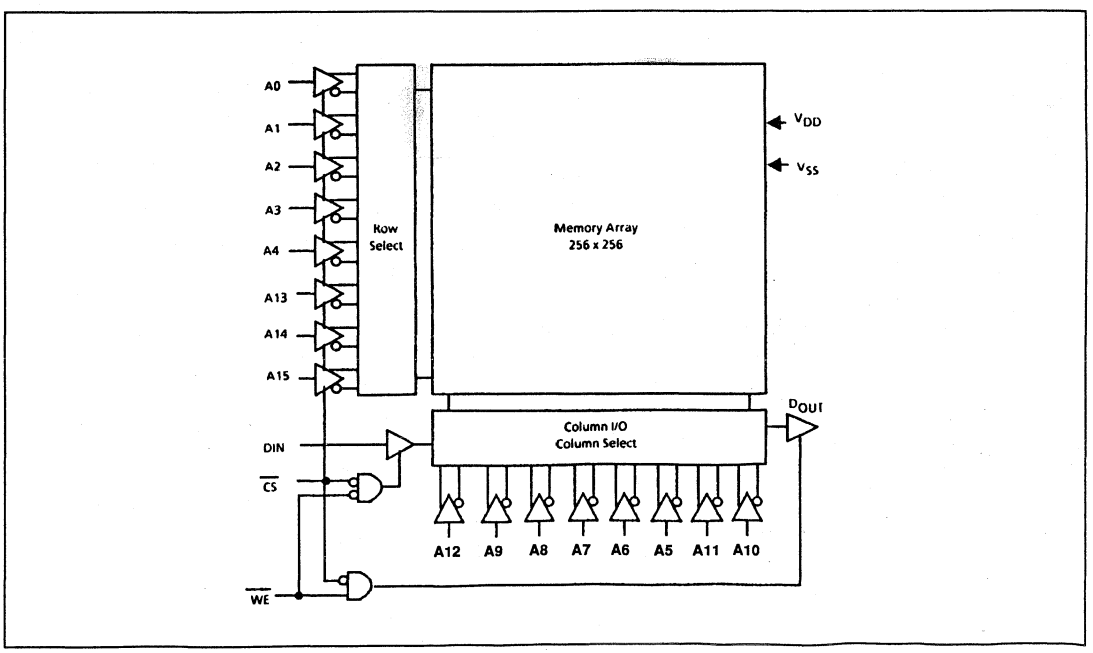


Figure 2: Block Diagram

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher levels available on request). Group A Subgroups 1, 2, 3.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-		4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	-	TTL CMOS	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	-	TTL CMOS	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA		2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA		V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA		-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs		-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}		-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{CS}$ = V_{SS} +0.2V	90ns 60ns 45ns	- - -	0.1 0.1 -	10 10 TBD	mA mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	90ns 60ns 45ns	- - -	3 3 -	13 13 TBD	mA mA
I_{SB2}	Standby Supply Current	$\overline{CS}$ = V_{DD} -0.2V	90ns 60ns 45ns	- - -	0.1 0.1 -	10 10 TBD	mA mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}		2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V	90ns 60ns 45ns	- - -	0.05 0.05 -	4 4 TBD	mA mA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3V (TTL) and V_{SS} to 4V (CMOS).
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MAX9187X45 Min	MAX9187X45 Max	MAX9187X60 Min	MAX9187X60 Max	MAX9187X90 Min	MAX9187X90 Max	Units
T_{AVAVR}	Read Cycle Time	45	-	60	-	90	-	ns
T_{AVOV}	Address Access Time	-	45	-	60	-	90	ns
T_{ELOV}	Chip select Access time	-	45	-	60	-	90	ns
T_{ELOX} (5,6)	Chip Selection to Output in Low Z	15	-	15	-	15	-	ns
T_{EHQZ} (5,6)	Chip Deselection to Output in High Z	0	20	0	20	0	20	ns
T_{AXOX}	Output Hold from Address change	15	-	20	-	30	-	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MAX9187X45 Min	MAX9187X45 Max	MAX9187X60 Min	MAX9187X60 Max	MAX9187X90 Min	MAX9187X90 Max	Units
T_{AVAVW}	Write~Cycle TIme	40	-	50	-	60	-	ns
T_{ELWH}	Chip Selection to End of Write	35	-	40	-	50	-	ns
T_{AVWH}	Address Valid to End of Write	35	-	40	-	50	-	ns
T_{AVWL}	Address Set Up Time	0	-	0	-	0	-	ns
T_{WLWH}	Write Pulse Width	28	-	30	-	35	-	ns
T_{WHAV}	Write Recovery Time	0	-	0	-	0	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	20	0	20	0	20	ns
T_{DVWH}	Data to Write Time Overlap	18	-	20	-	25	-	ns
T_{WHDX}	Data Hold from Write	0	-	0	-	0	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	0	20	0	20	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

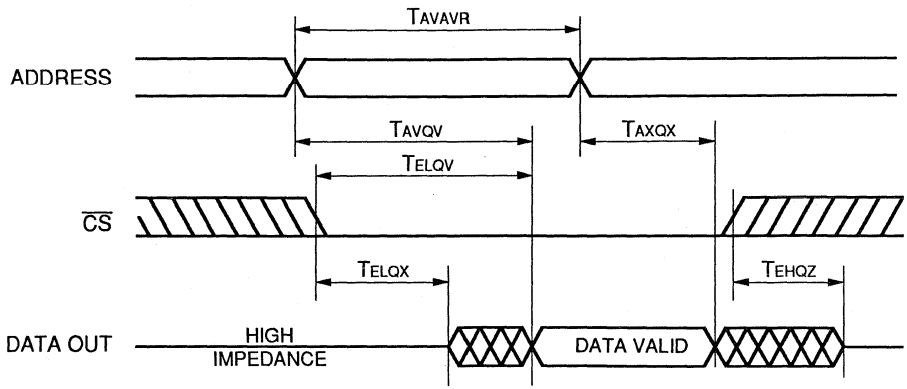
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

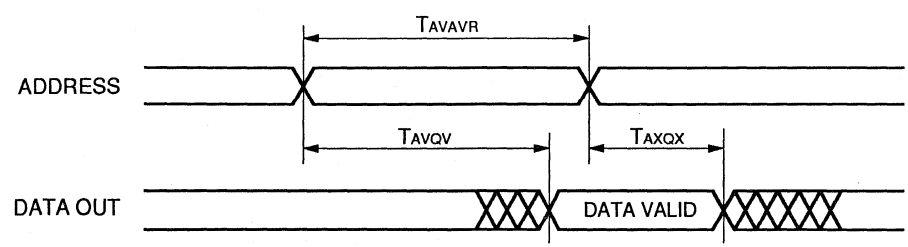
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



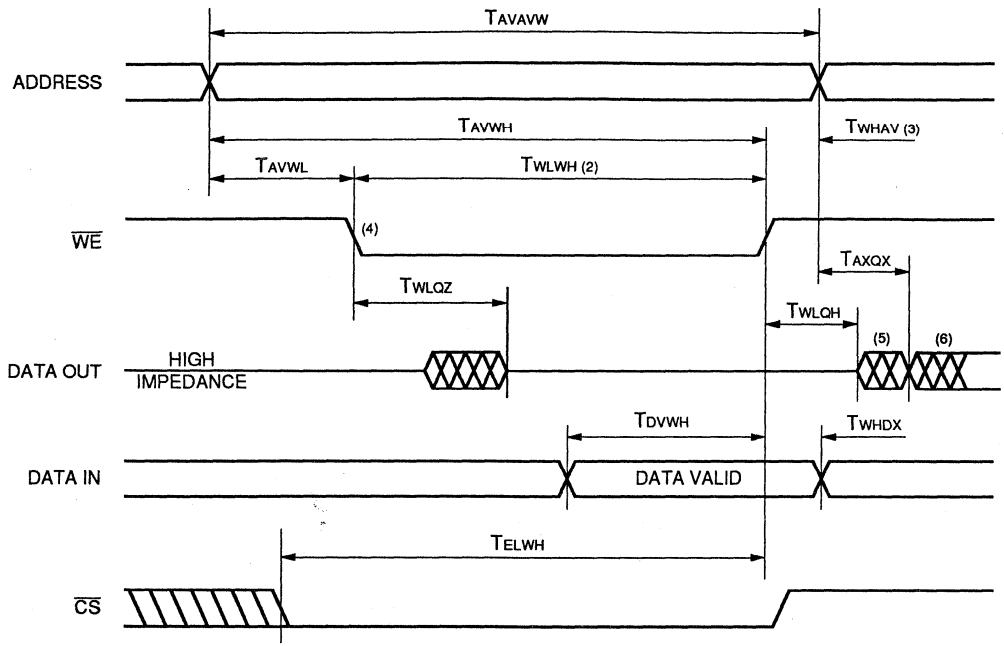
1. $\overline{WE}$ is high for Read Cycle.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low.

Figure 11: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$ low.

Figure 12: Read Cycle 2

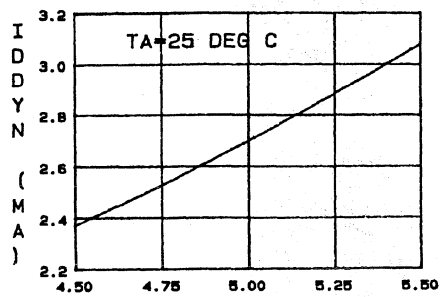


1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is the write data of the current cycle, if selected.
6. DATA OUT is the read data of the next address, if selected.

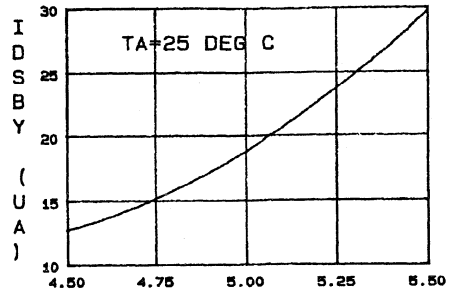
Figure 13: Write Cycle

TYPICAL PERFORMANCE CHARACTERISTICS MAx9187x60

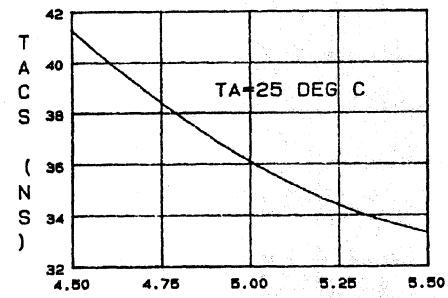
DYNAMIC CURRENT VS SUPPLY VOLTAGE



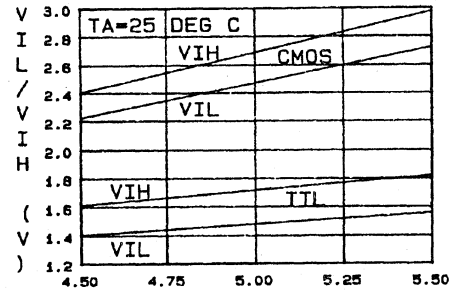
STANDBY CURRENT VS SUPPLY VOLTAGE



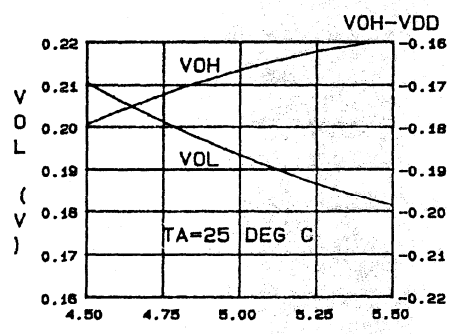
CS ACCESS TIME VS SUPPLY VOLTAGE



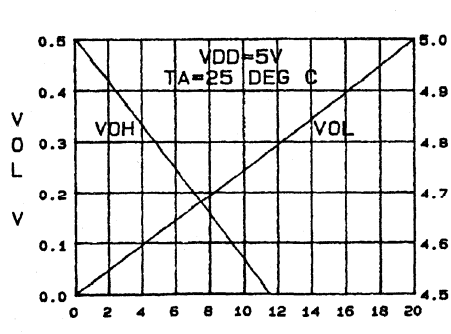
INPUT LEVELS VS SUPPLY VOLTAGE



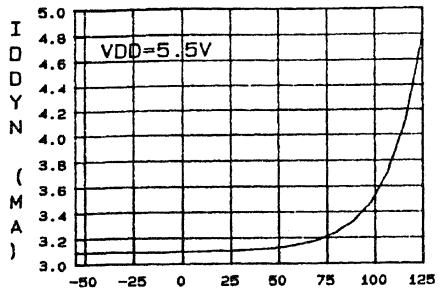
OUTPUT LEVELS VS SUPPLY VOLTAGE



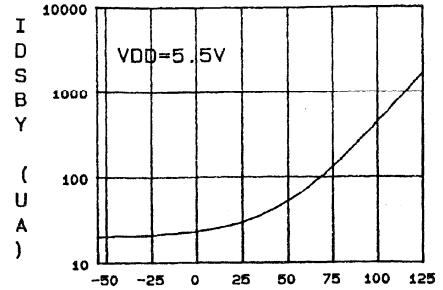
OUTPUT VOLTAGE VS CURRENT



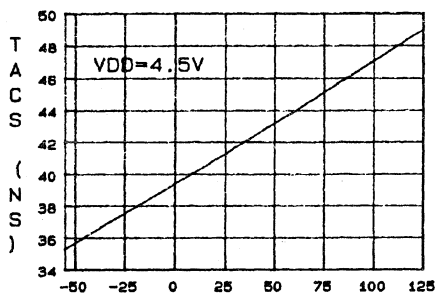
DYNAMIC CURRENT VS TEMPERATURE



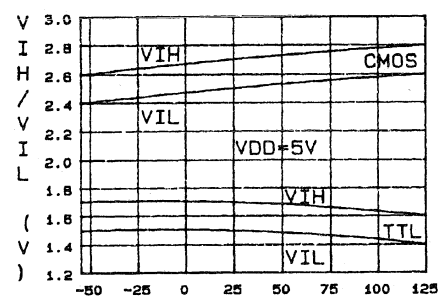
STANDBY CURRENT VS TEMPERATURE



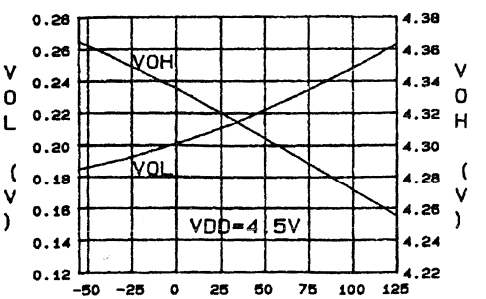
CS ACCESS TIME VS TEMPERATURE



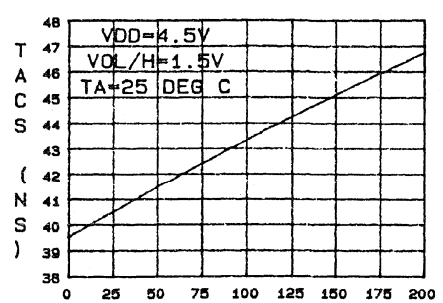
INPUT LEVELS VS TEMPERATURE



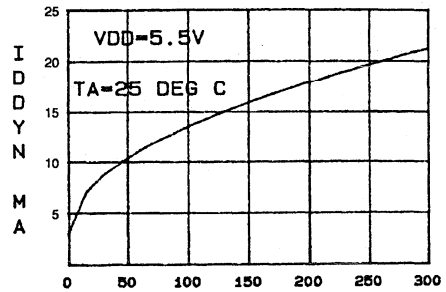
OUTPUT LEVELS VS TEMPERATURE



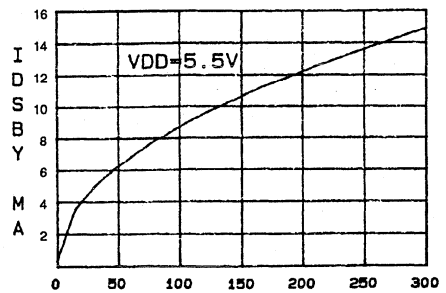
CS ACCESS TIME VS OUTPUT LOAD



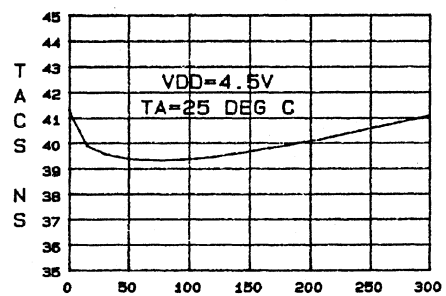
DYNAMIC CURRENT VS RADIATION



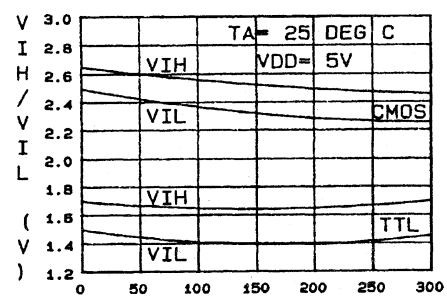
STANDBY CURRENT VS RADIATION



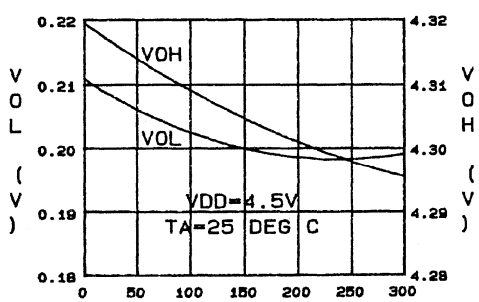
CS ACCESS TIME VS RADIATION



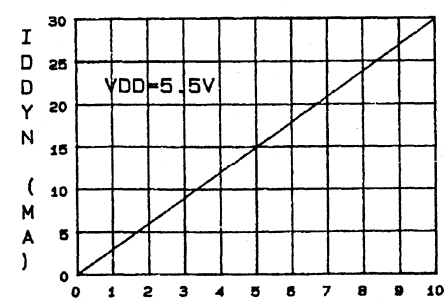
INPUT LEVELS VS RADIATION



OUTPUT LEVELS VS RADIATION



DYNAMIC CURRENT VS FREQUENCY



PIN ASSIGNMENTS

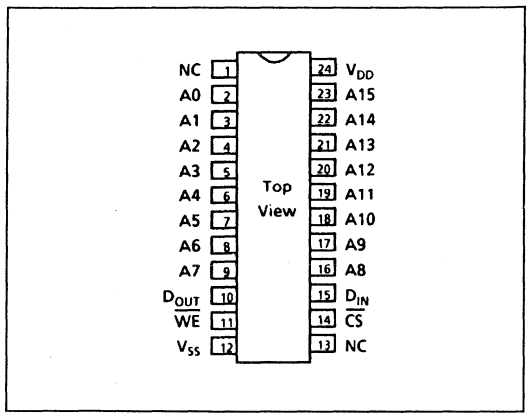


Figure 14: 24 Lead Ceramic DIL (Solder Seal) - Package Style C

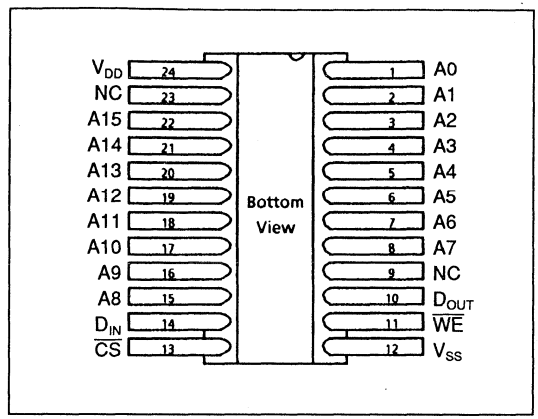


Figure 15: 24 Lead Ceramic Flatpack (Solder Seal) - Package Style B

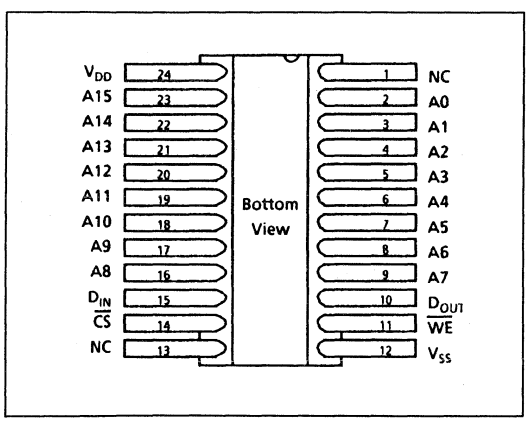


Figure 16: 24 Lead Ceramic Flatpack (Solder Seal) - Package Style F

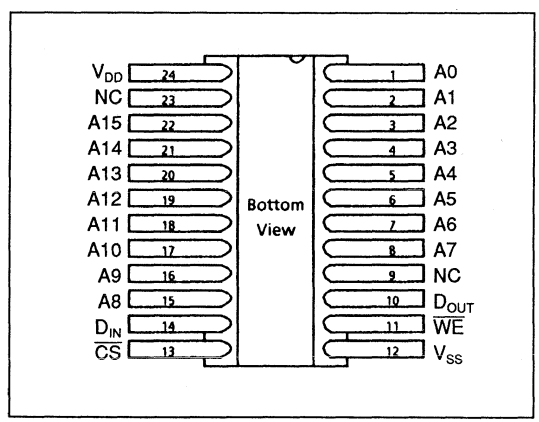


Figure 17: 24 Lead Ceramic Flatpack (Solder Seal) - Package Style Y

OUTLINES Dimensions are shown in mm (in)

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	30.79	-	-	1.212
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG403

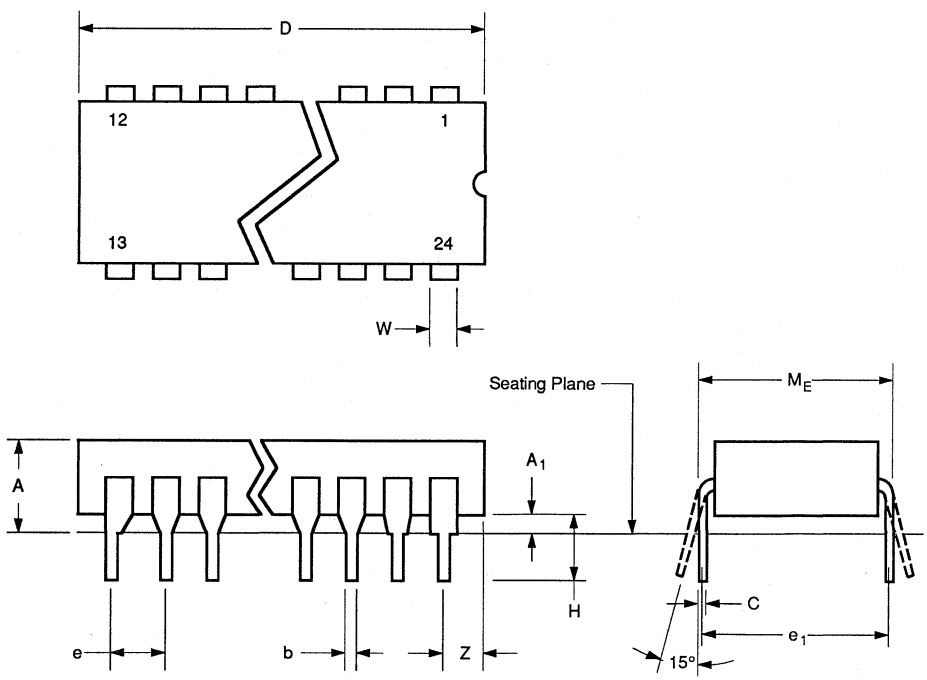
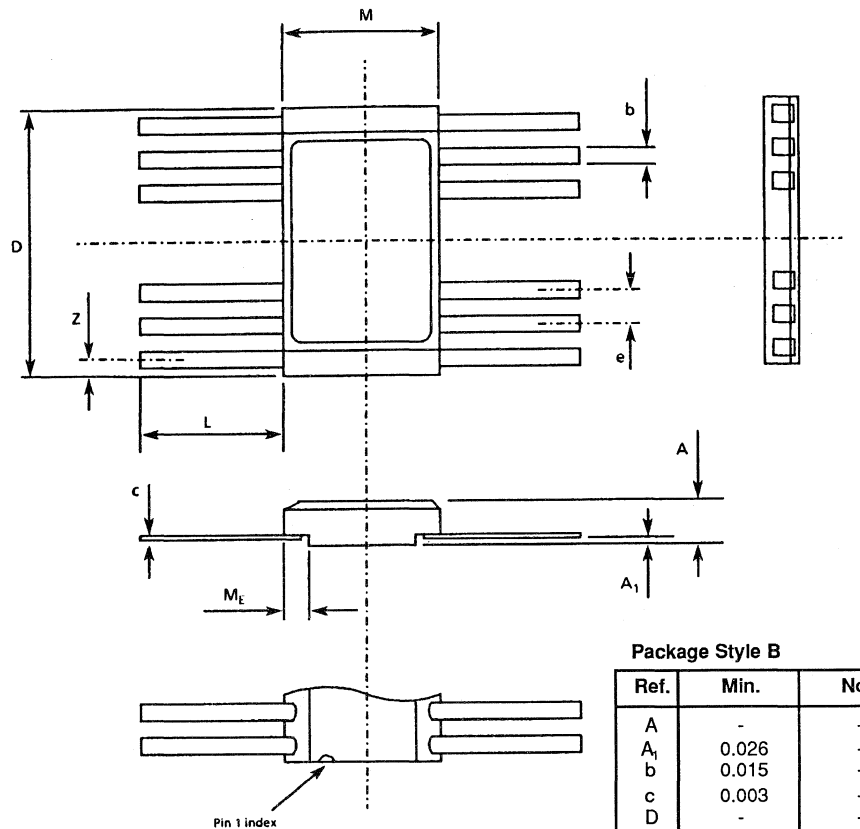


Figure 18: 24 Lead Ceramic DIL (Solder Seal) - Package Style C



Package Style B

Ref.	Min.	Nom.	Max.
A	-	-	0.115
A_1	0.026	-	0.035
b	0.015	-	0.019
c	0.003	-	0.006
D	-	-	0.600
e	-	0.050 Typ.	-
L	0.385	-	0.405
M	0.392	-	0.408
M_E	0.030	-	-
Z	0.005	-	0.045

Dimensions in inches

XG745

Package Style F

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.07	-	-	0.121
A1	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.08	-	0.152	0.003	-	0.006
D	14.99	-	15.50	0.590	-	0.610
e	-	2.54	-	-	0.050	-
L	6.73	-	7.75	0.265	-	0.305
M	9.96	-	10.36	0.392	-	0.408
Me	7.6	-	-	0.30	-	-
Z	0.13	-	1.14	0.005	-	0.045

XG544

Package Style Y

Ref.	Min.	Nom.	Max.
A	-	-	0.115
A_1	0.026	-	0.035
b	0.015	-	0.019
c	0.003	-	0.006
D	-	-	0.600
e	-	0.050 Typ.	-
L	0.330	-	-
M	0.392	-	0.408
M_E	0.030	-	-
Z	0.005	-	0.045

Dimensions in inches

XG146

Figure 19: 24 Lead Ceramic Flatpack (Solder Seal) - Package Styles B, F and Y

Function	Pin Number		Via	Static 1	Static 2	Dynamic	Radiation
	Pkg. Opt.	Pkg. Opt.					
A0	1	2	R1	0V	6v	F2	5V
A1	2	3	R1	0V	6v	F3	5V
A2	3	4	R1	0V	6v	F4	5V
A3	4	5	R1	0V	6v	F5	5V
A4	5	6	R1	0V	6v	F6	5V
A5	6	7	R1	0V	6v	F7	5V
A6	7	8	R1	0V	6v	F8	5V
A7	8	9	R1	0V	6v	F9	5V
DOUT	10	10	R2	0V	6v	3V	5V
WEB	11	11	R1	0V	6v	F0	5V
VSS	12	12	Direct	0V	0V	0V	0V
CSB	13	14	R1	0V	6v	F18	5V
DIN	14	15	R1	0V	6v	F1	5V
A8	15	16	R1	0V	6v	F10	5V
A9	16	17	R1	0V	6v	F11	5V
A10	17	18	R1	0V	6v	F12	5V
A11	18	19	R1	0V	6v	F13	5V
A12	19	20	R1	0V	6v	F14	5V
A13	20	21	R1	0V	6v	F15	5V
A14	21	22	R1	0V	6v	F16	5V
A15	22	23	R1	0V	6v	F17	5V
VDD	24	24	Direct	6v	6v	6v	5V

1. Static 1, Static 2 and Dynamic: R1=1k2, R2=330Ω
2. Radiation: R1 =10k, R2=10k
3. F0=100kHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.

Figure 20: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$4.3x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 21: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

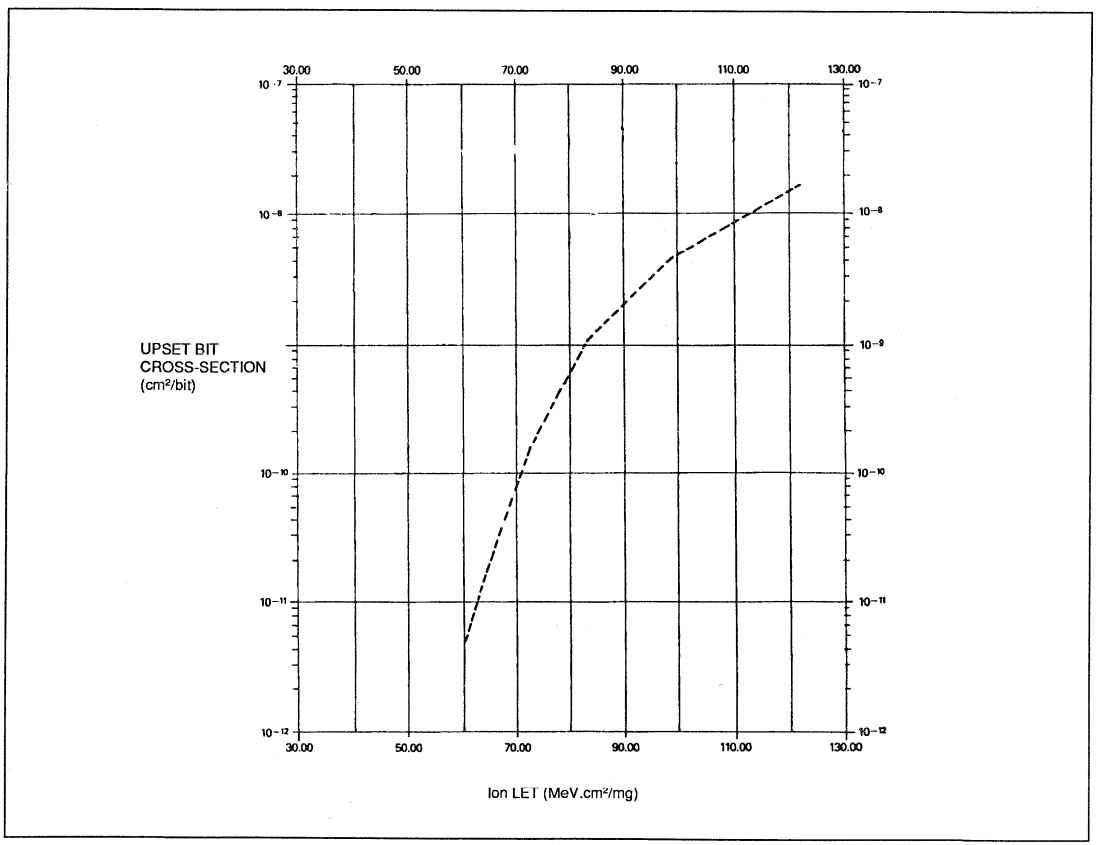
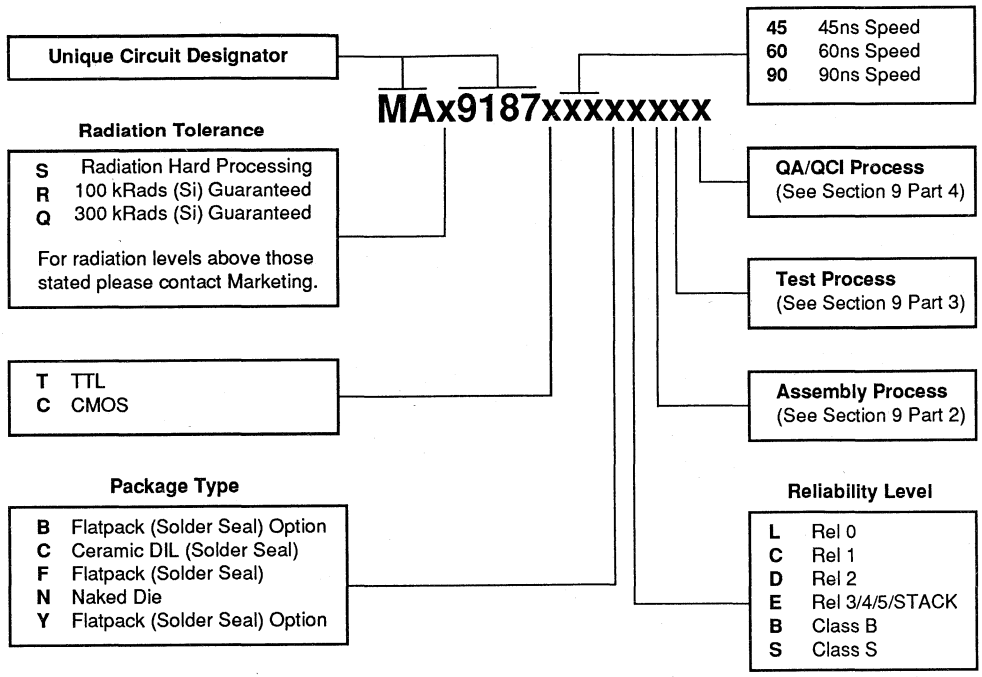


Figure 22: Typical Per-Bit Upset Cross-Section v Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA9264

RADIATION HARD 8192 x 8 BIT STATIC RAM

The MA9264 64k Static RAM is configured as 8192x8 bits and manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

See Application Note "Overview of the GPS Radiation Hard 1.5µm CMOS/SOS SRAM Range".

Operation Mode	$\overline{CS}$	CE	$\overline{OE}$	$\overline{WE}$	I/O	Power
Read	L	H	L	H	D OUT	
Write	L	H	X	L	D IN	ISB1
Output Disable	L	H	H	H	High Z	
Standby	H	X	X	X	High Z	ISB2
	X	L	X	X	X	

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 70ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{11} Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation

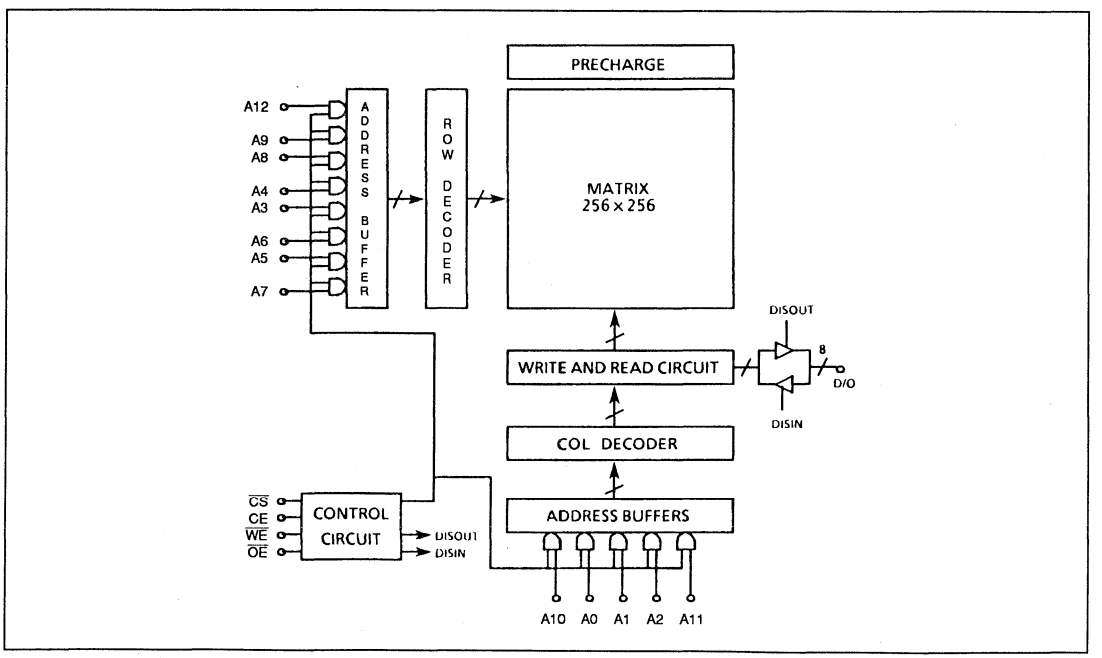


Figure 2: Block Diagram

SIGNAL DEFINITIONS

A0-12
Address input pins which select a particular eight bit word within the memory array.

D0-7
Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

$\overline{CS}$
Chip Select, which, at low level, activates a read or write operation. When at a high level it defaults the SRAM to a prechargencondition and holds the data output drivers in a high impedance state.

$\overline{WE}$
Write Enable which when at a low level enables a write and holds data output drivers in a high impedance state. When at a high level, it enables a read.

$\overline{OE}$
Output Enable which when at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by $\overline{CS}$, $\overline{WE}$ and CE. If this signal is not used it must be connected to VSS.

CE
Chip Enable which when at a high level allows normal operation. When at a low level it defaults the SRAM to a precharge condition, disables the input circuits on all input pins and holds the data output drivers in a high impedance state. If this signal is not used it must be connected to VDD.

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -2mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -1mA	V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 4mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{CS}$ = V_{SS} +0.2V	-	0.1	10	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	-	6	18	mA
I_{SB2}	Standby Supply Current	$\overline{CS}$ = V_{DD} -0.2V CE = V_{SS} +0.2V	-	0.1	10	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}, CE = V_{SS}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V CE = V_{SS}	-	0.05	4	mA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V (TTL) and V_{SS} to 4.0V (CMOS).
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MAX9264X70 Min	MAX9264X70 Max	MAX9264X95 Min	MAX9264X95 Max	Units
T_{AVAVR}	Read Cycle Time	70	-	95	-	ns
T_{AVQV}	Address Access Time	-	65	-	90	ns
T_{EHQV}	Chip Select Access Time	-	70	-	95	ns
T_{SLQV}	Chip Enable Access Time	-	70	-	95	ns
T_{EHQX} (5,6)	Chip Selection to Output in Low Z	15	-	15	-	ns
T_{SLQX} (5,6)	Chip Enable to Output in Low Z	15	-	15	-	ns
T_{ELQZ} (5,6)	Chip Deselection to Output in High Z	0	20	0	20	ns
T_{SHQZ} (5,6)	Chip Disable to Output in High Z	0	20	0	20	ns
T_{AXQX}	Output Hold from Address Change	30	-	40	-	ns
T_{GLQV}	Output Enable Access Time	-	25	-	30	ns
T_{GLQX} (5,6)	Output Enable to Output in Low Z	15	-	15	-	ns
T_{GHQZ} (5,6)	Output Enable to Output in High Z	0	20	0	20	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MAX9264X70 Min	MAX9264X70 Max	MAX9264X95 Min	MAX9264X95 Max	Units
T_{AVAVW}	Write Cycle Tlme	55	-	60	-	ns
T_{EHWH}	Chip Selection to End of Write	50	-	60	-	ns
T_{SLWH}	Chip Enable to End of Write	50	-	60	-	ns
T_{AVWH}	Address Valid to End of Write	50	-	55	-	ns
T_{AVWL}	Address Set Up Time	0	-	0	-	ns
T_{WLWH}	Write Pulse Width	40	-	45	-	ns
T_{WHAV}	Write Recovery Time	0	-	0	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	20	0	20	ns
T_{DVWH}	Data to Write Time Overlap	25	-	30	-	ns
T_{WHDX}	Data Hold from Write	0	-	0	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	0	20	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

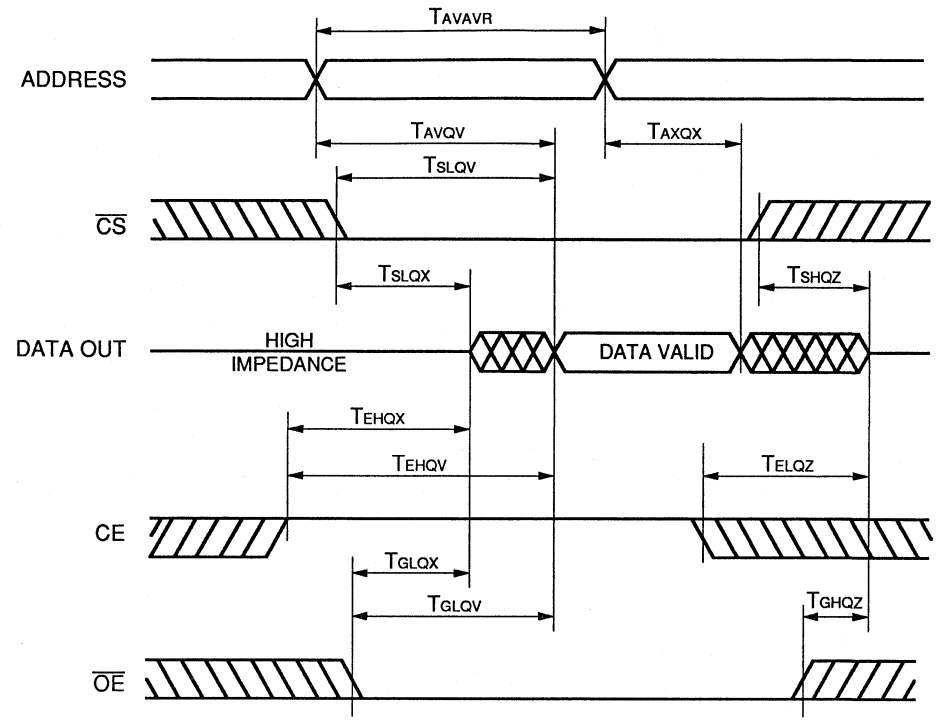
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

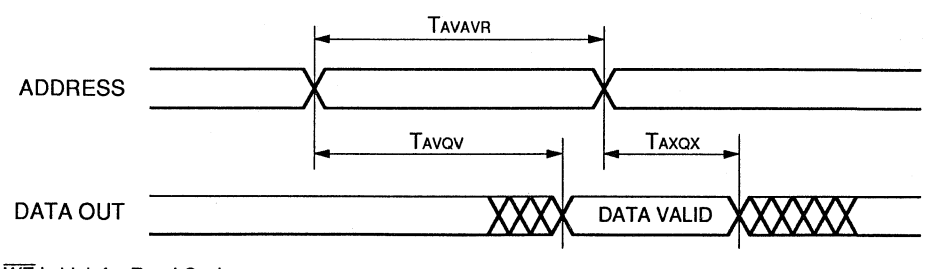
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



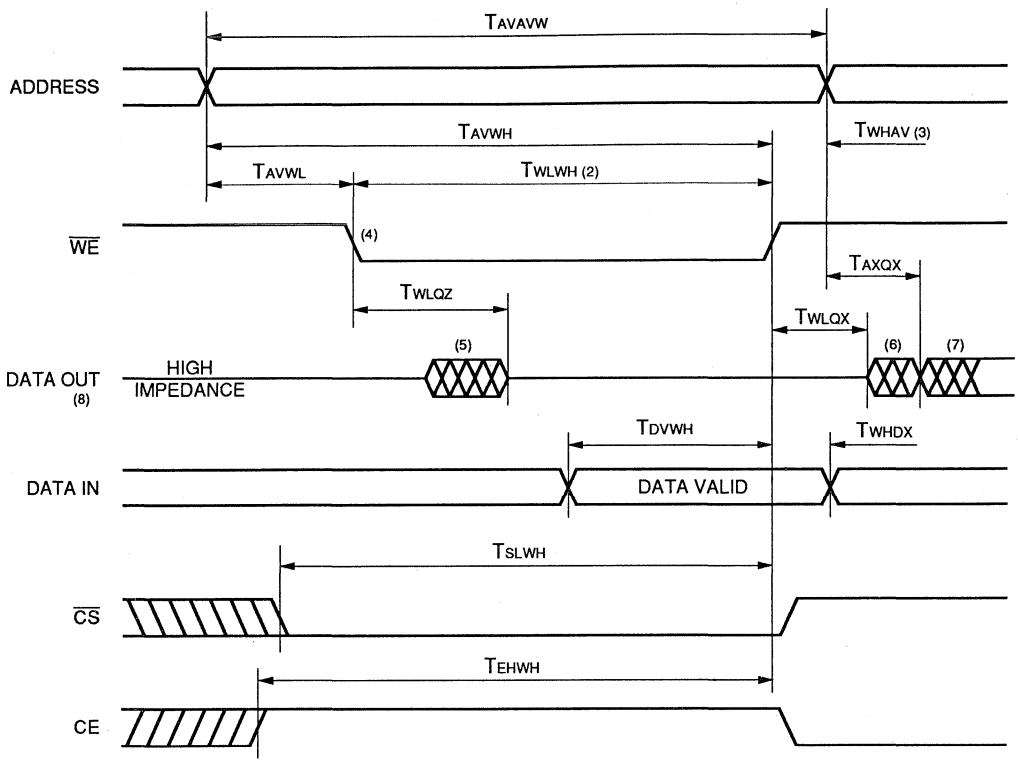
1. $\overline{WE}$ is high for Read Cycle.
2. Address Vaild prior to or coincident with $\overline{CS}$ transition low or CE transition high.

Figure 11a: Read Cycle 1



1. $\overline{WE}$ is high for Read Cycle.
2. Device is continually selected. $\overline{CS}$, $\overline{OE}$ low, CE high.

Figure 11b: Read Cycle 2

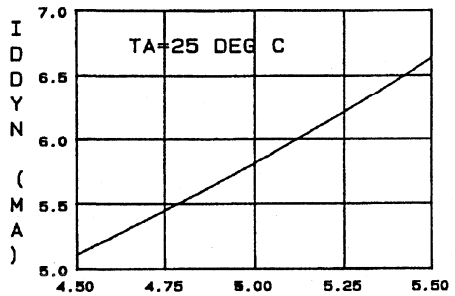


1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$, a high CE and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high or CE going low, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low or CE high transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is in the active state, so DATA IN must not be in the opposing state.
6. DATA OUT is the write data of the current cycle, if selected.
7. DATA OUT is the read data of the next address,if selected.
8. $\overline{OE}$ is low. (If $\overline{OE}$ is high then DATA OUT remains in the high impedance state throughout the cycle).

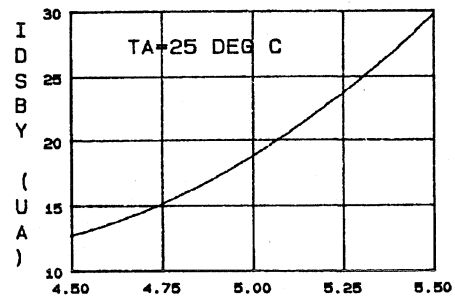
Figure 12: Write Cycle

TYPICAL PERFORMANCE CHARACTERISTICS MAx9264x70

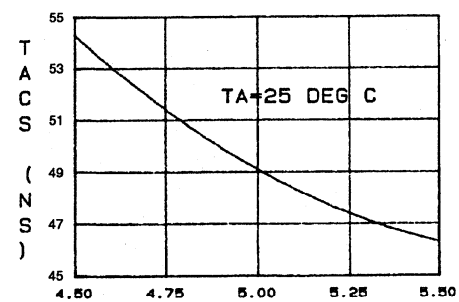
DYNAMIC CURRENT VS SUPPLY VOLTAGE



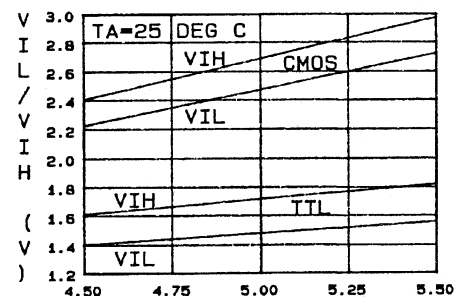
STANDBY CURRENT VS SUPPLY VOLTAGE



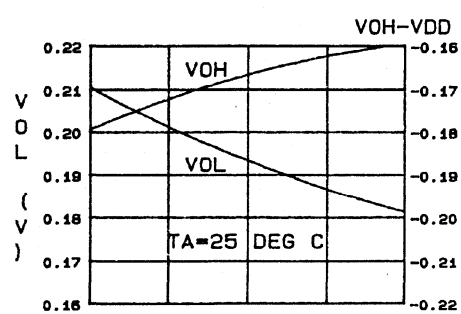
CS ACCESS TIME VS SUPPLY VOLTAGE



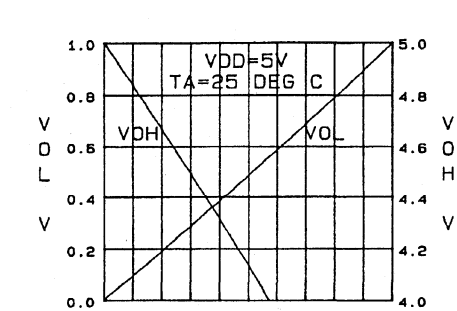
INPUT LEVELS VS SUPPLY VOLTAGE



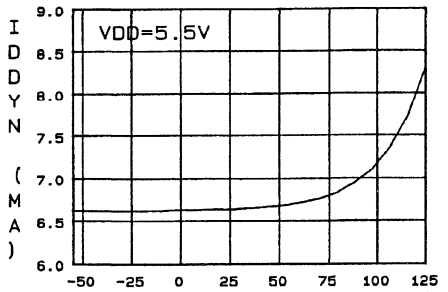
OUTPUT LEVELS VS SUPPLY VOLTAGE



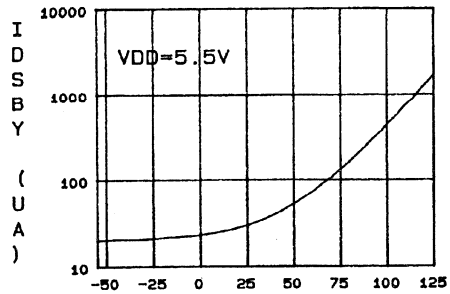
OUTPUT VOLTAGE VS CURRENT



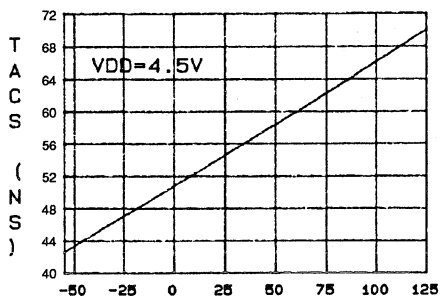
DYNAMIC CURRENT VS TEMPERATURE



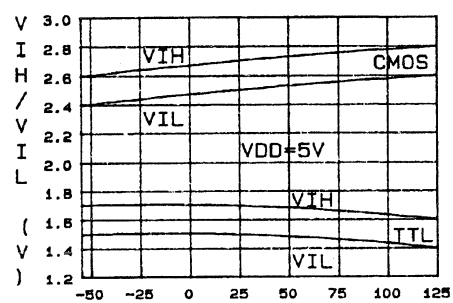
STANDBY CURRENT VS TEMPERATURE



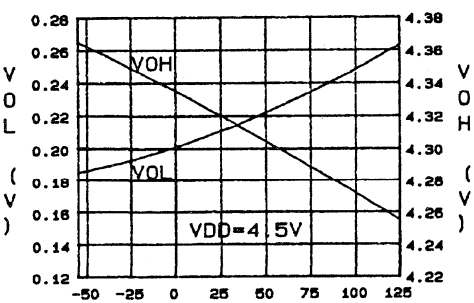
CS ACCESS TIME VS TEMPERATURE



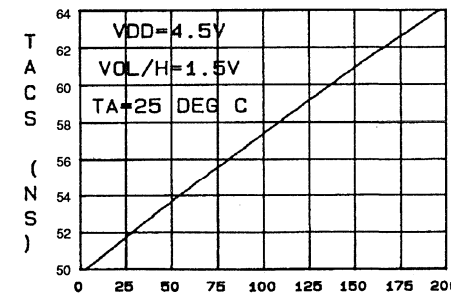
INPUT LEVELS VS TEMPERATURE



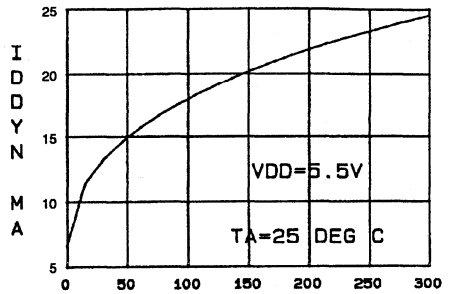
OUTPUT LEVELS VS TEMPERATURE



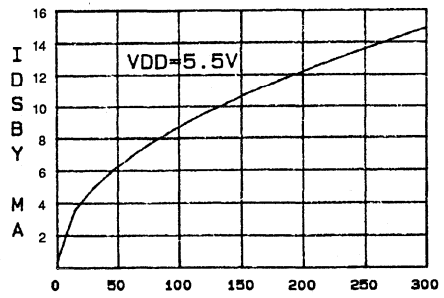
CS ACCESS TIME VS OUTPUT LOAD



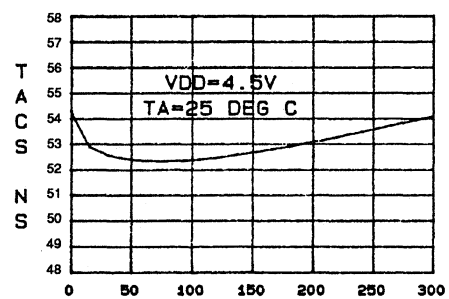
DYNAMIC CURRENT VS RADIATION



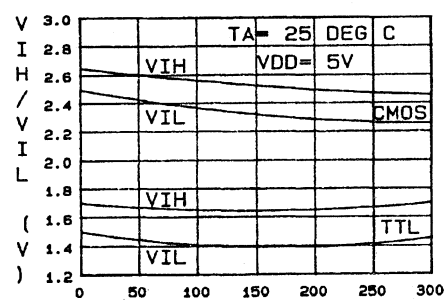
STANDBY CURRENT VS RADIATION



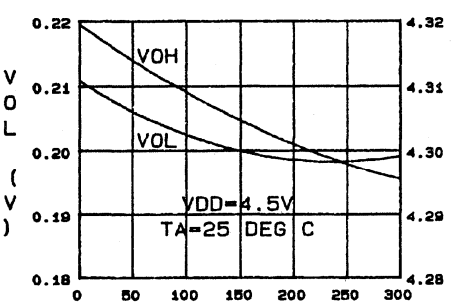
CS ACCESS TIME VS RADIATION



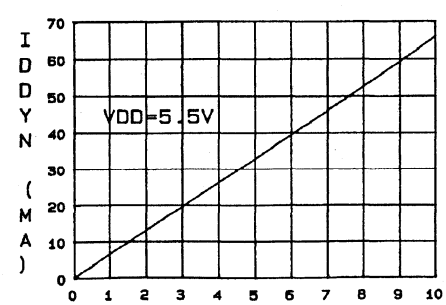
INPUT LEVELS VS RADIATION



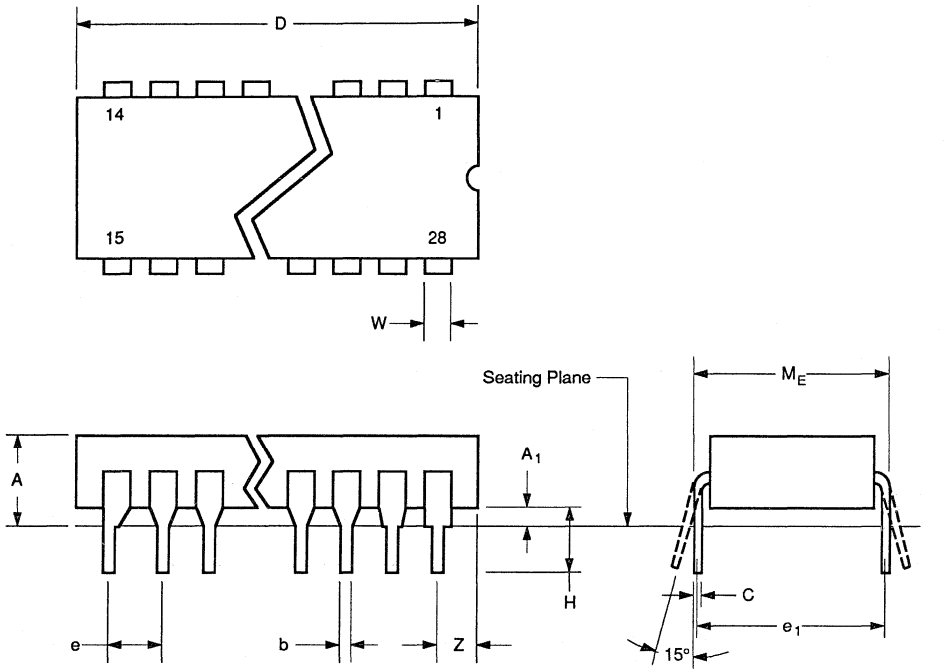
OUTPUT LEVELS VS RADIATION



DYNAMIC CURRENT VS FREQUENCY



OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

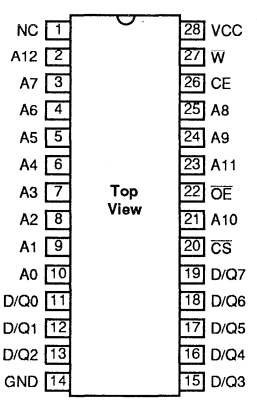
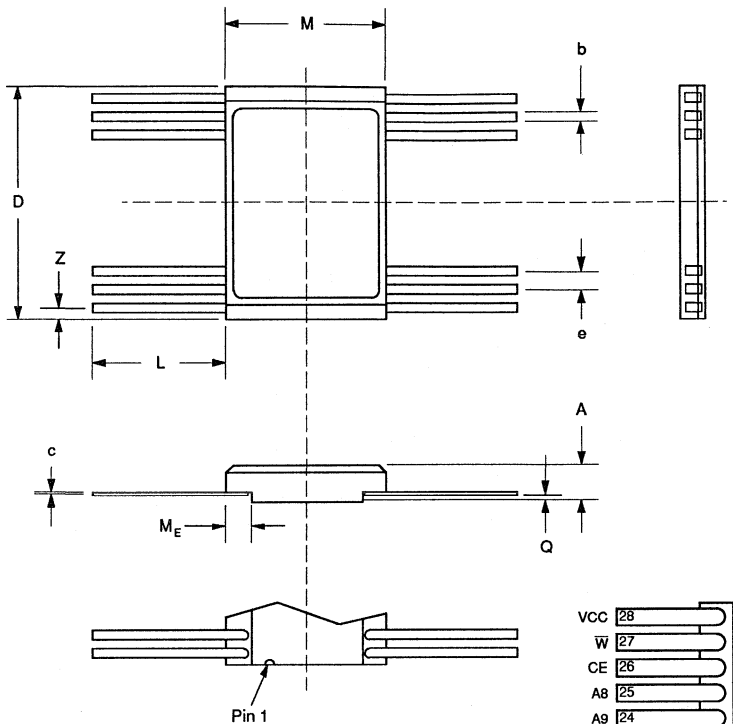
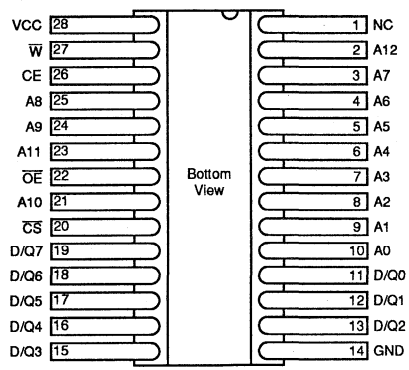


Figure 13: 28-Lead Ceramic DIL (Solder Seal) - Package Style C





Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.18	-	-	0.125
Q	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.10	-	0.18	0.004	-	0.007
D	18.08	-	18.49	0.712	-	0.728
e	-	1.27	-	-	0.050	-
L	7.62	-	9.91	0.300	-	0.390
M	12.50	-	12.09	0.492	-	0.508

XG530

Figure 14: 28-Lead Ceramic Flatpack (Solder Seal) - Package Style F

Function	Pin Number Option D and F	Via	Static 1	Static 2	Dynamic	Radiation
A12	2	R	5V	0V	F14	5V
A7	3	R	5V	0V	F7	5V
A6	4	R	5V	0V	F9	5V
A5	5	R	5V	0V	F8	5V
A4	6	R	5V	0V	F11	5V
A3	7	R	5V	0V	F10	5V
A2	8	R	5V	0V	F5	5V
A1	9	R	5V	0V	F4	5V
A0	10	R	5V	0V	F3	5V
D/Q0	11	R	5V	0V	F1	5V
D/Q1	12	R	5V	0V	F1	5V
D/Q2	13	R	5V	0V	F1	5V
GND(VSS)	14	Direct	0V	0V	0V	0V
D/Q3	15	R	5V	0V	F1	5V
D/Q4	16	R	5V	0V	F1	5V
D/Q5	17	R	5V	0V	F1	5V
D/Q6	18	R	5V	0V	F1	5V
D/Q7	19	R	5V	0V	F1	5V
CSB	20	R	5V	0V	F15	5V
A10	21	R	5V	0V	F2	5V
OEB	22	R	5V	0V	F15	5V
A11	23	R	5V	0V	F6	5V
A9	24	R	5V	0V	F13	5V
A8	25	R	5V	0V	F12	5V
CE	26	R	5V	0V	F15B	5V
WB	27	R	5V	0V	F0	5V
VDD	28	Direct	5V	5V	5V	5V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Static 1, Static 2 and Dynamic: R=4k7.
3. Radiation: R=10k.

Figure 15: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$4.3x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 16: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

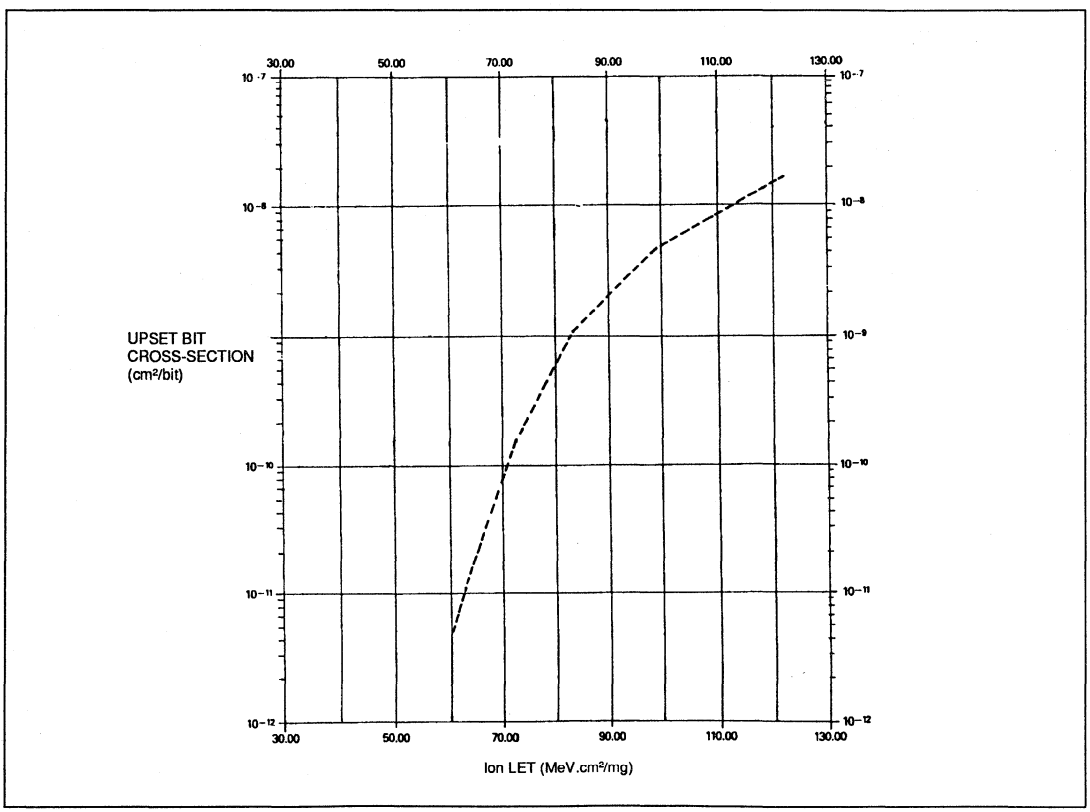
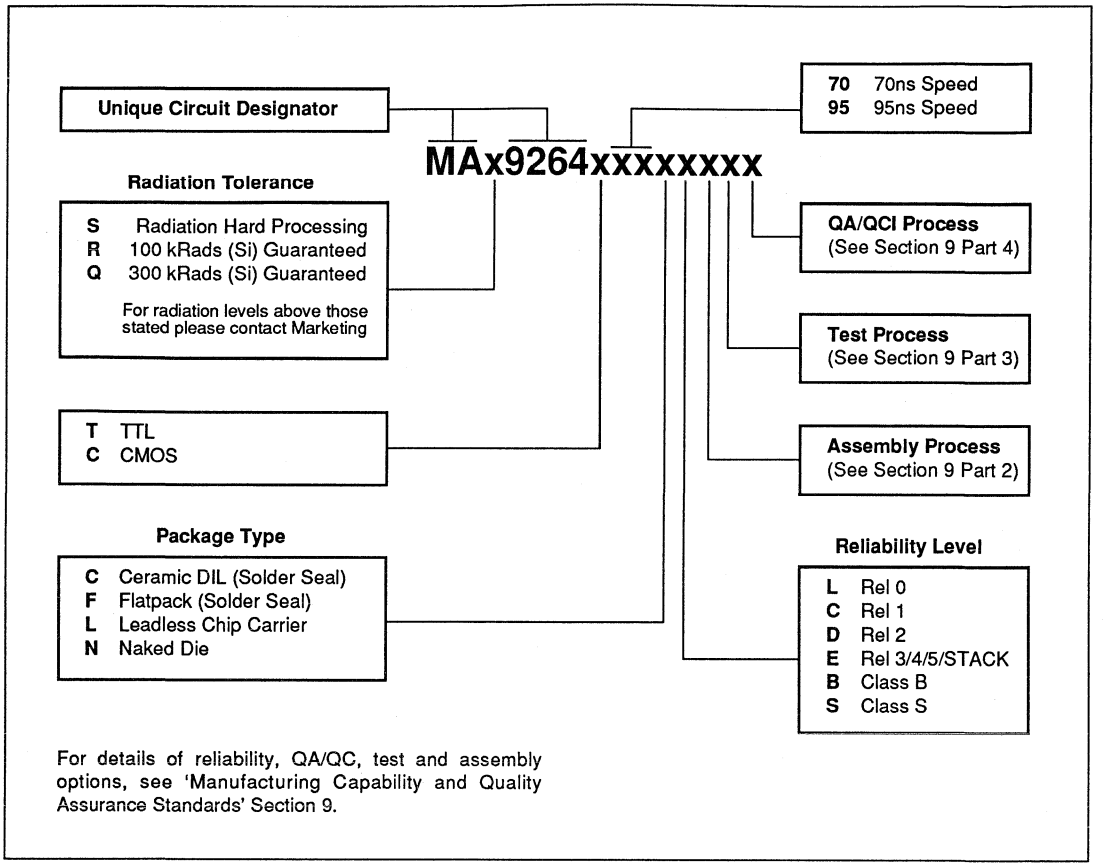


Figure 17: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA9564

HIGH TRANSIENT/RADIATION HARD 8192 x 8 BIT STATIC RAM

The MA9564 64k Static RAM is configured as 8192 x 8 bits and manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology. The device has been designed specifically for high transient gamma applications and is pin compatible with the Honeywell MC6364 device.

The design uses a 6 transistor cell and has full static operation with no clock or timing strobe required. Address input buffers are deselected when chip select is in the HIGH state.

See Application Note "Overview of the GPS Radiation Hard 1.5µm CMOS/SOS SRAM Range".

Operation Mode	$\overline{CS}$	CE	$\overline{OE}$	$\overline{WE}$	$\overline{AS}$	I/O	Power
Read	L	H	L	H	X	D OUT	
Write	L	H	X	L	X	D IN	ISB1
Output Disable	L	H	H	H	X	High Z	
Standby	H	X	X	X	X	High Z	ISB2
	X	L	X	X	X		

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 70ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset $>10^{12}$ Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Optional Capacitors on Package and Lid to Hold Up Power Rail
- Multiple 5V Supply Pins
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation

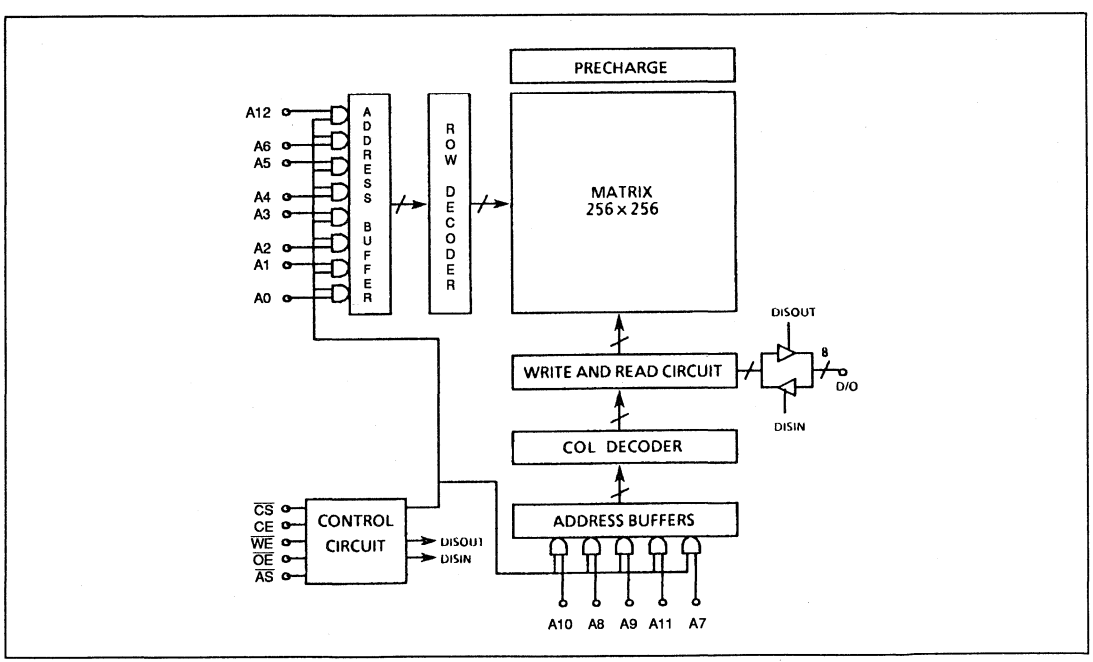


Figure 2: Block Diagram

SIGNAL DEFINITIONS

A0-12
Address input pins which select a particular eight bit word within the memory array.

D0-7
Bidirectional data pins which serve as data outputs during a read operation and as data inputs during a write operation.

$\overline{CS}$
Chip Select, which, at low level, activates a read or write operation. When at a high level it defaults the SRAM to a prechargencondition and holds the data output drivers in a high impedance state.

$\overline{WE}$
Write Enable which when at a low level enables a write and holds data output drivers in a high impedance state. When at a high level, it enables a read.

$\overline{OE}$
Output Enable which when at a high level holds the data output drivers in a high impedance state. When at a low level, data output driver state is defined by $\overline{CS}$, $\overline{WE}$ and CE. If this signal is not used it must be connected to VSS.

$\overline{AS}$
Address Strobe which when at a low level maintains on chip address latches in a transparent state allowing the loading of address inputs. When at a high level, it latches the loaded address state. If this signal is not used it must be connected to VSS,($\overline{AS}$ can be connected to VSS in the package as a pinout option). $\overline{AS}$ can be connected to $\overline{CS}$ during normal operation.

CE
Chip Enable which when at a high level allows normal operation. When at a low level it defaults the SRAM to a precharge condition, disables the input circuits on all input pins and holds the data output drivers in a high impedance state. If this signal is not used it must be connected to VDD, (CE can be connected to VDD in the package as a pinout option).

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Tables 4 and 5:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 8mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{CS}$ = V_{SS} +0.2V	-	0.1	15	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	-	8	23	mA
I_{SB2}	Standby Supply Current	$\overline{CS}$ = V_{DD} -0.2V CE = V_{SS} +0.2V	-	0.1	15	mA

Figure 4: Electrical Characteristics

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ = V_{DR}, CE = V_{SS}	2.0	-	-	V
I_{DDR}	Data Retention Current	$\overline{CS}$ = V_{DR}, V_{DR} = 2.0V CE = V_{SS}	-	0.05	6	mA

Figure 5: Data Retention Characteristics

AC CHARACTERISTICS

Conditions of Test for Tables 5 and 6:
1. Input pulse = V_{SS} to 3.0V (TTL) and V_{SS} to 4.0V (CMOS).
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state.
6. This parameter is sampled and not 100% tested.

Notes for Tables 6 and 7:
Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	MAX9564X70 Min	MAX9564X70 Max	MAX9564X90 Min	MAX9564X90 Max	Units
T_{AVAVR}	Read Cycle Time	70	-	90	-	ns
T_{AVQV}	Address Access Time	-	65	-	85	ns
T_{EHQV}	Chip Select Access Time	-	70	-	90	ns
T_{SLQV}	Chip Enable Access Time	-	70	-	90	ns
T_{EHQX} (5,6)	Chip Selection to Output in Low Z	15	-	15	-	ns
T_{SLQX} (5,6)	Chip Enable to Output in Low Z	15	-	15	-	ns
T_{ELQZ} (5,6)	Chip Deselection to Output in High Z	0	20	0	20	ns
T_{SHQZ} (5,6)	Chip Disable to Output in High Z	0	20	0	20	ns
T_{AXQX}	Output Hold from Address Change	30	-	40	-	ns
T_{GLQV}	Output Enable Access Time	-	25	-	30	ns
T_{GLQX} (5,6)	Output Enable to Output in Low Z	15	-	15	-	ns
T_{GHQZ} (5,6)	Output Enable to Output in High Z	0	20	0	20	ns

Figure 6: Read Cycle AC Electrical Characteristics

Symbol	Parameter	MAX9564X70 Min	MAX9564X70 Max	MAX9564X90 Min	MAX9564X90 Max	Units
T_{AVAVW}	Write Cycle Tlme	50	-	60	-	ns
T_{EHWH}	Chip Selection to End of Write	45	-	55	-	ns
T_{SLWH}	Chip Enable to End of Write	45	-	55	-	ns
T_{AVWH}	Address Valid to End of Write	45	-	55	-	ns
T_{AVWL}	Address Set Up Time	0	-	0	-	ns
T_{WLWH}	Write Pulse Width	35	-	40	-	ns
T_{WHAV}	Write Recovery Time	0	-	0	-	ns
T_{WLQZ} (5,6)	Wnte to Output in High Z	0	20	0	20	ns
T_{DVWH}	Data to Write Time Overlap	25	-	30	-	ns
T_{WHDX}	Data Hold from Write	0	-	0	-	ns
T_{WHQX} (5,6)	Output Active from End to Write	0	20	0	20	ns

Figure 7: Write Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 8: Capacitance

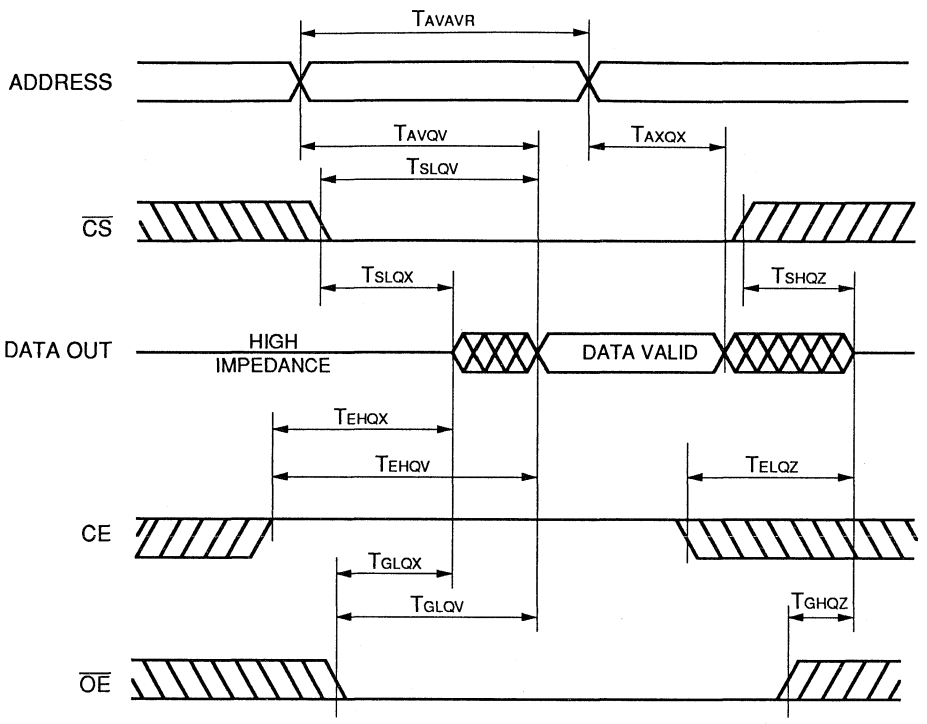
Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Tables 4 and 5 at +25°C
2	Static characteristics specified in Tables 4 and 5 at +125°C
3	Static characteristics specified in Tables 4 and 5 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 6 and 7 at +25°C
10	Switching characteristics specified in Tables 6 and 7 at +125°C
11	Switching characteristics specified in Tables 6 and 7 at -55°C

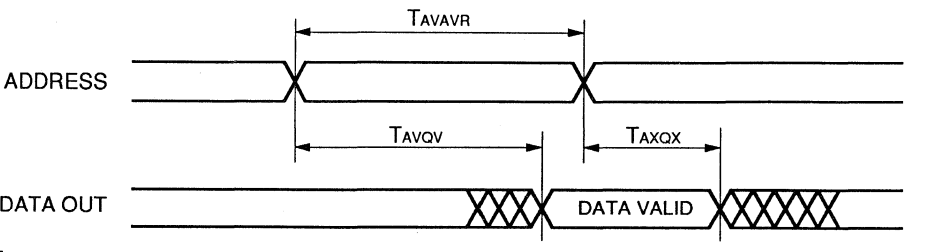
Figure 10: Definition of Subgroups

TIMING DIAGRAMS



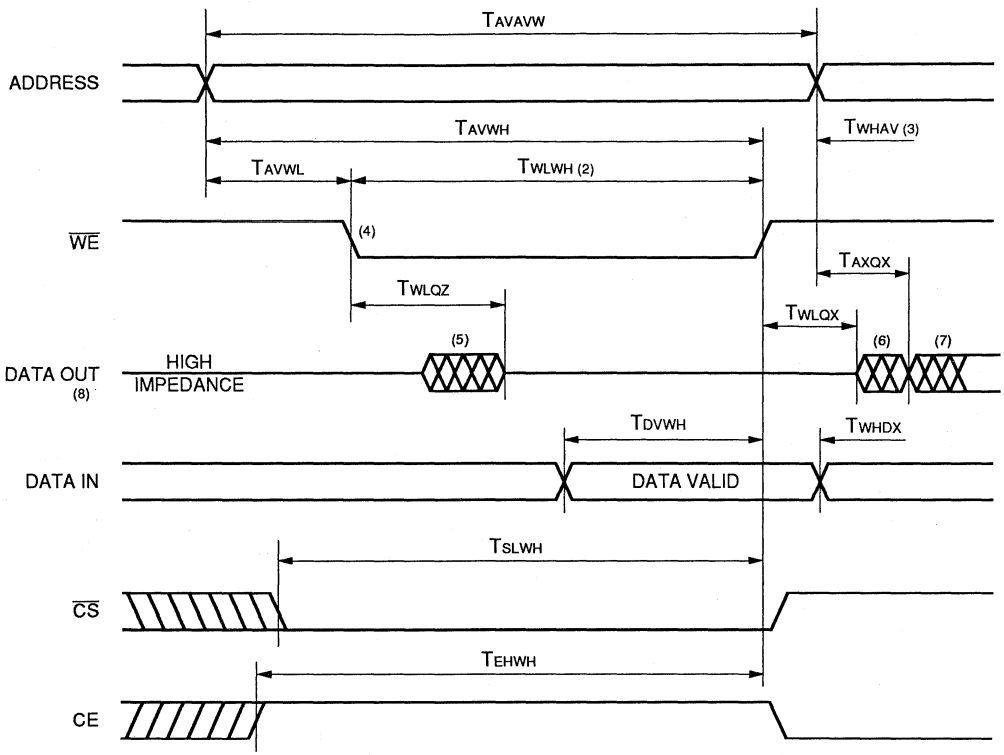
1. WE is high for Read Cycle.
2. Address Vaild prior to or coincident with CS transition low or CE transition high.
3. AS is low.

Figure 11a: Read Cycle 1



1. WE is high for Read Cycle.
2. Device is continually selected. CS, AS, OE low, CE high.

Figure 11b: Read Cycle 2

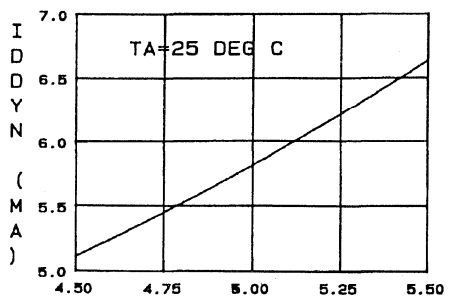


1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (T_{WLWH}) of a low $\overline{CS}$, a high CE and a low $\overline{WE}$.
3. T_{WHAV} is measured from either $\overline{CS}$ or $\overline{WE}$ going high or CE going low, whichever is the earlier, to the end of the write cycle.
4. If the $\overline{CS}$ low or CE high transition occurs simultaneously with, or after, the $\overline{WE}$ low transition, the output remains in the high impedance state.
5. DATA OUT is in the active state, so DATA IN must not be in the opposing state.
6. DATA OUT is the write data of the current cycle, if selected.
7. DATA OUT is the read data of the next address,if selected.
8. $\overline{AS}$ is low. $\overline{OE}$ is low. (If $\overline{OE}$ is high then DATA OUT remains in the high impedance state throughout the cycle).

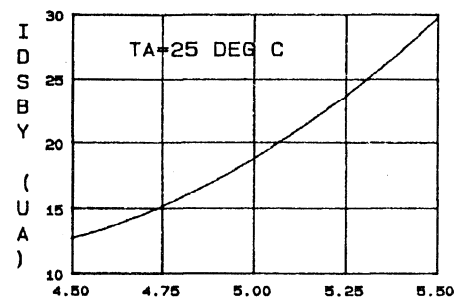
Figure 12: Write Cycle

TYPICAL PERFORMANCE CHARACTERISTICS MAx9564x90

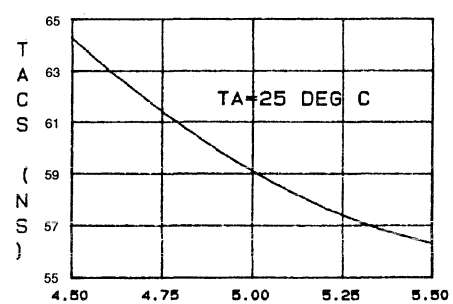
DYNAMIC CURRENT VS SUPPLY VOLTAGE



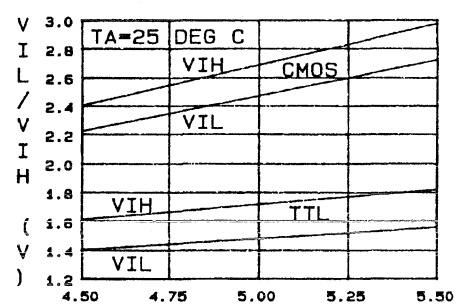
STANDBY CURRENT VS SUPPLY VOLTAGE



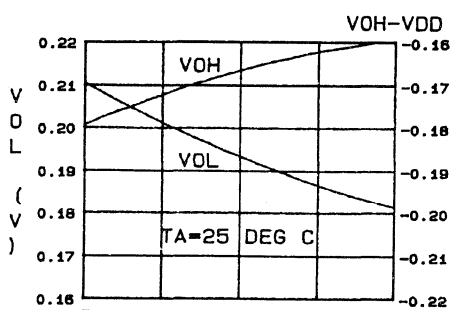
CS ACCESS TIME VS SUPPLY VOLTAGE



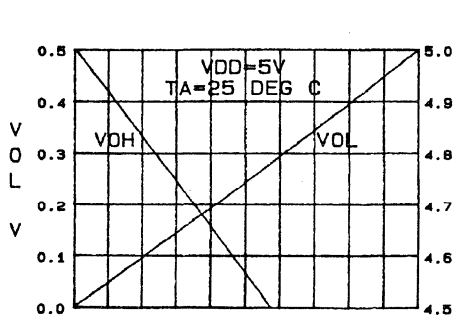
INPUT LEVELS VS SUPPLY VOLTAGE



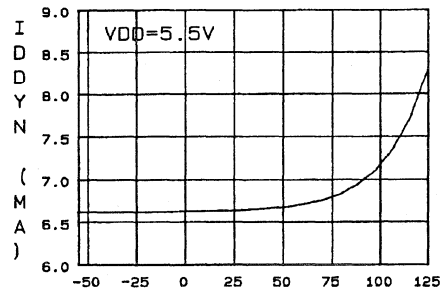
OUTPUT LEVELS VS SUPPLY VOLTAGE



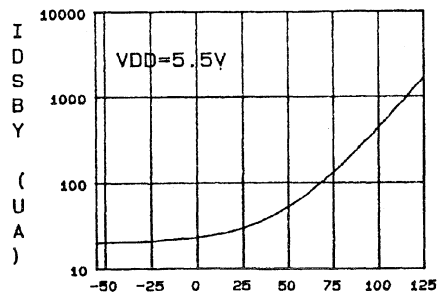
OUTPUT VOLTAGE VS CURRENT



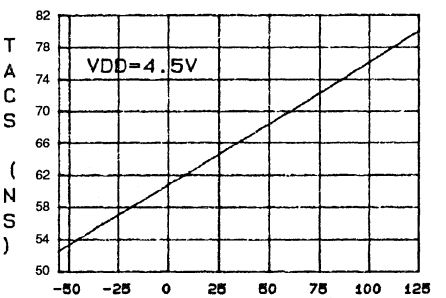
DYNAMIC CURRENT VS TEMPERATURE



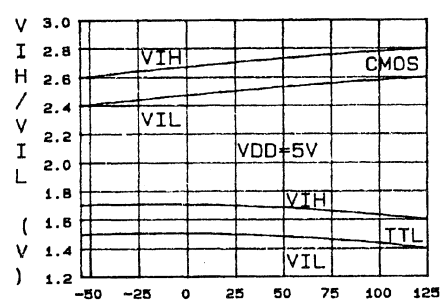
STANDBY CURRENT VS TEMPERATURE



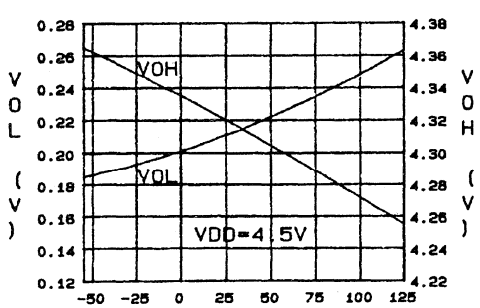
CS ACCESS TIME VS TEMPERATURE



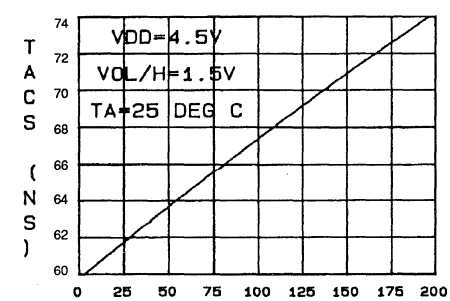
INPUT LEVELS VS TEMPERATURE



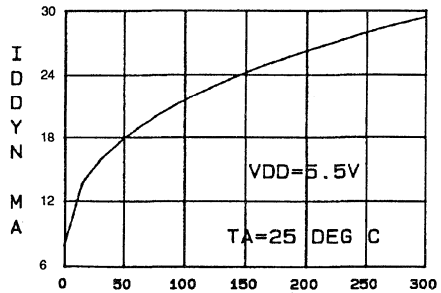
OUTPUT LEVELS VS TEMPERATURE



CS ACCESS TIME VS OUTPUT LOAD

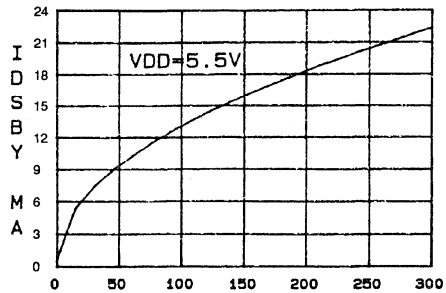


DYNAMIC CURRENT VS RADIATION



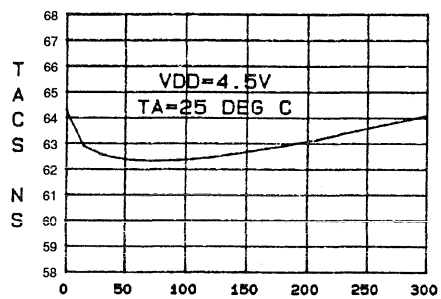
RAD DOSE (KRADS)

STANDBY CURRENT VS RADIATION



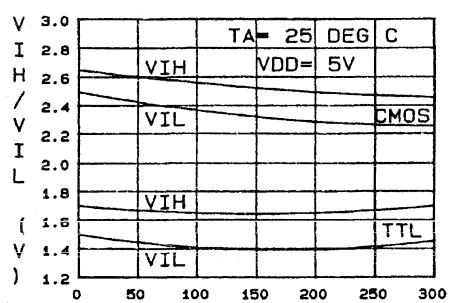
RAD DOSE (KRADS)

CS ACCESS TIME VS RADIATION



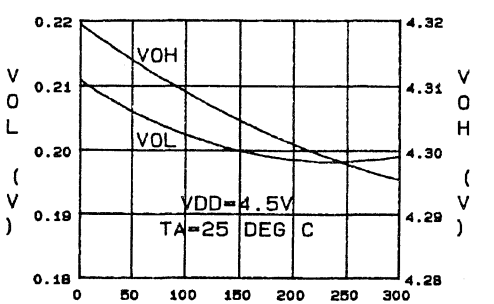
RAD DOSE (KRADS)

INPUT LEVELS VS RADIATION



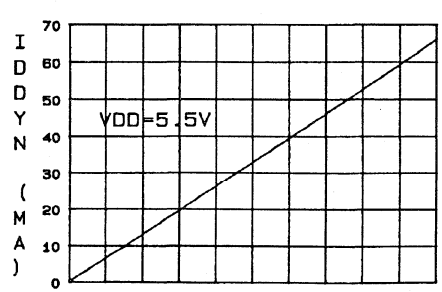
RAD DOSE (KRADS)

OUTPUT LEVELS VS RADIATION



RAD DOSE (KRADS)

DYNAMIC CURRENT VS FREQUENCY



FREQUENCY (MHZ)

PIN ASSIGNMENT

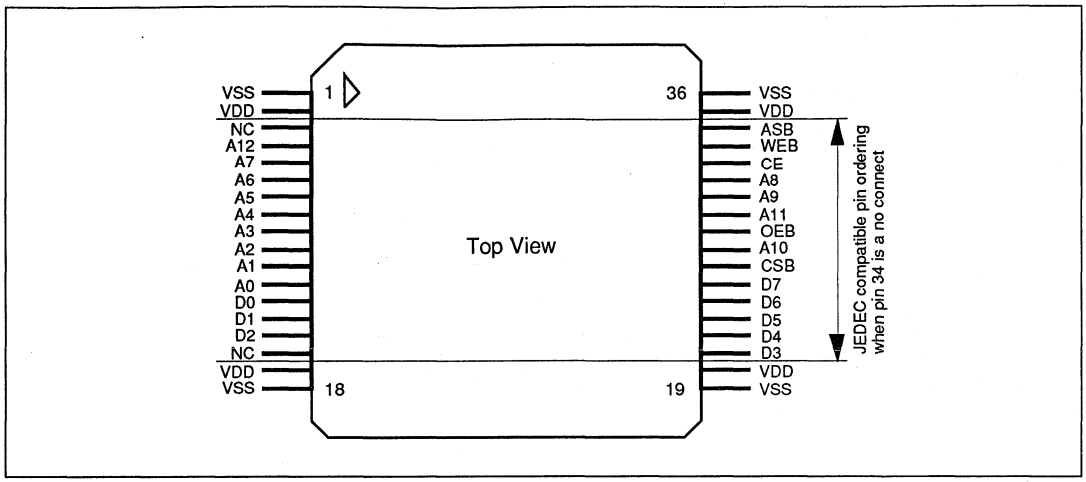


Figure 13: 36 Lead Ceramic Flatpack (Solder Seal) - Package Style F

OUTLINE

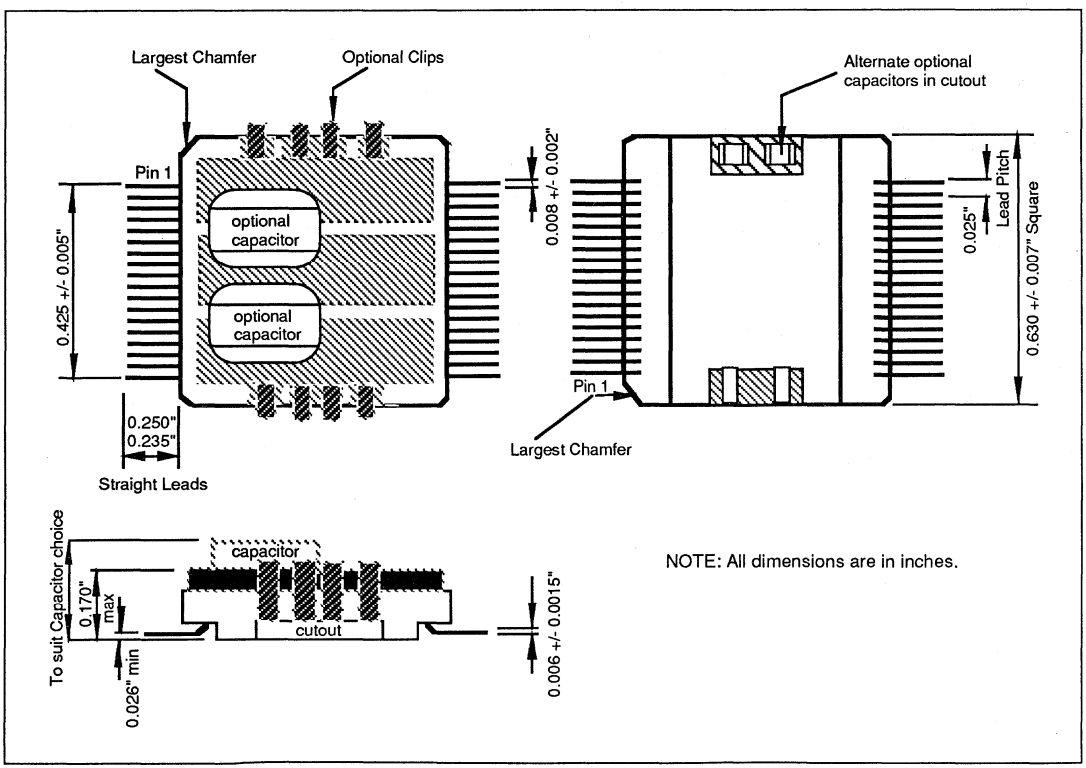


Figure 14: 36 Lead Ceramic Flatpack (Solder Seal) - Package Style F

Pin No.	Function	Connection	Static 1	Static 2	Dynamic	Radiation
1	VSS	DIRECT	0V	0V	0V	0V
2	VDD	DIRECT	5V	5V	5V	5V
4	A12	R	5V	0V	F2	5V
5	A7	R	5V	0V	F3	5V
6	A6	R	5V	0V	F14	5V
7	A5	R	5V	0V	F13	5V
8	A4	R	5V	0V	F12	5V
9	A3	R	5V	0V	F11	5V
10	A2	R	5V	0V	F10	5V
11	A1	R	5V	0V	F9	5V
12	A0	R	5V	0V	F8	5V
13	D0	R	5V	0V	F1	5V
14	D1	R	5V	0V	F1	5V
15	D2	R	5V	0V	F1	5V
17	VDD	DIRECT	5V	5V	5V	5V
18	VSS	DIRECT	0V	0V	0V	0V
19	VSS	DIRECT	0V	0V	0V	0V
20	VDD	DIRECT	5V	5V	5V	5V
21	D3	R	5V	0V	F1	5V
22	D4	R	5V	0V	F1	5V
23	D5	R	5V	0V	F1	5V
24	D6	R	5V	0V	F1	5V
25	D7	R	5V	0V	F1	5V
26	CSB	R	5V	0V	F15	5V
27	A10	R	5V	0V	F4	5V
28	0EB	R	5V	0V	F15	5V
29	A11	R	5V	0V	F7	5V
30	A9	R	5V	0V	F6	5V
31	A8	R	5V	0V	F5	5V
32	CE	R	5V	0V	F15B	5V
33	WEB	R	5V	0V	F0	5V
34	ASB	R	5V	0V	F15	5V
35	VDD	DIRECT	5V	5V	5V	5V
36	VSS	DIRECT	0V	0V	0V	0V

1. F0=150KHz, F1=F0/2, F2=F0/4, F3=F0/8 etc.
2. Static 1, Static 2 and Dynamic: R=4k7.
3. Radiation: R=10k.

Figure 15: Burnin and Radiation Configuration

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{12}$ Rad(Si)/sec
Transient Upset (Survivability)	$>5x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$4.3x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 16: Radiation Hardness Parameters

SINGLE EVENT UPSET CHARACTERISTICS

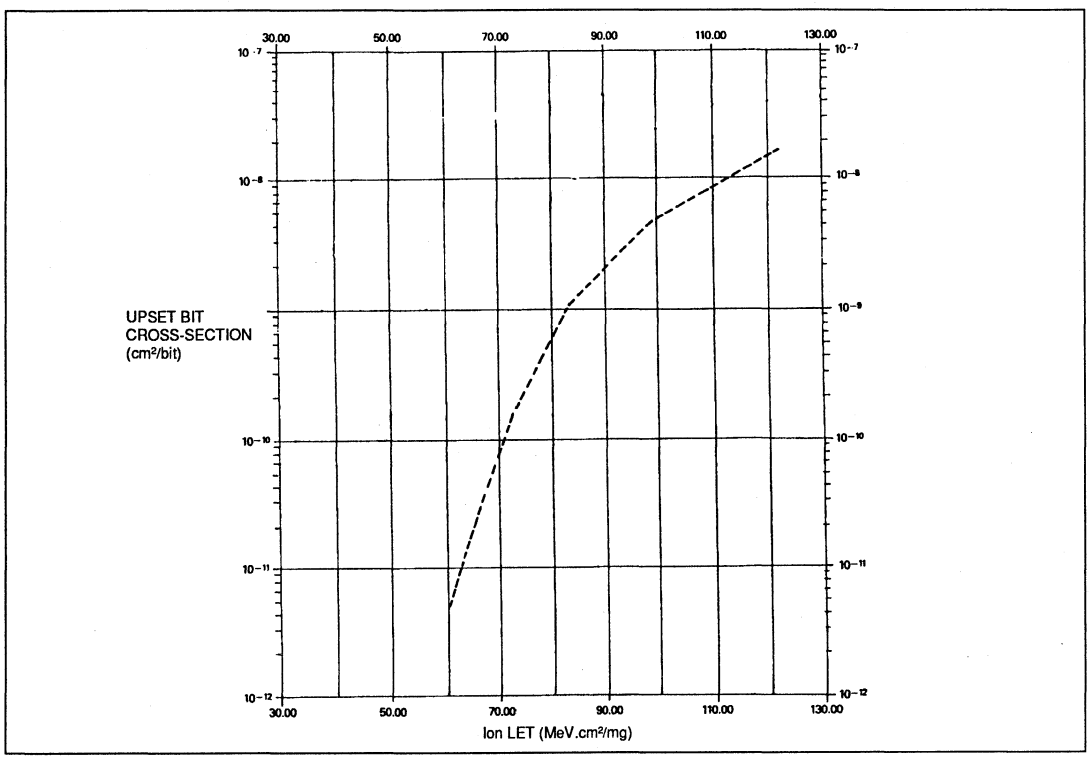
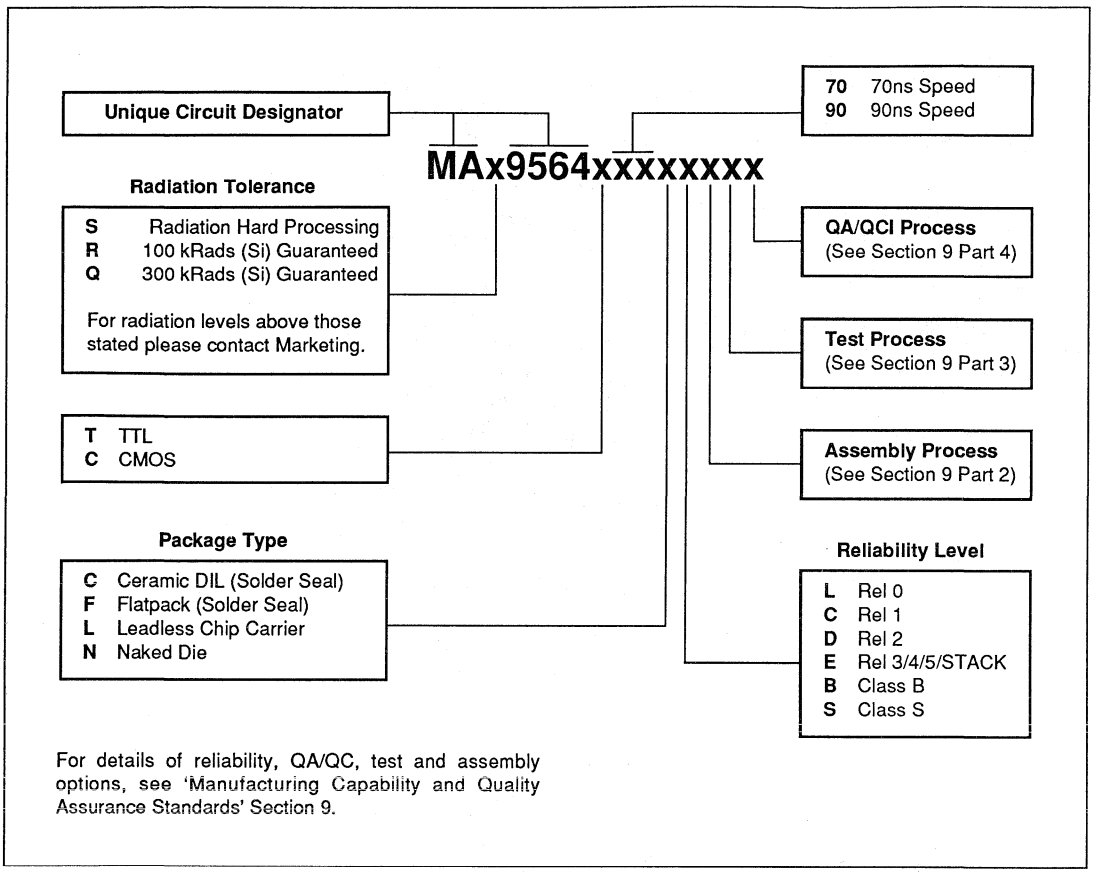


Figure 17: Typical Per-Bit Upset Cross-Section vs Ion LET

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3518-3.2

MA7001

RADIATION HARD 512 x 9 BIT FIFO

The MA7001 512 x 9 FIFO is manufactured using GPS's CMOS-SOS high performance, radiation hard, 3µm technology.

The GPS Silicon-on-Sapphire process provides significant advantages over bulk silicon substrate technologies In addition to very good total dose hardness and neutron hardness >10^{15}n/cm^2, the GPS technology provides very high transient gamma and single event upset performance without compromising speed of operation The Sapphire substrate also eliminates latch-up giving greater flexibility of use in electrically severe environments.

The MA7001 implements a First-In First-Out algorithm that reads and writes data on a first-in first-out basis. The dual-port static RAM memory is organised as 512 words of 9 bits (8 bit data and 1 bit for parity or control purposes).

Sequential read and write accesses are achieved using a ring pointer architecture that requires no external addressing information. Data is toggled in and out of the device by using the WRITE ($\overline{W}$) and READ ($\overline{R}$) pins.

Full and Empty status flags prevent data overflow and underflow. Expansion logic on the device allows for unlimited expansion capability in both word size and depth. A RETRANSMIT ($\overline{RT}$) feature allows for reset of the read pointer to its initial position to allow retransmission of data.

The device is designed for applications requiring asynchronous and simultaneous read/write in multiprocessing and rate buffering (sourcing and sinking data at different rates eg. interfacing fast processors and slow peripherals).

FEATURES

- Radiation Hard CMOS-SOS Technology
- Fast Access Time 60ns Typical
- Single 5V Supply
- Inputs Fully TTL and CMOS Compatible
- -55°C to +125°C Operation

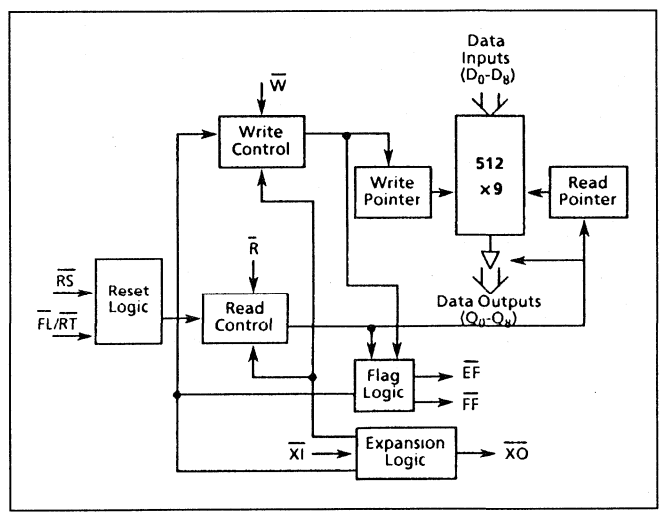


Figure 1: Block Diagram

DC CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	-0.5	7.0	V
V_{IN}	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not Implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 2: Absolute Maximum Ratings

The following D.C. and A.C. electrical characteristics apply to pre-radiation at T_A = -55°C to +125°C, V_{DD} = 5V ±10% and post 100kRad(Si) total dose radiation at T_A = 25°C, V_{DD} = 5V ±10%. GROUP A SUBGROUP 1, 2, 3.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input logic '1' voltage	-	2.0	-	-	V
V_{IL}	Input logic '0' voltage	-	-	-	0.8	V
I_{IL}	Input leakage current (any input) (Note 4)	Note 1	-10	-	10	µA
I_{OL}	Output leakage current (Note 4)	Note 2	-50	-	50	µA
V_{OH}	Output logic '1' voltage	I_{OUT} = -1mA	2.4	-	-	V
V_{OL}	Output logic '0' voltage	I_{OUT} = 2mA	-	-	0.4	V
I_{DD1}	Average V_{DD} power supply current (Note 3)	Freq = 10MHz	-	70	100	mA
I_{DD2}	Average standby current (Note 3)	$\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = $V_{DD}/2$	-	8	15	mA
$I_{DD3(L)}$	Powerdown current (Note 3)	All Inputs = V_{DD} -0.2V	-	-	3.0	mA

NOTES:

1. Measurements with $V_{SS} \leq V_{IN} \leq V_{DD}$
2. $\overline{R} > V_{iH}$, $V_{SS} \leq V_{OUT} \leq V_{DD}$
3. I_{DD} measurements are made with outputs open, V_{DD} = 5.5V
4. Guaranteed but not measured at -55°C

Figure 3a: DC Electrical Characteristics

AC CHARACTERISTICS

Characteristics apply to pre-radiation at T_A = -55°C to +125°C, V_{DD} = 5V ±10% and post 100kRad(Si) total dose radiation at T_A = 25°C, V_{DD} = 5V ±10%. GROUP A SUBGROUP 9, 10, 11.

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	110	-	ns
t_A	Access Time	-	100	ns
t_{RR}	Read Recovery Time	25	-	ns
t_{RPW}	Read Pulse Width (Note 2)	85	-	ns
t_{RLZ}	Read Pulse Low to Data Bus at Low Z (Note 3)	10	-	ns
t_{DV}	Data Valid from Read Pulse High	20	-	ns
t_{RHZ}	Read Pulse High to Data Bus at High Z (Note 3)	-	30	ns
t_{WC}	Write Cycle Time	100	-	ns
t_{WPW}	Write Pulse Width (Note 2)	80	-	ns
t_{WR}	Write Recovery Time	20	-	ns
t_{DS}	Data Setup Time	40	-	ns
t_{DH}	Data Hold Time	10	-	ns
t_{RSC}	Reset Cycle Time (Note 3)	100	-	ns
t_{RS}	Reset Pulse Width (Note 2)	80	-	ns
t_{RSR}	Reset Recovery Time (Note 3)	20	-	ns
t_{RTC}	Retransmit Cycle Time (Note 3)	100	-	ns
t_{RT}	Retransmit Pulse Width (Note 2)	80	-	ns
t_{RTR}	Retransmit Recovery Time (Note 3)	20	-	ns
t_{EFL}	Reset to Empty Flag Low	-	100	ns
t_{REF}	Read Low to Empty Flag Low	-	90	ns
t_{RFF}	Read High to Full Flag High	-	70	ns
t_{WEF}	Write High to Empty Flag High	-	70	ns
t_{WFF}	Write Low to Full Flag Low	-	90	ns
t_{EFR}	EF High to Valid Read (Note 3)	10	-	ns
t_{RPI}	Read Protect Indeterminant (Note 3)	-	35	ns
t_{FFW}	FF High to Valid Write (Note 3)	10	-	ns
t_{WPI}	Write Protect Indeterminant (Note 3)	-	35	ns

Notes:
1. Timings referenced as in A.C. Test Conditions, figure 5
2. Pulse widths less than minimum values are not allowed
3. Values guaranteed by design, not currently tested

Figure 3b: AC Characteristics

Symbol	Parameter	Conditions
FT	Functionality	V_{DD} = 3-6V, FREQ = 100kHz - 9MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55 to +125°C, RADIATION 1MRAD TOTAL DOSE GROUP A SUBGROUPS 7, 8A, 8B

Figure 3b: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 3a at +25°C
2	Static characteristics specified in Table 3a at +125°C
3	Static characteristics specified in Table 3a at -55°C
7	Functional characteristics specified in Table 3c at +25°C
8A	Functional characteristics specified in Table 3c at +125°C
8B	Functional characteristics specified in Table 3c at -55°C
9	Switching characteristics specified in Table 3b at +25°C
10	Switching characteristics specified in Table 3b at +125°C
11	Switching characteristics specified in Table 3b at -55°C

Figure 4: Definition of Subgroups

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 7

Figure 5: AC Test Conditions

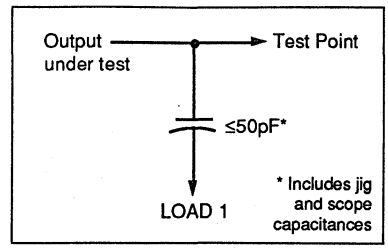


Figure 7: Output Load

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance (Note 1)	V_{IN} = 0V	7	pF
C_{OUT}	Output Capacitance (Notes 1 and 2)	V_{OUT} = 0V	12	pF

NOTES:
1. Characterized values, not currently tested.
2. With output deselected.

Figure 6: Capacitance

TRUTH TABLES

Operation	Input					Output			Pointer	
	$\overline{R}$	$\overline{W}$	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	$\overline{EF}$	$\overline{FF}$	Data	Read	Write
Reset	1	1	0	x	0	0	1	Z	Zero	Zero
Retransmit*	1	1	1	0	0	1	1	Z	Zero	N/C
Read	1→0	x	1	1	0	1	1	valid	Increment	N/C
Read	x	x	1	1	0	0	1	Z	N/C	N/C
Write	x	1→0	1	1	0	x	1	x	N/C	Increment
Write	x	x	1	1	0	1	0	x	N/C	N/C

* Only available if less than 512 writes since last reset.

Figure 8: Single Device or Width Expansion: Read, Write, Reset and Retransmit

Operation	Input					Output			Pointer	
	$\overline{R}$	$\overline{W}$	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	$\overline{EF}$	$\overline{FF}$	Data	Read	Write
Reset First	1	1	0	0	1	0	1	Z	Zero	Zero
Reset Rest	1	1	0	1	1	0	1	Z	Zero	Zero

NOTES:
1. See Modes of Operation for connections of $\overline{XI}$ and $\overline{XO}$ in depth expansion mode.
2. $\overline{XI}$ is connected to $\overline{XO}$ of previous device (Figure 12).

Figure 9: Depth Expansion: Reset and First Load

SIGNAL DESCRIPTIONS

Reset (RS)
Reset occurs when $\overline{RS}$ is in a low state, setting both read and write pointers to the first location in memory. Reset is required prior to the first write. Both READ ($\overline{R}$) and WRITE ($\overline{W}$) signals must be in high states during reset.

Read Enable ($\overline{R}$):
Providing the EMPTY FLAG ($\overline{EF}$) is not set, i.e. there is still data to be read, a read cycle commences on the falling edge of R, (see Figure 16). Data is read in a First-In First-Out manner independent of write operations. When reads are disabled data outputs (Q0 - Q8) are in a high impedance state. Reading the last available memory location sets the EMPTY FLAG ($\overline{EF}$), which is cleared following a write cycle.

Write Enable ($\overline{W}$):
Providing the FULL FLAG ($\overline{FF}$) is not set, i.e. there exists at least one memory location for writing, a write cycle commences on the falling edge of ($\overline{W}$), (see Figure 17). Data is written into consecutive memory locations independent of read operations on the rising edge of W. Data set up and hold times are with respect to the rising edge of $\overline{W}$.

Expansion In ($\overline{XI}$):
There are two possible modes of operation for the FIFO. One with $\overline{XI}$ grounded in which the device is in singledevice mode, the other is a depth expension mode or daisy chain configuration. In the latter mode $\overline{XI}$ inputs come from EXPANSION OUT ($\overline{XO}$) outputs of the device preceding it in the chain.

Expansion Out ($\overline{XO}$):
In depth expansion mode $\overline{XO}$ from one device signals the next device in the chain that the last location in its memory has been accessed.

Full Flag ($\overline{FF}$):
$\overline{FF}$ becomes active when the last available memory location has been written to, (see Figure 18). In general, this occurs whenever the write pointer coincides with the read pointer following a write cycle. Writes are inhibited while $\overline{FF}$ is active, and may only proceed after a read cycle has occured.

$\overline{FF}$ will go high t_{RFF} after completion of a valid READ operation. $\overline{FF}$ will go low t_{WFF} from the beginning of a subsequent WRITE operation, provided that a second READ has not been completed. Writes beginning t_{FFW} after $\overline{FF}$ goes high, are valid. Writes beginning after $\overline{FF}$ goes low and ending more than t_{WPI} before FF goes high, are invalid (ignored). Writes beginning less than twpl before $\overline{FF}$ goes high and less than t_{FFW} later, may or may not occur (be valid) depending on the internal flag status (see Figure 19).

If a Write to the last but one physical location completes while the last location (511th) is being Read, the $\overline{FF}$ will not be activated. The next Read should start after the last Write has completed.

As a WRITE operation is being performed to the last physical memory location (511th) whilst the READ pointer is waiting at the 510th physical location the FULL flag is activated for a duration less than 20ns.

Note: The last physical location (511th) is accessed after 511 WRITE or READ operations after RESET.

Empty Flag ($\overline{EF}$):
Following an initial RESET $\overline{EF}$ is active, becoming inactive after the first write cycle, (see Figure 20). $\overline{EF}$ becomes active once the read and write pointers are coincident following a read cycle. Reading will not take place whilst $\overline{EF}$ is active, and may only proceed once a write cycle has occured.

$\overline{EF}$ will go high t_{WEF} after completion of a valid WRITE operation. $\overline{EF}$ will again go low t_{REF} from the beginning of a subsequent READ operation, provided that a second WRITE has not been completed. Reads beginning t_{EFR} after $\overline{EF}$ goes high, are valid. Reads begun after $\overline{EF}$ goes low and ending more than t_{RPI} before $\overline{EF}$ goes high, are invalid (ignored). Reads beginning less than t_{RIP} before $\overline{EF}$ goes high and less than t_{EFR} later, may or may not occur (be valid) depending on the internal flag status (See Figure 21). If a Read to the last but one physical location completes while the last location (511th) is being written, the $\overline{EF}$ will not be activated. The next Read should be activated after the last Write has completed.

First Load/Retransmit ($\overline{FL}/\overline{RT}$):
This is a dual purpose input depending on the mode of operation of the device. In single device mode $\overline{XI}$ = 0 data may be retransmitted, i.e. it may be re-read. In depth expansion mode $\overline{FL}$ signifies the first device in the chain. When $\overline{RT}$ is pulsed low the read pointer is set to the first memory location. The write pointer is unaffected. This feature is disabled in depth expansion mode, and can only be applied when $\overline{R}$ and $\overline{W}$ are inactive (See Figure 22).

Data Inputs (D0 - D8): Data inputs, 9 bit word, for write operations.

Data Outputs (Q0 - Q8):
Data outputs, 9 bit word, for read operations. When $\overline{R}$ is inactive these outputs are in a high impedance state.

MODES OF OPERATION

Single Device Mode:
The single device mode is used with $\overline{XI}$ grounded. (See Figure 10). In this mode the retransmit facility may be used to re-read the data when less than 512 have been performed between resets.

Width Expansion Mode:
In this mode two or more devices are used, depending on the word length required, with the same control inputs applied to each. The same operations are applied to all devices, thus warning flags $\overline{EF}$ and $\overline{FF}$ are available from any or all of the devices. Output Signals from devices in this mode should not be merged. Figure 11 illustrates two devices configured in width expansion mode to give an 18 bitword, (512 x 18).

Depth Expansion Mode:
This has applications where more than 512 words are required. The RETRANSMIT facility is not available in this mode.

Two or more devices are organised in a daisy chain. The first device in the chain has $\overline{FL}$ grounded, all others have $\overline{FL}$ in high states. $\overline{XO}$ of each device is connected to $\overline{XI}$ of the next device in the chain.

The same read, write and reset signals are applied to each device. External logic is required to form new empty and full flags, i.e. all $\overline{EF}$'s are ORed together and all $\overline{FF}$'s are ORed together to form new empty and full flags respectively.

Figure 12 illustrates depth expansion of 2 devices (1024 x 9).

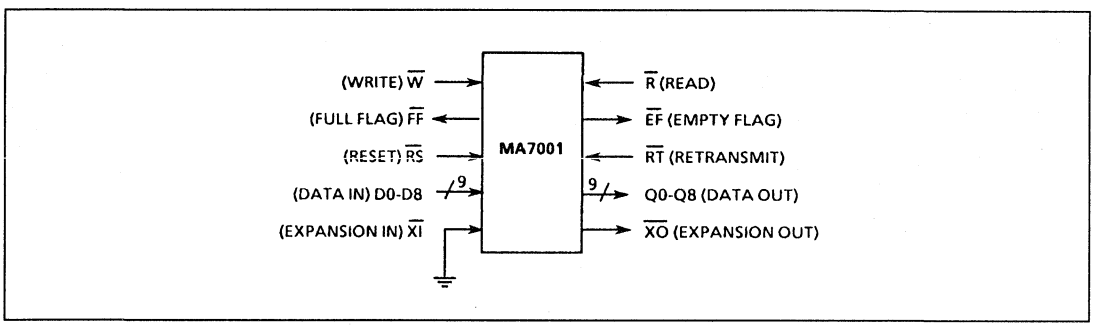


Figure 10: Single Device Mode (512 x 9 bits)

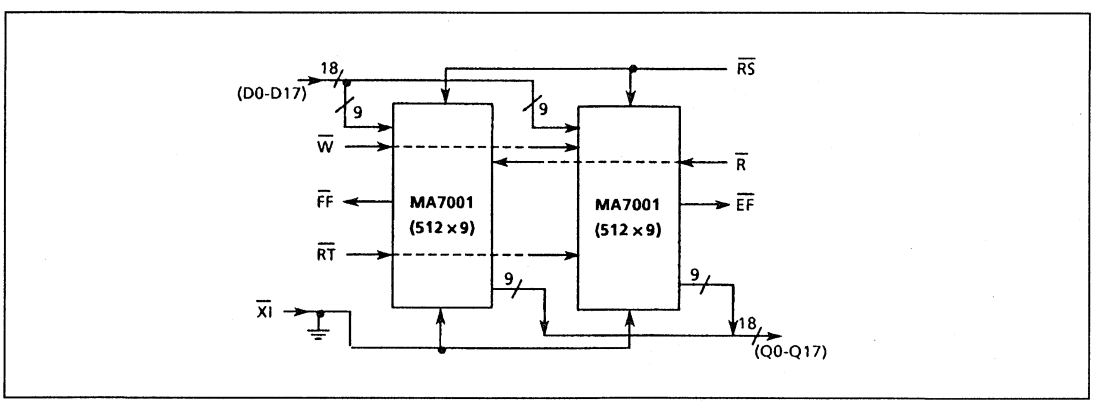


Figure 11: Width Expansion Mode (512 x 18 bits)

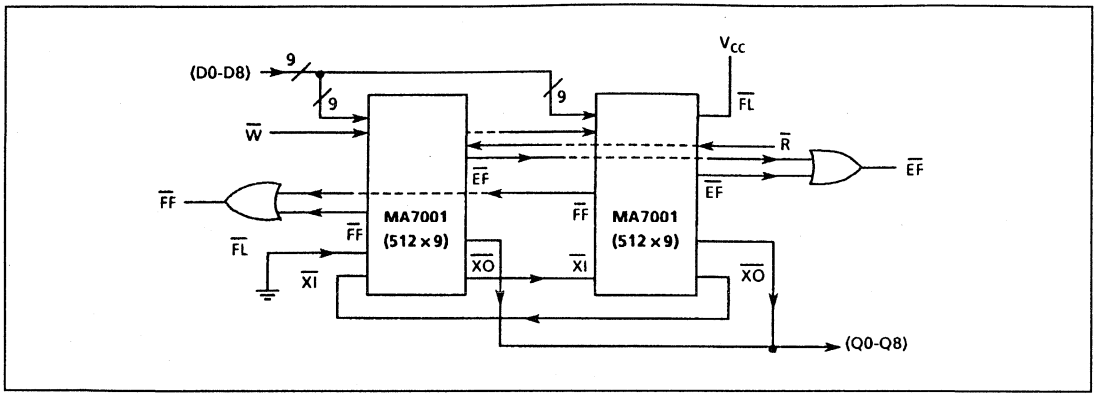


Figure 12: Depth Expansion Mode (1024 x 9 bits)

Compound Expansion Mode:
Both width and depth expansion can be implemented into the same expansion block. Note that no control signals are in conflict in either of the two expansion modes, i.e. width or depth expansion modes. Utilising compound expansion large FIFO arrays are possible. Figure 13 illustrates the use of compound expansion.

Bidirectional Mode:
The FIFO is a unidirectional device, i.e. one system reads, another writes. In cases where full communication is required between two or more systems, two or more groups of devices can be used. These groups can utilise any or all of the expansion modes already mentioned. Figure 14 illustrates 2 systems connected so that each can transmit data to and recieve data from each other, (see Modes of Operation for connection of control and data signals).

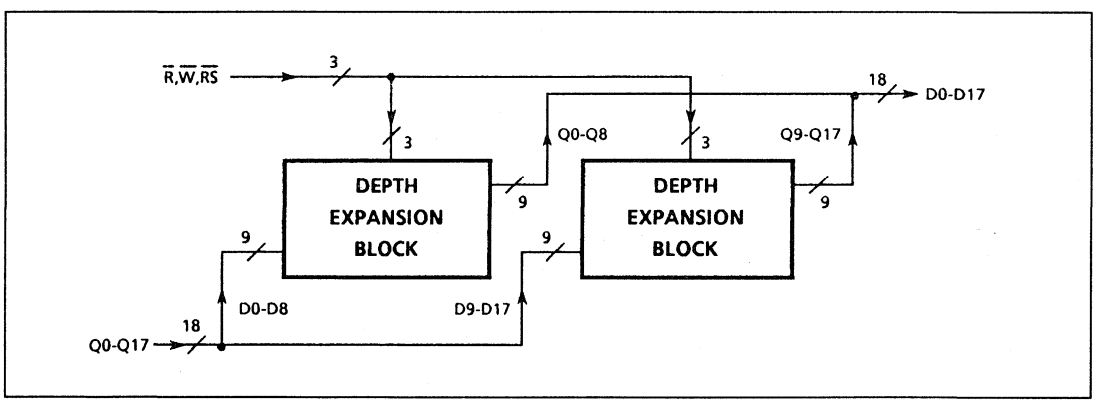


Figure 13: Compound Expansion

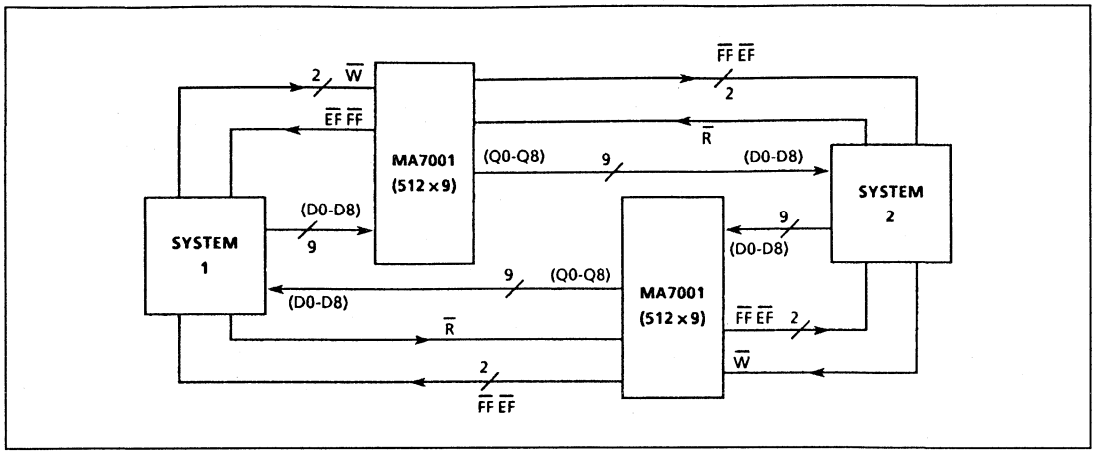


Figure 14: Bidirectional Mode (512 x 9 bits each way)

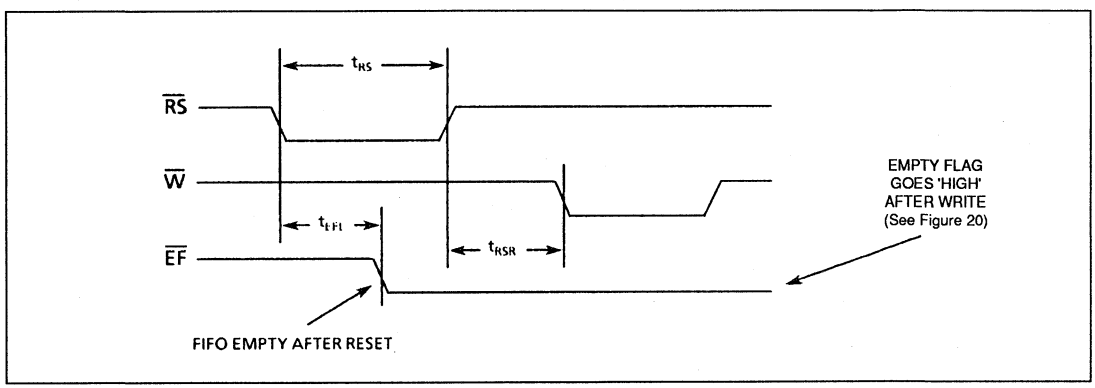


Figure 15: Reset

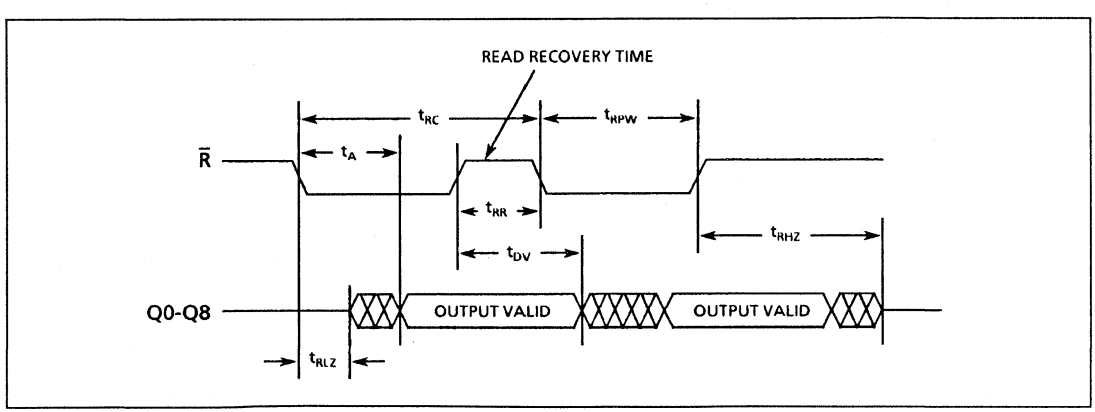


Figure 16: Asynchronous Read

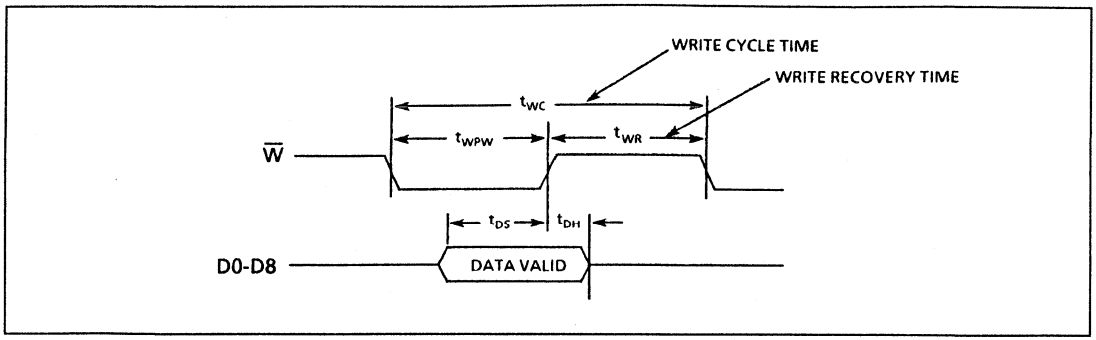


Figure 17: Asynchronous Write

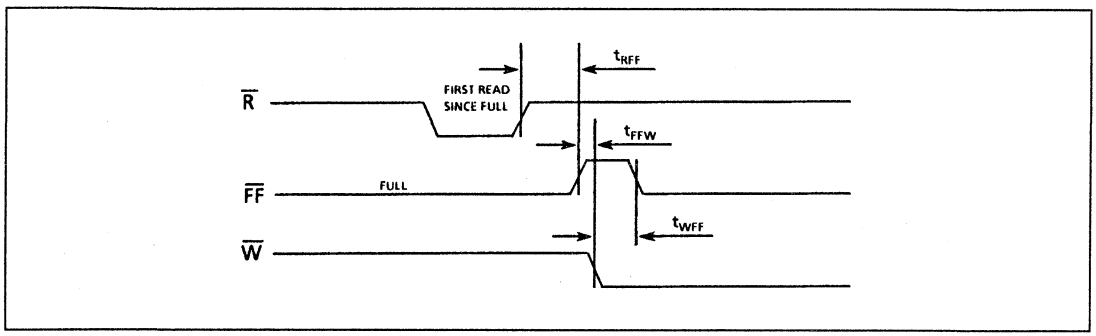


Figure 18: Read/Write to Full Flag

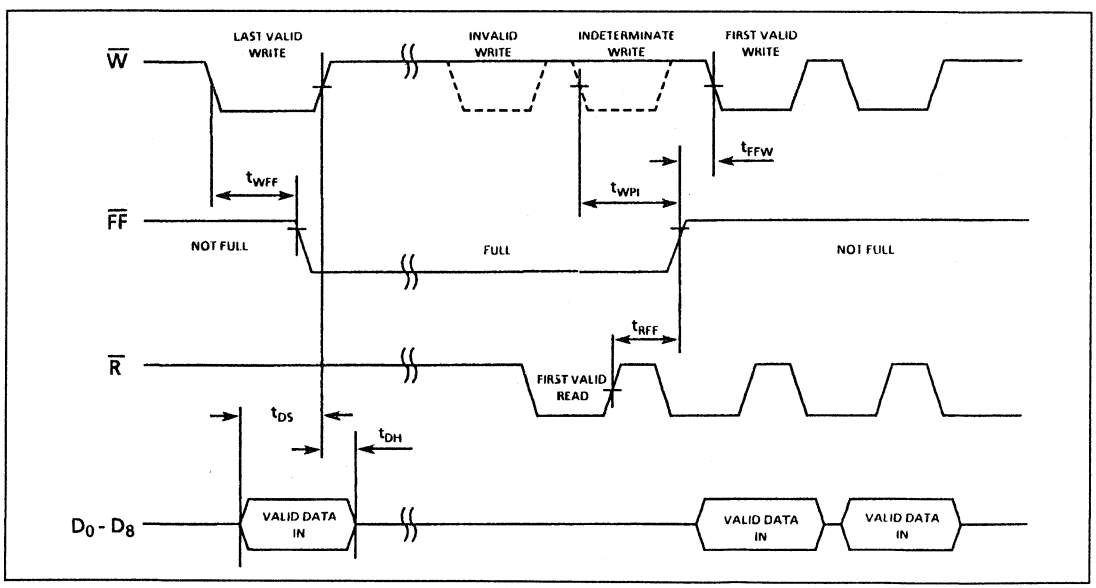


Figure 19: Write and Full Flag

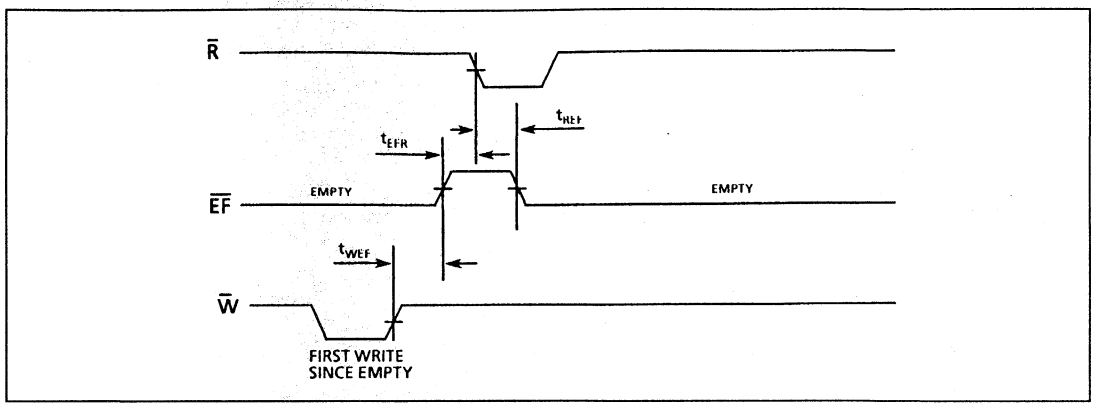


Figure 20: Write/Read to Empty Flag

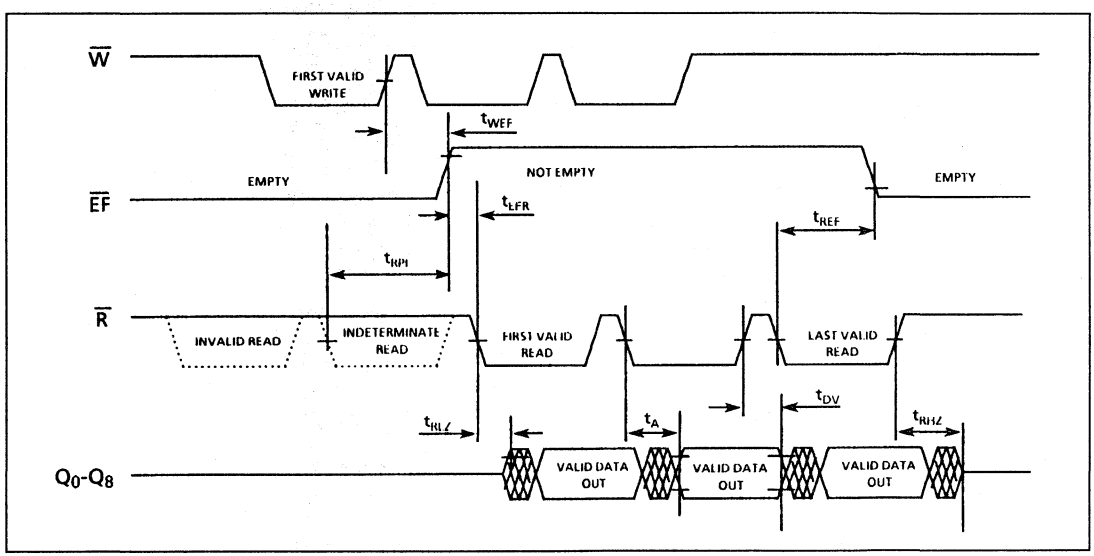


Figure 21: Read and Empty Flag

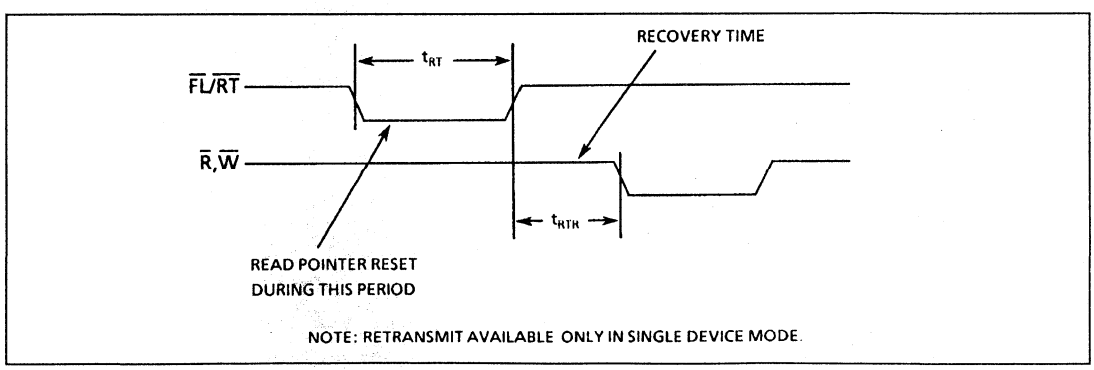
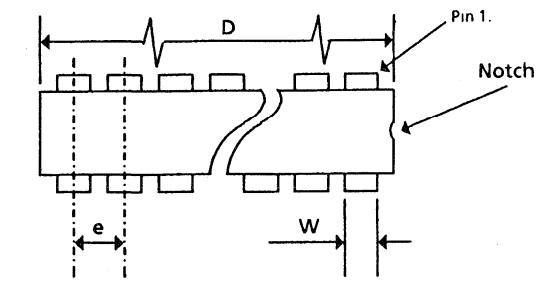
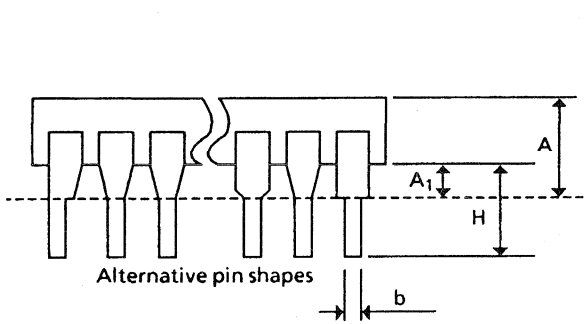
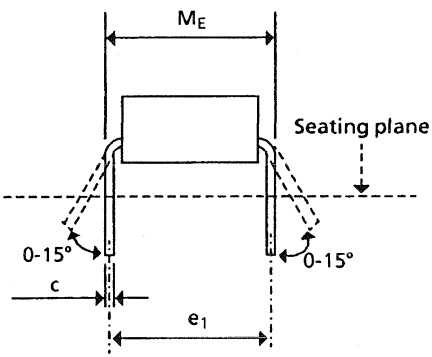


Figure 22: Retransmit Timing

OUTLINES AND PIN ASSIGNMENTS







Ref.	Min.	Nom.	Max.
A	-	-	5.71 (0.225)
A_1	0.38 (0.015)	-	1.53 (0.060)
b	0.35 (0.014)	-	0.59 (0.023)
c	0.20 (0.008)	-	0.36 (0.014)
D	-	-	36.02 (1.418)
e	-	2.54 (0.100) typ.	-
e_1	-	15.24 (0.600) typ.	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.90 (0.626)
W	-	-	1.53 (0.060)

Dimensions in mm (inches)

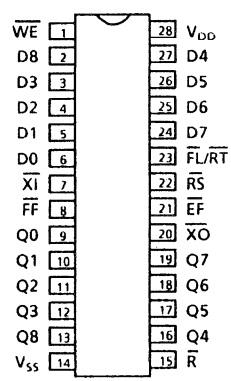
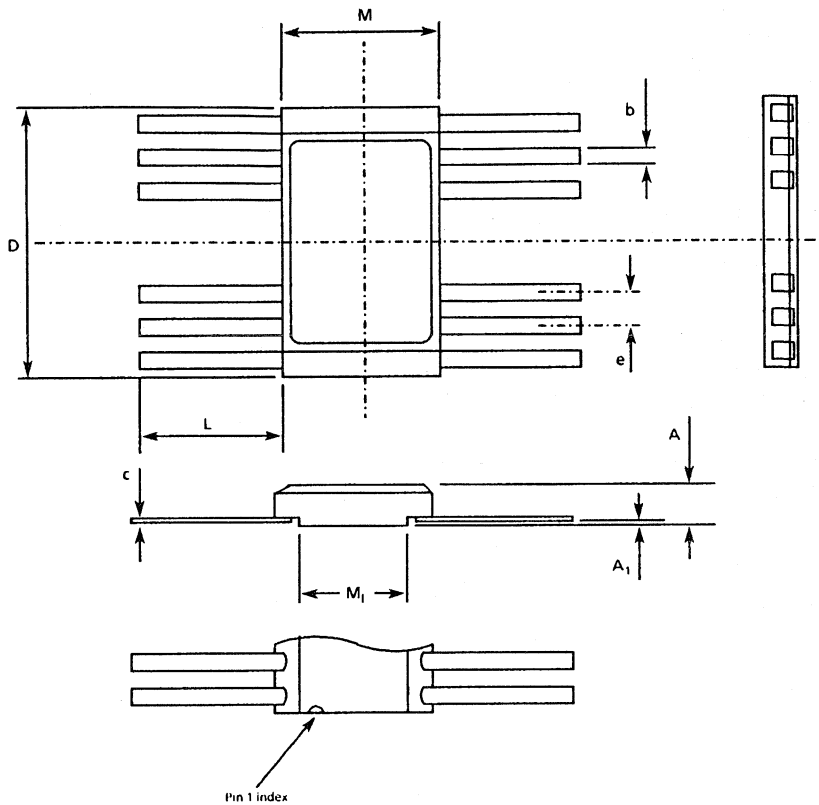


Figure 23: 28 Lead Ceramic DIL (Solder Seal) - Package Style C



Ref.	Min.	Nom.	Max.
A	-	-	2.97 (0.117)
A_1	(0.026)	-	-
b	(0.015)	-	0.48 (0.019)
c	0.10 (0.003)	-	0.15 (0.006)
D	18.08 (0.712)	-	18.49 (0.728)
e	-	1.27 (0.050) typ.	-
L	(0.315)	-	(0.365)
M	12.50 (0.492)	-	12.09 (0.508)
M1	(0.372)	-	(0.388)

Dimensions in mm (inches)

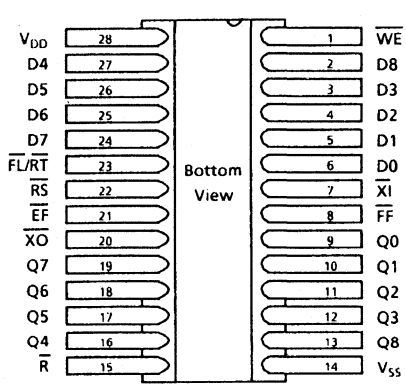


Figure 24: 28 Lead Ceramic Flatpack (Solder Seal) - Package Style F

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

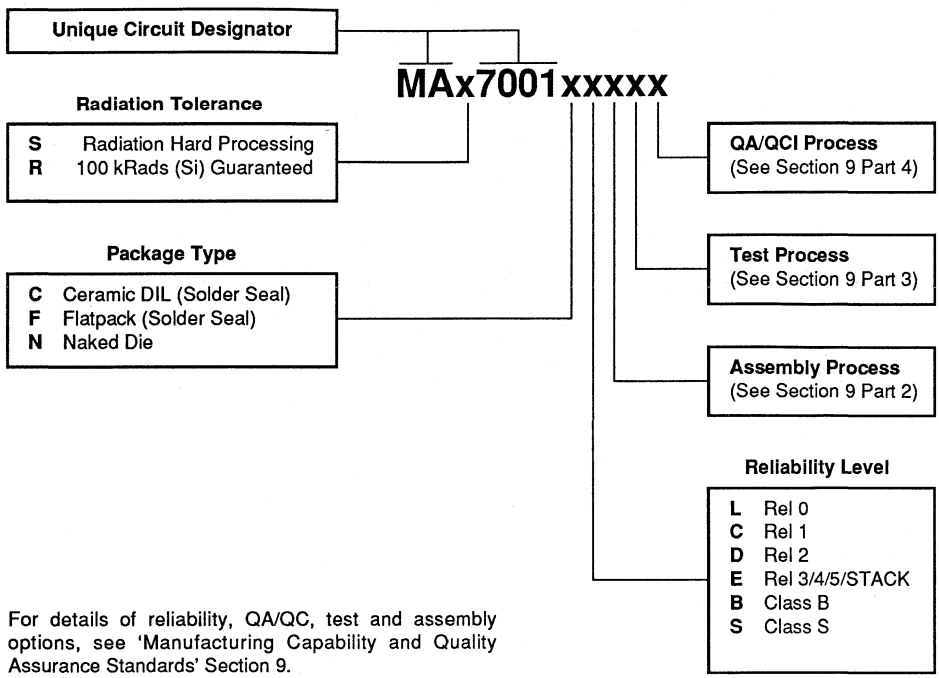
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$3.4x10^{-9}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 25: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA3764

RADIATION HARD 8192 x 8 BIT MASK-PROGRAMMABLE ROM

The MA3764 64k Mask Programmable ROM is configured as 8192x8 bits and manufactured using CMOS-SOS high performance, radiation hard, 1.5µm technology.

The design has fully static operation synchronised to the clock input. There are 3 mask programmable chip-select inputs to enable on chip decoding of the select signals. These may also be programmed so that any or all of them disable the address input buffers to conserve power when the chip is de-selected. An output enable signal is also provided to provide separate tristsate control for the output buffers.

Programming is performed during fabrication by customising the penultimate layer of the process. Programming data may be supplied in EPROM or as a data file in the standard INTEL Hex format.

Operation Mode	*$\overline{E}$	$\overline{C}$	$\overline{G}$	I/O	Power
Precharge	L	H	L	'I'	
Evaluate (Read)	L	L	L	D OUT	ISB 1
Output Disable	L	X	H	High Z	
Standby	H		X	High Z	ISB 2
	X		X	X	

*$\overline{E}$ is a mask programmed NAND function of E1, E2, E3 and their inverses.

Figure 1: Truth Table

FEATURES

- 1.5µm CMOS-SOS Technology
- Latch-up Free
- Fast Access Time 45ns Typical
- Total Dose 10^6 Rad(Si)
- Transient Upset >10^{11} Rad(Si)/sec
- SEU 4.3 x 10^{-11} Errors/bitday
- Single 5V Supply
- Three State Output
- Low Standby Current 100µA Typical
- -55°C to +125°C Operation
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Fully Static Operation
- Programmable at Via Level for Fast Turnaround
- 3 Mask Programmable Chip Selects

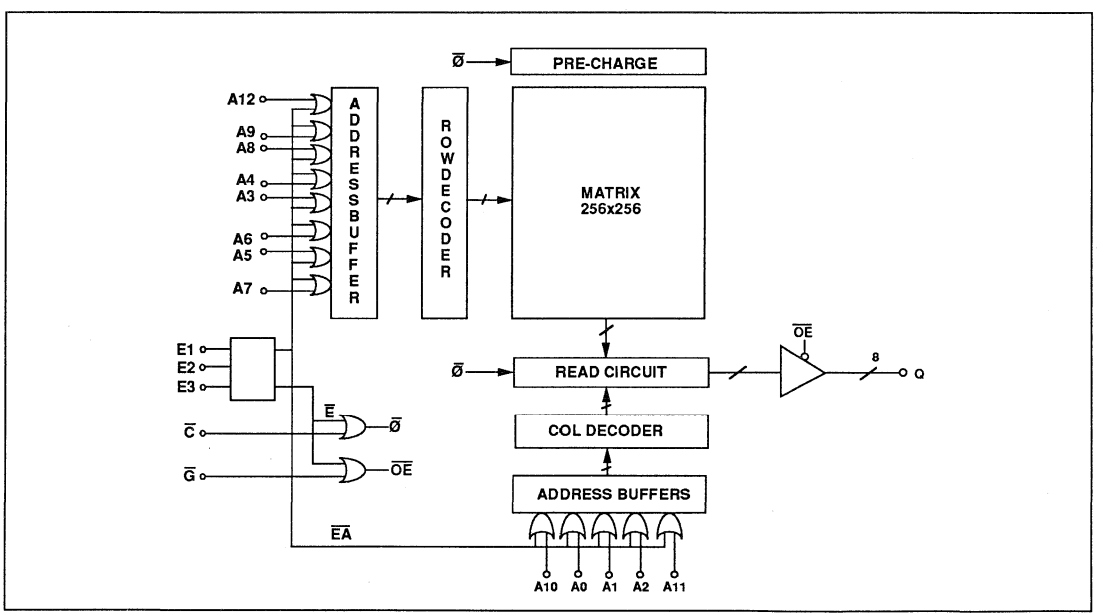


Figure 2: Block Diagram

SIGNAL DEFINITIONS

A0-A12
Address input pins, these select a particular word within the memory array.

Q0-Q7
Data output pins, these are tristated when $\overline{E}$ is high (chip is de-selected). When the chip is selected, data is available an access time after a falling edge on $\overline{C}$ and is held during the time that $\overline{C}$ is high. This data appears on the output pins if the output enable ($\overline{G}$) is asserted, otherwise the output pins are tristated.

E1, E2, E3
Are mask-programmed to the customer's specification to form the active low chip select function, $\overline{E}$. $\overline{E}$ is driven by a 3-input NAND gate which has E1, E2 and E3 or their inverses as its inputs. Unused NAND gate inputs will be tied high internally. When $\overline{E}$ is at a high level it defaults the ROM to a precharge condition and holds the data output drivers in a high impedance state.
Similarly the E inputs may also be programmed to disable the address buffers when not asserted. This introduces a chip-select to clock-falling setup time for the relevant inputs but also reduces power consumption caused by the address lines changing while the chip is de-selected.

$\overline{C}$
A falling edge on this signal initiates a read operation. The chip is precharging during the time that $\overline{C}$ is high but the data from the previous read is held available for enabling to the output data pins.

$\overline{G}$
Output enable, when at a high level, this holds the data output pins in a high impedance state. When at low level, the data output driver state is defined by $\overline{E}$. If this signal is not used, it must be connected to V_{SS}.

CHARACTERISTICS AND RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	7.0	V
V_I	Input Voltage	-0.3	V_{DD}+0.3	V
T_A	Operating Temperature	-55	125	°C
T_S	Storage Temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 3: Absolute Maximum Ratings

Notes for Table 4:
Characteristics apply to pre radiation at T_A = -55°C to +125°C with V_{DD} = 5V ±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10% (characteristics at higher radiation levels available on request). GROUP A SUBGROUPS 1, 2, 3.

Symbol	Parameter	Conditions (Option)	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH}	Logical '1' Input Voltage	- (TTL) (CMOS)	V_{DD}/2 0.8 V_{DD}	- -	V_{DD} V_{DD}	V V
V_{IL}	Logical '0' Input Voltage	- (TTL) (CMOS)	V_{SS} V_{SS}	- -	0.8 0.2 V_{DD}	V V
V_{OH1}	Logical '1' Output Voltage	I_{OH1} = -4mA	2.4	-	-	V
V_{OH2}	Logical '1' Output Voltage	I_{OH2} = -3mA	V_{DD} -0.5	-	-	V
V_{OL}	Logical '0' Output Voltage	I_{OL} = 5mA	-	-	0.4	V
I_{LI}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} all inputs	-	-	±10	µA
I_{LO}	Output Leakage Current	Chip disabled, V_{OUT} = V_{DD} or V_{SS}	-	-	±10	µA
I_{SB1}	Selected Static Current (CMOS)	All inputs = V_{DD} -0.2V except $\overline{E}$ = V_{SS} +0.2V	-	0.1	2	mA
I_{DD}	Dynamic Operating Current (CMOS)	f_{RC} = 1MHz, all inputs switching, V_{IH} = V_{DD} -0.2V	-	3	10	mA
I_{SB2}	Standby Supply Current	$\overline{E}$ = V_{DD} -0.2V	-	0.1	2	mA

Figure 4: Electrical Characteristics

AC CHARACTERISTICS

Conditions of Test for Table 5:
1. Input pulse = V_{SS} to 4.0V.
2. Times measurement reference level = 1.5V.
3. Input Rise and Fall times ≤5ns.
4. Output load 1TTL gate and CL = 60pF.
5. Transition is measured at ±500mV from steady state (T_{EVQX}, T_{EXQZ}, T_{GLQX}, T_{GHQZ}).
6. These parameters are sampled and not 100% tested (T_{EVQX}, T_{EXQZ}, T_{GLQX}, T_{GHQZ}).

Characteristics apply to pre-radiation at T_A = -55°C to +125°C with V_{DD} = 5V±10% and to post 100k Rad(Si) total dose radiation at T_A = 25°C with V_{DD} = 5V ±10%. GROUP A SUBGROUPS 9, 10, 11.

Symbol	Parameter	Min	Max	Units
TEAVCL (Note 1)	Enable 1 valid to clock low	40	-	ns
TEVCL (Note 2)	Enable valid to clock low	5	-	ns
TEVQX	Enable valid to outputs driven	-	30	ns
TCLQV	Access time	-	55	ns
TCLCH	Clock low time	60	-	ns
TCHCL	Clock high time	40	-	ns
TAVCL	Address setup time	40	-	ns
TCHAX	Address hold time	0	-	ns
TCLQX	Data hold time after falling clock	0	-	ns
TEXQZ (Note 2)	Chip disabled to outputs tristate	-	30	ns
TGLQX	Output enable low to outputs driven	-	15	ns
TGHQZ	Output enable high to outputs tristate	-	10	ns

Note 1: Applies to E inputs which are programmed to disable the address inputs. Time is to clock-low from the last of such inputs to be asserted.
Note 2: TEVCL and TEXQZ are timed from the last of the E inputs being asserted. This does not apply to inputs which are used to disable the address inputs in the case of TEVCL.

Figure 5: Read Cycle AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Figure 6: Capacitance

Symbol	Parameter	Conditions
F_T	Basic Functionality	V_{DD} = 4.5V - 5.5V, FREQ = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} \leq 1.5V$, $V_{OH} \geq 1.5V$ TEMP = -55°C to +125°C, GPS PATTERN SET GROUP A SUBGROUPS 7, 8A, 8B

Figure 7: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 4 at +25°C
2	Static characteristics specified in Table 4 at +125°C
3	Static characteristics specified in Table 4 at -55°C
7	Functional characteristics specified in Table 7 at +25°C
8A	Functional characteristics specified in Table 7 at +125°C
8B	Functional characteristics specified in Table 7 at -55°C
9	Switching characteristics specified in Table 5 at +25°C
10	Switching characteristics specified in Table 5 at +125°C
11	Switching characteristics specified in Table 5 at -55°C

Figure 8: Definition of Subgroups

TIMING DIAGRAMS

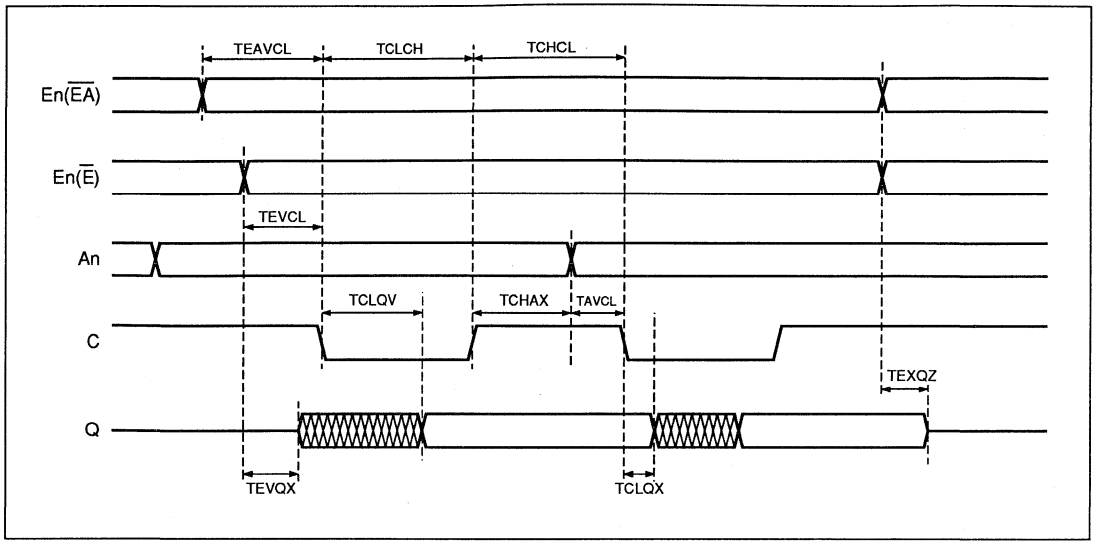


Figure 9: Read Cycles

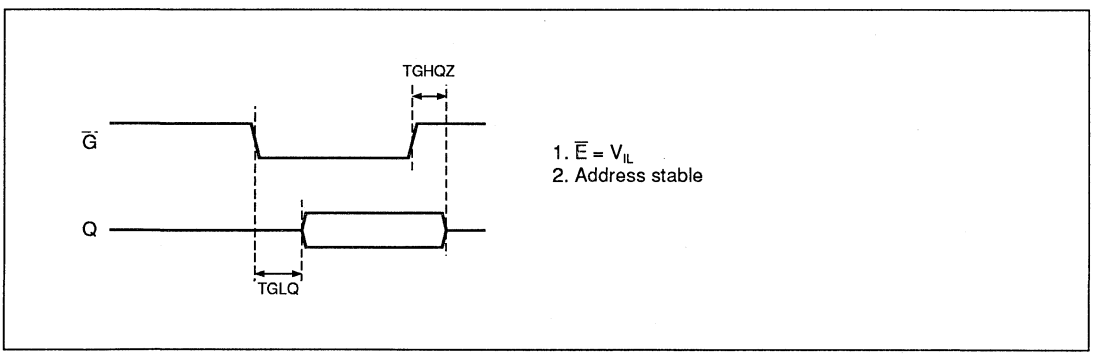
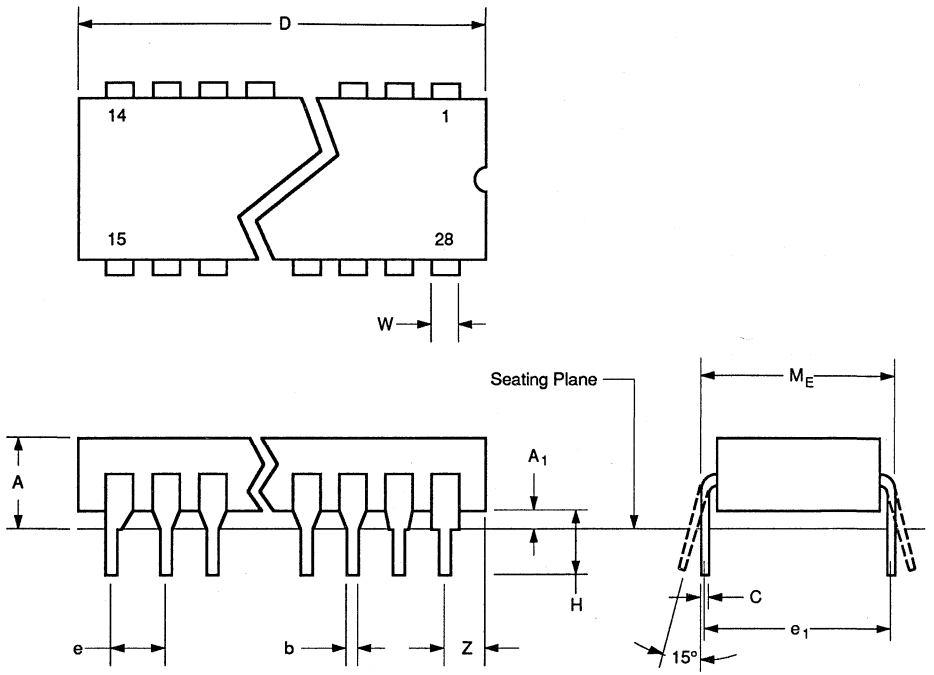


Figure 10: Output Enable Operation

OUTLINES AND PIN ASSIGNMENTS



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

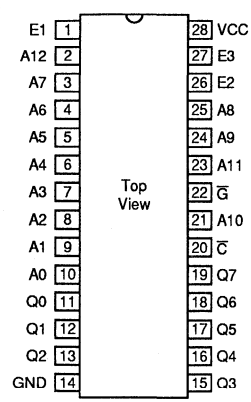
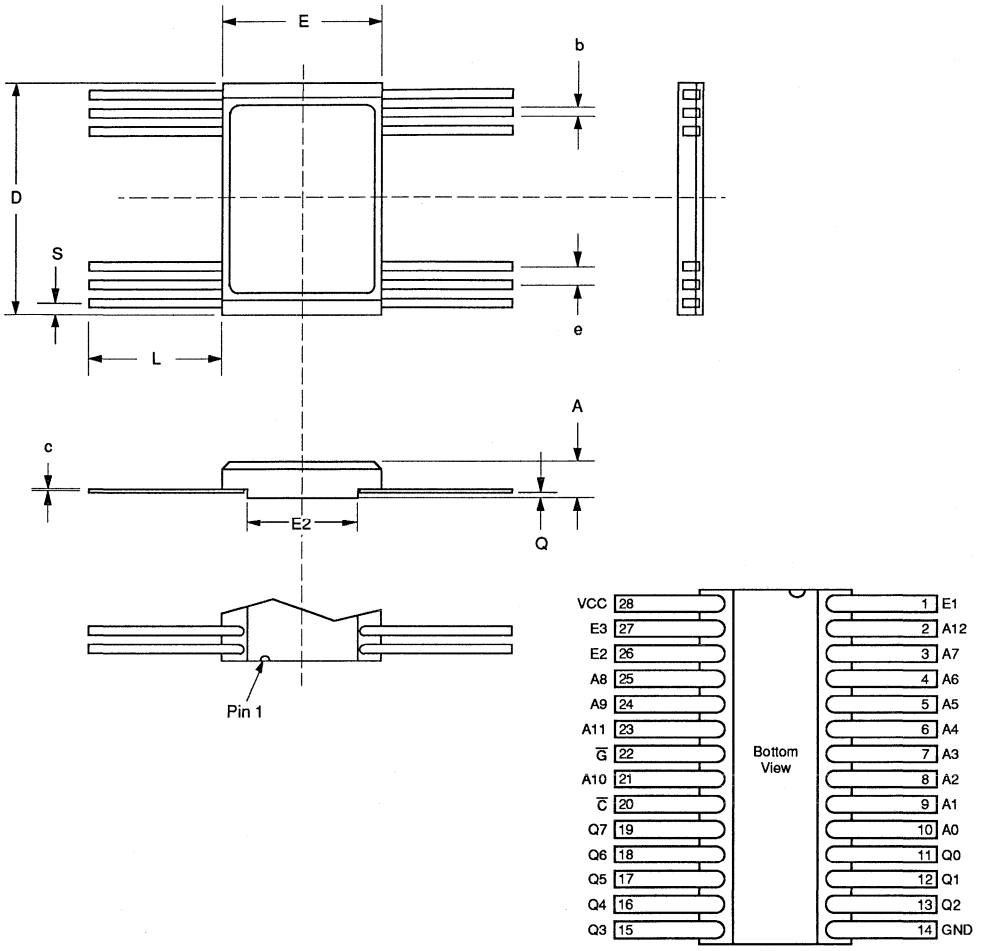


Figure 11: 28-Lead Ceramic DIL (Solder Seal) - Package Style C



Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.97	-	-	0.117
b	0.381	-	0.482	0.015	-	0.019
c	0.076	-	0.152	0.003	-	0.006
D	18.08	-	18.49	0.712	-	0.728
E	12.50	-	12.9	0.492	-	0.508
E2	9.45	-	9.85	0.372	-	0.388
e	1.143	-	1.40	0.045	-	0.055
L	8.00	-	9.27	0.315	-	0.365
Q	0.66	-	-	0.026	-	-
S	-	-	1.14	-	-	0.045

XG543

Figure 12: 28-Lead Ceramic Flatpack (Solder Seal) - Package Style F

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

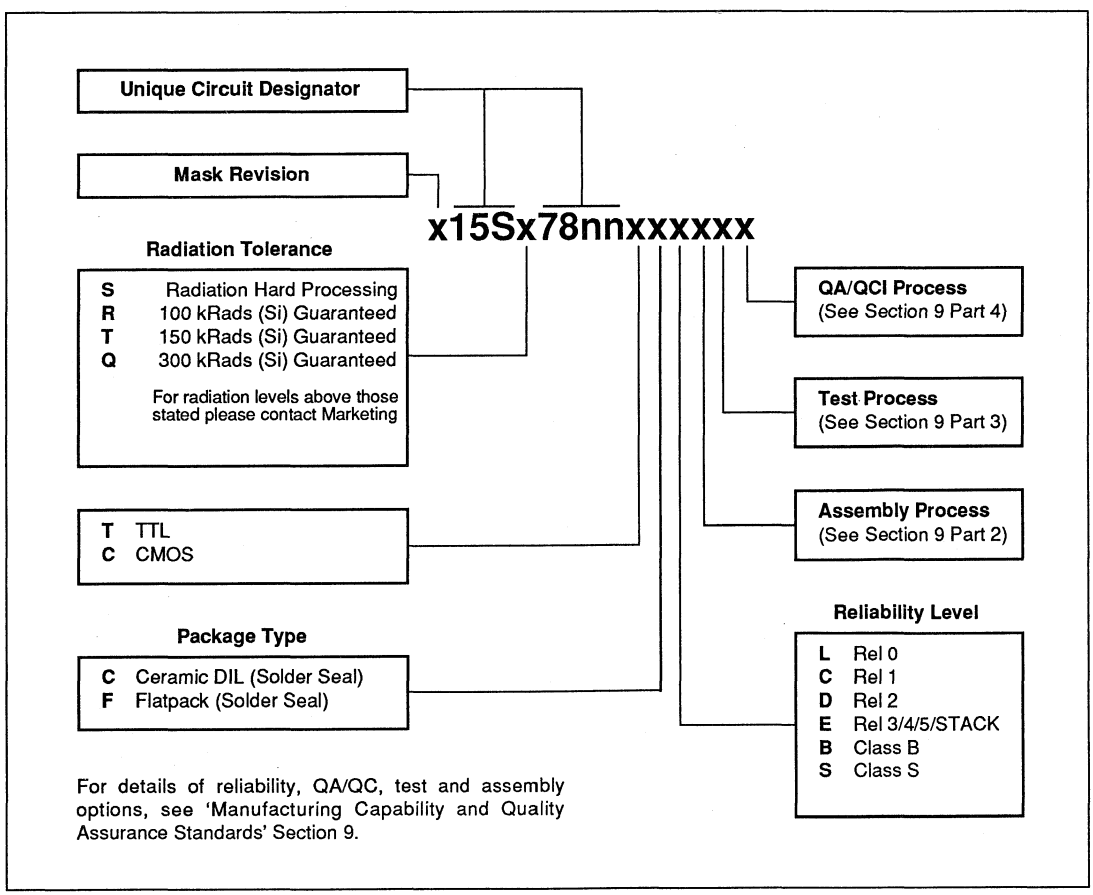
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 13: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

Section 5
Databus

DS3587-3.4

MA3690/1/3

1553B BUS CONTROLLER/REMOTE TERMINAL

The MA3690/1 chip set has three modes of operation: remote terminal, bus controller, and passive monitor It has a dual bus capability, requires minimum support hardware / software and is implemented on a radiation hard, CMOS/SOS process. For applications requiring access to Terminal Flag, a 48-Pin DIL MA3693 is available as an alternative to the MA3690.

As a remote terminal, the MA3690/1 is fully compatible with Mil-Std-1553B. The chip set obtained SEAFAC approval in December 1987. All options and mode commands specified by the Mil Std are implemented Full and meaningful use is made of status word bits and a comprehensive bit word is provided.

A unique mechanism has been incorporated that allows the subsystem to declare illegal commands legal, and vice versa, before the chip set services the command. It should be noted that use of this mechanism is optional and that the system defaults to normal operation if the option is not required. The chip set is easily interfaced to subsystem memory and is sufficiently flexible to ensure compatibility with a wide range of microprocessors.

As a bus controller the MA3690/1 has the ability to initiate all types of 1553B transfer on either of the two buses An instruction word is set up by the subsystem, prior to transmission, which contains details of transfer type and bus selection. Four bits of the instruction word have been used to specify the conditions under which the chip set will generate a subsystem interrupt. The most significant bits of the instruction word have been used to specify the conditions under which the chip set will perform an automatic retry and the number of retries to be carried out (max. 3). At the end of each instruction execution cycle, the chip set writes a report word into the subsystem memory; the contents of which give the subsystem an indication of the degree of success of the transfer.

The bus controller may be used in either of two configurations, i.e. single shot or table driven.

In the single shot configuration, the controller is under direct control from the subsystem (processor). In table driven configuration, the controller is given greater autonomy to execute a table of instructions held in either ROM or RAM.

As a passive monitor, the chip set will monitor all bus activity and pass any associated information to the subsystem. As the name implies, in this mode of operation, the chip set is truly passive and will not reply to command instructions.

FEATURES

- Radiation Hard to 1MRads (Si)
- High SEU Immunity, Latch-Up Free
- CMOS-SOS Technology
- All Inputs and Outputs Fully TTL or CMOS Compatible
- Military Temperature Range -55 to +125°C
- Dual Bus Capability
- Minimal Subsystem Interface
- Powerful Bus Control Facility
- Complete Remote Terminal Protocol
- SEAFAC Approved

SIGNAL DESCRIPTIONS

All signals are TTL compatible unless stated otherwise. An 'N' at the end of the signal name denotes an active low signal.

SUPPLIES

VDD 5 volts positive supply

VSS Ground

CLOCK INPUTS

CK12 12MHz clock

BUS INTERFACE LINES

PDIN0 Input
Positive threshold exceeded on bus 0.

NDIN0 Input
Negative threshold exceeded on bus 0.

TXEN0N Output
Transmit enable for driver on bus 0.

PDOUT0N Output
Positive Manchester data for driver on bus 0.

NDOUT0N Output
Negative Manchester data for driver on bus 0.

PDIN1 Input
Positive threshold exceeded on bus 1.

NDIN1 Input
Negative threshold exceeded on bus 1.

TXEN1N Output
Transmit enable for driver on bus 1.

PDOUT1N Output
Positive Manchester data for driver on bus 1.

NDOUT1N Output
Negative Manchester data for driver on bus 1.

SUBSYSTEM INTERFACE LINES

STROBEN Output
STROBE - Information transfer strobe pulse for words being transferred on the data highway.

BUFENN Output
BUFFER ENABLE - This line goes low to enable the data highway buffer between the terminal and the subsystem.

R/WN Output
READ/WRITE - This line indicates the direction of information transfer between the terminal and the subsystem. When low, information is being written from the terminal to the subsystem.

DTRQN Output
DATA TRANSFER REQUEST - This line goes low to request permission to transfer a non mode data word to or from the subsystem.

DTAKN Input
DATA TRANSFER ACKNOWLEDGE - This line should be driven low to grant permission to perform the requested data word transfer.

MDTN Output
MODE DATA TRANSFER -
RT: This line goes low to indicate that the data word being transferred is assosiated with a mode command.
BC: When operating as a passive monitor this line goes low to indicate that a valid data word is on the data highway and should be written into the received data latch.

GBRN Output
GOOD BLOCK RECEIVED - When in RT mode this line will pulse low to inform the subsystem that the received non mode data words are valid and may be used.

ADENN Output
ADDRESS ENABLE - When in RT mode this line will go low as part of the reset routine to enable the terminal address on to the data highway.

SYNCN Output
SYNCHRONISE - This line will pulse low if a valid synchronise mode command without data is received and passes all validity checks.

STATENN Output
STATUS ENABLE -
RT: When low this line enables the contents of the subsystem status latch on to the data highway.
BC: When low this line enables the BC report word on to the data highway.

MDRN Output
MODE DATA RECEIVED - This line will pulse low to inform the subsystem that the received mode data is valid and may be used.

RXCMDN Output
RECEIVED COMMAND -
RT: This line goes low to indicate that a valid command word for this RT is on the highway and should be written into the command word latch.
BC: When operating as a passive monitor this line goes low to indicate that a valid command / status word is on the data highway and should be written into the received status latch.

BUSYREQN / HALTREQN Input
BUSY REQUEST / HALT REQUEST -
RT: This line should be driven low as a request for the terminal to set the busy bit and inhibit non mode data transfers to or from the subsystem.
BC: This line should be driven low as a request for the terminal to halt table execution and all subsystem access.

BUSYACKN / HALTEDN Output
BUSY ACKNOWLEDGE / HALTED -
RT: This line will go low to indicate that the subsystem has free access to the shared store.
BC: This line will go low to indicate that all terminal operation has been halted and hence the subsystem has free access to the shared store.

CODENN Output
CODE ENABLE - This line when low indicates that a word transfer between the terminal and either the Instruction Store or the Report Store is taking place.

C0 Output
CODE 0 - This line is the least significant address line from the terminal to the Instruction and Report Stores.

C1 Output
CODE 1 - This line is the least significant but one address line from the terminal to the Instruction and Report Stores.

INCADRN Output
INCREMENT ADDRESS - This line pulses low to increment the external instruction addressing counter.

HSFN/IRQN Output
HANDSHAKE FAIL / INTERRUPT REQUEST
RT: This line pulses low to inform the subsystem that it has not responded to a data transfer request to take place.
BC: This line pulses low to generate an interrupt to the BC subsystem processor.

INCMDN Output
IN COMMAND - When low this line indicates that the terminal is currently servicing a command word.

EOTN Output
END OF TRANSMISSION - When low this line indicates that the selected bus is quiet and hence available for use.

ABORTN Output
This line will pulse low to abort execution of the current command if an error is detected.

B0-B15 Input/Output
HIGHWAY LINES - 16 line bidirectional Output data highway. (B0 = LSB).

CLDN Inter-chip (CMOS)
COMMAND LOAD - When low this line indicates that the word on the data highway should be loaded into the transmitter for transmission with a command sync.

DLDN Inter-chip (CMOS)
DATA LOAD - When low this line indicates that the word on the data highway should be loaded into the transmitter for transmission with a data sync.

OBFN Inter-chip (CMOS)
OUTPUT BUFFER FULL - When low this line indicates that the transmitter output buffer is full and cannot be overwritten.

VALDRN Inter-chip (CMOS)
VALID DATA RECEIVED - When low this line indicates that a valid data word has been received and is on the data highway.

VALCRN Inter-chip (CMOS)
VALID COMMAND RECEIVED -
RT: When low this line indicates that a valid command word for this RT has been received.
BC: When low this line indicates that a valid word with a command sync has been received.

RT/BCN Input
REMOTE TERMINAL/BUS CONTROLLER - When high the terminal will function as an RT.When low the terminal will function as a bus controller.

CK4 Output
4MHz system clock.

PUCN Input
POWER UP CLEAR - This line should be pulsed low following power-up.

RESETN Input/Output
RESET - This line when low, forces the internal circuitry to reset to the quiescent initialised state. This is a 'TTL' level input on both devices and an open-drain output on the MA3690. The subsystem should drive this line via an open drain/collector device with external pull up fitted.

RT0 / RT1 Inputs
REPLY TIMEOUT DECODE - These lines on the MA3690 allow four different timeout values to be used. On the MA3693, the RT1 signal is not available and is pulled down internally.

RT1	RT0	Timeout (us)
0	0	16
0	1	22
1	0	44
1	1	108

Note: Under normal operation, option 00 should be used. (i.e. 16uS)
The measurement is taken between mid parity and mid sync - measured at PDIN/NDIN terminals.

TF Output
TERMINAL FLAG - This line is available only on the 64-pin MA3690 and on the MA3693 (where it replaces RT1). The line indicates the state of the Terminal Flag bit in the Status Word, and can be inhibited by the mode code Inhibit Terminal Flag. This is an active LOW signal.

TEST/SOT Inputs
These lines are for test purposes only and for normal chip set operation must both be tied low.

OPERATION IN BUS CONTROL MODE

For this mode of operation the RT/BC pin must be held in the logic zero state. On power up the PUC or RESET line must be pulsed low for a minimum of 500ns causing the chip set to initialise and assume the halted state with the HALTED output low. To release the terminal from the halted state, the subsystem must drive the HALTREQ line through a low to high transition, at which time the HALTED line will go inactive.

When the HALTED line goes inactive,the terminal will address a four word deep Instruction Store as shown below, using the C0 and CI outputs.

This first instruction after a Reset is a NOOP.

INSTRUCTION STORE

C1	C0	Word
0	0	Instruction
0	1	Receive Command
1	0	Transmit Command
1	1	Data Pointer

The instruction word specifies the operation which the terminal is to carry out, and is formatted in the following way:

Instruction Word

Bit

15.14.	13.12.11.	10.9.8.7.	6.5.	4.3.	2.1.0.
Retry Count	Retry Condition	Interrupt Conditlon	Bus Select	Functlon Code	Message Code

The significance of the instruction word bits are as follows:

Message Code

Code	Transfer Type
000	RT to BC
001	BC to RT
010	RT to RT, data to BC subsystem
011	RT to RT, no data to BC subsystem
100	Broadcast RT to BC, non data mode commands only
101	Broadcast BC to RT
110	Broadcast RT to RT, data to BC subsystem
111	Broadcast RT to RT, no data to BC subsystem

Mode Codes without data are followed by a NOOP.

Function Code

Code	Terminal Function
00	Execute message code
01	Perform self test
10	Monitor bus
11	No operation (NOOP)

The Function Code (bits 4 and 3 of the Instruction Word) specifies the required terminal mode of operation.

Execute - Code 00

With the Function code bits set to 00, the terminal will execute the message as defined in the Message code bits

Self Test - Code 01

If the terminal has been selected to perform a Self Test then the terminal transmitter output stages will be disabled and the self test sequence entered. At the end of the Self Test the transmitter stages will be re-enabled and a Report sequence will be activated, in order to report on the success, or failure, of the Self Test.

Passive Monitor - Code 10

If the Function code of the Instruction word is 10 the terminal will disable the transmitter output stages, suspend table execution and merely monitor the specified bus for valid words.

No Operation - Code 11

The No Operation code provides a means of introducing delay or a wait sequence into the table operation. In selecting this code the terminal will be forced into the Report sequence and provide either an increment signal (INCADRN) or an interrupt (IRQN) if the Interrupt Always flag in the Instruction word has been selected.

Bus Select

Code	Definition
00	Transmit on bus 0
01	Transmit on bus 1

Note: Bit 6 of the instruction word is tied low internally.

The required data bus on which transactions take place is defined by bit 5. In addition to this, this bit defines the bus on which the Transmitter Self Test operation will be conducted and the choice of the bus for monitor purposes in Passive Monitor mode.

Interrupt Condition

Code	Definition
0001	Interrupt if no response
0010	Interrupt if status bit set
0100	Interrupt always
1000	Interrupt if word error

If the terminal detects one of the above conditions and the appropriate flag is set, the the IRQ line will pulse low for 250ns.

Four bits of the Instruction word (bits 10-7) define conditions under which the terminal will generate an interrupt to the subsystem (IRQN). Note that the generation of IRQN will only take place after any selected retry conditions have been exhausted.

The interrupt conditions which may be selected can be categorised as follows:

1. Interrupt if no response - the terminal will generate an interrupt if the RT does not respond.
2. Interrupt if Status bit set - the terminal will generate an interrupt if a received status word has a bit set other than in the RT address field or if the wrong RT responds.
3. Interrupt Always - the terminal will generate an interrupt regardless of whether the message was successful or not.
4. Interrupt if word error - the terminal will generate an interrupt if a word encoding or word count error occurs.

In all of the above cases, the terminal will generate a 250ns pulse on IRQN and enter the halted state. This will occur after the Report sequence has been executed.

Note the INCADRN will not be produced.

Retry Condition

Code	Definition
001	Retry if error
010	Retry if status bit set
100	Retry if busy set

Three bits of the Instruction word (bits 13-11) are used as flags to specify conditions under which the terminal will execute automatic message retries until the retry number count is zero. The retry flags are involved with the following conditions:

1. Retry if error - this includes a no-status response, a word encoding error, or a wrong word count from a responding RT.
2. Retry if Status bit set - an automatic retry will take place if a received status word has a bit set, other than in the RT address field, or if the wrong RT responds.
3. Retry if Busy - this is a specific check for the setting of the Busy bit in a responding RT's status word.

The remaining two bits of the Instruction word specify the number of message retries which the Bus Controller will attempt automatically. A code of 00 specifies no retries, a code of 11 specifies the maximum of three retries. The retries are in addition to the initial message transmitted, hence a message may be transmitted four times in total, if not successful. Note that if the condition which is being tested becomes invalid, the retry sequence will discontinue on the next message with the Bus Controller completing execution of the message in the relevant manner.

Retry Count

The two most significant bits of the instruction word specify the number of retries to be carried out when a retry condition has been detected. (Maximun 3 given by code 11)

RECEIVE COMMAND WORD

The receive command word is addressed when CODENN and C1 are both low and R/WN and C0 are both high. This word is the command word which will be transmitted for a BC to RT transfer or as the first command word of an RT to RT transfer.

Note: This word should be set to 1111 HEX if the message code is 000 or 100, or if the Function Code is not 00.

TRANSMIT COMMAND WORD

The transmit command word is addressed when CODENN and C0 are both low and R/WN and C1 are both high. This word is the command word which will be transmitted for an RT to BC transfer or as the second command word of an RT to RT transfer.

Note: This word should be set to 1111 HEX if the message code is 001 or 101, or if the Function Code is not 00.

DATA POINTER WORD

The data pointer word is addressed when CODENN is low and C0, C1 and R/WN are all high. This word is intended as a base address pointer to the subsystem data store thus specifying where any data words associated with the current instruction should be stored or retrieved from. As such, this word is not read into the terminal itself but is merely transferred from the Instruction Store to a suitable external address latch. (The BUFENN signal is therefore inactive during this transfer).

REPORT STORE

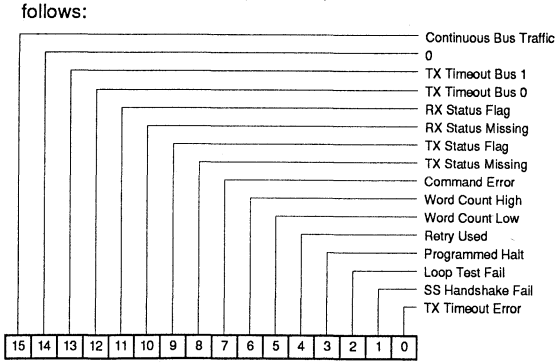
The report store holds information concerning the success or failure of the execution of the last instruction, and is addressed by means of the CODENN, C0 and C1 lines as for the instruction store The report store is addressed when the R/WN line is low, the instruction store when the R/WN line is high.

The report store comprises a Report word, a receive status word (if applicable) and a transmit status word (if applicable). The fourth location has no meaning and is not at anytime addressed.

C1	C0	Word
0	0	Report word
0	1	RX status word
1	0	TX status word
1	1	Not used

REPORT WORD

The report word gives the subsystem information as to the type of error associated with the last transfer (the word will be clear if no error occurred). The report word is formatted as follows:



The Report word is written at the end of message execution, after all retries have been exhausted and prior to the IRQN line being set active This word indicates the health of the terminal as well as information relating to the message execution.

Transmitter Timeout Error

This bit will be set if a transmitter timeout error occurs while the terminal is transmittting or if a self test on the transmitter timeout mechanism fails. This will come into effect 800us after the commencement of the Self Test. The setting of this bit will also cause a subsystem interrupt to be generated.

This bit will be reset to logic zero if the terminal is reset.

Subsystem Handshake Failure

This bit will be set if the subsystem fails to acknowledge a terminal request to transfer a data word in 0.75us for a received data word or 13.5us for a transmit data word. If this condition takes place while the terminal is transmitting the transmission will be aborted. The setting of this bit will also cause a subsystem interrupt to be generated..

This bit will be reset to logic zero if the terminal is reset.

Loop Test Failure

This bit will be set if the receiver circuitry detects an absence of terminal transmission or a waveform encoding error occurs while the terminal is transmitting. The seting of this bit while the terminal is transmitting will cause the transmission to be aborted and a subsystem interrupt to be generated.

This bit will be reset to logic zero if the terminal is reset.

Programmed Halt

This bit will be set if the Interrupt Always flag of the Instruction word has been selected.

This bit will be reset at the start of each new instruction execution cycle.

Retry Used

This bit will be set if one or more message retries has been attempted.

This bit will be reset at the start of each new instruction execution cycle.

Word Count Low

This bit will be set if the terminal detects fewer valid data words than specified by the Transmit Command word of the Instruction set.

This bit will be set low at the start of each instruction execution cycle or message retry.

Word County High

This bit will be set if the terminal detects more valid data words than specified by the Transmit Command word of the Instruction set.

This bit will be set low at the start of each instruction execution cycle or message retry.

Command Error

This bit will be set if an error occurs in the Instruction set. The setting of this bit will cause instruction execution to be aborted and a subsystem interrupt to be generated.

This bit will be reset at the start of each new instruction execution cycle.

TX Status Missing

This bit will be set if a no-response is detected from an RT which has been commanded to transmit and the relevant RT address was not the Broadcast address.

This bit will be reset at the start of each new instruction cycle or message retry.

TX Status Flag

This bit will be set if the status word received from a transmitting RT has a bit set or has the wrong terminal address.

This bit will be reset at the start of each new instruction execution cycle or message retry.

RX Status Missing

This bit will be set if a no-response is detected from an RT which has been commanded to receive and the relevant RT address was not the Broadcast address.

This bit will be reset at the start of each new instruction cycle or message retry.

RX Status Flag

This bit will be set if the status word received from a receiving RT has a bit set or has the wrong terminal address.

This bit will be reset at the start of each new instruction execution cycle or message retry.

Transmitter Timeout On Bus 0

This bit will be set if the transmitter timeout mechanism operates on Bus 0. This will be set under Self Test execution with Bus 0 selected in the Instruction word.

This bit will be reset to logic zero if the terminal is reset.

Transmitter Timeout On Bus 1

This bit will be set if the transmitter timeout mechanism operates on Bus 1. This will be set under Self Test execution with Bus 1 selected in the Instruction word.

This bit will be reset to logic zero if the terminal is reset.

Continuous Bus Traffic

This bit will be set if the terminal detected that the data bus is already active when the BC is instructed to execute a message on that data bus. An active data bus is defined as a data stream of one command word or status word and greater than 32 continguous data words being received by the terminal. The setting of this bit will cause transmission to be suppressed and a subsystem interrupt to be generated.

It should be noted that:

1. This condition is only likely to be caused by a runaway RT which transmits continuously.
2. If this condition is present the subsystem is able to specify the use of the alternative bus for its transmissions.

This bit will be reset to logic zero when the terminal is reset or when the terminal detected a quiet bus.

RECEIVE STATUS WORD

The receive status word location is addressed when CODENN, C1 and R/WN are low and C0 is high. This location is used by the terminal to store the status word, if any, received from a receiving RT. In self test mode this location is updated with the contents of the receive command word during the instruction fetch cycle.

TRANSMIT STATUS WORD

The transmit status word location is addressed when CODENN, C0 and R/WN are low and C1 is high. This location is used by the terminal to store the status word, if any, received from a transmitting RT. In self test mode this location is updated with the contents of the transmit command word during the instruction fetch cycle.

MODES OF OPERATION

The Bus Controller may be controlled in either a single shot mode or in a table driven mode. In the former, the execution of the message table would be under direct control of the subsystem, on a message by message basis.

The table driven mode would provide a subsystem capable of more autonomous operation, leading to a greatly reduced level of processor intervention in the message execution level, at least. In either case the procedure of Instruction fetch, message execute and reporting would be the same. The difference arises from the value of the HALTREQN line when it is resampled at the end of message execution. This is further described below.

SINGLE SHOT OPERATION

To commence a message execution the subsystem must take the HALTREQN line low to high for a minimum of 1us. This will be followed by the terminal acknowledging this action by the HALTEDN line being set inactive (high). The HALTEDN line will remain high until the message has been completed, at which time the HALTREQN line is further sampled. If it is low then the terminal will halt and wait until the request line is taken high again, in effect a single instruction execution.

It is important to the integrity of the system that the HALTREQN line is strictly glitch free, otherwise problems will arise with the terminal attempting to execute commands at a time when no terminal access to the various stores can be guaranteed.

CONTINUOUS OPERATION

The continuous message table operation mode can be achieved by ensuring that at the end of a message the HALTREQN line is high. Thus, assuming that the message has executed correctly, the terminal will generate a signal to increment the external address counter (INCADRN) and continue to the next instruction. If, however there has been an interrupt generated (IRQN active) the terminal will halt in the HALTEDN state until specifically requested to continue. Note that no address increment will take place. To continue execution the HALTREQN line should be taken low to high for the appropriate time.

Continuous table driven operation results in an intermessage gap of 20us.

Figure 1 shows the instruction fetch and execute cycle.

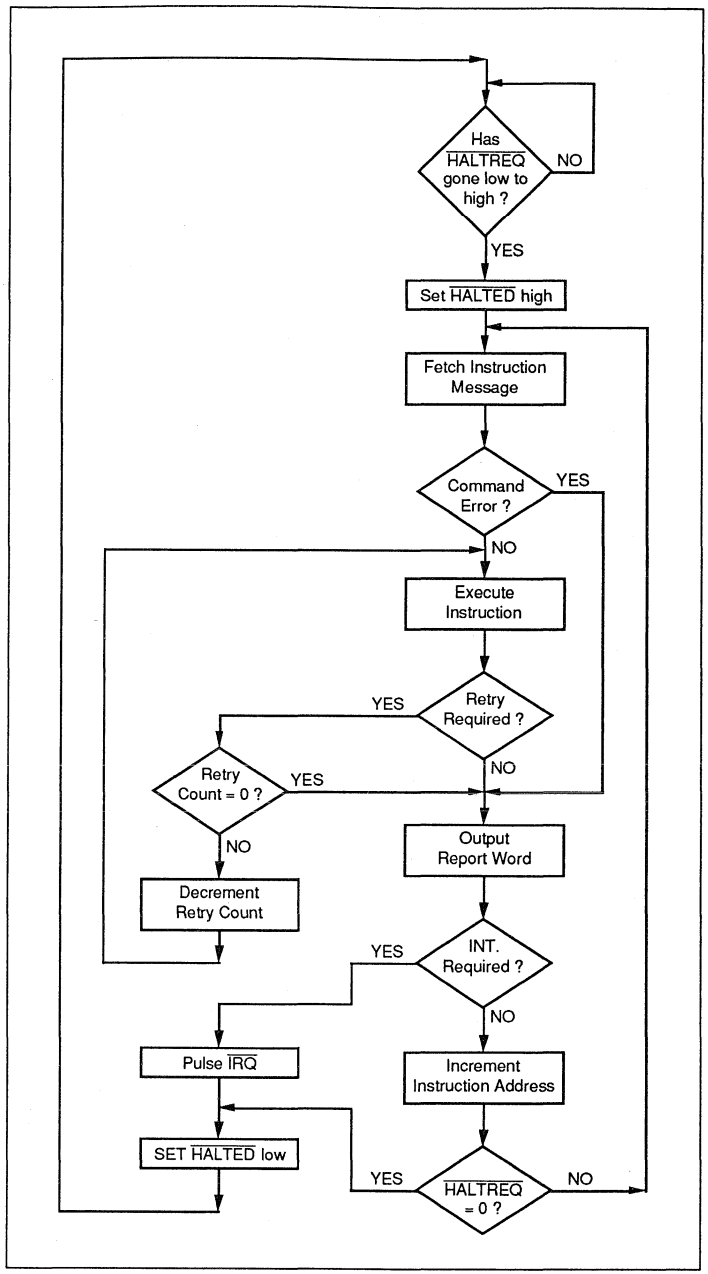


Figure 1: BC Instruction Fetch and Execute Cycle

PASSIVE MONITOR

The terminal may be configured into a Passive Monitor (or Bus Monitor) merely by selecting the appropriate Function Code of the Instruction word. By doing this the terminal will not take part in any further Instruction execution but instead will monitor the selected bus for data transmissions.

INTERRUPT / RETRY CAPABILITY

The terminal has certain in-built functions which permit the terminal to retrieve situations which would normally cause a greater degree of subsystem intervention. This is achieved by having an automatic retry facility in-built to the terminal which is selectable from the Instruction word. In this case both the condition and number of attempts for which the terminal must try may be specified. After completion of the required number of attempts, terminal operation may be halted with the possibility of an interrupt generated also.

The interrupt facility provides a means of more direct subsystem interaction in the event of a failure. Similar flags are required to be set in the Instruction word before a selectable interrupt may be generated. This form of interrupt also includes an Interrupt Always flag whose application may be used to determine subsystem/system timing requirements.

It should be noted that an interrupt may also be generated by the error checking procedures of the terminal which verify aspects of the Instruction word and associated Receive/ Transmit command words.

STANDBY BUS CONTROLLER

The terminal provides a number of signals to the subsystem for message addressing and execution. Two address lines are provided (CO, CI) plus a signal to increment an external counter (INCADRN). This, together with the on-chip sequencing, error checking, etc., enables a standby bus controller, using a fixed table of messages, to be realised in few devices as shown in Figure 2. It is therefore possible to attain a standby BC on a single 6 x 4 PCB card.

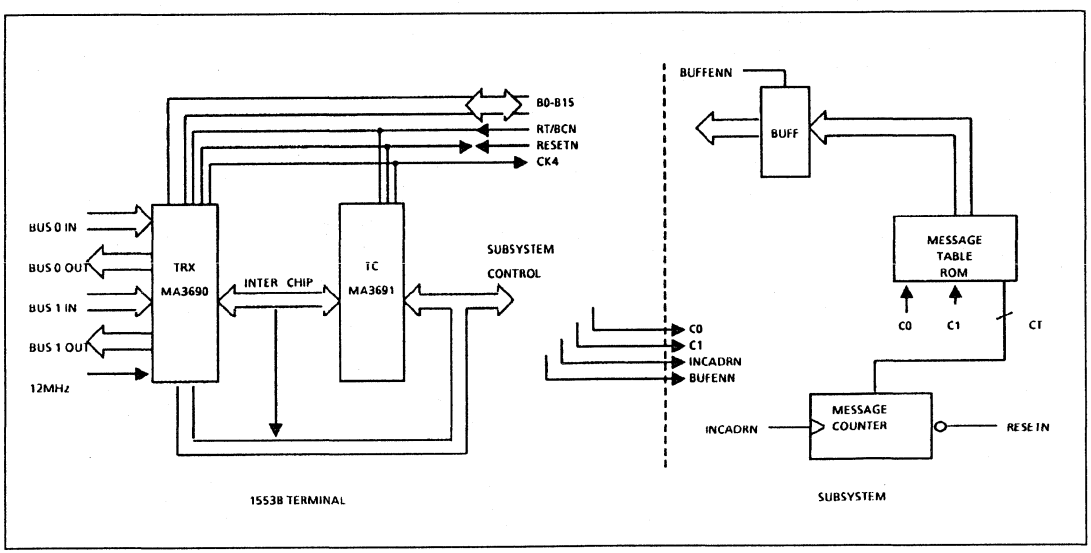


Figure 2: Standby Bus Controller

FULL BUS CONTROLLER

To make use of the SOS chipset's capabilities a processor-based system would be more applicable. A block diagram of such a system, using shared store technique is shown in Figure 3. In this, the instruction word store would be alterable by the processor for use in various system conditions, i.e. a basic message table would initialy be set up with the processor monitoring the results of execution from the report word store and / or the interrupt request (IRQN) line. On detection of an erroneous condition, the processor could write a new message table to test the RT in error by, for example, a self test mode command. The inclusion of automatic retry, with a maximum of 3 retries, in the instruction word, removes the requirement from the processor to retry under simple RT faults, e.g., status bit set.

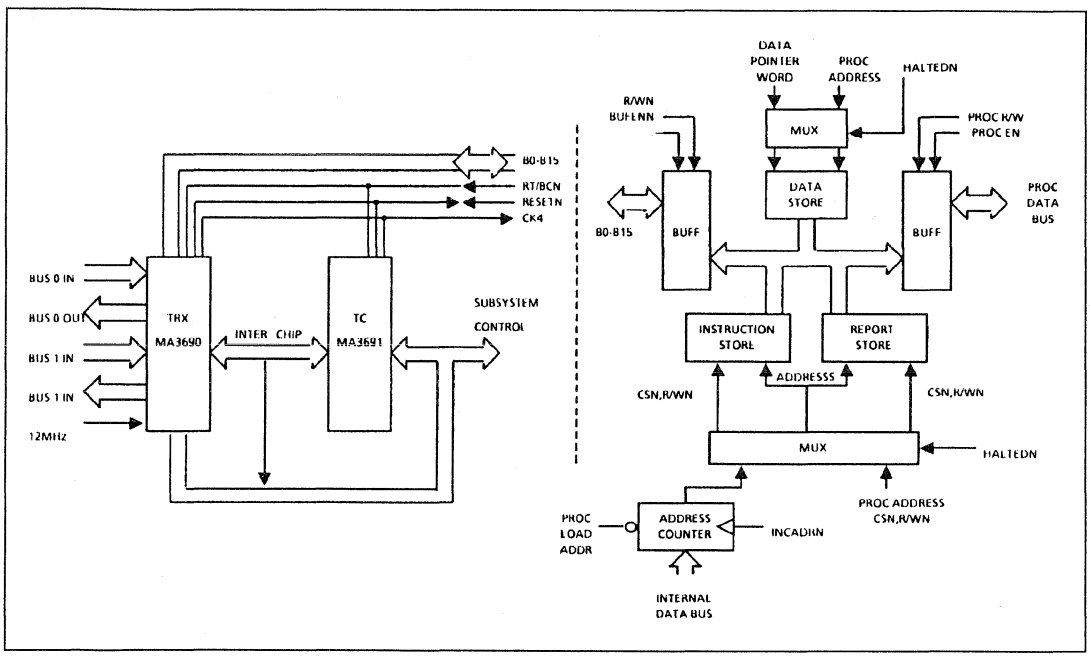


Figure 3: Full Bus Controller

SUBSYSTEM INTERFACE

The terminal / subsystem interface consists of a 16 bit bidirectional data highway and a number of control lines, many of which are of optional use. The subsystem lines have been arranged such as to allow a simple shared store technique to be readily implemented but sufficient flexibility has been designed to allow optimisation of the interface for a particular subsystem design.

REMOTE TERMINAL MODE

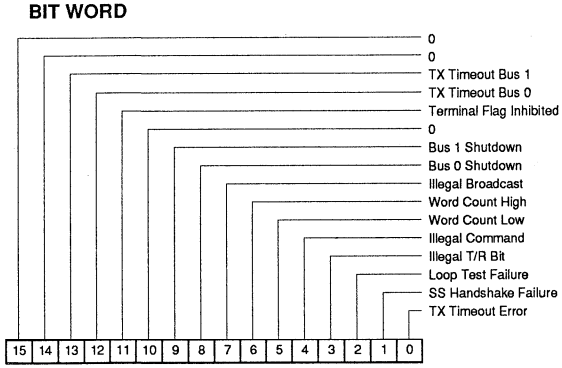
On initialisation, the RT address, address parity and broadcast enables are loaded from the subsystem via the data highway, Figure 4. The subsystem status bits are also loaded in a similar manner when required, Figure 5.

This terminal uses two distinct methods for dealing with non mode data and mode data. In the first, a busy request / acknowledge handshake is used to ensure no data transfer takes place when the subsystem is busy thus ensuring no addressing / data conflict of the main data store. Mode data, however, may be transferred even if the subsystem has declared itself busy. This represents a departure from previous chipset philosophy.

The validation of a data transfer also depends on data type. For non mode data, a data transfer request / acknowledge handshake is used to transfer each data word to or from the subsystem (both RT and BC) with a good block received (GBRN) denoting a correct transfer. For mode data, a mode data transfer (MDTN) is used to signal a mode data word with correct transfer being denoted by mode data received (MDRN). Thus, dependant on application, the I/O signals may be significantly reduced.

An RT subsystem interface signal transfer is shown in Figure 6.

BIT WORD



The terminal contains a 16 regisiter, called BIT word, which records message errors and terminal status information. The entire BIT word contents are reset by power up initialisation or a legal mode command to reset remote terminal. The conditions for the setting of the BIT, and any additional reset conditions are given for each signal.

The contents of the BIT word register shall not be altered by any of the following legal mode commands. Transmit Status Word (TSW), Transmit Last Command (TLC) and Transmit BIT Word (TBW).

Transmitter Timeout Error

This BIT shall be set to logic one if transmitter timeout occurs while the terminal is tranmitting. In addition, if the terminal is issued with a legal mode command to Initiate Self Test (code 00011) this bit shall be set if the range transmitter timeout mechanism does not operate within the of 660 µs to 800 µs.

Subsystem Handshake Failure

This bit shall be set to logic one if the subsystem does not acknowledge a terminal request to transfer a data word in time for the transfer to take place correctly.

Loop Test Failure

At all times while the terminal is transmitting the relevant receiver circuitry checks for an absence of transmission or any sync, Manchester, parity or contiguity error in the terminals transmission. This bit shall be set to logic one if any of these error conditions are detected.

Illegal T/R Bit

This bit shall be reset to logic zero by the reception of any valid command word with the exception TSW,TLC and TBW.

This bit shall be set to logic one if a valid mode command is received with a transmit/receive (T/R) bit opposite to that specified by MIL-STD-1553B.

Illegal Command

This bit shall be reset to logic zero by the reception of any valid command word with exceptions TSW, TLC and TBW.

This bit shall be set to logic one if any of the following conditions arise:

(a) The ILLEGAL COMMAND line to the subsystem status latch is low at the time when INCMD goes active low.
(b) A valid mode command is received with a reserved mode code and the ALLOW CODE line to the subsystem staus latch is high at the time when $\overline{\text{INCMD}}$ goes low.
(c) An illegal transitter shutdown mode command is received.

Word Count Low

This bit shall be reset to logic zero by the reception of any valid command word with the exception of TSW, TLC and TBW.

This bit shall be set to logic one if fewer valid data words are received than specified by the preceding command word.

Word Count High

This bit shall be rest to logic zero by the reception of any valid command word with the exception of TSW, TLC and TBW.

This bit shall be set to logic one if the received message is longer than stipulated by the preceeding command word.

Illegal Broadcast

This bit shall be reset to logic zero by the reception of any valid command word with the exception of TSW, TLC and TBW.

This bit shall be set to logic one if a valid command word which by definition requires terminal transmission is received with the broadcast address.

Bus 0 Shutdown

This bit shall be set to logic one if bus 0 is shutdown.

Bus 1 Shutdown

This bit shall be set to logic one if bus 1 is shutdown.

Terminal Flag Inhibited

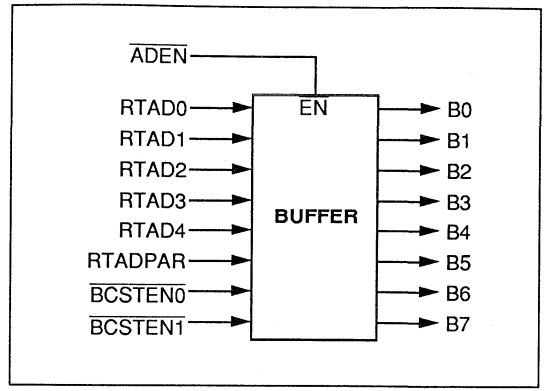
This bit shall be set to logic one if the internal terminal flag inhibit is set.

Transmitter Timeout on Bus 0

This bit shall be set to logic one if a transmitter timeout has occured on bus 0.

Transmitter Timeout on Bus 1

This bit shall be set to logic one if a transmitter timeout has occured on bus 1.

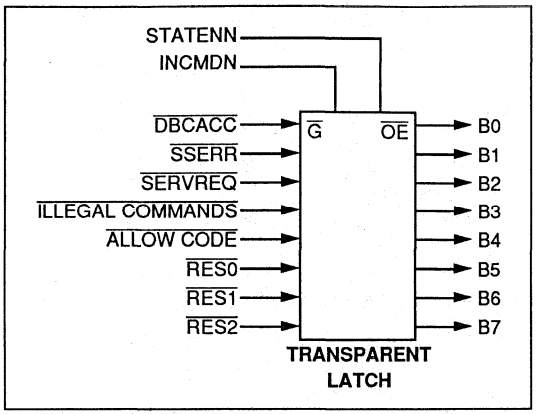


Note: RTAD0, RTAD1, RTAD2, RTAD3, RTAD4 define the RT address RTADPAR odd parity with the address bits

BCSTEN0 - Broadcast enable for BUS0

BCSTEN1 - Broadcast enable for BUS1

Figure 4: Subsystem RT Address Buffer



$\overline{\text{DBACC}}$ - Dynamic Bus Acceptance. If low then the Dynamic Acceptance bit of the terminal status word will be set in response to a legal Mode Command for Dynamic Bus Control allocation. After switching to the BC mode of operation the first instruction must be a NOOP.

$\overline{\text{SSERR}}$ - A low will cause the Subsystem flag to be set in the terminal status word.

$\overline{\text{SERVREQ}}$ - A low will set the service request bit of the terminal status word.

$\overline{\text{ILLEGAL COMMAND}}$ - Allows the subsystem to declare any command word illegal. When low the terminal will inhibit data transfers to or from the subsystem, and after message validation will respond with the message error bit set in the terminal status word.

$\overline{\text{ALLOW CODE}}$ - Provides the subsystem with the capability to declare any of the reserved mode codes as being meaningful. If a reserved mode code is received when high the command is treated as illegal and after message validation responds with ME bit set in the terminal status word. If low the most significant bit of the mode code and the T/R bit determine whether any data words are involved and their direction.

$\overline{\text{RES0}}$, $\overline{\text{RES1}}$, $\overline{\text{RES2}}$ - Provides the subsystem the capability of setting any of the currently reserved bits of the terminal status word.

Figure 5: Subsystem Status Latch

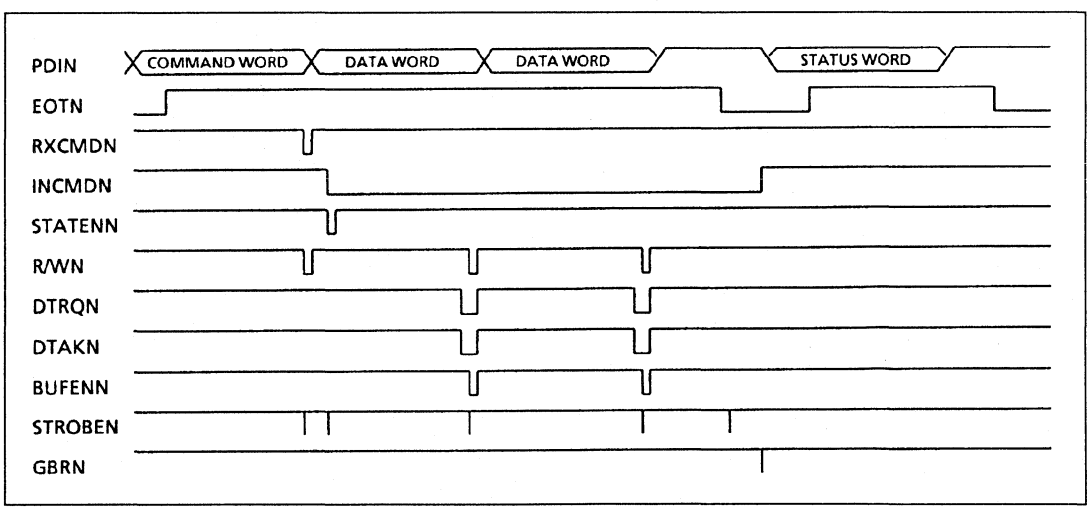


Figure 6: Remote Terminal Subsystem Interface Signal Transfer

BUS CONTROLLER MODE

For data transfers generally, 750ns enable signals (BUFENN,R/WN etc.) are produced by the terminal with a 250ns strobe signal upon which the data will be valid.

The bus controller terminal provides signals to fetch the message and write out a report and any associated data. The HALTREQN and HALTEDN handshake lines operate in a similar fasion to the BUSYREQN / BUSYACKN RT lines in that if HALTREQN is taken low the terminal will complete the current instruction and then halt, taking HALTEDN low to indicate that it has done so

A BC subsystem may be operated in either a single shot or table driven mode. In either case, the two least significant address lines (C0,C1) to the instruction and report word stores are provided by the terminal. On taking HALTREQN high (for a minimum of 1us) the subsystem initiates an instruction fetch cycle which consists of the terminal reading the instruction word, receive command word and transmit command word from the instruction store and transferring the data pointer word from the instruction store to an external data address latch. Further operation is dependent on the instruction word.

On executing a message sequence the terminal will write out the report word and either:

1. Increment the instruction address and proceed to the next instruction,
2. Increment the instruction address and halt,
3. Do not increment the instruction address, interrupt subsystem and halt.

Any data associated with the command will be transferred to or from the data store in a similar manner as used by the RT.

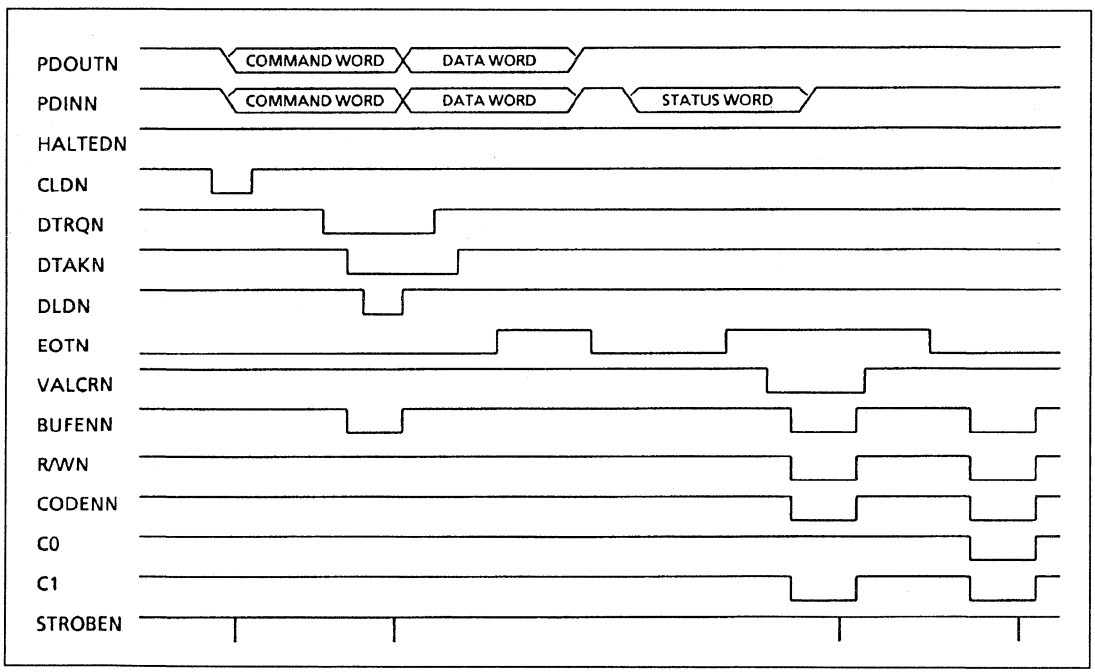


Figure 7: Bus Controller Subsystem Interface Signal Transfer

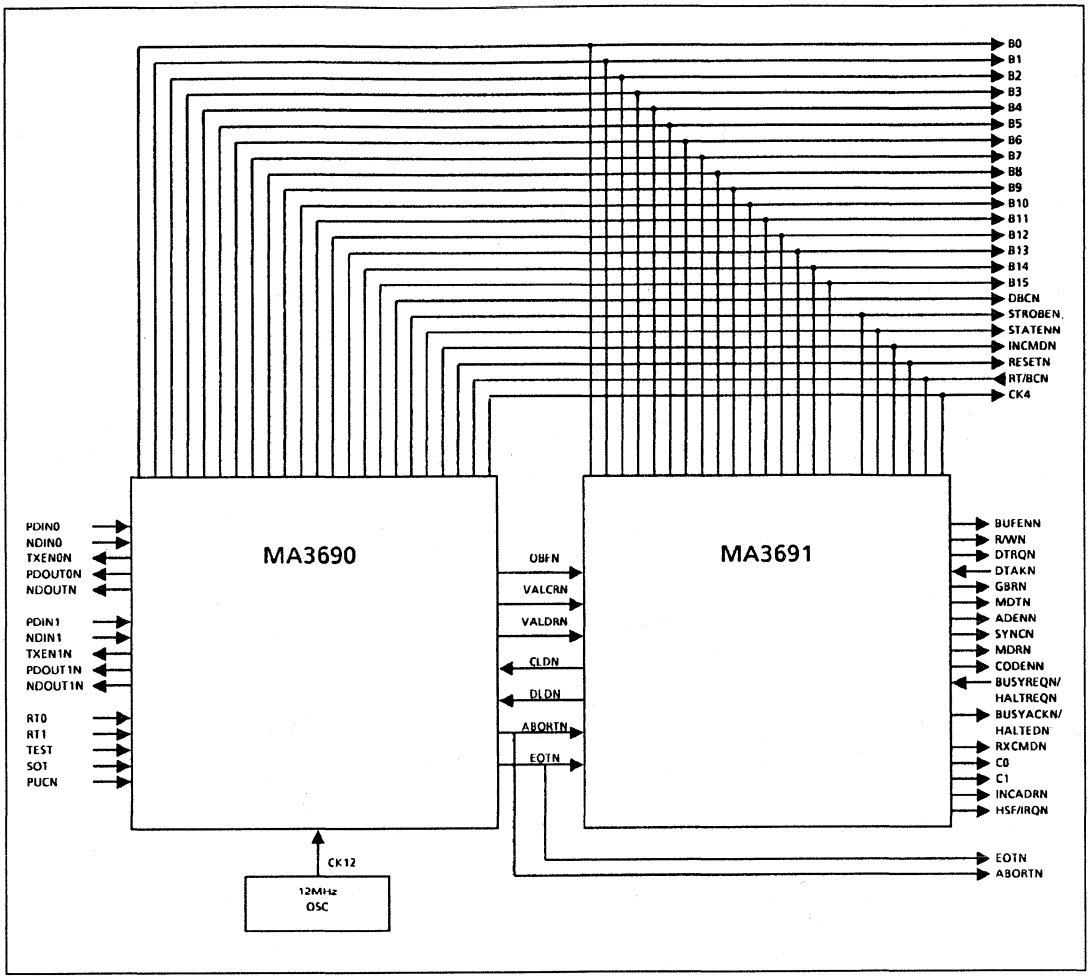


Figure 8: Chip Set Interconnection Diagram

Subgroup	Definition
1	Static characteristics specified in Figure 11 at +25°C
2	Static characteristics specified in Figure 11 at +125°C
3	Static characteristics specified in Figure 11 at -55°C
7	Functional characteristics specified at +25°C
8a	Functional characteristics specified at +125°C
8b	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figure 12 at +25°C
10	Switching characteristics specified in Figure 12 at +125°C
11	Switching characteristics specified in Figure 12 at -55°C

Figure 9: Definition of Subgroups

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 10: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL Input High Voltage	-	2.0	-	-	V
V_{IL1}	TTL Input Low Voltage	-	-	-	0.8	V
V_{IH2}	CMOS Input High Voltage	-	3.5	-	-	V
V_{IL2}	CMOS Input Low Voltage	-	-	-	1.5	V
V_{OH1}	TTL Output High Voltage	I_{OH} = -1mA	V_{DD}-0.4	-	-	V
V_{OL1}	TTL Output Low Voltage	I_{OL} = 2mA	-	-	0.4	V
V_{OH2}	CMOS Output High Voltage	I_{OH} = -1mA	V_{DD}-0.4	-	-	V
V_{OL2}	CMOS Output Low Voltage	I_{OL} = 2mA	-	-	0.4	V
I_{IL1}	Input Low Current	V_{IN} = V_{SS} (Note 1)	-	-	-10	µA
I_{IH1}	Input High Current	V_{IN} = V_{DD} (Note 1)	-	-	10	µA
I_{IL2}	Input Low Current (RT1)	V_{IN} = V_{SS} (Note 1)	-	-	-50	µA
I_{IH2}	Input High Current (RT2)	V_{IN} = V_{DD} (Note 1)	50	-	150	µA
I_{OZL}	IO Low Current	V_{IN} = V_{SS} (Note 1)	-	-	-50	µA
I_{OZH}	IO High Current	V_{IN} = V_{DD} (Note 1)	-	-	50	µA
I_{DD}	Power Supply Current	-	-	-	25	mA

V_{DD} = 5V±10%, over full operating temperature range.
Note 1: Guaranteed but not tested at -55°C
Mil-Std-883, method 5005, subgroups 1, 2, 3

Figure 11: Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
t1	CK4 to BUS [B0:B15] VALID			235	nS
t2	CK4 to BUS [B0:B15] High Impedance			220	nS
t3	B0: B15 set up wrt STROBEN ↑	15			nS
t4	B0: B15 hold wrt STROBEN ↑	25			
t5	VALCRN ↓ to RXCMDN ↓		3t		
t6	Pulse width RXCMDN, R/WN, STATENN, BUFENN, CLDN, DLDN, MDTN, CODENN		3t		
t7	Pulse width STROBEN, GBRN, MDRN, SYNCN, IRQN		1t		
t7a	RXCMDN/R/WN/STATENN/BUFENN/CLDN/DLDN /MDTN, CODENN ↓ to STROBEN		1t		
t7b	As 7a from STROBEN ↑		1t		
t8	RXCMDN ↑ to INCMD ↓		4t		
t9	INCMDN ↓ to STATENN ↓		3t		
t10	VALCRN pulse width		5t		
t11	VALDRN ↓ to DTRQN ↓			1t	
t12	DTRQN ↓ to DTAKN ↓ (RXDATA)	0		3t	
t13	DTAKN ↓ to BUFENN ↓	1t		2t	
t14	DTRQN ↑ to CLDN ↓		24t		
t15	CLDN ↑ to GBRN ↓	15t		16t	
t16	CLDN ↓ to STATUS valid BUS B0:B15			100	nS
t17	CLDN ↑ to STATUS invalid on B0:B15	35			nS
t18	DTRQN ↑ to DTAKN ↑	0			
t19	STATENN to CLDN ↓ Non mode data	11t		12t	
t20	CLDN ↑ to DTRQN ↓		15t		
t21	DTRQN ↓ to DTAKN ↓ (TX data)	0		54t	
t22	VALDRN ↓ to R/WN ↓	2t		3t	
t23	MDTN ↓ to CLDN ↓		24t		
t24	CLDN ↑ to MDRN ↓		14t		
t25	STATENN to CLDN ↓ mode data	11t		12t	
t26	CLDN ↑ to MDTN ↓	15t		16t	
t27	MDTN ↑ to INCMDN ↑	77t		78t	
t28	DTRQN ↑ to INCMDN ↑ (non broadcast)	77t		78t	
t29	DTRQN ↑ to INCMDN ↑ (broadcast)		25t		
t30	MDTN ↑ to INCMDN ↑ (broadcast)		25t		
t31	CLDN ↑ to INCMDN ↑ (mode)	11t		12t	
t32	CLDN ↑ to TXENN ↓	1t		2t	
t33	TXENN/PDOUTN/NDOUTN/prop delay difference		6		nS
t34	Start of transmission to EOTN ↑		$76t_{12}$		
t34a	End of transmission to EOTN ↓		$82t_{12}$		
t35	End of transmission to ABORTN ↓				
	1) RT1 = 0 RT0 = 0			20	uS
	2) RT1 = 0 RT0 = 1			26	uS
	3) RT1 = 1 RT0 = 0			48	uS
	4) RT1 = 1 RT0 = 1			112	uS
t36	Minimum no response timeout				
	1) RT1 = 0 RT0 = 0	15.75		16.25	uS
	2) RT1 = 0 RT0 = 1	21.75		22.25	uS
	3) RT1 = 1 RT0 = 0	43.75		44.25	uS
	4) RT1 = 1 RT0 = 1	107.75		108.25	uS
t37	Remote terminal response time	10.3		11.25	uS
t38	Minimum PUCN pulse width	20			nS
t39	PUCN ↓ to RESET ↓			90	nS

Figure 12: AC Electrical Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
t40	RESETN ↓ to ADEN ↓			80	nS
t41	PUCN ↑ to RESETN ↑		2t		
t42	RESETN ↑ to ADENN ↑		2t	2t + 80	nS
t43	Initialisation word set-up wrt RESETN ↑	15			nS
t44	Initialisation word HOLD wrt RESETN ↑	20			nS
t45	Minimum RESETN pulse width	90			nS
t46	Minimum CK12 high	33			nS
t47	Minimum CK12 low	20			nS
t48	CK12 ↑ to CK4 ↑			90	nS
t49	CK12 ↓ to CK4 ↓			90	nS
t50	HALTREQN pulse width	1t			
t51	HALTREQN ↑ to HALTEDN ↑			55	nS
t52	HALTREQN ↑ to CODENN ↓	1t		2t	
t53	CODENN ↑ to CODENN ↓		2t		
t54	RT-RT minimum validation time				
	1) RT1 = 0 RT0 = 0	55.75		56.25	uS
	2) RT1 = 0 RT0 = 1	61 75		62.25	uS
	3) RT1 = 1 RT0 = 0	83.75		84.25	uS
	4) RT1 = 1 RT0 = 1	147.75		148.25	uS
t55	HALTREQN setup for next message wrt to INCMDN ↑		150		nS
t56	R/WN ↓ to R/WN ↓ RT-BC Report cycle		80t		
t57	BUFENN ↑ to BUFENN ↓ Data word to report word		29t		
t58	BC intermessage gap				
	1) without a No Operation instruction		20		uS
	2) with a No Operation instruction		28		uS
t59	CODENN interval high between received status and report word during report cycle		24t		
t60	CODENN interval between report word and next message fetch for continuous operation		6t		
t61	CODEN interval between BC Noop data pointer fetch and report word		5t		
t62	INCMDN ↑ to INCADDRN ↓		1t		
t63	BUSYREQN ↓ to BUSYACKN ↓			60	nS
t64	BUSYREQN ↑ to BUSYACKN ↑			60	nS
t65	INCMDN ↑ to BUSYACKN ↓		60		nS
t66	INCMDN ↑ to BUSYACKN ↑		100		nS
t67	CK4 ↑ to R/WN/BUFENN/CO/C1/CODENN/MDTN			115	nS

Mil-Std-883, method 5005, subgroups 9, 10, 11

Notes: 1. t = CK4 period, t_{12} = CK12 period

2. Times quoted as typical means a fixed number of CK4 clock cycles but excludes slight variations due to propagation delays.

Conditions: V_{dd} = 4.5 to 5.5V, T_{amb} = -55°C to +125°C, V_{IL} = 0V, V_{IH} = 4V, V_{OUT} Threshold = 1.5V except t_2 where measured by a 1V change in output voltage. Load = 50pf except t_2 where additional 1K load to 0V or V_{DD}.

Figure 12: AC Electrical Characteristics (continued)

LIST OF TIMINGS

14	Clock Timing
15	Power Up Clear Initialisation
16	Subsystem Reset
17	Minimum No Response Timeout
18	Abort
19	Start of Transmission Detect
20	End of Transmission Detect
21	RT Command Reception and Subsystem Status Read
22	BC-RT Data Transfer (Non Mode) + Status
23	RT Status + RT-BC Data Transfer (Non Mode)
24	Received Mode Data Transfer + Status
25	RT Status + Transfer Mode Data Transfer
26	Broadcast BC-RT Data Transfer (Non Mode)
27	RT-Broadcast Received Mode Data Transfer
28	Mode Command No Data (TIR)
29	Remote Terminal Response Time
30	RT-RT Validation Timeout
31	Remote Terminal Busy Handshake
32	RT Status Load
33	BC-Message Fetch Sequence
34	BC-Report Cycle (shown for RT-RT no data to subsystem)
35	RT-BC Report Cycle
36	BC Intermessage Gap
37	BC-No Operation
38	BC-Self Test (Report Sequence)
39	BC-Passive Monitor
40	BC-Retry
41	BC-Data Transfer Handshake

Figure 13: List of Timings

TIMING DIAGRAMS

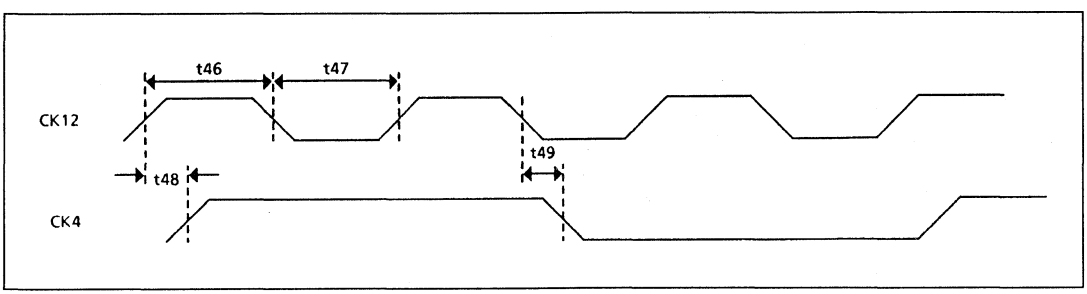


Figure 14: Clock Timing

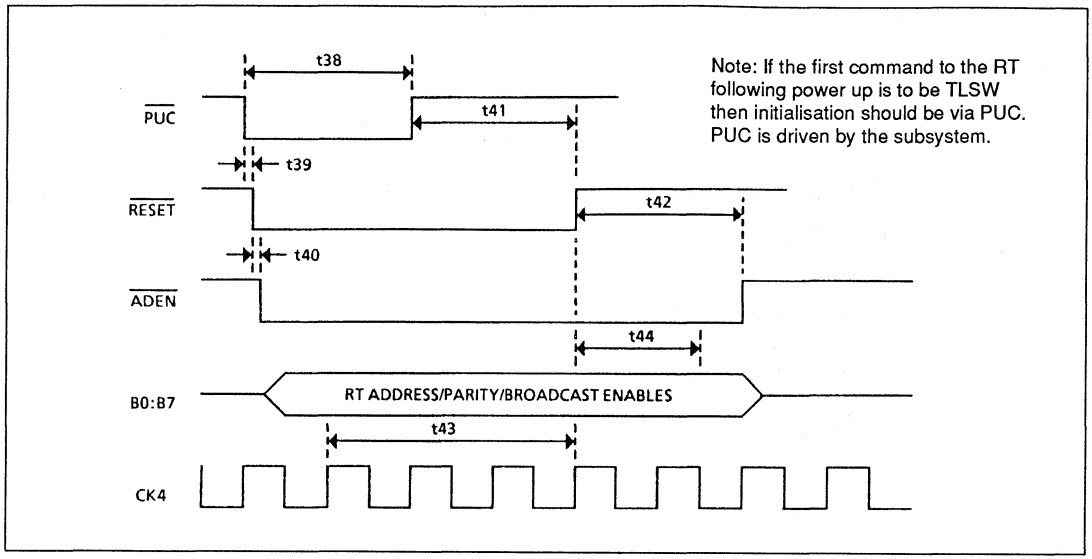


Figure 15: Power Up Clear Initialisation

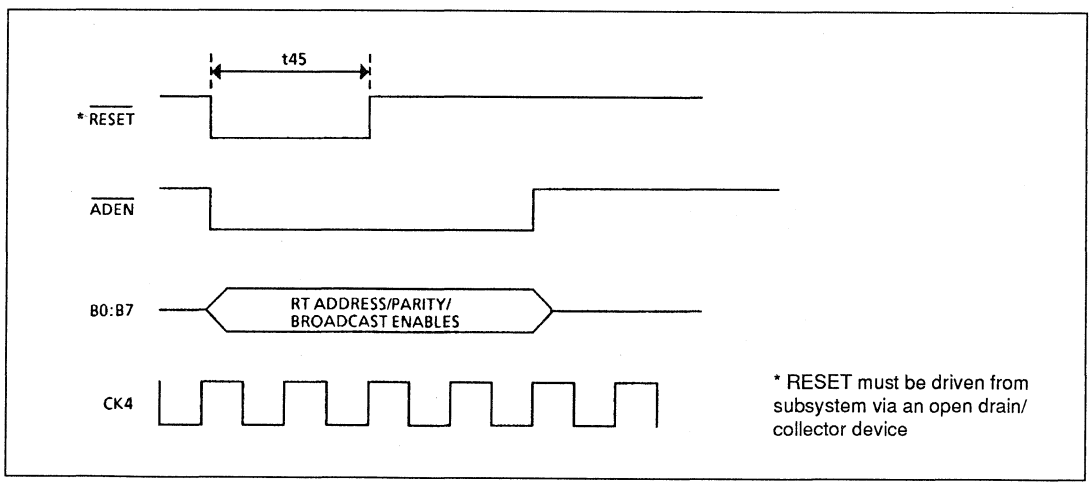
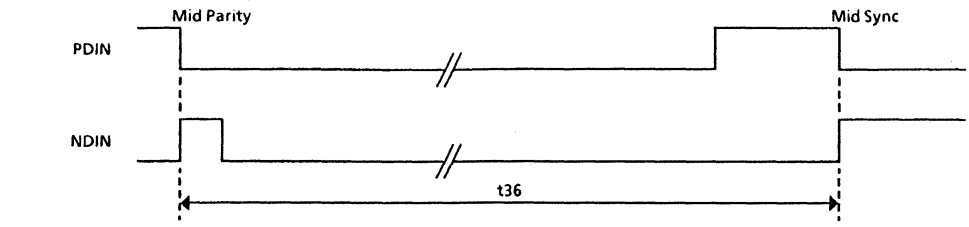
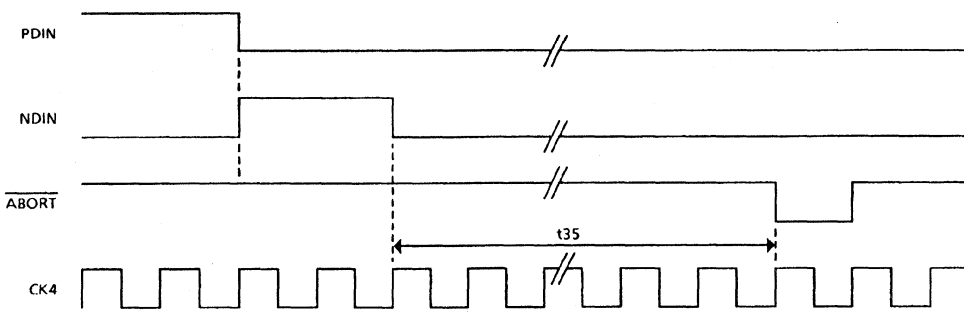


Figure 16: Subsystem Reset



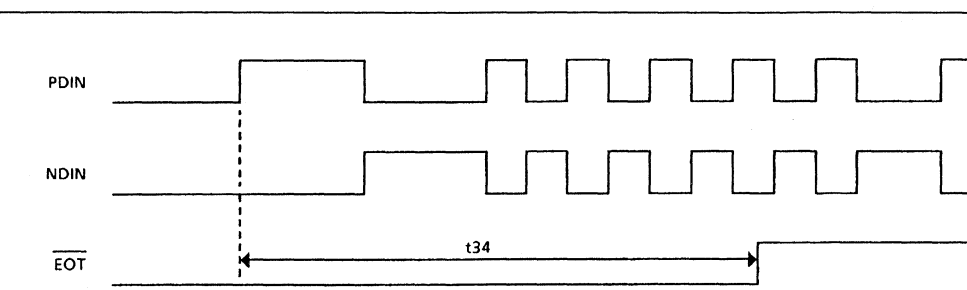
This value is programmable using the RT0/RT1 inputs

Figure 17: Minimum No Response Timeout



This sequence will also occur at the **end** of each message unless a new message is received.

Figure 18: Abort



Note: Detection is sync + 3 data bits

Figure 19: Start of Transmission Detect

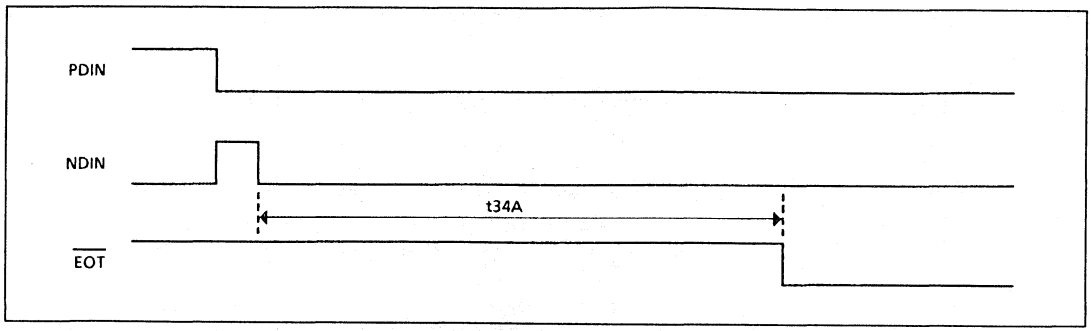
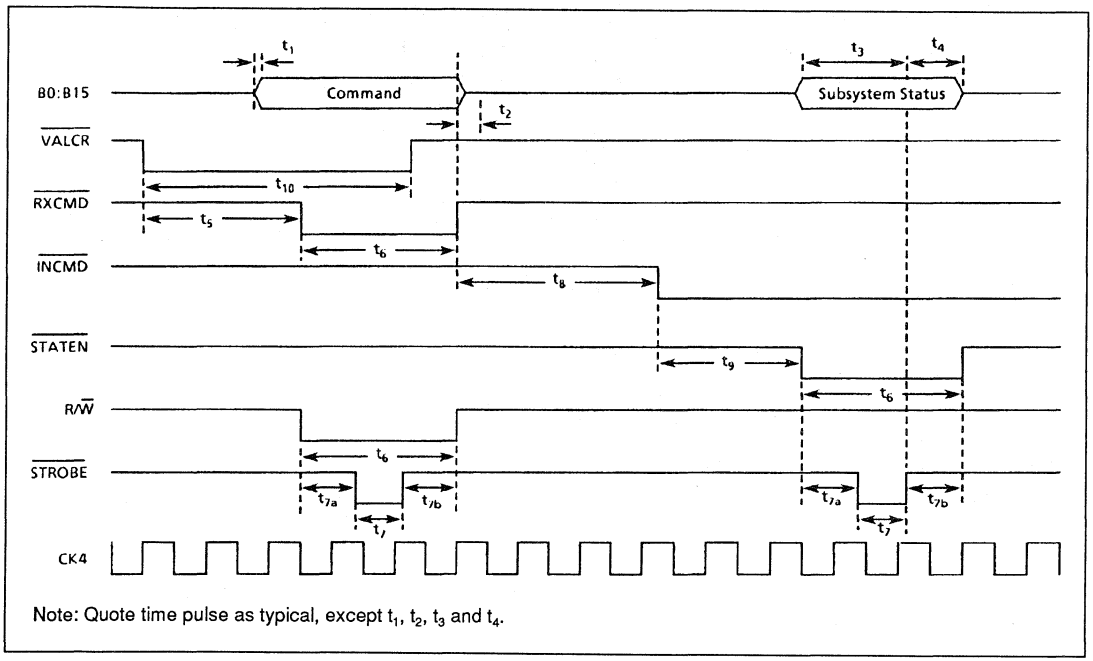


Figure 20: End of Transmission Detect



Note: Quote time pulse as typical, except t_1, t_2, t_3 and t_4.

Figure 21: RT Command Reception and Subsystem Status Read

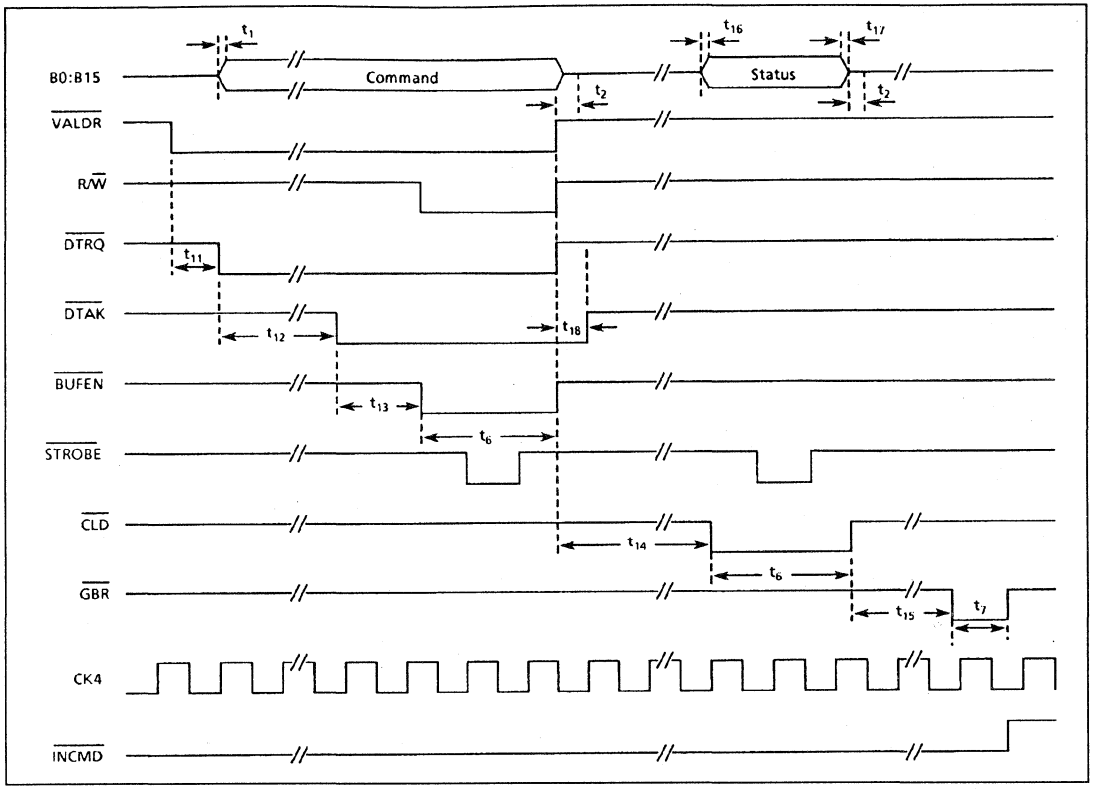


Figure 22: BC-RT Data Transfer (Non-Mode) + Status

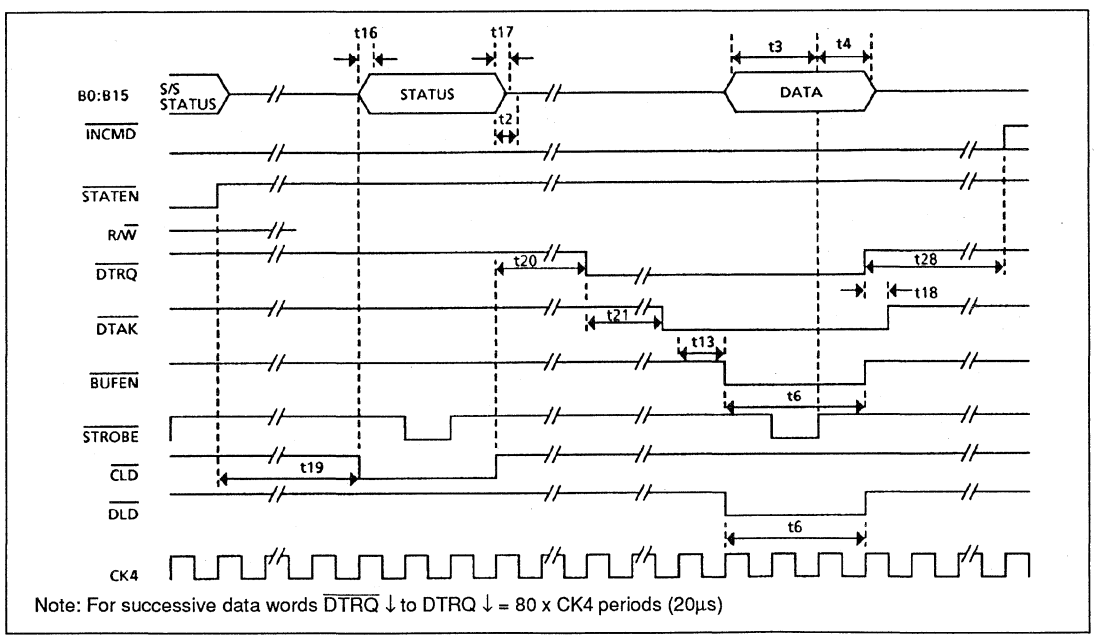


Figure 23: RT Status + RT-BC Data Transfer (Non Mode)

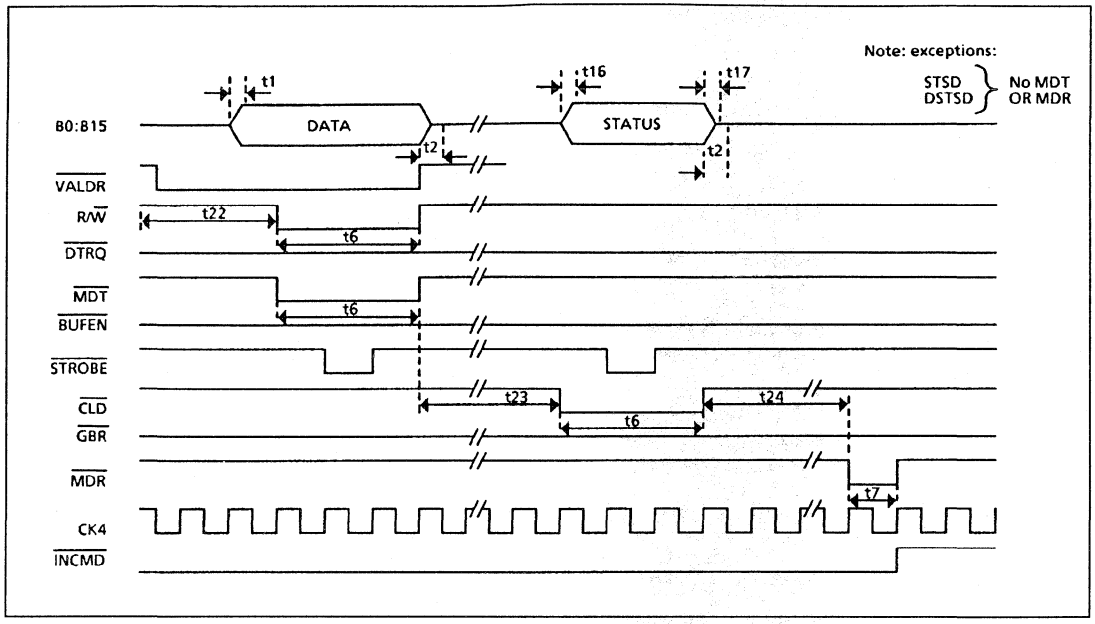


Figure 24: Received Mode Data Transfer + Status

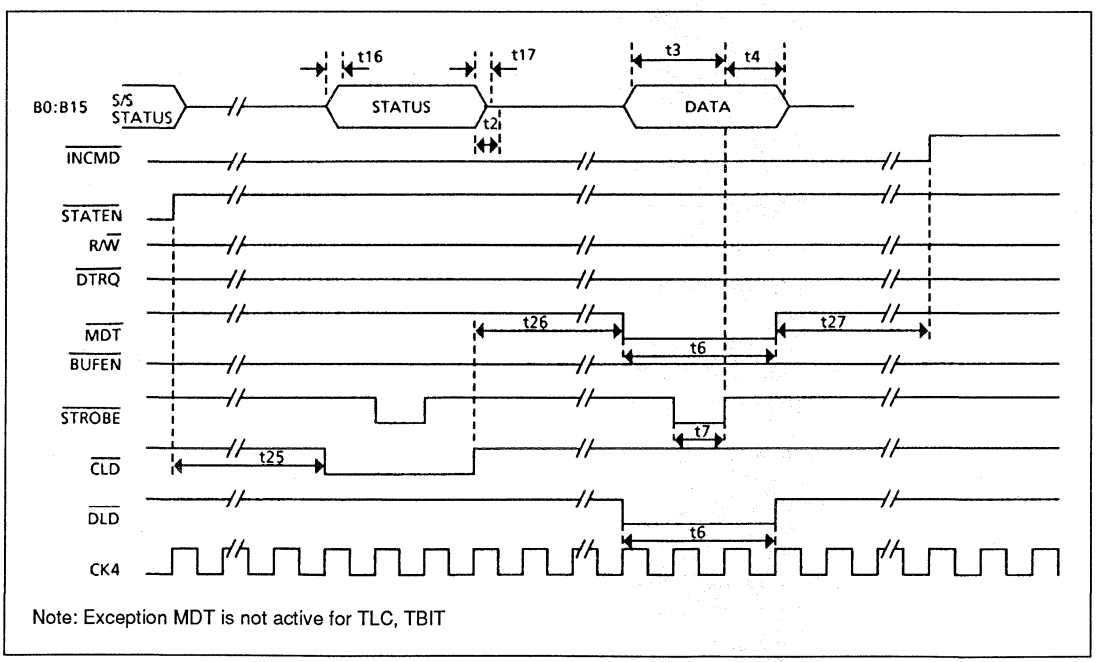


Figure 25: RT Status + Transfer Mode Data Transfer

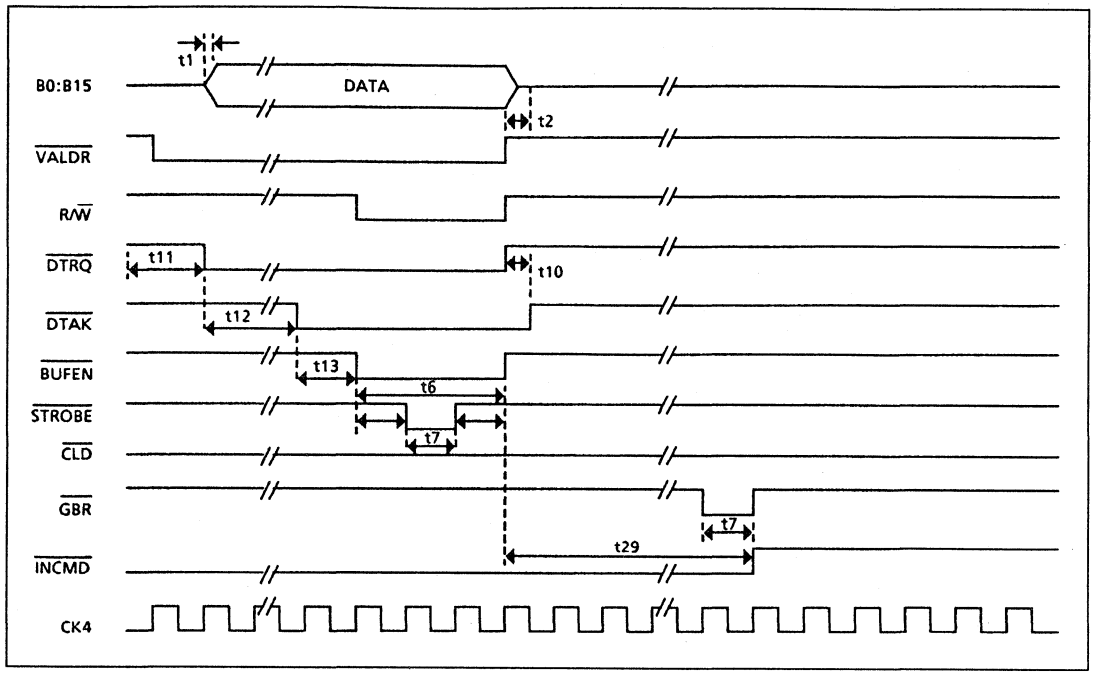
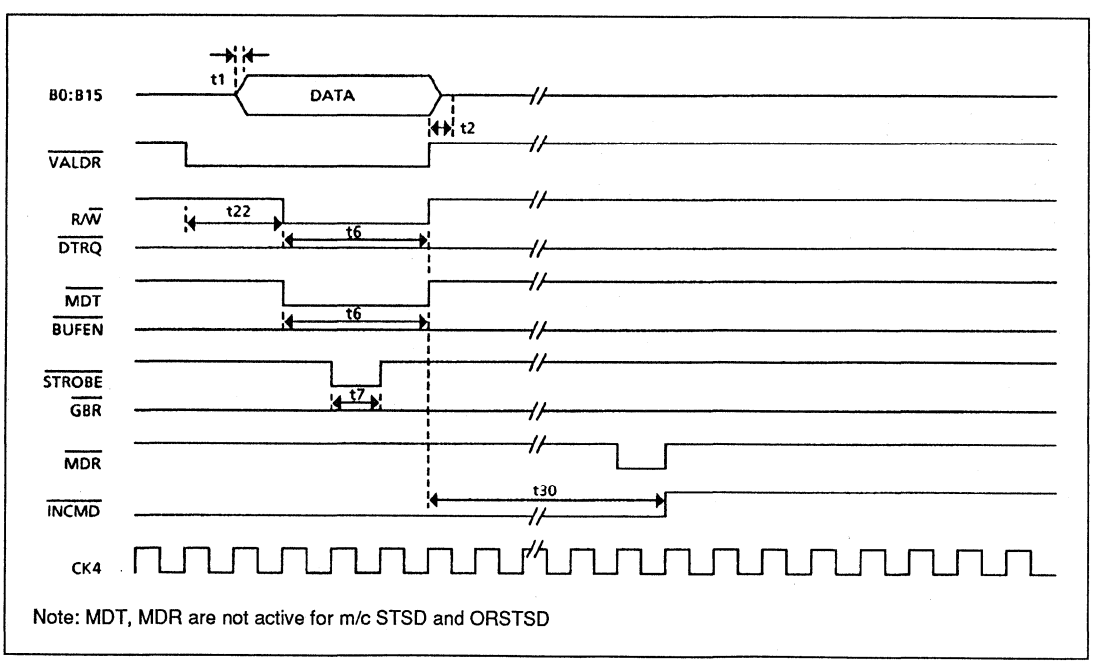
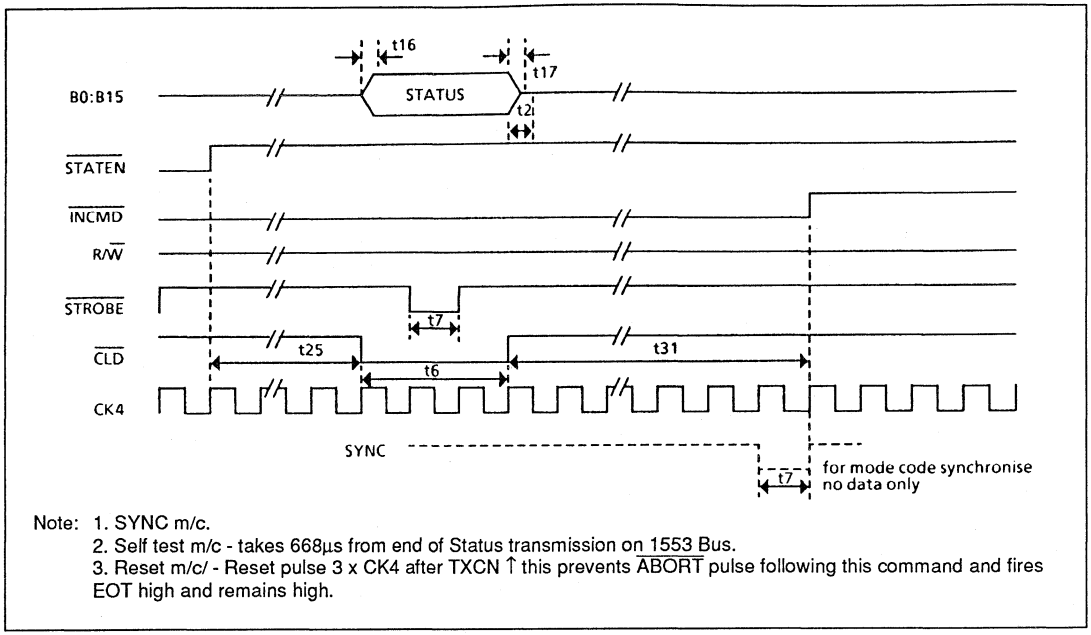


Figure 26: Broadcast BC-RT Data Transfer (Non Mode)



Note: MDT, MDR are not active for m/c STSD and ORSTSD

Figure 27: RT-Broadcast Received Mode Data Transfer



Note: 1. SYNC m/c.
2. Self test m/c - takes 668µs from end of Status transmission on 1553 Bus.
3. Reset m/c/ - Reset pulse 3 x CK4 after TXCN ↑ this prevents ABORT pulse following this command and fires EOT high and remains high.

Figure 28: Mode Command No Data (TIR)

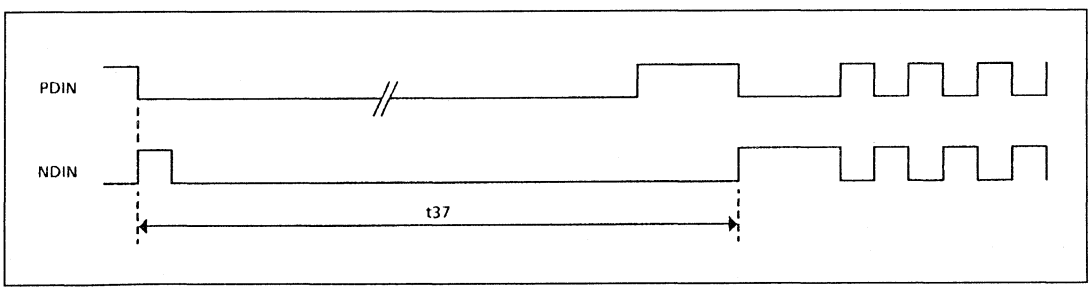


Figure 29: Remote Terminal Response Time

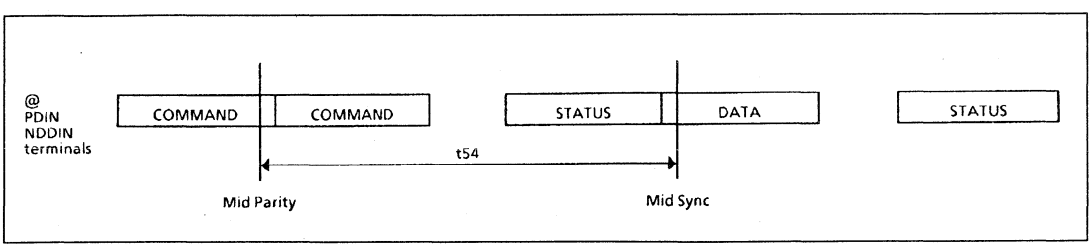


Figure 30: RT-RT Validation Timeout

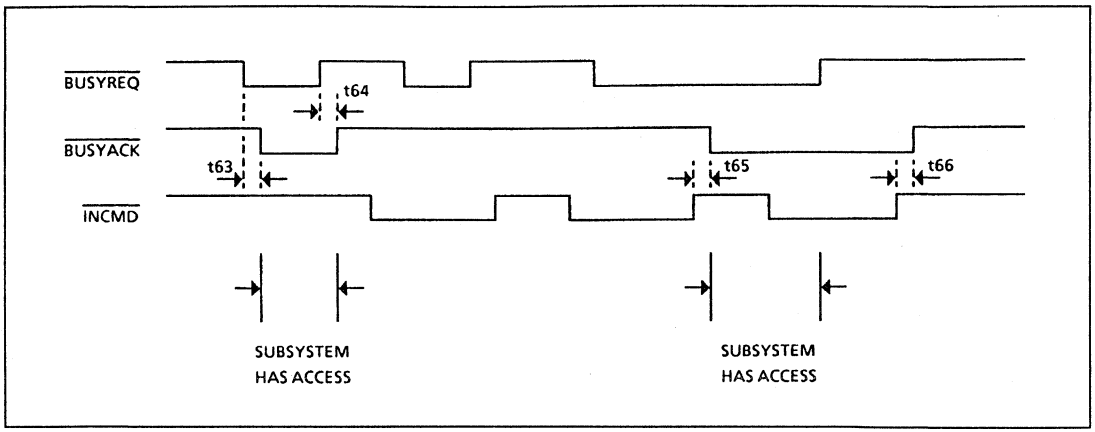


Figure 31: Remote Terminal Busy Handshake

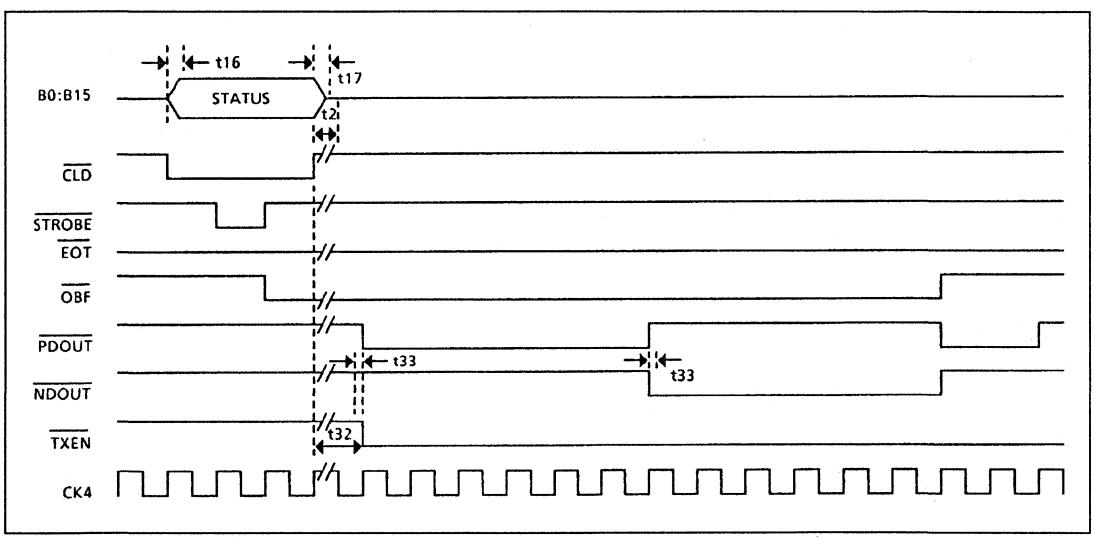
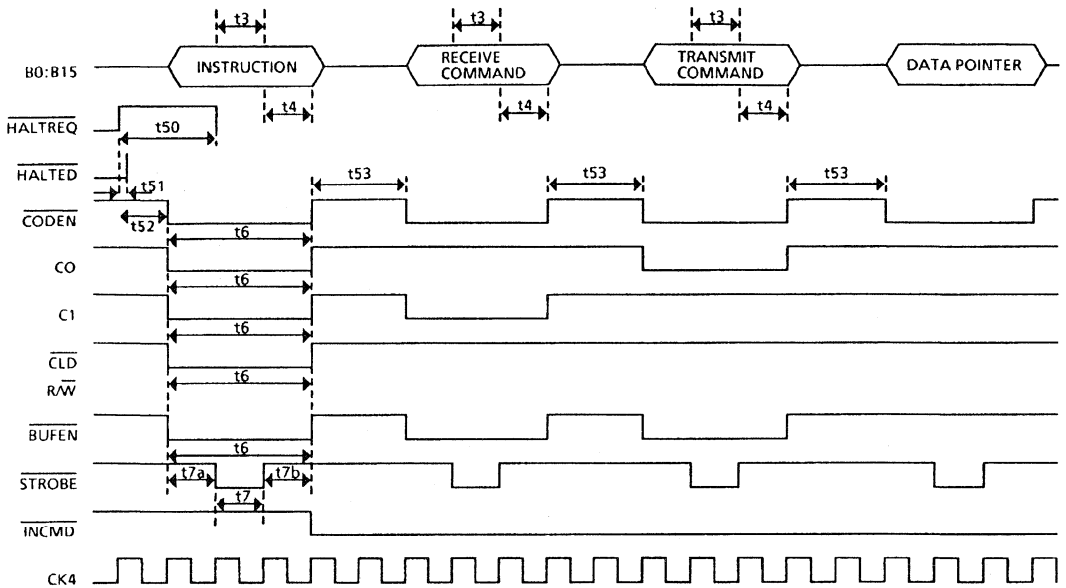
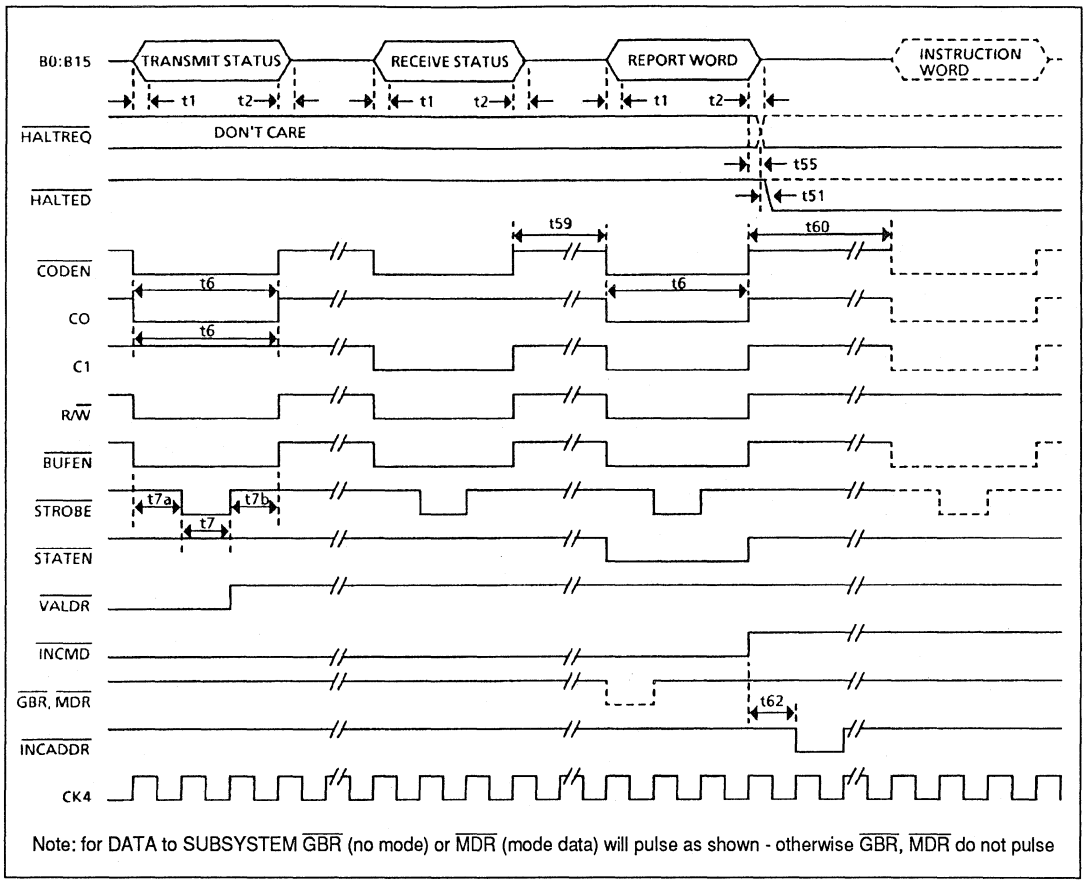


Figure 32: RT Status Load



Note: BUFEN is not active for the DATA POINTER WORD as the 3690/1 does not use the word. It is required by subsystem only.

Figure 33: BC-Message Fetch Sequence



Note: for DATA to SUBSYSTEM $\overline{GBR}$ (no mode) or $\overline{MDR}$ (mode data) will pulse as shown - otherwise $\overline{GBR}$, $\overline{MDR}$ do not pulse

Figure 34: BC-Report Cycle (shown for RT-RT no data to subsystem)

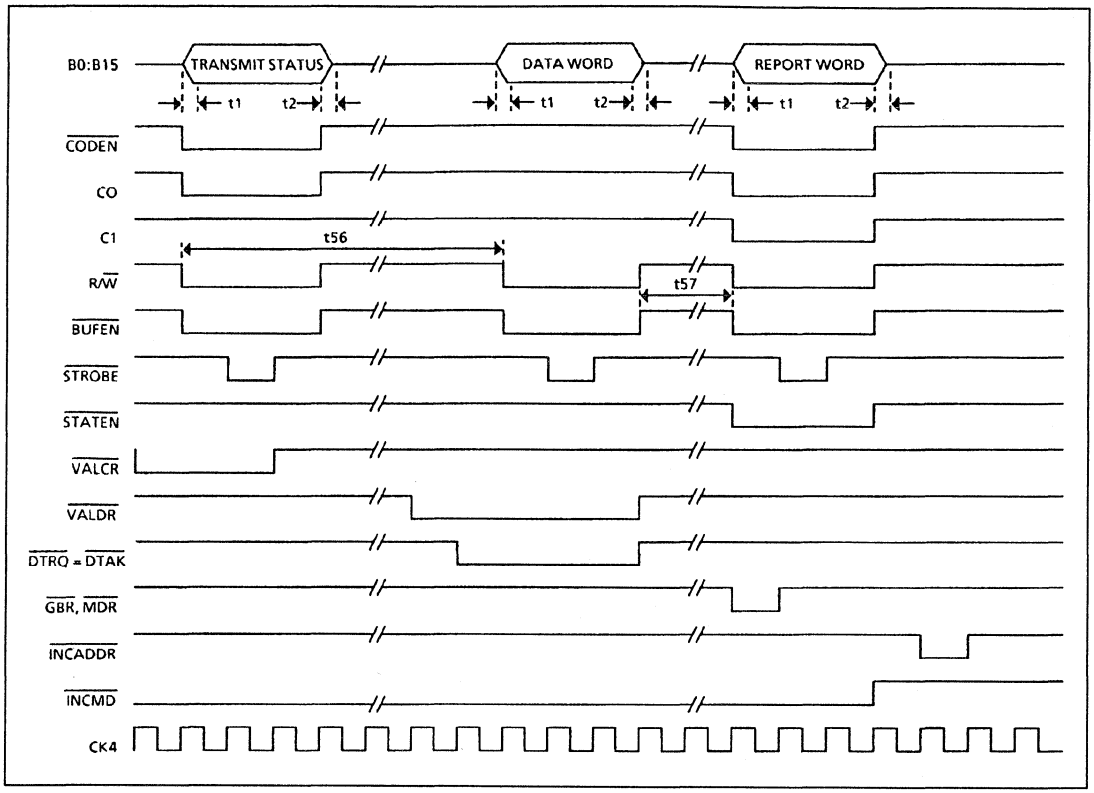


Figure 35: RT-BC Report Cycle

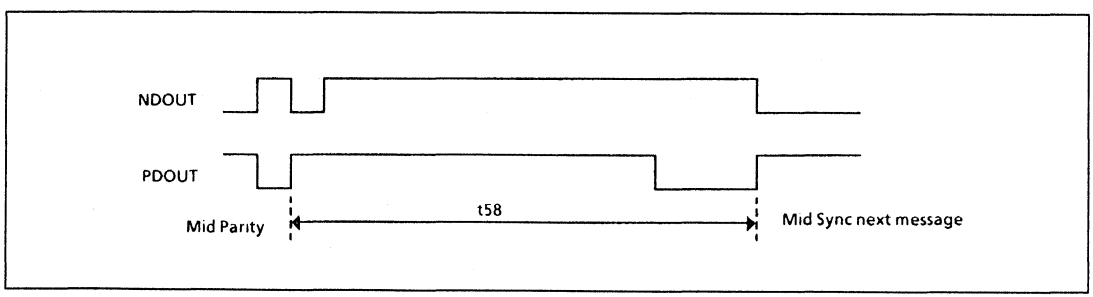


Figure 36: BC Intermessage Gap

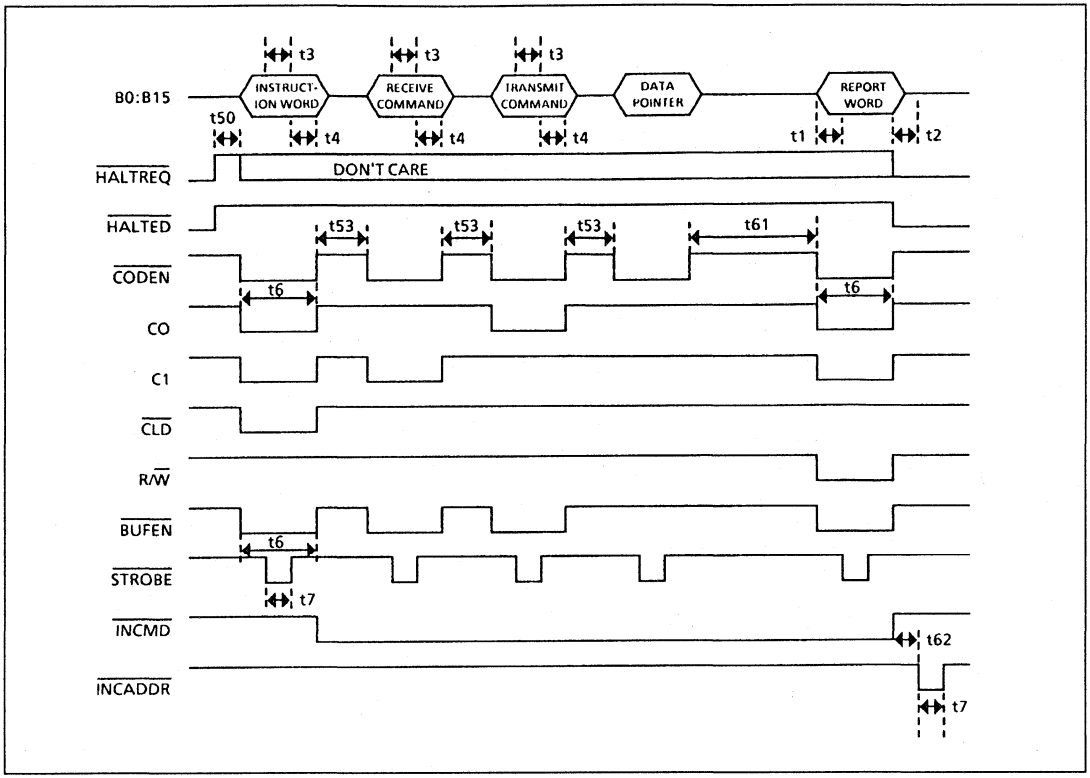


Figure 37: BC - No Operation

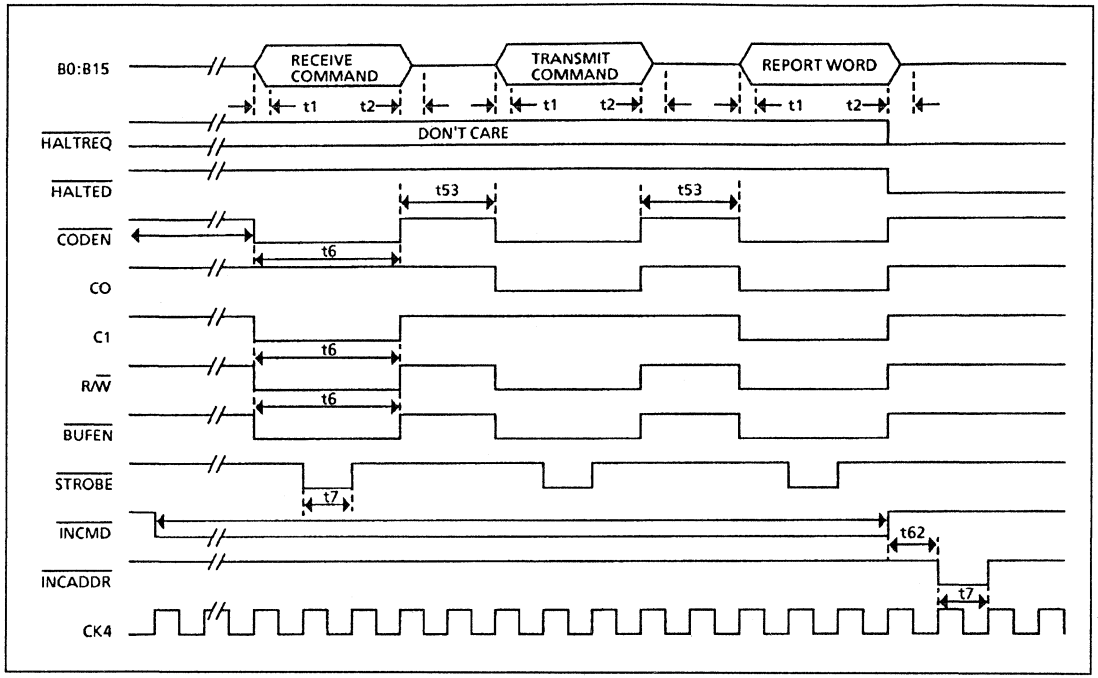


Figure 38: BC - Self Test (Report Sequence)

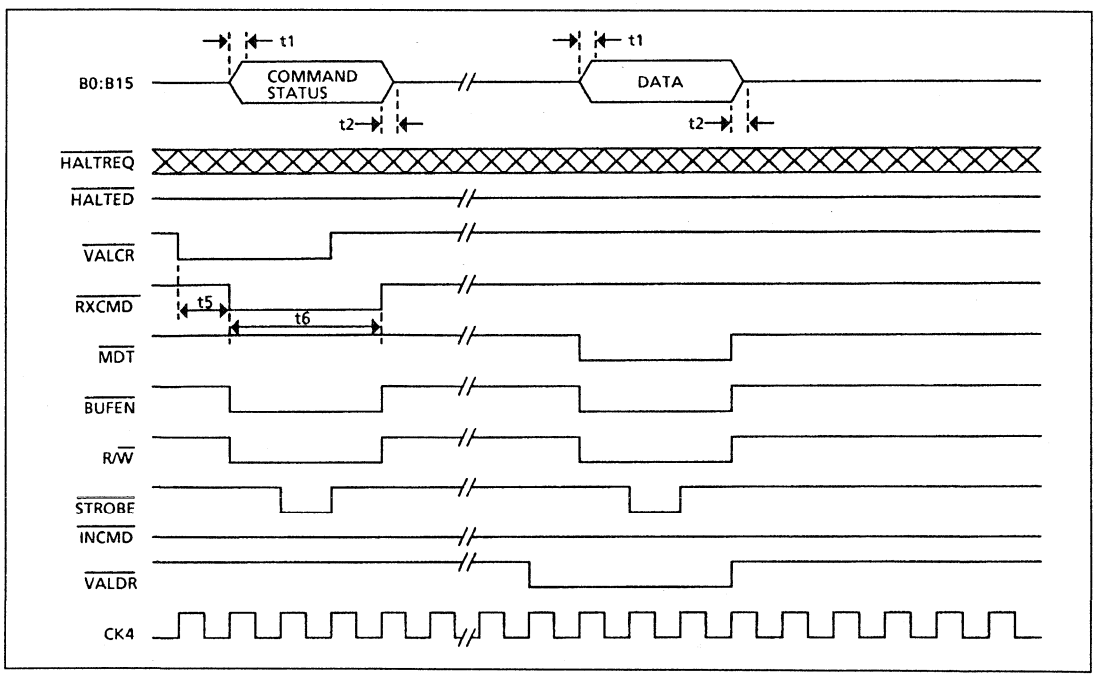
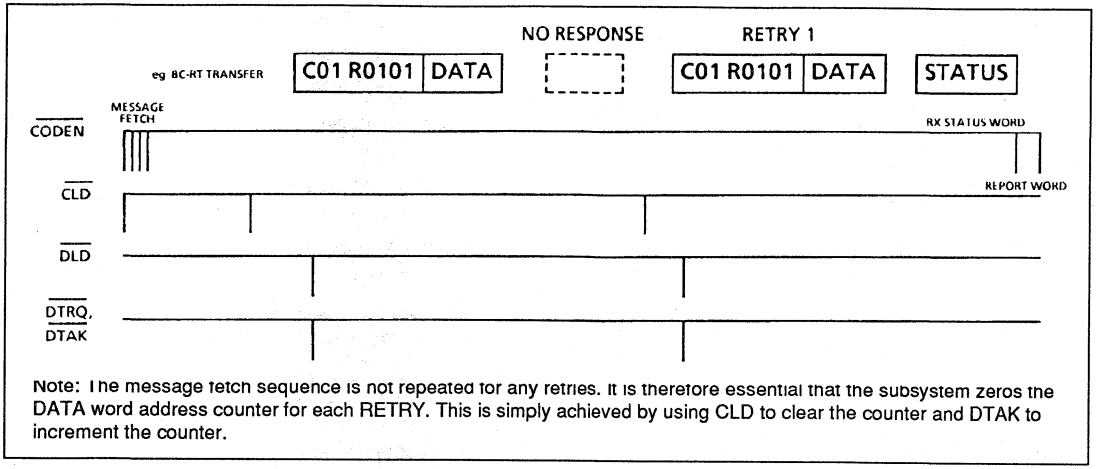


Figure 39: BC - Passive Monitor



Note: The message fetch sequence is not repeated for any retries. It is therefore essential that the subsystem zeros the DATA word address counter for each RETRY. This is simply achieved by using CLD to clear the counter and DTAK to increment the counter.

Figure 40: BC - Retry

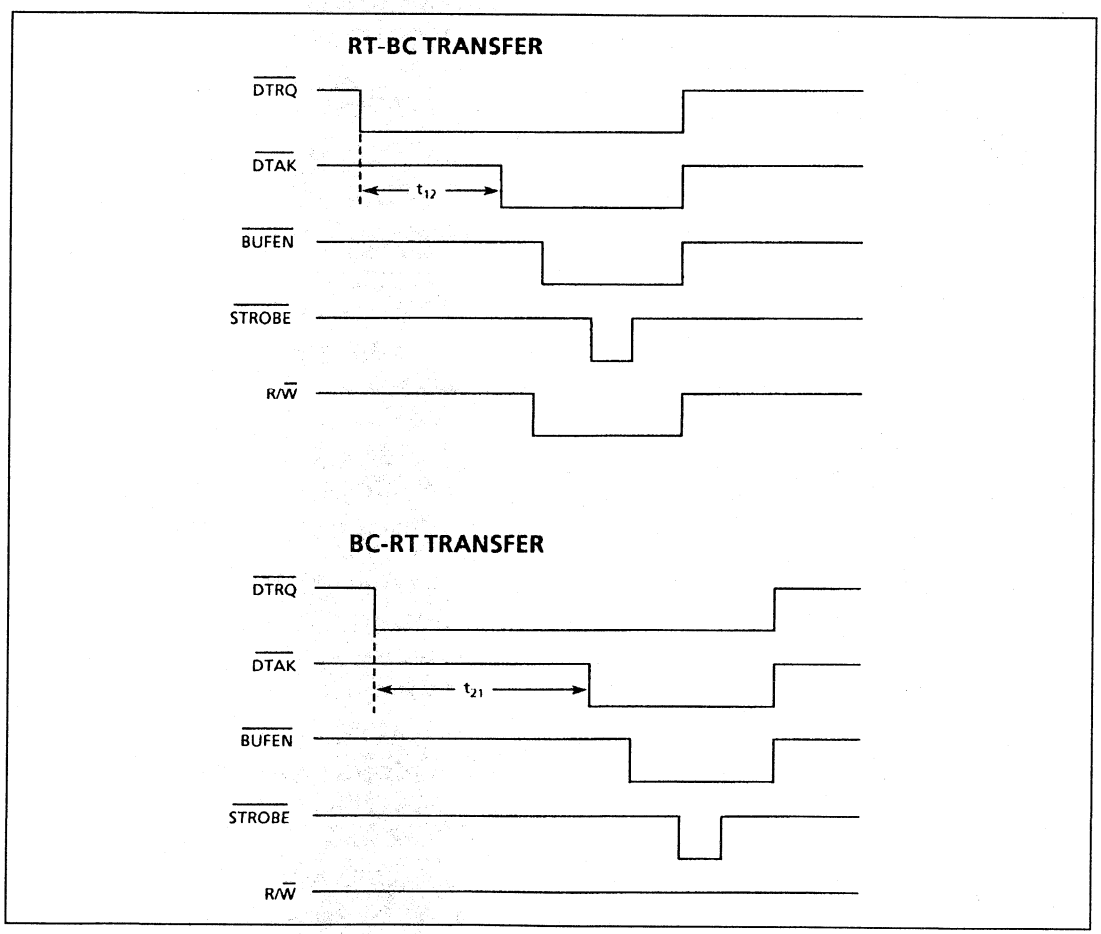


Figure 41: BC - Data Transfer Handshake

OUTLINES

Ref.	Min.	Nom.	Max.
A	-	-	4.37 (0.172)
A_1	1.016 (0.04)	-	1.53 (0.060)
b	0.40 (0.016)	-	0.508 (0.020)
c	0.20 (0.009)	-	0.305 (0.012)
D	-	-	61.57 (2.424)
e	-	2.54 (0.100)	-
e_1	-	15.24 (0.600)	-
H	4.71 (0.185)	-	5.38 (0.212)
M_E	-	-	15.75 (0.620)
W	-	-	1.53 (0.060)
Dimensions in mm (inches)			

GPS XG426

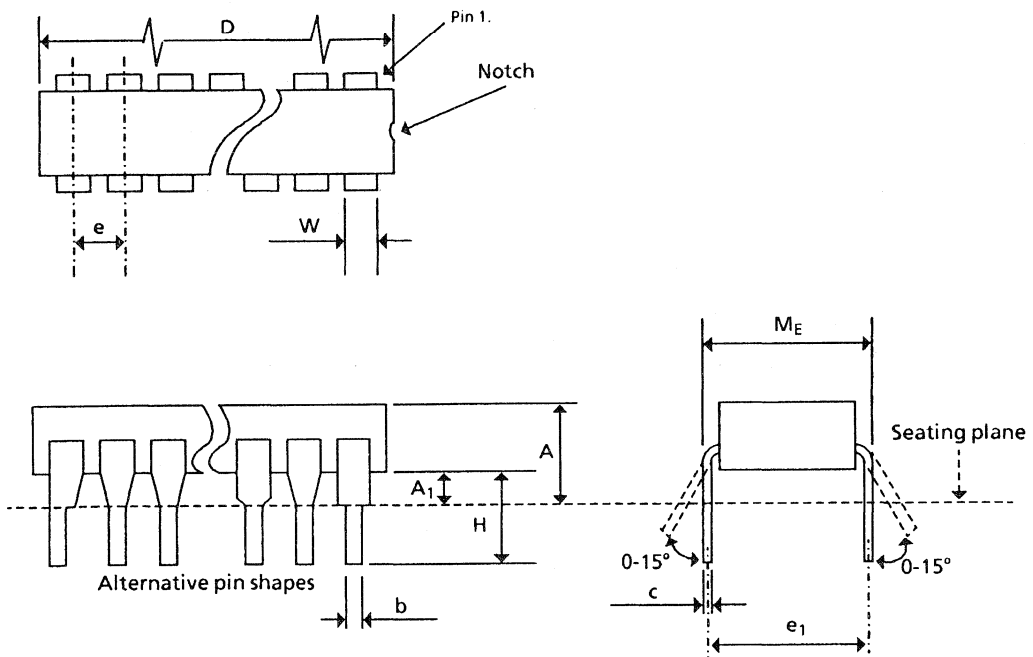
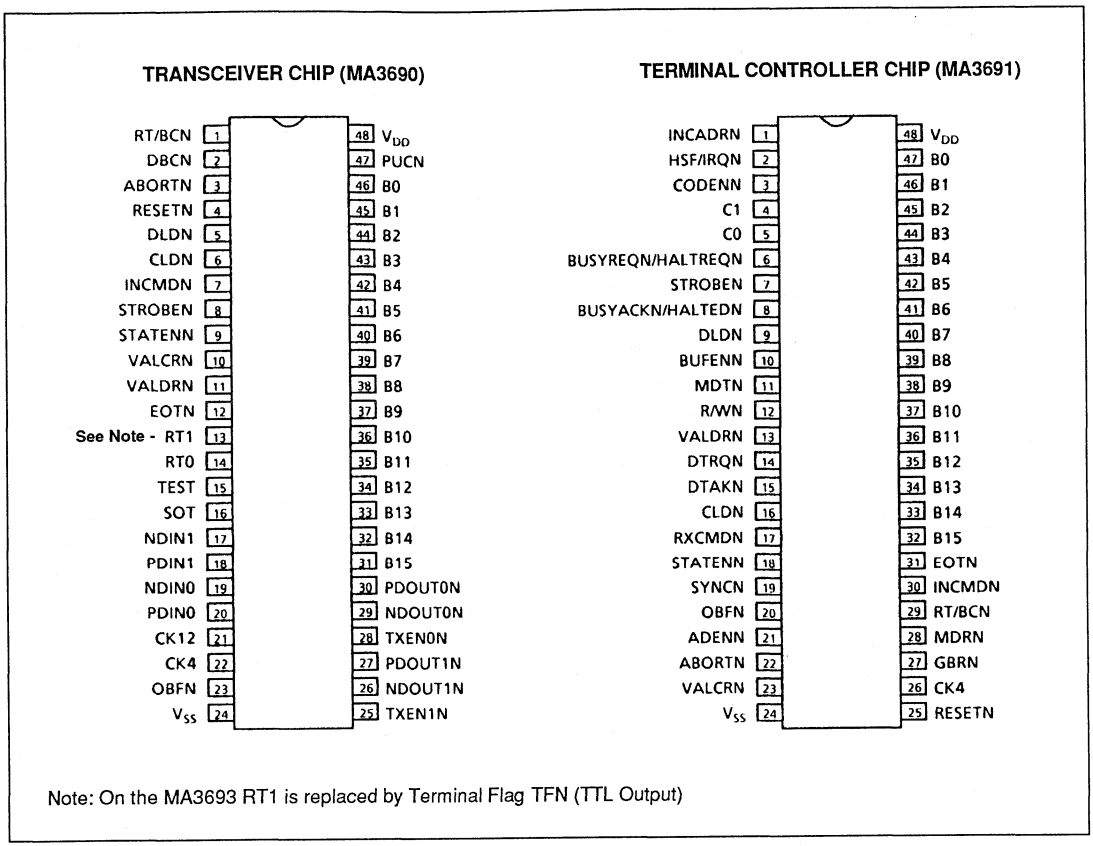


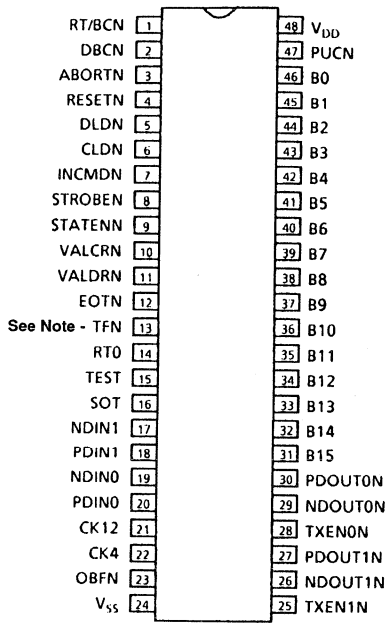
Figure 42a: 48-Lead Ceramic DIL (solder seal) - Package Style C



Note: On the MA3693 RT1 is replaced by Terminal Flag TFN (TTL Output)

Figure 42b: 48-Lead Ceramic DIL (solder seal) - Package Style C

TRANSCEIVER CHIP (MA3693)
(For applications that require access to Terminal Flag)



Note: The MA3693 has Terminal Flag (TFN) latched signal OUTPUT on pin 13 (TTL).
This replaces the RT1 signal INPUT that is used on the MA3690 standard version.

Figure 42c: 48-Lead Ceramic DIL (solder seal) - Package Style C

Ref.	Min.	Nom.	Max.
A	-	-	2.1 (0.083)
A_1	0.96 (0.038)	-	1.07 (0.042)
b	0.41 (0.016)	-	0.51 (0.020)
c	0.178 (0.007)	-	0.254 (0.010)
D1,D2	-	-	23.11 (0.910)
E	15.54 (0.612)	-	15.95 (0.628)
e	-	1.27 (0.050)	-
L	8.89 (0.350)	-	9.27 (0.365)
Z	1.73 (0.068)	-	2.16 (0.085)
Dimensions in mm (inches)			

GPS XG487

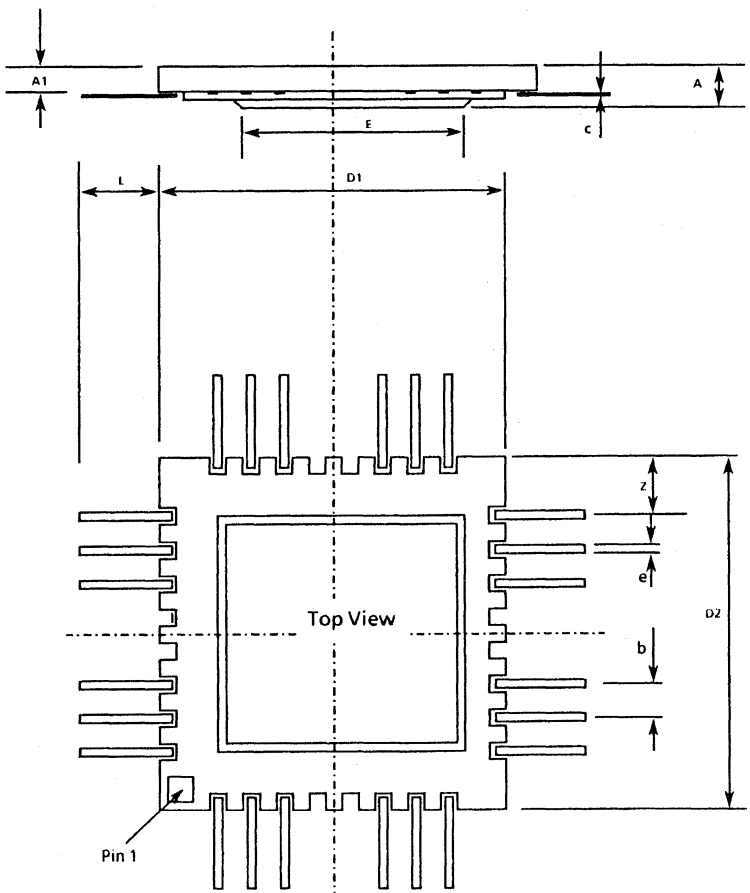


Figure 43a: 64-Lead Topbraze Flatpack (Package Style F)

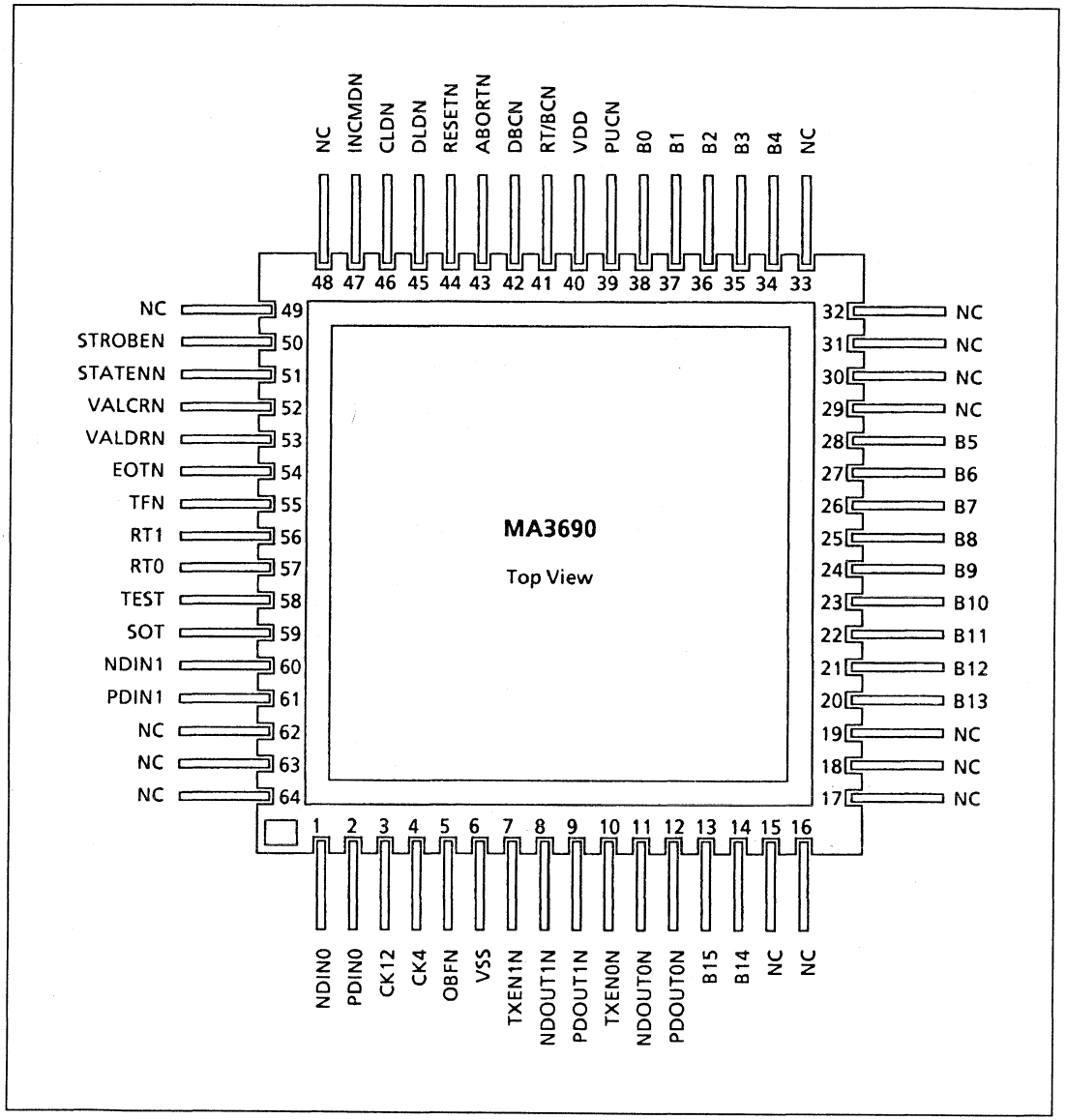


Figure 43b: 64-Lead Topbraze Flatpack (Package Style F)

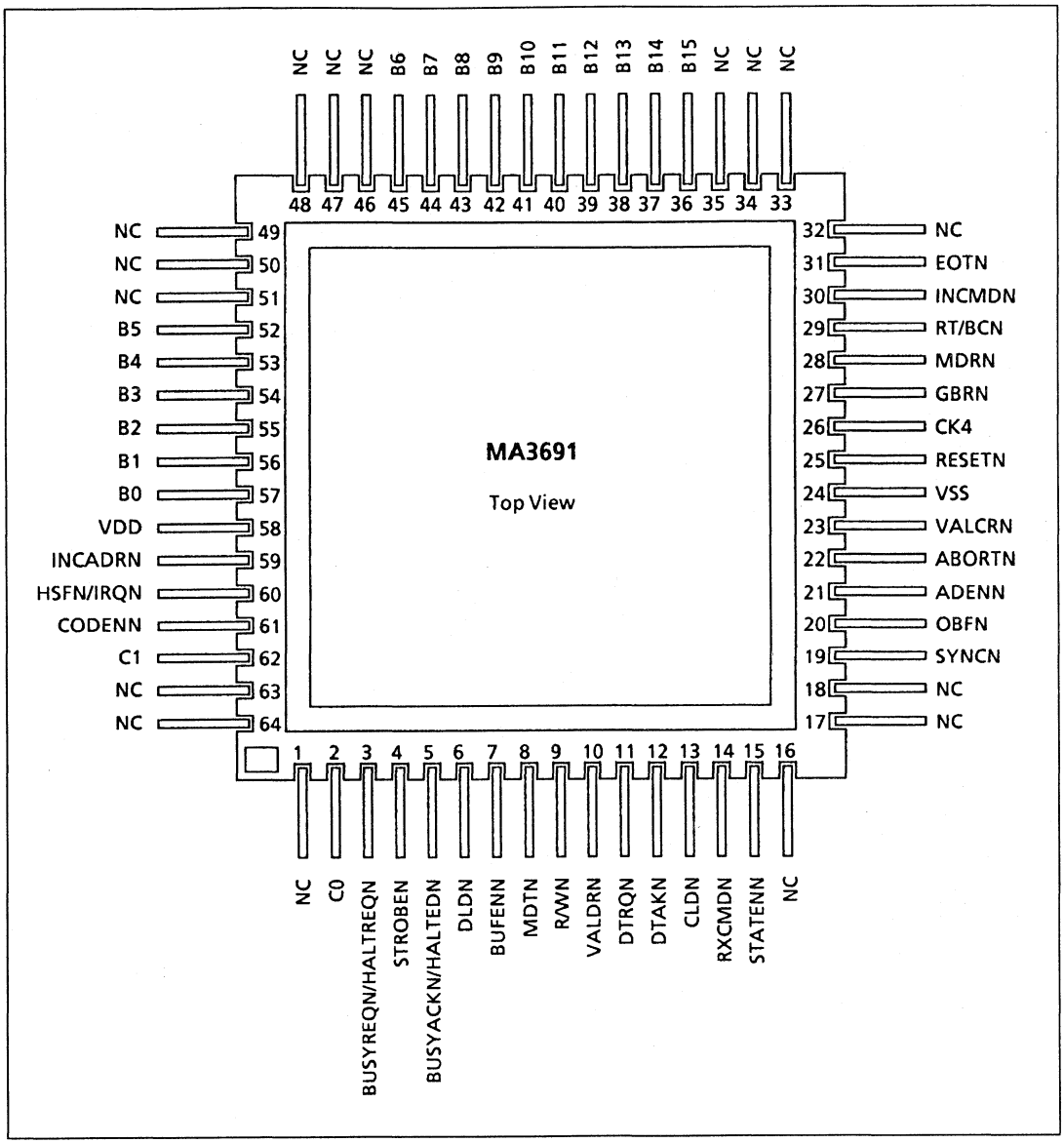


Figure 43c: 64-Lead Topbraze Flatpack (Package Style F)

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

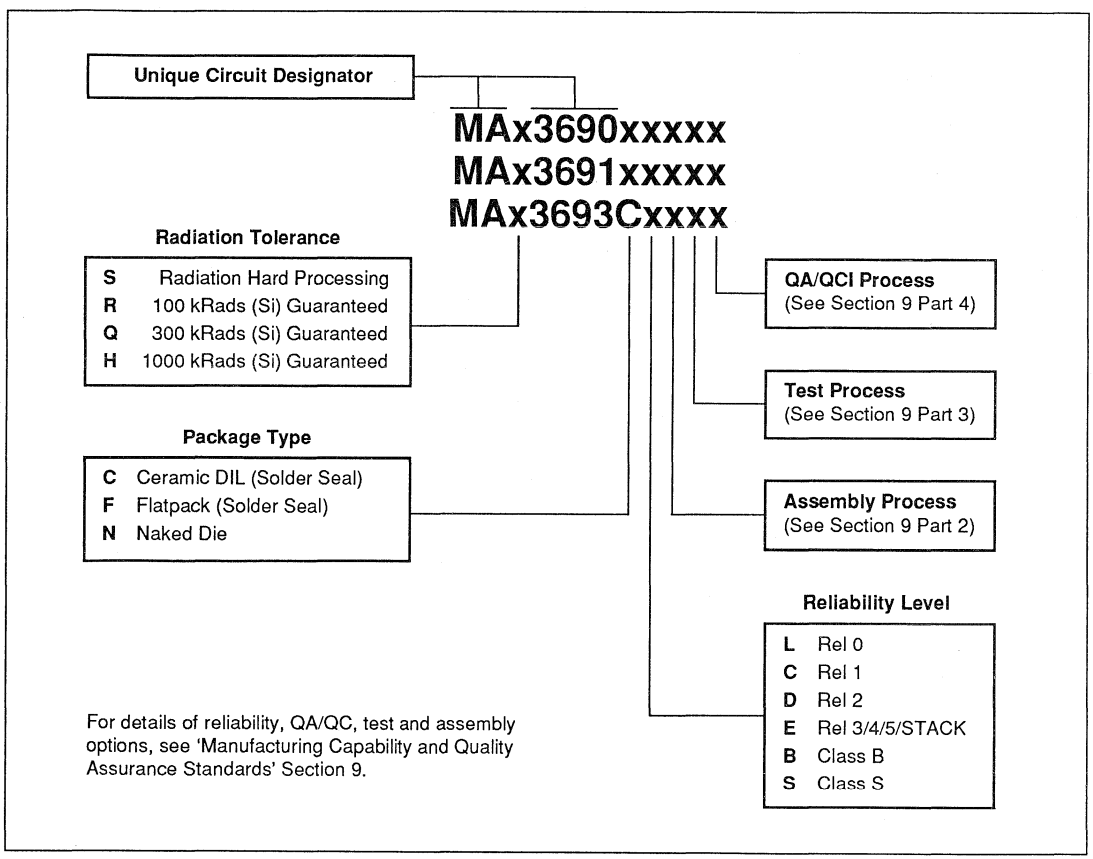
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 44: Radiation Hardness Parameters

ORDERING INFORMATION



MAS15530

MANCHESTER ENCODER/DECODER

The MAS15530 is a high performance CMOS integrated circuit used to implement MIL-STD-1553 and similar Manchester II encoded, time division multiplexed, serial data protocols. The device is divided into two independent sections, encoder and decoder, with a common master reset. The function of the encoder section is to produce the sync pulse and parity bit, and encode the data bits. The decoder section recognises the sync pulse, decodes the data bits and checks for parity.

The MAS15530 is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over the full temperature and supply voltage ranges. The device interfaces with CMOS, TTL and N-channel support circuitry and operates from a standard 5 volt supply. Applications of Manchester Encoding include serial data links, security systems, environmental controls, data communications.

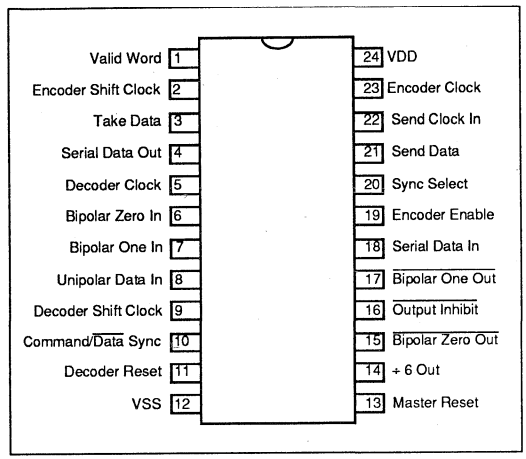


Figure 1: Pin Assignment

FEATURES

- MIL-STD-1553 Compatible
- Sync Identification and Lock-in
- Clock Recovery
- Manchester II Encode/Decode
- Separate Encoder and Decoder Sections
- Low Operating Power
- Direct Replacement for Harris HD15530
- Available to Military and Commercial Grades

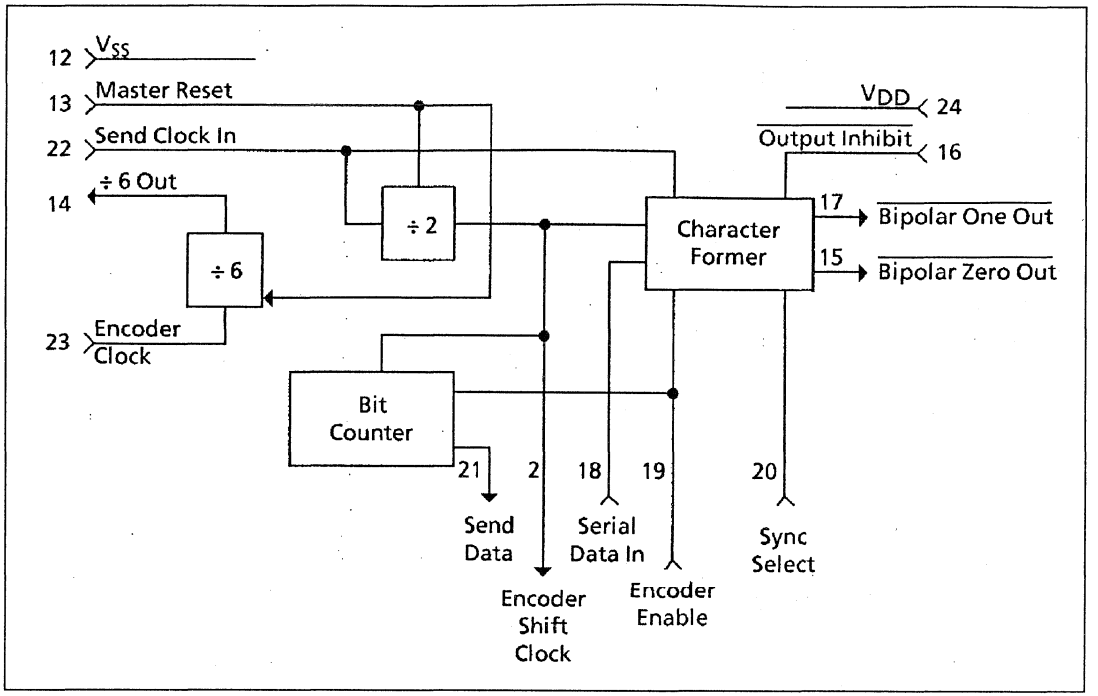


Figure 2: Encoder Block Diagram

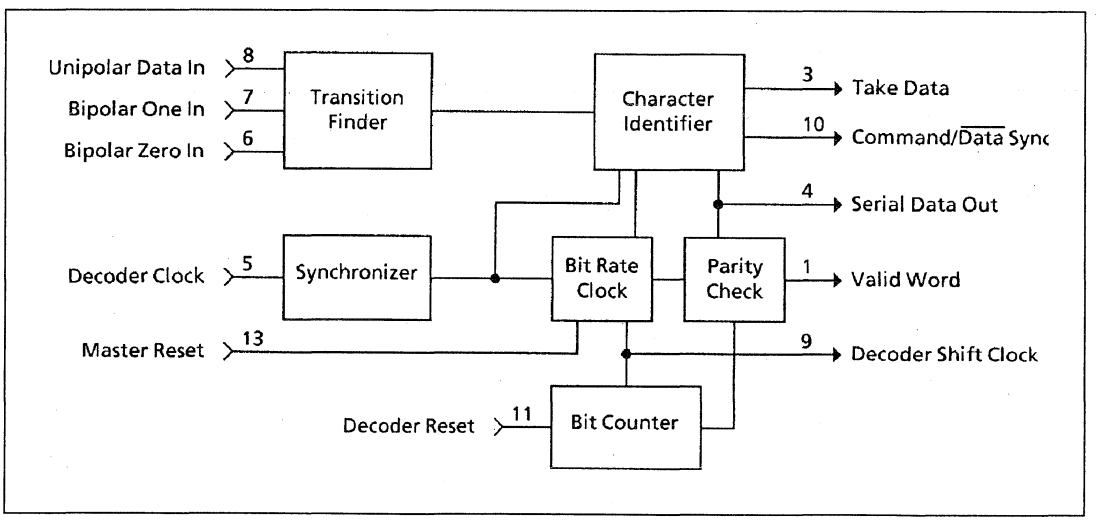


Figure 3: Decoder Block Diagram

PIN DESIGNATIONS

Pin	Input	Output	Enc	Dec	Function	Comment
1		√		√	Valid word	A 'high' signals the receipt of a valid word
2		√	√		Encoder Shift Clock	Shifts data into the encoder on a'low' to 'high' transition
3		√		√	Take Data	'High' during data reception after the sync pulse is identified
4		√		√	Serial Data Out	NRZ output of received data
5	√			√	Decoder Clock	Clock for the transition finder and synchronizer which generates the clock for the rest of the decoder
6	√			√	Bipolar Zero In	Should be 'high' when the bus is in a negative state. Must be tied 'high' when the unipolar input is used
7	√			√	Bipolar One In	Should be 'high' when the bus is in a positive state. Must be tied 'low' when the unipolar input is used
8	√			√	Unipolar Data In	Input for unipolar data to the transition finder. Must be tied 'low' when not in use
9		√		√	Decoder Shift Clock	Provides the DECODER CLOCK divided by 12, synchronized by the recovered serial data
10		√		√	Command/$\overline{\text{Data}}$ Sync	This output indicates the type of sychronizing character received as follows: If a data synchronizing character was received, this pin is low while the data is decoded. If a command synchronizing character was received, this pin is high during data decoding
11	√			√	Decoder Reset	A 'high' during a DECODER SHIFT CLOCK rising edge resets the bit counter
12	–	–	√	√	V_{SS}	Ground
13	√		√	√	Master Reset	A 'high' clears the counter in both directions
14		√	√		÷ 6 Out	Provides the ENCODER CLOCK divided by 6
15		√	√		$\overline{\text{Bipolar Zero Out}}$	Provides an active 'low' output to the zero or negative sense of a bipolar line driver
16	√		√		$\overline{\text{Output Inhibit}}$	A 'low' inhibits the $\overline{\text{BIPOLAR ZERO OUT}}$ and $\overline{\text{BIPOLAR ONE OUT}}$ by forcing them to inactive, 'high', states
17		√	√		$\overline{\text{Bipolar One Out}}$	Provides an active 'low' output to the one or positive sense of a bipolar line driver
18	√		√		Serial Data In	Receives serial data at the rate of the ENCODER SHIFT CLOCK
19	√		√		Encoder Enable	A 'high' starts the encode cycle provided that the previous cycle is complete
20	√		√		Sync Select	A 'high' selects the command sync and a 'low' selects the data sync
21		√	√		Send Data	Provides an active 'high' to enable the external serial data source
22	√		√		Send Clock In	Clock input at 2 times the data rate
23	√		√		Encoder Clock	Input to the divide by 6 circuit
24	–	–	√	√	V_{DD}	Positive supply

Figure 4: Pin Designations

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	3	7	V
V_I	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
-	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Figure 5: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Subgroup	Definition
1	Static characteristics specified in Figure 7 at +25°C
2	Static characteristics specified in Figure 7 at +125°C
3	Static characteristics specified in Figure 7 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Figures 8 and 9 at +25°C
10	Switching characteristics specified in Figures 8 and 9 at +125°C
11	Switching characteristics specified in Figures 8 and 9 at -55°C

Figure 6: Definition of Subgroups

DC CHARACTERISTICS

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic "1" Input Voltage	70%V_{DD}	-	-	V	
V_{IL}	Logic "0" Input Voltage	-	-	30%V_{DD}	V	
V_{IHC}	Logic "1" Input Voltage (clock)	V_{DD}-0.5	-	-	V	
V_{ILC}	Logic "0" Input Voltage (clock)	-	-	V_{SS}+0.5	V	
I_{IL}	Input Leakage Current	-10	-	+10	µA	$0V \le V_{IN} \le V_{DD}$
V_{OH}	Logic "1" Output Voltage	2.4	-	-	V	I_{OH}=-3mA
V_{OL}	Logic "0" Output Voltage	-	-	0.4	V	I_{OL}=1.8mA
I_{DDSB}	Standby Supply Current	-	0.5	2.0	mA	Outputs Open $V_{IN}=V_{DD}$=5.5V
I_{DDOP}	Operating Supply Current	-	8.0	10.0	mA	V_{DD}=5.5V, f=1MHz
C_{IN}	Input Capacitance	-	5.0	7.0	pF	
C_{OUT}	Output Capacitance	-	8.0	10.0	pF	

Mil-Std-883, method 5005, subgroups 1, 2, 3

1. V_{DD} = 5V ±10%, over full operating temperature range and 300K Rad(Si). Values for other radiation levels available on request.

Figure 7: DC Characteristics

AC CHARACTERISTICS

Symbol	Parameter	Min.	Max.	Units
f_{EC}	Encoder clock frequency	-	13	MHz
f_{ESC}	Send clock frequency	-	2.2	MHz
t_{ECR}	Encoder clock rise time	-	8	ns
t_{ECF}	Encoder clock fall time	-	8	ns
f_{ED}	Data rate	-	1.1	MHz
t_{MR}	Master reset pulse width	150	-	ns
t_{E1}	Shift clock delay	-	125	ns
t_{E2}	Serial data setup time	75	-	ns
t_{E3}	Serial data hold time	75	-	ns
t_{E4}	Enable setup time	90	-	ns
t_{E5}	Enable pulse width	80	-	ns
t_{E6}	Sync setup time	55	-	ns
t_{E7}	Sync pulse width	150	-	ns
t_{E8}	Send data delay	-	50	ns
t_{E9}	Bipolar output delay	-	130	ns

1. V_{DD} = 5V ±10%, over full operating temperature range. 2.C_L = 50pF

Figure 8: Encoder Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{DC}	Decoder clock frequency	-	-	15	MHz
f_{DCR}	Decoder clock rise time	-	-	8	ns
t_{DCF}	Decoder clock fall time	-	-	8	ns
f_{DD}	Data rate	-	-	1.1	MHz
t_{DR}	Decoder reset pulse width	150	-	-	ns
t_{DRS}	Decoder reset setup time	75	-	-	ns
t_{MR}	Master reset pulse width	150	-	-	ns
t_{D1}	Bipolar data pulse width	t_{DC} + 10	-	-	ns
t_{D2}	Sync transition span	-	$18t_{DC}$	-	ns
t_{D3}	One-Zero overlap	-	-	t_{DC} -10	ns
t_{D4}	Short data transition span	-	$6t_{DC}$	-	ns
t_{D5}	Long data transition span	-	$12t_{DC}$	-	ns
t_{D6}	Sync delay (on)	-	-	110	ns
t_{D7}	Take data delay (on)	-	-	110	ns
t_{D8}	Serial data out delay	-	-	80	ns
t_{D9}	Sync delay (off)	-	-	110	ns
t_{D10}	Take data delay (off)	-	-	110	ns
t_{D11}	Valid word delay	-	-	110	ns

Mil-Std-883, method 5005, subgroups 9, 10, 11
1. V_{DD} = 5V ±10%, over full operating temperature range. 2.C_L = 50pF
3. t_{DC} = Decoder clock period = $1/f_{DC}$. 4. Total Dose = 300K Rad(Si). Values for other radiation levels available on request.

Figure 9: Decoder Electrical Characteristics

ENCODER OPERATION

The encoder requires a single clock with a frequency of twice the desired rate applied at the SEND CLOCK input. An auxiliary divide by six counter is provided on chip which can be utilised to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK (1). This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word (2). When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods (3). During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK (3) - (4). After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word (5). At any time a low in $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.

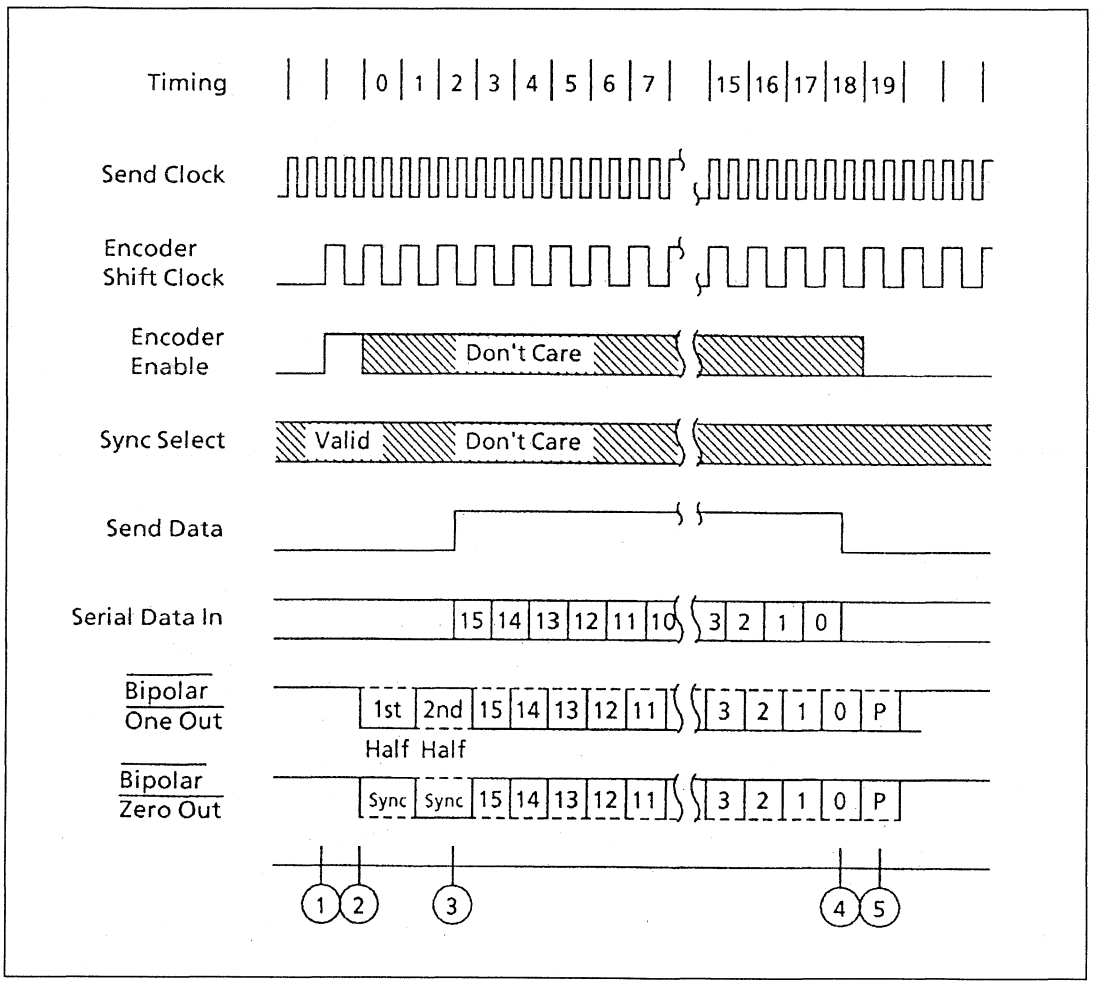


Figure 10: Encoder Operation

DECODER OPERATION

The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in MIL-STD-1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder).

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized (1), the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high (2) and remain high for sixteen DECODER SHIFT CLOCK periods (3), otherwise it will remain low. The TAKE DATA output will go high and remain high (2) - (3) while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock (2) - (3).

After all sixteen decoded bits have been transmitted (3) the data is checked for odd parity. A high on VALID WORD output (4) indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence, a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

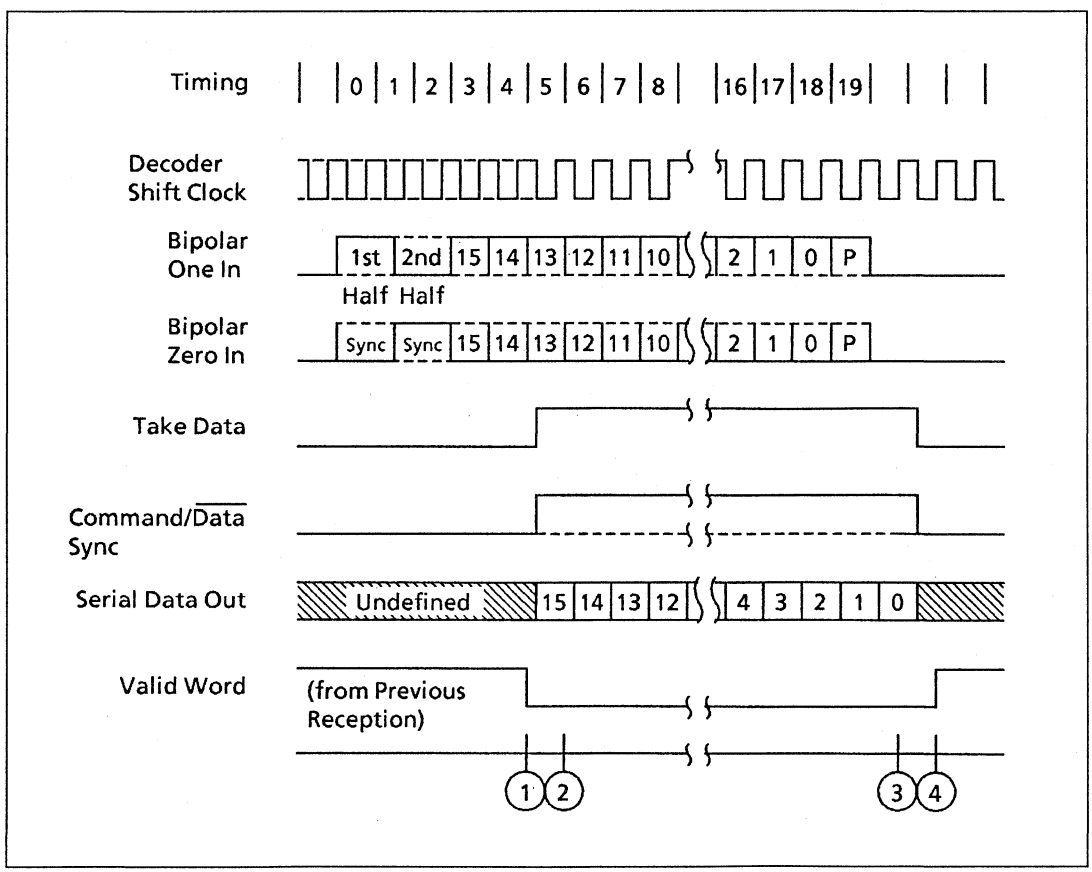


Figure 11: Decoder Operation

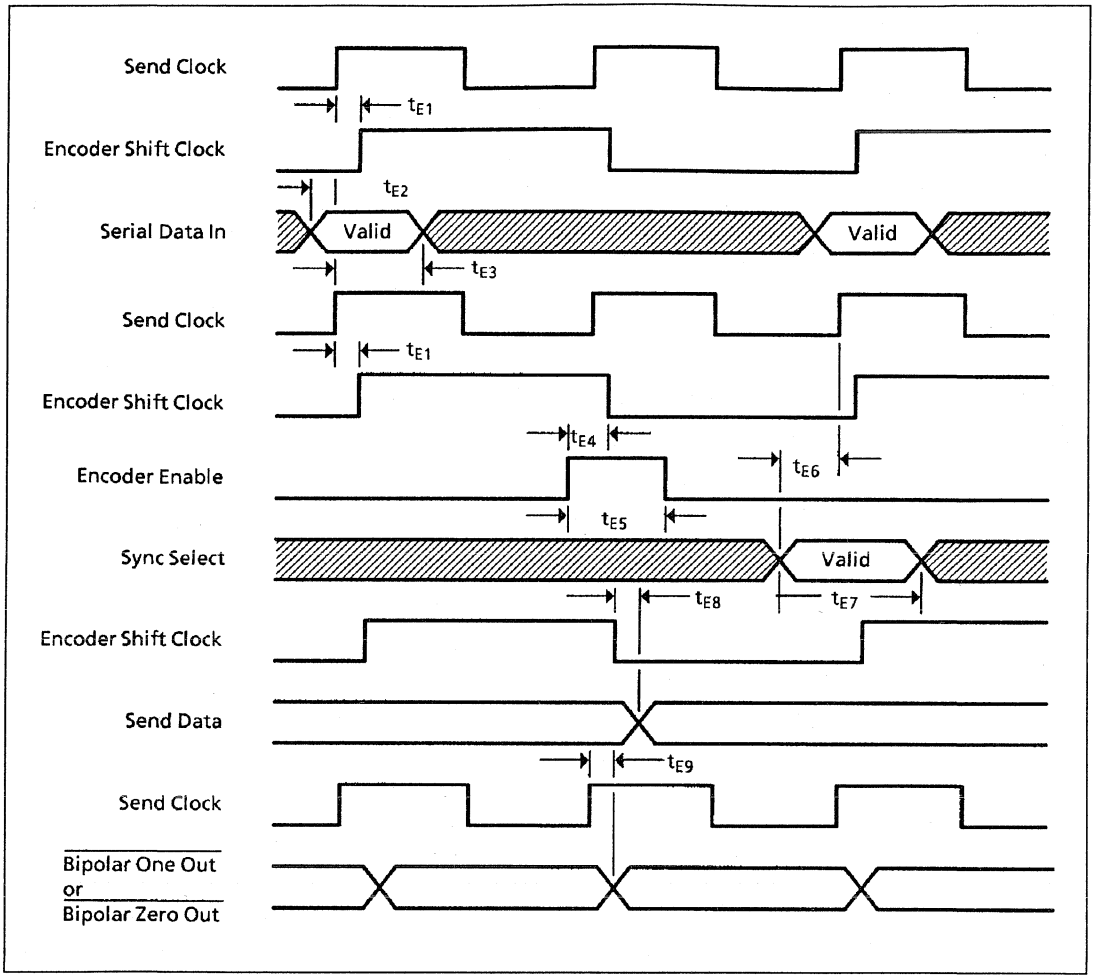
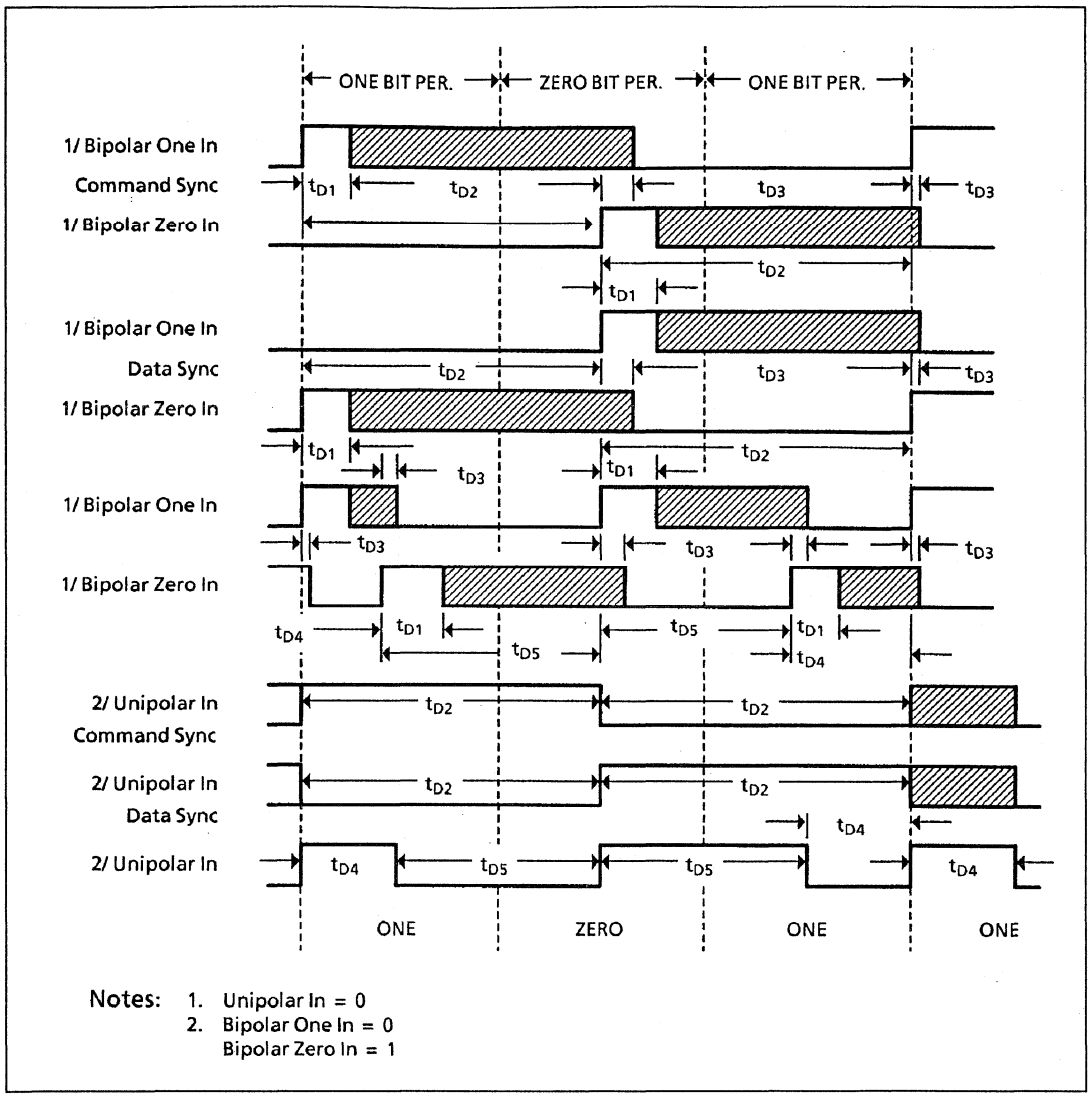


Figure 12: Encoder Timing Diagram



Notes:
1. Unipolar In = 0
2. Bipolar One In = 0
   Bipolar Zero In = 1

Figure 13: Decoder Timing Diagram

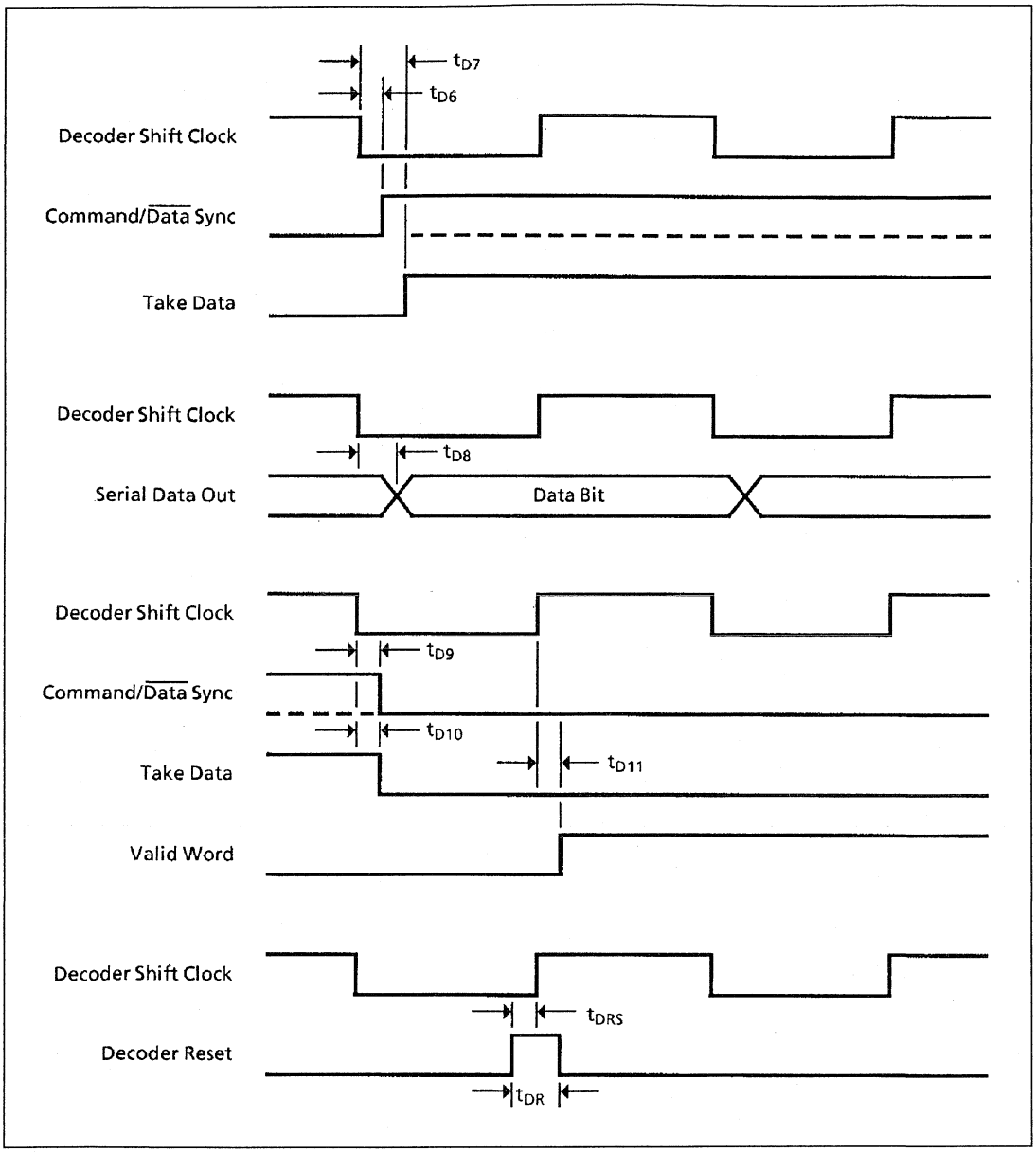


Figure 14: Decoder Timing Details

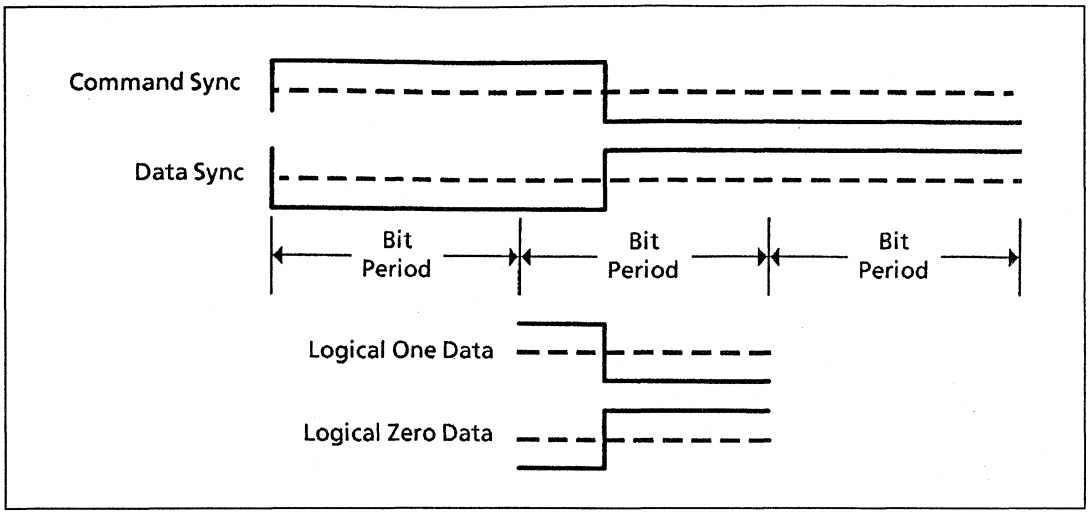


Figure 15: Character Formats

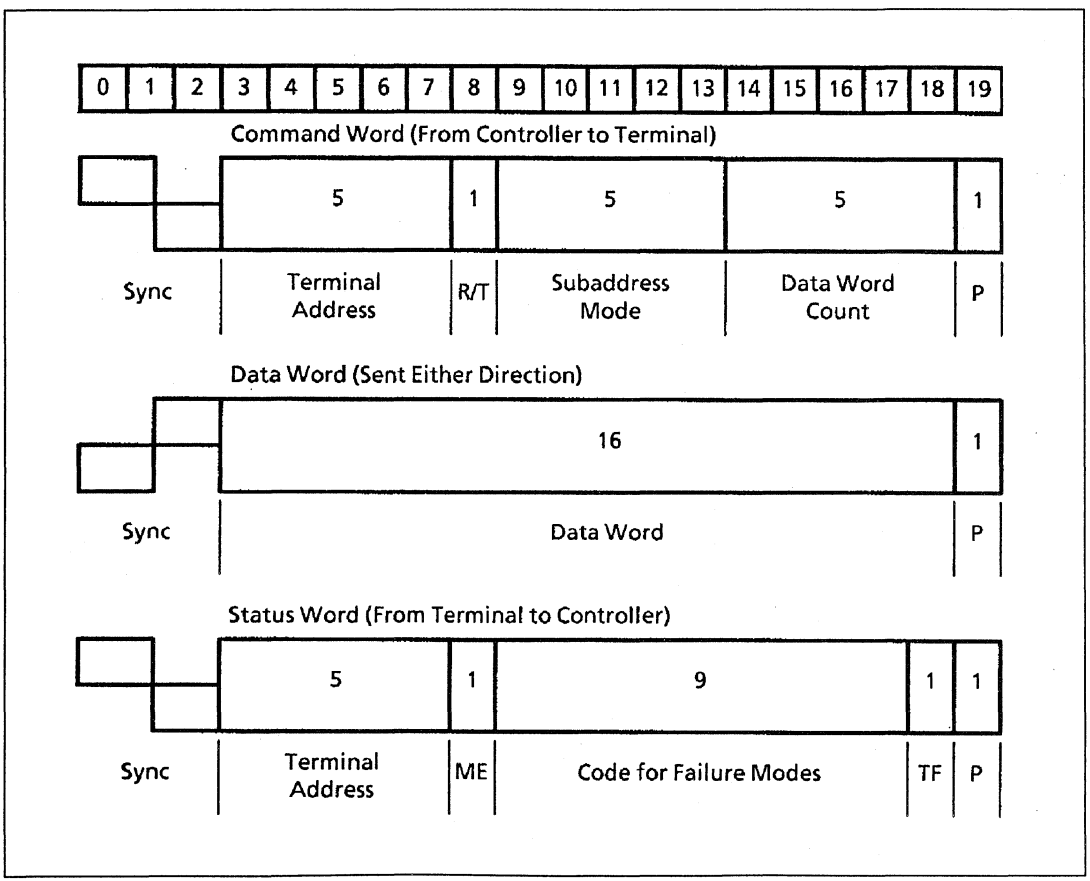


Figure 16: Word Formats

OUTLINES AND PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.60	-	-	0.220
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	30.79	-	-	1.212
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	?	-	-	?
W	-	-	1.53	-	-	0.060

XG403

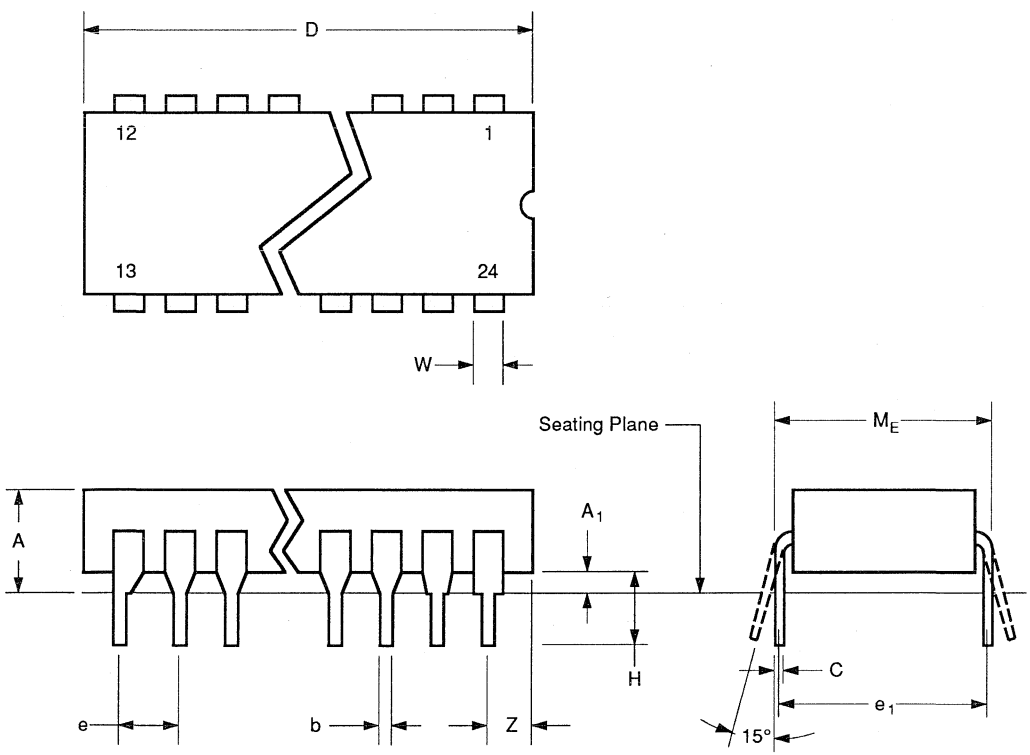


Figure 17: 24-Lead Ceramic DIL (Solder Seal) - Package Style C

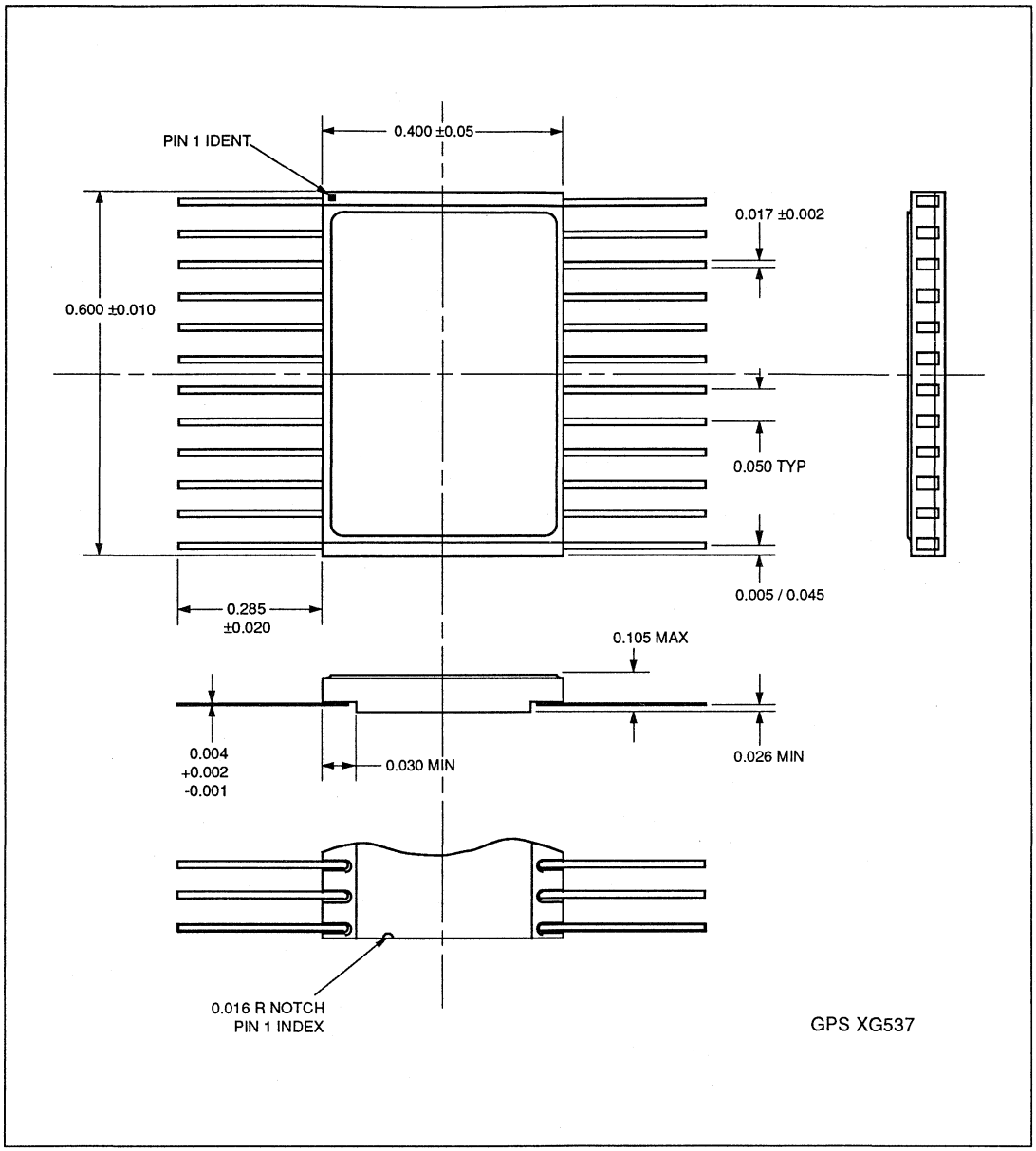


Figure 18: 24-Lead Ceramic Flatpack (Solder Seal) - Package Style F

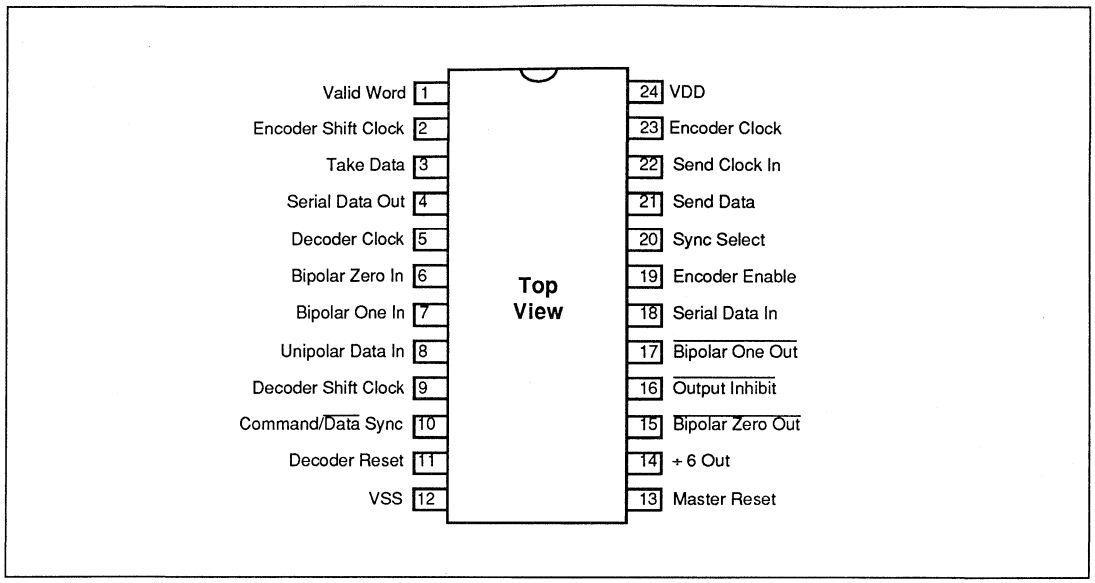


Figure 19: Pin Out - Plug-In

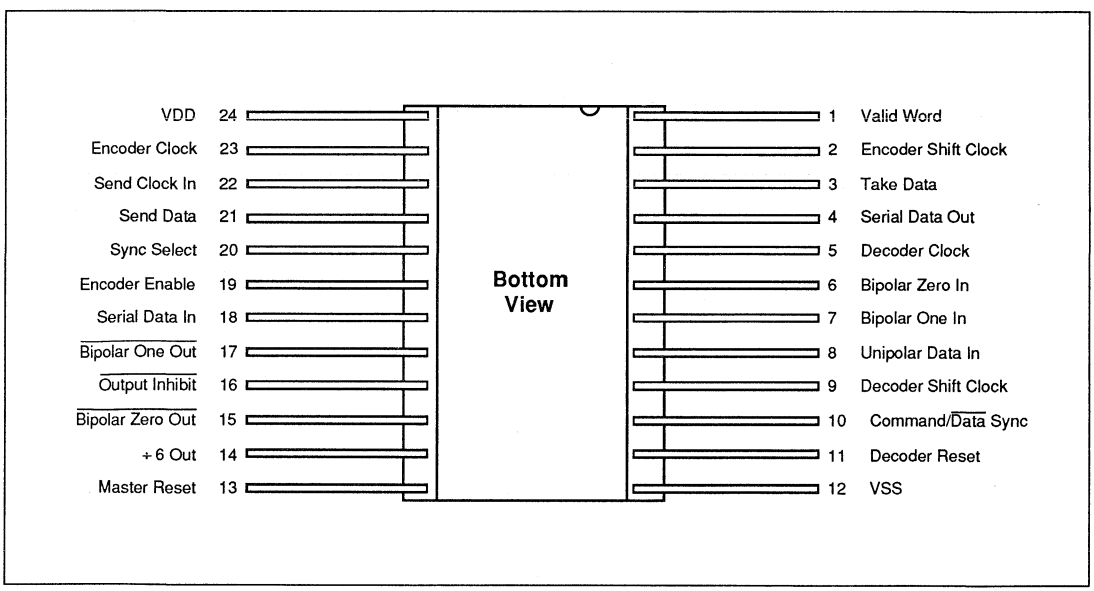


Figure 20: Pin Out - Flatpack

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 ionizing radiation (total dose) test method 1019.

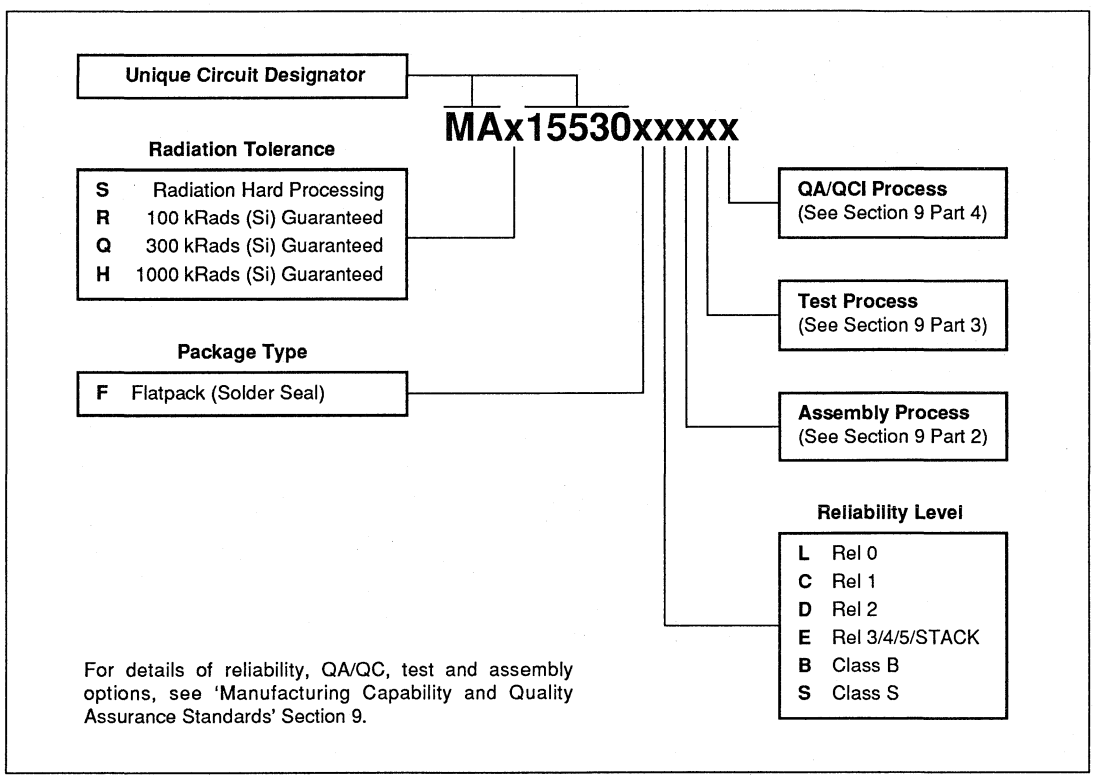
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 21: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3590-3.2

MA1916

RADIATION HARD REED-SOLOMON & CONVOLUTION ENCODER

The purpose of the MA1916 is to encode serial data to allow error correction when the data is transmitted over a noisy communication link. As the name suggests, the unit contains two encoding elements. The Reed-Solomon encoder appends a checksum to a block of data, guarding against burst errors in a message. The convolution encoder continuously creates two code bits for each data bit it receives, increasing the noise immunity by doubling the band width of the message. The unit also contains a test pattern generator which can be connected to check the functionality of the RS encoder and to provide a message timing signal (SMC_OUT).

Protection against a long error-burst can be increased by interleaving a number of message packets passing through the RS encoder. The MA1916 provides pin selectable interleave depths of 1, 4 or 5. Interleave depths of greater than 5 do not significantly improve performance.

The MA1916 is designed to conform to the CCSDS standard for telemetry 101.0.B.2. It is manufactured in a radiation hard low power CMOS technology. This makes it ideal for use in satellite communications systems. The encoder reduces the risk of data corruption and allows the designer to minimize the transmitter power needed to establish an effective communications link.

FEATURES

- Radiation Hard CMOS-SOS Technology
- Low Power Consumption
- Latch-up Free
- High SEU Immunity
- CCSDS Standard RS (255, 223)
- Selectable Interleave Depths of 1, 4 or 5
- 5MBit/sec Input Data Rate

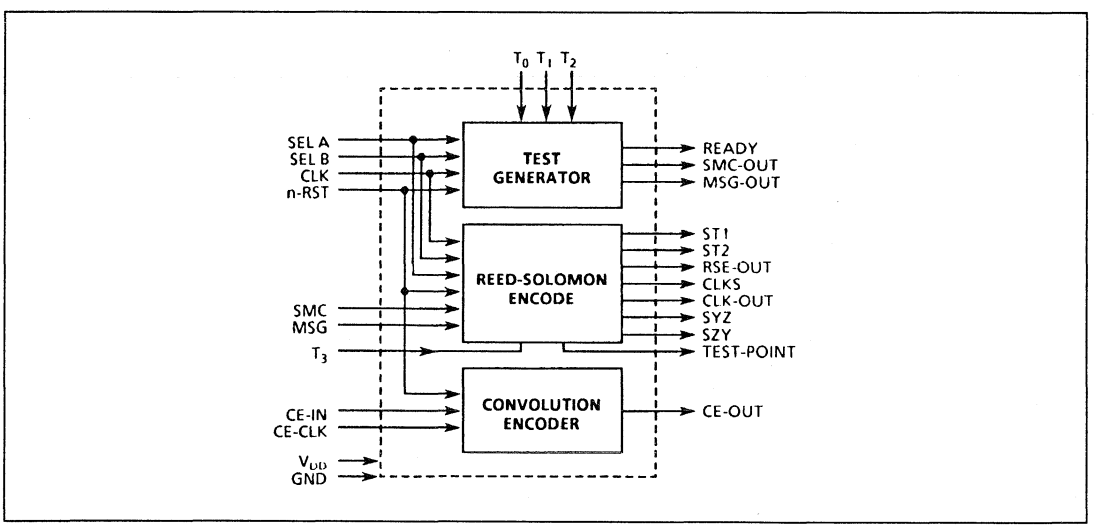


Figure 1: Block Diagram

OPERATION

REED-SOLOMON ENCODER

The function of the Reed-Solomon (RS) encoder is to take a block of 223 bytes of serial data and to append a checksum of 32 bytes. The purpose of the checksum is to allow error correction within the data block. One important feature of the Reed-Solomon algorithm is that it allows correction of a burst error which corrupts upto 16 consecutive bytes. If a number of messages are interleaved this length can be increased. The MA1916 provides pin selectable interleave depths of 1, 4 or 5 blocks (see Table 1), each of 223 bytes. An interleave depth of 5 is the maximum recommended by the CCSDS standard. This will allow correction of up to 80 sequencial bytes in a data packet.

The RS encoder operates from a clock input CLK which must be driven at twice the input data rate. Internally CLK is divided to give a clock CLKS which runs at half the frequency. This signal is available as an output and is used to time data into the RS encoder.

A high input on SMC is used to tell the RS encoder that data to be encoded is present on the MSG pin (see Figure 2). While SMC is high the data on MSG is buffered and appears on RSE_OUT as well as being clocked into the encoder. As soon as SMC goes low the checksum is clocked out of the encoder onto RSE_OUT.

While SMC is high the RSE_OUT signal follows the input MSG. When SMC is low RSE_OUT is produced from the exclusive-OR of MSG and the checksum signal. For this reason MSG must be held low while the encoder outputs the checksum.

A gap can be left between successive data packets by holding SMC and MSG low after the checksum has been sent. Alternatively, synchronisation code can be inserted before a data block by holding SMC low and placing the code on MSG. As soon as SMC goes high any further data on MSG is assumed to form part of a message and will be encoded accordingly.

Note: External logic must guarantee the SMC is high for the correct period, ie only while 223 x I bytes (I = interleave depth) of data are clocked through. Otherwise when SMC falls an invalid checksum will be produced.

SEL_A	SEL_B	Interleave	SMC_OUT Period (Bytes)	
		I = Depth	SMC_OUT = 1	SMC_OUT = 0
0	0	5	5 x 223	5 x 32
0	1	4	4 x 223	4 x 32
1	0	1	1 x 223	1 x 32
1	1	5	5 x 223	5 x 32

Table 1: Interleave Length Defined by SEL_A and SEL_B

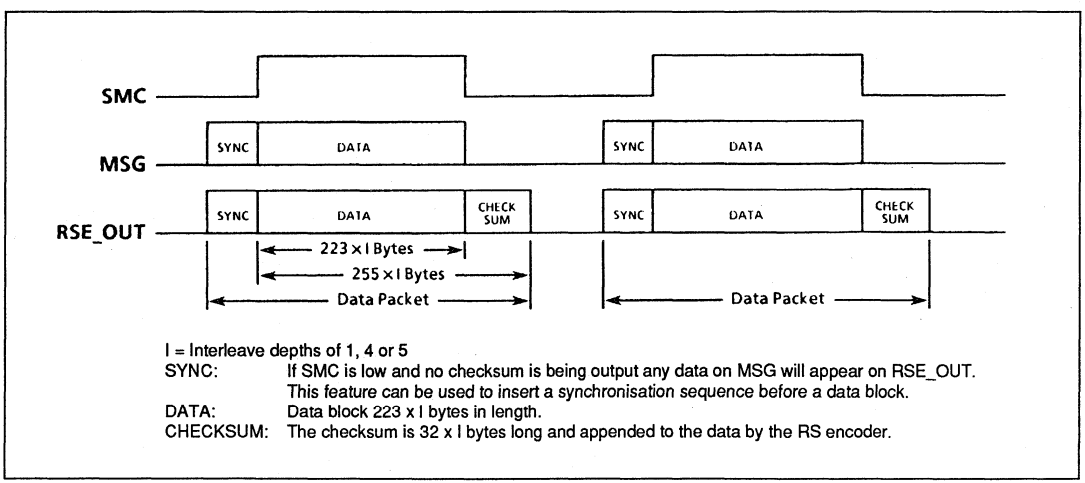


Figure 2: Reed-Solomon Encoder Operation

CONVOLUTION ENCODER

The convolution encoder generates 2 serial bits of output data for each bit it reads in. The coding operates cyclically over a length of 7 bits. It increases the bandwidth of the signal but establishes a correlation between succesive bits in the output signal.

The convolution encoder operates continuously using CE_CLK to read data in on CE_IN and to write the encoded data to CE_OUT.

If required the output of the Reed-Solomon encoder can be fed directly into the convolution encoder by connecting RSE_OUT to CE_ IN and CLKS to CE_CLK.

TEST GENERATOR

The MA1916 contains its own built-in test pattern generator, this can be connected to the RS encoder for in service testing. The test generator supplies test patterns and the SMC signal according to the inputs on T0-2 (see Table 2) and the interleave depth selected using SEL_A and SEL_B. Figure 3 shows the necessary connections for feeding test patterns through both the RS and the convolution encoder.

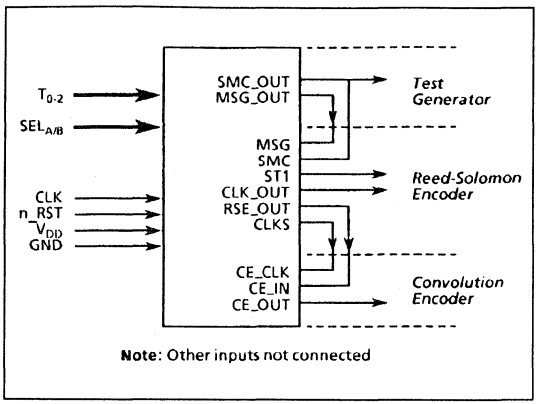


Figure 3: Test Configuration

T2	T1	T0	Test	Interleave Depth		
				I = 5 (1115 bytes)	I = 4 (892 bytes)	I = 1 (223 bytes)
0	0	0	N/A			0
0	0	1	1	(1, 2, 3, 4, 5) x 223	(1, 2, 3, 4) x 223	(1) x 223
0	1	0	2	(0) x 222 x 5, (0) x 4, (7B)	(0) x 222 x 4, (0) x 3, (7B)	(0) x 222, 7B
0	1	1	3	(0) x 222 x 5, (7B, AF, 99, FA, B7)	(0) x 222 x4, (7B, AF, 99, FA)	(0) x 222, 7B
1	0	0	4	(0) x 221 x 5, (7B) x 5, (47) x 5	(0) x 221 x 4, (7B) x 4, (47) x 4	(0) x 222, 7B
Other			N/A			

Table 2: Test Pattern on MSG_OUT Defined by T0-2

PIN DESCRIPTION

V_{DD} and GND (Power and Ground)

The MA1916 uses a single power supply of 5V ±10%.

CLK (Clock)

This input supplies a clock signal to the RS encoder and the Test generator. It requires a signal with a nominal 50% duty cycle running at twice the input data rate for the RS encoder. The rising edge of CLK is used to generate the internal CLKS signal which clocks data through the RS encoder.

n_RST (Reset)

This active low signal is a reset supplied to the RS encoder, the test generator and the convolution encoder. It should be noted that the reset does not clear the check sum in the RS encoder and a complete dummy data packet should be run through before valid data is sent.

SEL_A and SEL_B (Interleave Depth Select)

These inputs define the interleave depth of a message passing through the RS encoder They also specify the message length to be produced by the test generator (see Table 1). The inputs are connected to internal pulldown resistors.

T_{0-2} (Test Pattern Select)

These inputs select the pattern to be produced by the test generator (see Table 2). Each input is connected to an internal pull-down resistor.

T_3 (Production Test Input)

This input is used for production testing only It has an internal pull-down resistor and should be left unconnected .

MSG_OUT (Test Message Output)

This output pin carries the test patterns defined by the inputs To-2 and produced by the test generator. This signal can be connected directly to MSG for testing purposes.

SMC_OUT (Select Message or Checksum)
This output signal is held high while the test generator clocks out a data packet on the MSG_OUT pin. When the packet is complete this signal goes low. It is held low for a period equal to the time required by the RS encoder to send the corresponding checksum. When this is complete the signal goes high and the test generator begins a new data packet. This signal can be connected directly to SMC for testing purposes.

READY (Test Data Valid)
This output is held low during reset and remains low for the first complete cycle of SMC_OUT. READY rises on the second rising edge of SMC_OUT and remains high to indicate the presence of valid data on MSG_OUT.

CLKS (Synchronisation Clock)
This output clock runs at half the speed of the input clock CLK. CLKS remains low after n_RST is raised until SMC is raised, SMC being captured on the falling edge of CLK (timing 4). CLKS then changes state on the rising edge of each CLK cycle regardless of the state of SMC. The signal is used to clock data into and out of the RS encoder.

MSG (Message)
MSG is the data input to the RS encoder. Each bit is read in on the rising edge of CLKS. While the SMC signal is high data on the input passes directly to the output RSE_OUT. While SMC is low RSE_OUT is the logical XOR of the MSG input and the output of the check-sum generator. Therefore MSG must be held low while the RS encoder is clocking out the check sum (see Figure 4).

SMC (Select Message or Checksum)
While the SMC input is high, data on the MSG pin is clocked into the RS encoder. SMC is held high for a period dictated by the interleave depth being used (see Table 1). When SMC falls the RS encoder begins to clock out the checksum for the preceeding data. SMC should be held low until the complete checksum has been output. The rising edge of SMC indicates the start of a new data block to be encoded.

RSE_OUT (Reed-Solomon Encoder Output)
This signal outputs the completed data packet comprised of the message followed by its associated checksum block. The data is valid on the rising edge of CLKS.

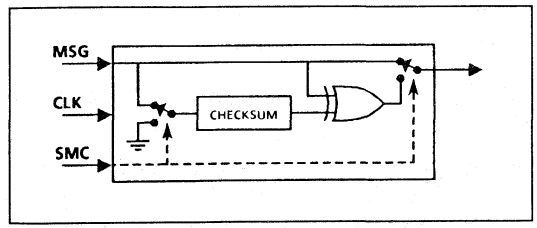


Figure 4: Reed-Solomon Encoder

ST1 (RS Encoder Output Valid)
This output is set low during a reset and goes high when sufficient dummy data has been clocked through the RS encoder to clear it (see Figure 5).

SYZ (Byte Rate Clock)
SYZ is a byte rate clock output derived from CLKS. It is high during every eighth period of CLKS and low at other times.

SZY (Byte Rate Clock)
SZY is a byte rate clock output derived from CLKS. It is low during every eighth period of CLKS and high at other times. It is the inverse of SYZ.

ST2 (Production Test Output)
The output is used for production testing and should be left unconnected.

TEST_POINT (Production Test Output)
This output is used for production testing and should be left unconnected.

CE_IN (Convolution Encoder Data In)
This input is used to read data into the convolution encoder. The state of CE_IN is read on the rising edge of CE_CLK.

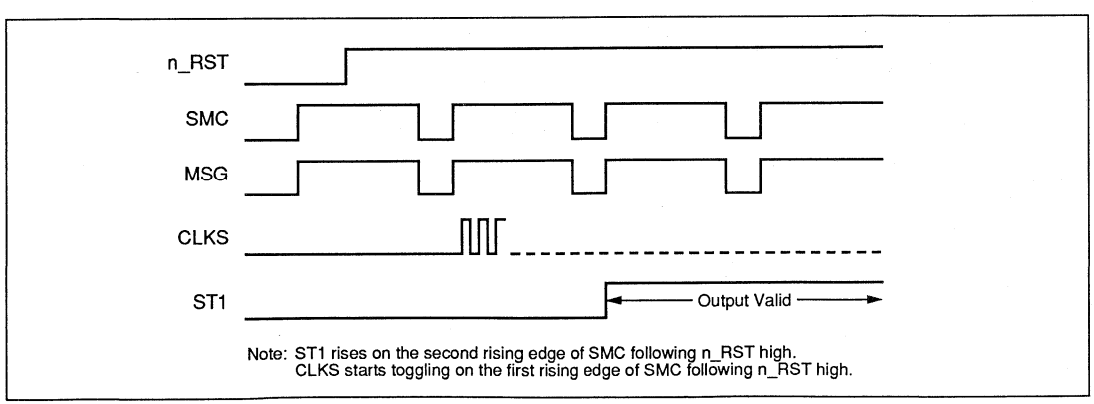


Figure 5: Reed-Solomon Encoder Operation

CE_CLK (Convolution Encoder Clock)

The CE_CLK input drives the timing of the convolution encoder. Data is read in on CE_IN on the rising edge of CE_CLK and output on CE_OUT on both the rising and falling edge of CE_CLK.

Note: The output data rate is twice the input data rate.

A 50% duty cycle clock is required. If this is provided by the CLKS output, data can be read directly from RSE_OUT to the CE_IN input (see figure 3).

CE_OUT (Convolution Encoder Output)

This signal carries the output data from the convolution encoder. The data rate on CE_OUT is twice that of CE_IN.

CLK_OUT (Clock Out)

CLK_OUT is a buffered output of the CLK input signal. If CLKS is connected to CE_CLK to drive the convolution encoder, CE_OUT can be captured on the falling edge of CLK_OUT.

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 3: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	CMOS Input High Voltage	V_{DD} = 5.5V	0.8 V_{DD}	-	V_{DD}	V
V_{IL}	CMOS Input Low Voltage	V_{DD} = 5.5V	V_{SS}	-	0.2 V_{DD}	V
V_{OH}	CMOS Output High Voltage	V_{DD} = 5V, I_{OH} = -1.0mA	V_{DD}-0.5	-	-	V
V_{OL}	CMOS Output Low Voltage	V_{DD} = 5V, I_{OL} = 4.0mA	-	-	0.4	V
I_{IL}	Input Leakage Current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-10	-	10	µA
I_{PDL}	Input Pull-Down Current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-20	-	150	µA
I_{DD1}	Static Power Supply Current	V_{DD} = 5.5V	-	0.1	2.5	mA
I_{DD2}	Dynamic Power Supply Current	CLK = 10MHz, V_{DD} = 5.5V	-	3	10	mA

Notes: 1. V_{DD} = 5V±10%, over full operating temperature range. 2. Total dose radiation not exceeding 1x10^5 Rads(Si) 3. Mil-Std-883, method 5005, subgroups 1, 2, 3

Table 4: DC Electrical Characteristics

AC CHARACTERISTICS

No.	Parameter	Min.	Max.	Units
1	CLK hlgh to CLKS	-	25	ns
2	CLK high to SYZ or SZY	-	30	ns
3	SMC hold after CLK low	0	-	ns
4	SMC setup to CLK low	30	-	ns
5	MSG set up to CLKS high	10	-	ns
6	MSG hold after CLKS high	10	-	ns
7	MSG to RSE_OUT propagation delay	-	30	ns
8	CLKS to RSE_OUT (SMC low)	-	25	ns
9	CLK to CLK_OUT propagation delay	-	25	ns
10	CE_IN setup to CE_CLK hlgh	10	-	ns
11	CE_IN hold after CE_CLK high	10	-	ns
12	CE_CLK to CE_OUT	-	25	ns
13	CLK CYCLE TIME	100	-	ns

Note: Mil-Std-883, method 5005, subgroups 9, 10, 11

Table 5: AC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Table 6: Capacitance

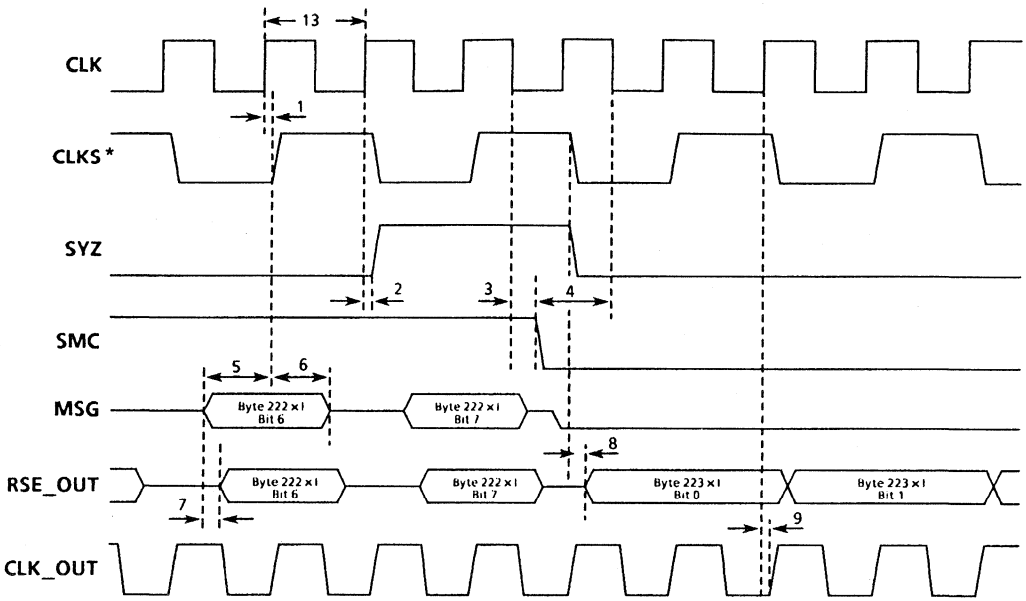
Symbol	Parameter	Conditions
F_T	Functionality	V_{DD} = 4.5V - 5.5V, Frequency = 1MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} = V_{OH} = V_{DD}/2$ Temperature = -55°C to +125°C, Radiation to 1MRad Total Dose Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Table 7: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 4 at +25°C
2	Static characteristics specified in Table 4 at +125°C
3	Static characteristics specified in Table 4 at -55°C
7	Functional characteristics specified in Table 7 at +25°C
8A	Functional characteristics specified in Table 7 at +125°C
8B	Functional characteristics specified in Table 7 at -55°C
9	Switching characteristics specified in Table 5 at +25°C
10	Switching characteristics specified in Table 5 at +125°C
11	Switching characteristics specified in Table 5 at -55°C

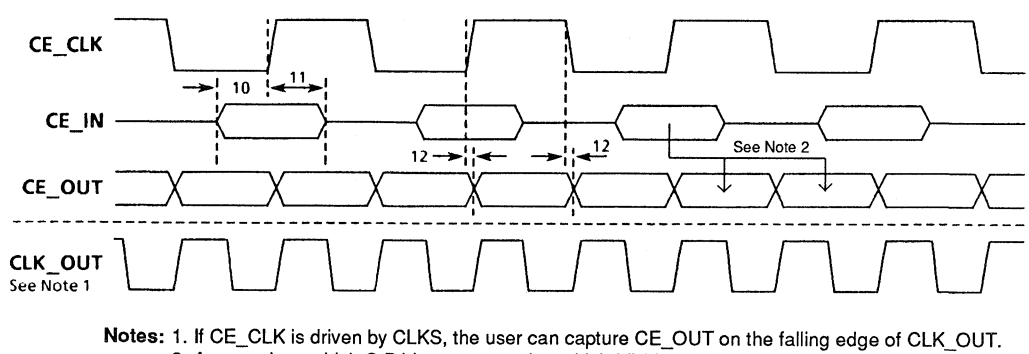
Table 8: Definition of Subgroups

TIMING DIAGRAMS



Note: Bytes of MSG labelled 0 to 222 x I
Bytes of RSE_OUT labelled 0 to 254 x I
Bits labelled 0 to 7
I = Interleave depth of 1, 4 or 5
* User can capture RSE_OUT on rising edge of CLKS

Figure 6: RS Encoder Timings



Notes: 1. If CE_CLK is driven by CLKS, the user can capture CE_OUT on the falling edge of CLK_OUT.
2. Arrows show which O/P bits correspond to which I/P bit.

Figure 7: Convolution Encoder Timings

OUTLINES AND PIN ASSIGNMENTS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

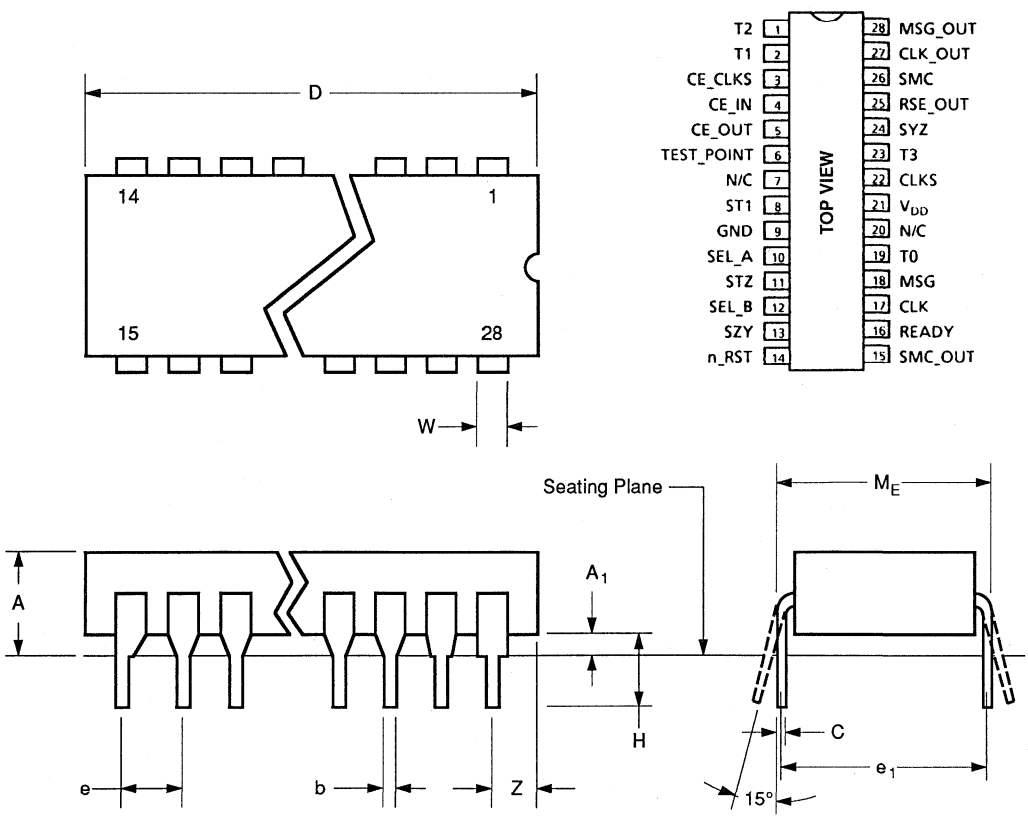


Figure 8: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	3.18	-	-	0.125
Q	0.66	-	-	0.026	-	-
b	0.38	-	0.48	0.015	-	0.019
c	0.10	-	0.18	0.004	-	0.007
D	18.08	-	18.49	0.712	-	0.728
e	-	1.27	-	-	0.050	-
L	7.62	-	9.91	0.300	-	0.390
M	12.50	-	12.09	0.492	-	0.508

XG530

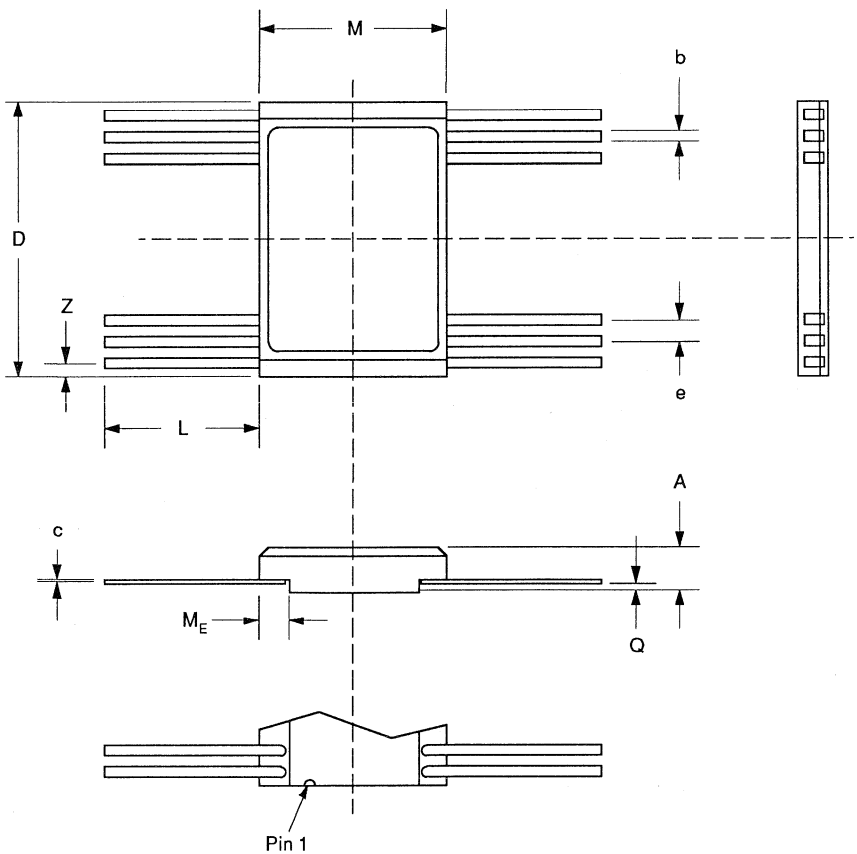


Figure 9: 28-Lead Ceramic Flatpack (Solder Seal) - Package Style F

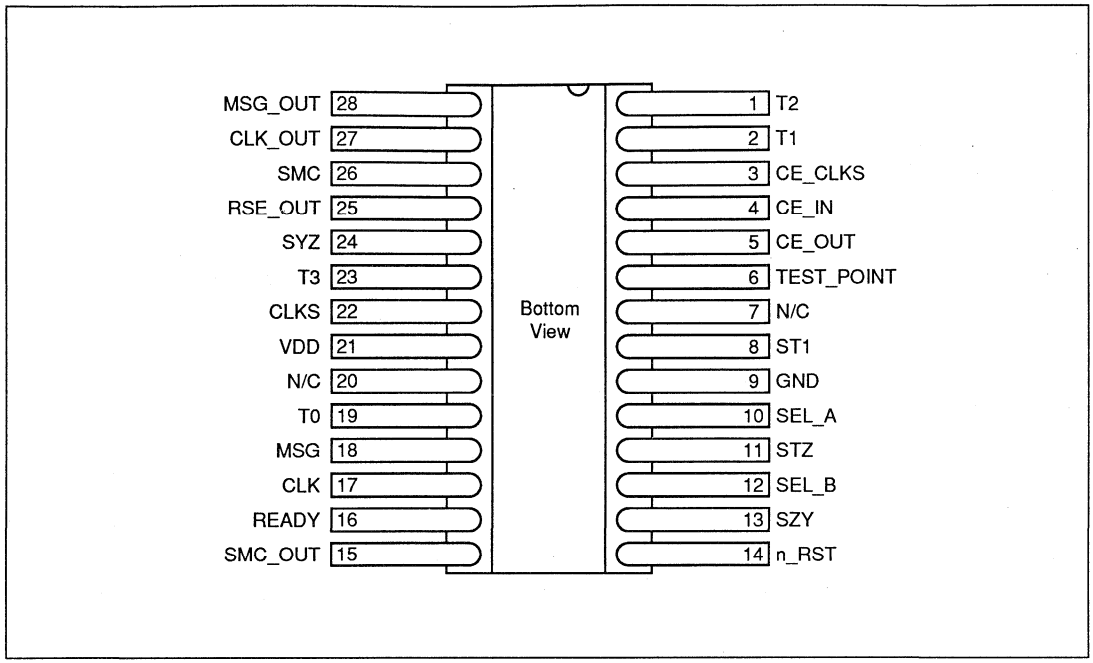


Figure 10: Flatpack Pinout

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019, Ionizing Radiation (Total Dose).

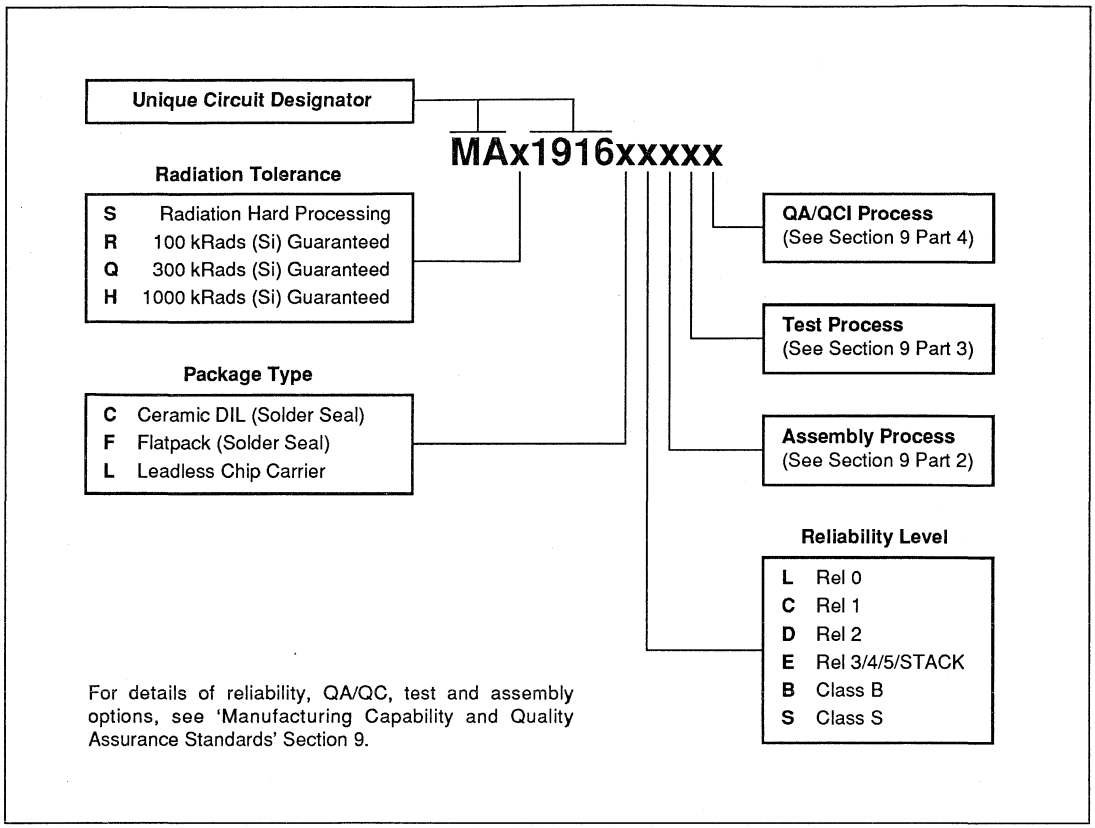
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 9: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

MA28138

OBDH REMOTE BUS INTERFACE

The MA28138 is an OBDH Remote Bus Interface (RBI) that provides the facilities required by a modern packet OBDH bus system but at the same time preserves compatibility with existing RTU hardware and software. Designed under an ESA contract, the RBI ASIC implements the ESA RBI-2 Remote Bus Interface and 8-bit Broadcast Polling protocols for transfers of data between the OBDH DBI bus and processor memory.

Linked to the OBDH bus via a bus terminal (MA28139 OBT), the RBI executes central terminal instructions from the Interrogation bus including mission configurable user commands and status. The RBI handshakes all CTU commands on the Response bus and traps DMA errors. The RBI supports bi-directional data transfers on the Response bus allowing the possibility of working without a Block Transfer bus. The inclusion of a Block Transfer bus using this RBI in an OBDH system will increase its throughput capacity by about a factor of four.

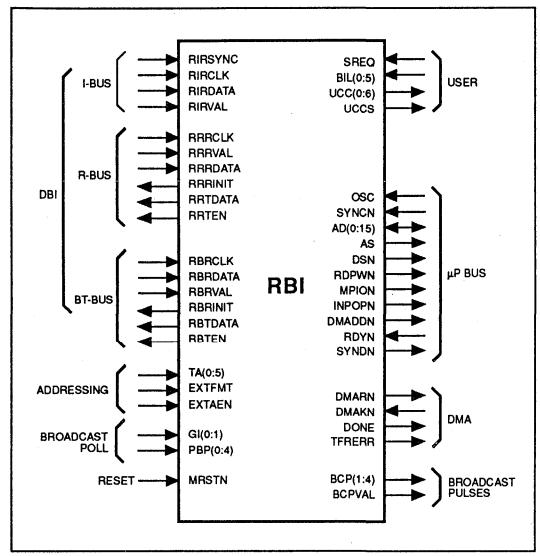


Figure 1: Block Diagram

FEATURES

- Radiation Hard
- Low Power Consumption
- Single CMOS-SOS ASIC Implementation
- Direct Connection to Processor Address/Data and Control Busses
- Programmable User-to-User Group Transfers
- Can Support Bi-directional DMA Transfers without Block Transfer Bus
- Block Transfers Supported
- Fully Compliant with ESA RBI-2 Protocol, ESTEC WDI/CS/928

TYPICAL CONFIGURATION

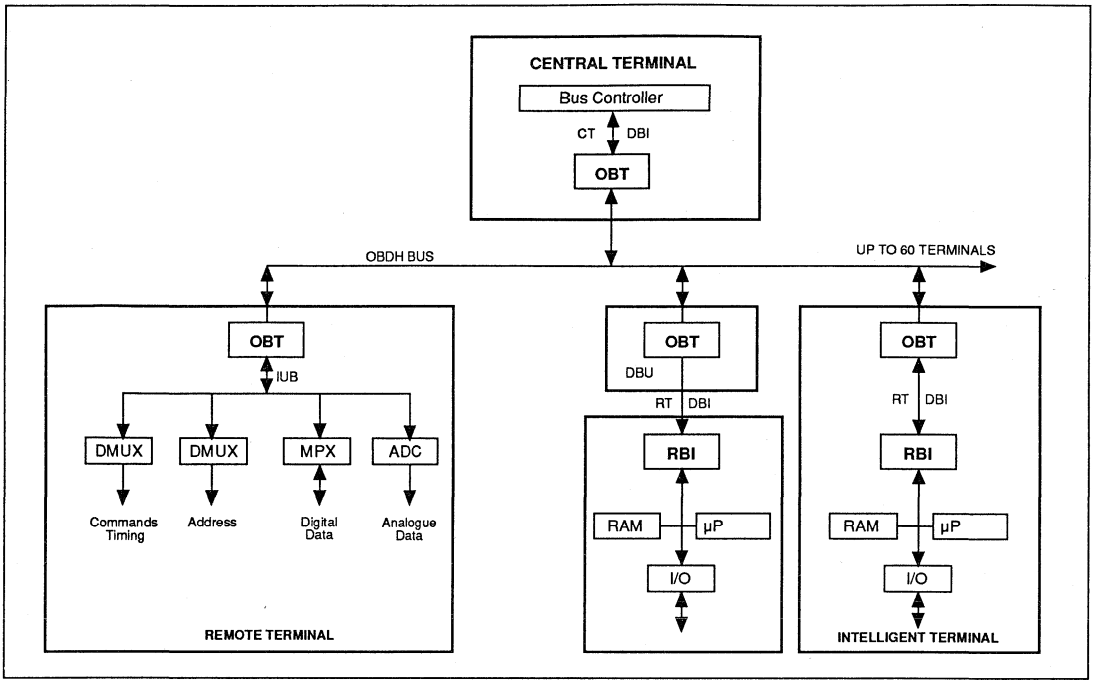


Figure 2: Typical Configuration

USER FACILITIES

1. SPACECRAFT TIME

The RBI places the BroadCast Pulses transmitted by the CTU onto the BCP(1:4) pins shortly after the SYNC pulse at the end of every Interrogation. BCPVAL indicates the overall validity of the previous Interrogation and hence the BroadCast Pulses within it. BCP(1:4) and BCPVAL Waveforms are shown in figure 10.

2. USER COMMANDS

The RBI latches the 7 bit UCC field from Mode 1 instructions to User Command pins, UCC(0:6), and generates an active high strobe pulse, UCCS, when the value on these pins change. The user can decode up to 126 commands. An all-'1's UCC field will not be loaded; this facility can be used if it is necessary to change the RBI's bus selection or Programmable Address without loading a new value into the UCC register.

3. USER STATUS

The RBI single bit 'Broadcast Poll' response is the SREQ (user Service Request) pin state. The RBI 'Read Status' 21-bit response includes the state of the 6 Bi-Level user input pins, BIL(0:5), and the state of the SREQ (user Service Request) pin.

4. DATA TRANSFERS

All data transfers are controlled by the RBI DMA controller. This can input (to user) data from the OBDH I, R or BT bus or output data to the R or BT bus in blocks of up to 4,095 words of 16-bits each.

The MA28138 DMA controller transfers one word (two words if the BT bus is selected) to the user's memory per 64µs OBDH slot in a single cycle-stealing DMA 'request, read/write, acknowledge' cycle in typically 1µs, slowing the user's internal CPU processing by less than 2%. The nominal bit rate is 500kBits/sec. Bit rates up to at least 10Mbits/sec are supportable by the RBI.

5. PROGRAMMABLE GROUP TRANSFERS

The RBI has a hard-wired Terminal Address (TA) and a Programmable Address (PA). The CTU is able to set up the PA, bus selection and transfer direction of each RBI within a group using its unique TA and then observe its status response as part of a handshake mechanism. The CTU should program one RBI within a group to act as the 'talker' to the chosen bus (or act as the 'talker' itself) and program the remainder of the group to act as 'listeners' from the same bus which use the TA of the 'talker' as their PA (or a unique dedicated TA).

A single 'Proceed' instruction sent by the CTU addressed to the TA of the 'talker' causes one data word to be transferred if either the I- or R-bus has been selected and a contiguous block of data words to be transferred if the BT-bus has been selected.

Facilities for conducting broadcast RBI setup and CTU-RBI transfers using the all-'1's BroadCast Address (BC) are also available when the Extended Addressing mode is enabled by setting the EXTAEN pin to '1'.

6. CONFIGURATION

The Broadcast Pulse outputs, User Control Command outputs and Bi-Level Status inputs can be configured to specific mission requirements.

7. TERMINAL ADDRESSING

Both standard (5 bit) and extended (6 bit) terminal addressing formats are provided. Setting the EXTFMT (Extended terminal address Format) pin to '0' causes standard (5 bit) terminal addressing to be used, Interrogation bit 6 to be regarded as BCP(4) and the hard-wired TA(0) (MSB) input to be ignored. Setting EXTFMT to '1' causes extended (6 bit) addressing to be used, Interrogation bit 6 to be regarded as TA(0) (MSB) and BCP(4) output to be forced to '0'.

8. ADDRESSING MODES

ESA specify the availability of each command in the RBI-2 protocol instruction set when addressing is performed at the hard-wired Terminal Address, the Programmable Address and the (all-'1's) Broadcast Address. The RBI-2 protocol only permits the use of a minimal set of commands which are needed to achieve the transport of data blocks (specifically only 'Proceed' commands are permitted at the Programmed Address and no commands are permitted at the Broadcast Address). This strategy does not, however, permit the CTU to perform operations such as the simultaneous set-up of a group of connected RBIs or the broadcast of blocks of data to all RBIs without explicitly addressing each RBI in turn.

The MA28138 instruction decoder is designed so that by setting the EXTAEN (Extended Addressing Enable) pin to '1', all commands which may be physically performed by a network of RBI devices without electrical hazard are permitted using either the Programmed Address or the Broadcast Address. The only restrictions on permissible commands in this mode are those caused by the need to have only one bus 'talker' on the network. Note, however, that in this mode, no response is generated by any 'listening' RBI device addressed using its PA. (One method here is to set the group's PA to be the same as the TA of the 'talker'). It will be necessary to check that each RBI in the group has been correctly set up or that transferred blocks of data have been successfully received, for example by asking each listener in turn for its status and/or next DMA address or to return a software-generated checksum.

For full compliance with the ESA RBI-2 WDI/CS/928 protocol, EXTAEN should be set to '0'. Full detatils of which commands are accepted under the Basic Addressing mode (EXTAEN = '0') and the Extended Addressing mode (EXTAEN = '1') are given in Table 2. Note that the Programmed Address (PA) within the MA28138 can not be programmed (in any way) by using commands directed to either the Programmed Address or the Broadcast Address. Setting the Programmed Address to a 5-bit or 6-bit all-'1's field (depending on the terminal address format in use) causes it to be considered as invalid.

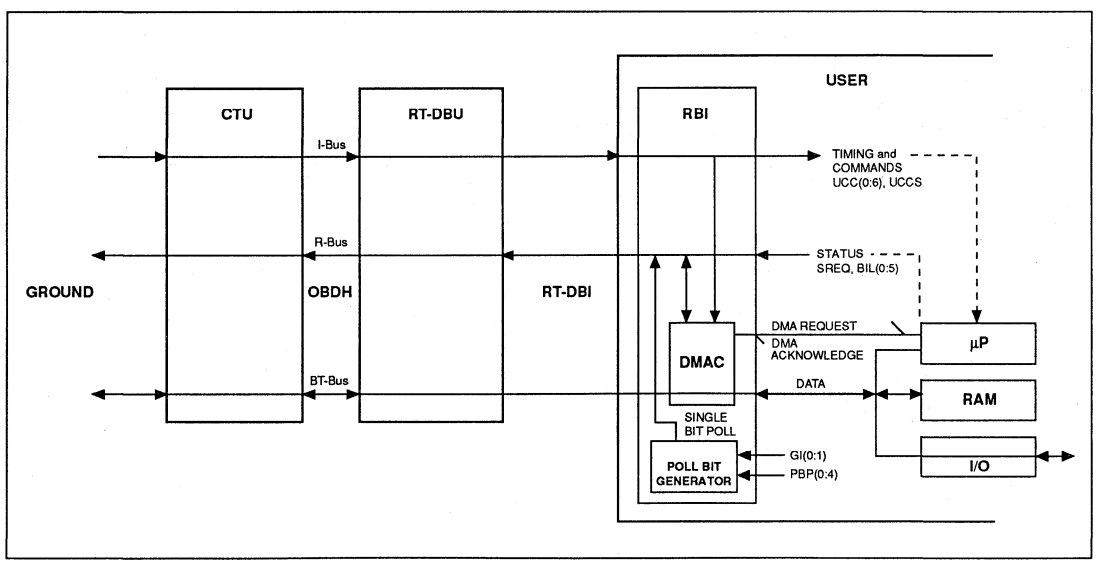


Figure 3: General System Block Diagram

RBI ARCHITECTURE

The MA28138 OBDH RBI basically acts as a DMA controller connected to the user's memory which is controlled from the OBDH bus. It contains five major components: an Interrogation Decoder and Sequencer, a Response Generator and Decoder, a Block Transfer Generator and Decoder, a single-bit Broadcast Poll Generator and the DMA Controller.

All data exchange with the user is accomplished in blocks using the DMA controller, but the OBDH bus used to carry the data can be selected by the CTU using appropriate set-up commands. The optional Block Transfer bus is fully supported.

The user's status can be inspected from the CTU via a 6-bit dedicated parallel input port (BIL(0:5)). Similarly, interrupts, hardware run/stop/halt signals, etc. can be delivered to a 7-bit dedicated parallel output port (UCC(0:6)). A single-bit status input pin (SREQ) can accessed using broadcast polling and Broadcast Pulses embedded within each Interrogation are also decoded.

RBI INSTRUCTION SET

The RBI only executes and responds to valid instructions (tables 1, 2 and 3). Below is a description of the RBI instruction modes (interrogation bits 12 to 14).

1. MODE O (READ STATUS)

Three Mode 0 commands (sent via the Interrogation bus) can be used by the CTU to read the RBI's DMA Address, block Length or internal Status. The RBI responds (via the Response bus) with the appropriate current setting obtained from the RBI's DMA controller and/or the user's Service Request (SREQ) and Bi-Level status (BIL(0:5)) input pins. The 'Read Status' command also resets any DMA error reports.

2. MODE 1 (INSTRUCT RBI/USER)

Mode 1 Interrogations sent by the CTU can be used to set the RBI transfer bus selection, Programmed Address and/or User Control Command (UCC(0:6)) output pins or to reset the RBI's DMA process. If this command is omitted, the next transfer uses the last bus selection, etc. (see the flowchart, Figure 9). Setting the Programmed Address to all-'1's causes it to be disabled; specifying all-'0's causes no change to be made. A UCC value of 127 will not be loaded; specifying this value causes no change to be made.

3. MODE 3 (LOAD START ADDRESS)

Mode 3 Interrogations load the RBI's DMA Start Address register. The associated response contains the RBI's new address provided that no data transfers have taken place (using the 'Proceed' command) before it is transmitted. If this instruction is omitted, the next transfer starts at the address following the last address of the last transfer.

4. MODE 4 (LOAD BLOCK LENGTH)

Mode 4 interrogations load the RBI's DMA Block Length register. In input modes, the associated response contains the RBI's new block length provided that no data transfers have taken place (using the 'Proceed' command) before it is transmitted. In output modes, the new block length indicated in the response will normally have been decremented since the RBI's DMA controller will have performed the first fetch from the CPU's memory. This command cannot be omitted. A value of 0 in the length register inhibits any transfer and sets the "DMA Overrun" flag in the RBI status register if a transfer is attempted.

5. MODE 7 (PROCEED)

If either the I-bus or the R-bus have been selected, the ESA OBDH RBI-2 protocol mandates that a Mode 7 'Proceed' instruction is given for every word transferred. The CTU can transfer words in consecutive slots (fastest) or in 'handshake' mode for highest data integrity or in-between servicing other OBDH users.

If the BT-bus has been selected, a Mode 7 'Proceed' instruction starts the autonomous transfer of a block of data.

The RBI's response to an 'Input from I-bus' Mode 7 'Proceed' instruction is the remaining DMA block length. When the R-bus has been selected for a transfer, it carries the data word in place of a response; consequently if 'Input from R-bus' is selected then no response is possible and if 'Output to R-bus' is selected then the RBI's response is the data word requested from the CPU's memory. If either 'Input from BTbus' or 'Output to BT-bus' is selected, the response associated the 'Proceed' instruction is the current RBI/user status (as for a 'Read Status' command).

Note: The data contained in any response is captured shortly before the response is transmitted to ensure that it contains current data and may be monitored at will during the transfer process.

For 'Input from I-bus' transfers, a continuous stream of 'Address, Length, Proceed' instructions may result (depending on DMA access timing) in 'Address, Length, Length' responses which differ from those previously set up because the first word transfer will commence in response to the 'Proceed' command. For output transfers, the address and length responses will also be incremented and decremented (respectively) by one word for R-bus transfers (two words for BT-bus transfers) as the RBI's DMA controller performs a pre-fetch from the CPU's memory in order to ensure that the required data is available for transmission.

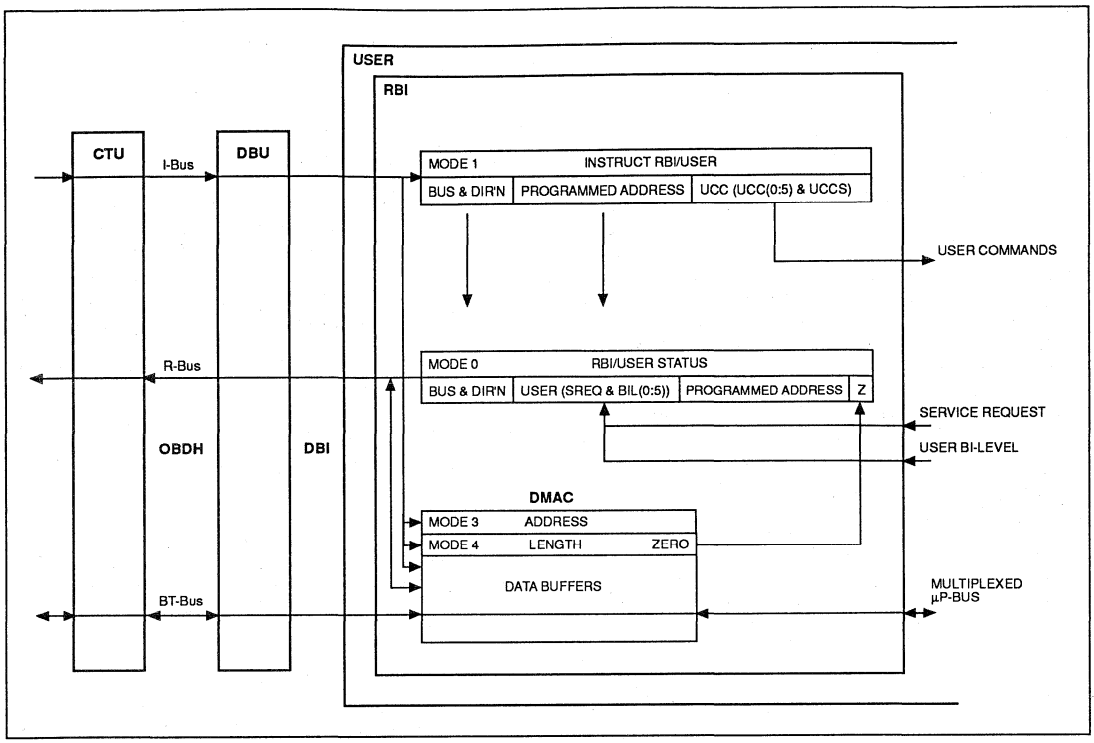


Figure 4: RBI Control Registers

USING THE RBI

1. BROADCAST POLLING

RBI executes single-bit broadcast poll instruction specified in ESA document THB/APo/1906/av. If the instruction poll group identifier (interrogation bits 29 and 30) match the RBI's hard-wired poll Group Identifier pins (GI(0:1)), the RBI generates a single-bit response containing the SREQ pin state.

Setting a value of 0 on the RBI's hard-wired Poll Bit Position pins (PBP(0:4)) causes the single-bit poll response to be generated (on the RRTDATA and RRTEN pins) after the usual '3 slot' response delay and to begin shortly after the RIRSYNC falling edge. Setting larger values cause the response bit to be delayed by successive bit periods up to a maximum value of 23. Values from 24 to 31 do not cause a response bit to be generated.

ESA document THB/1229/LJ/mvg defines the use of up to 4 groups of up to 8 broadcast poll response bit windows, each 3 bit periods long. Within each window, a single broadcast poll bit is surrounded by two bit guard bits to protect against OBDH bus propagation delays and reflections. Values of 1, 4, 7, 10, 13, 16, 19 or 22 should be specified for PBP(0:4) to comply with this scheme.

The value of the Poll Bit Position pins (PBP(0:4)) may be dynamically changed during the response period if it is required to create multiple broadcast poll response bits; to be useful, the value of SREQ must also be changed. Changes to both of these signals should be made as RIRCLK ↑ and this facility should be used with caution.

2. CTU SETS UP ONE RBI OR A GROUP OF RBIs FOR DATA TRANSFERS

Each RBI within the group (or just one) is set up individually using a combination of Mode 1 'Set Bus Selection, etc.', Mode 3 'Load Start Address' and Mode 4 'Load Block Length' instructions (see Table 1) whose embedded terminal address matches the RBI's unique Terminal Address (TA(0:5)) pins. The RBI response(s) confirm(s) correct RBI operation and the new RBI setting(s). A single RBI or one or more pre-defined groups of RBIs may be set up in this way. See Figure 5. If the Extended Addressing mode is Enabled (EXTAEN = 1), it is also possible to set up groups of RBIs using instructions whose embedded terminal address matches the RBI's internal Programmed Address register - see Table 2 for more details.

3. CTU DATA TRANSFER TO OR FROM ONE RBI

Depending upon the selected transfer bus, the CTU sends either one or a series of Mode 7 'Proceed' commands to one RBI's unique hard-wired Terminal Address. I- or R-bus transfers will require one 'Proceed' command to be sent per data word transferred; BT-bus transfers require only one 'Proceed' per data block. Data for 'Input from I-bus' transfers must be embedded in bits 15-30 of the Interrogation as immediate data; data for R- or BT-bus transfers must be driven onto or read from the selected bus after the usual '3 slot delay' by the CTU. I- and R-bus data transfer is rigidly controlled by the CTU on a 'word-by-word' basis; BT-bus transfer is merely initiated by the CTU and then proceeds autonomously. The selected RBI responds as per Table 1 and can be monitored accordingly. An example R-bus transfer to or from a single RBI is shown in Figure 6.

4. CTU DATA BROADCAST TO A GROUP OF RBIs

Each RBI has a Programmable Address which can be changed using a Mode 1 'Set Bus Selection, direction, PA, UCC' command directed to the RBI's unique Terminal Address. The CTU sets a group of RBIs to use the same bus and the same PA (ensuring that it is both an unused TA and unique) and then transmits data to them. The CTU places the chosen PA in the terminal address field of each Mode 7 'Proceed' command. Similar data transfer criteria to those described in 2. above will apply, but none of the RBIs are able to generate a response. An example I-bus transfer to a group of RBIs is shown in Figure 7.

5. RBI DATA BROADCAST TO A GROUP OF RBIs (AND CTU)

The CTU sets one RBI within the group to act as the 'talker' to the desired bus. There can be only one 'talker' per group. The CTU sets the remainder of the RBIs within the group to act as 'listeners' from the same bus and sets their PA to be the same as the talker's TA. The CTU places the talker's unique TA in the terminal address field of each Mode 7 'Proceed' command so that the talker's output data is copied into all listeners within the group (and CTU if needed). Similar data transfer criteria to those described in 2. above will apply, but only the talker will be able to generate a response.

If desired, the talker's PA can be set to its TA or be disabled for added security. Groups can be reconfigured by the CTU so that, for example, one RBI can belong to more than one group. An example BT-bus transfer from one RBI to the remainder of its group is shown in Figure 8.

6. CTU CHECKS FOR PROPER TRANSFER

The CTU may check the data transfer process as it occurs by monitoring available response(s) to the 'Proceed' command(s) and/or by periodically performing Mode 0 'Read Address', 'Read Length' and 'Read Status' instructions addressed in turn to each RBI within the group and checking those responses (see Table 1 for details). Alternatively, it may simply perform such Mode 0 checks just once - after the transfer process has been completed. The CTU should inspect the 'Read Status' response for DMA error or DMA overrun indications in bits 4-6.

7. RBI ANOMALY DETECTION

Power up resets the RBI length, UCC, PA and bus selection registers to length = 0, UCC = 0, PA = 63 (= disabled), status bits 4 - 6 = 111.

RBI cannot transfer data when it receives:

1) a Proceed command (all modes) or input data (II, IR and IB modes) when the DONE pin is high, i.e. when the RBI length counter = 0 or the DMA controller's buffer is not empty. This error will also cause a DMA error to be flagged. (DMA overrun).

2) no processor DMAKn before the next data word (II, IR and OR modes) or two data words (IB mode) must be transferred to or from the user's memory, i.e. the DMA controller's buffer is not empty. (DMA error). Note that DMA overrun will also cause this error to be indicated.

3) OBDH input data from Response or Block Transfer busses with validity error(s), i.e. RRRVAL = 0 or RBRVAL = 0. (DMA error).

The RBI remains fully functional throughout: errors only stop the current transfer and jam status bits 4 - 6 to 011 (DMA overrun) or 111 (DMA error) until a Mode 0 'Read Status' command reads the error, after which the status bits report the bus selection etc. as normal.

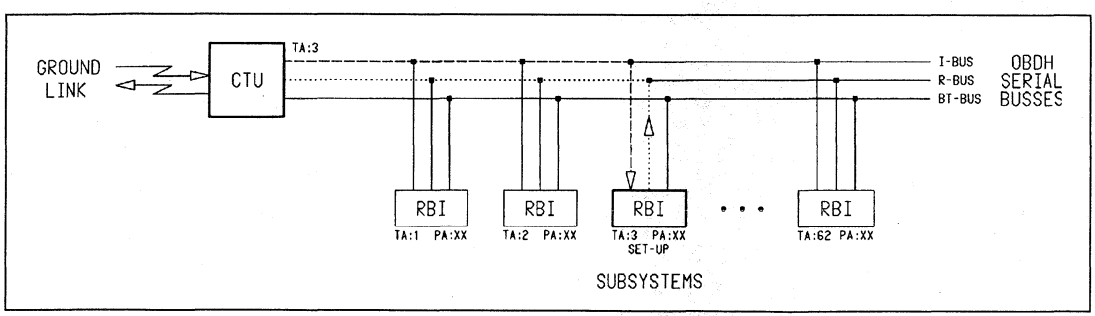


Figure 5: CTU set up of an individual RBI.
All RBIs within the required group must be set up individually unless the Extended Addressing mode is enabled (EXTAEN = 1)

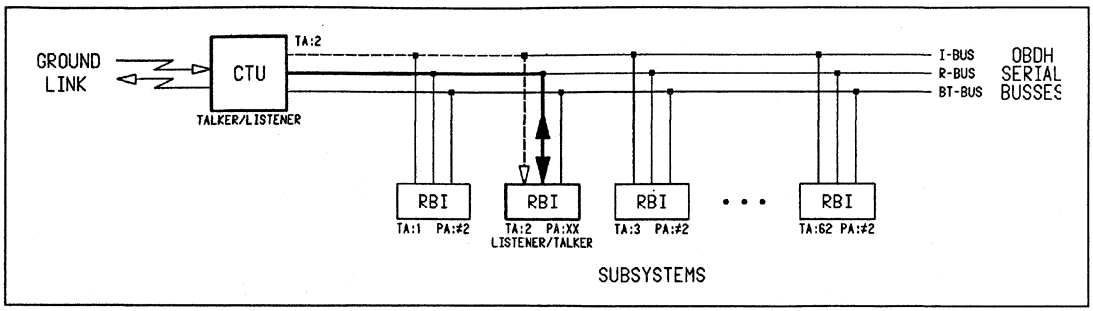


Figure 6: CTU transfer to/from a single RBI via the R-bus.
Transfers on other busses are similar and will also produce a response.

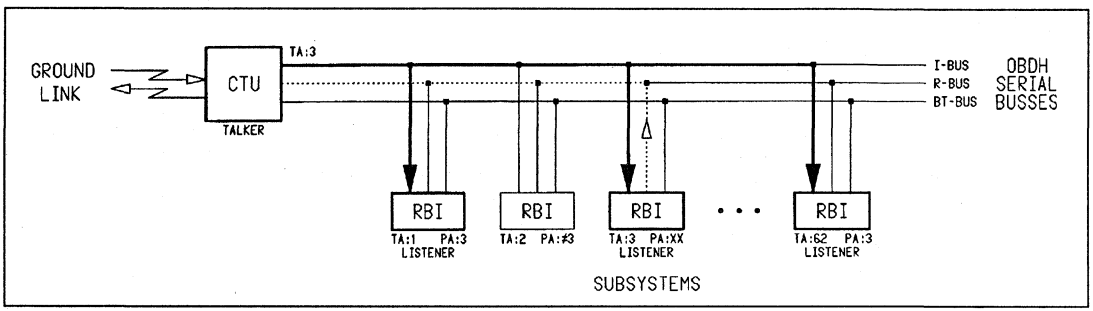


Figure 7: CTU transfer to a group of RBIs via the I-bus. Transfers on other busses are similar.
A response will only be generated if the R-bus is not used for transfer and the Terminal Address of one member of the group corresponds to the Programmable Address assigned to the group

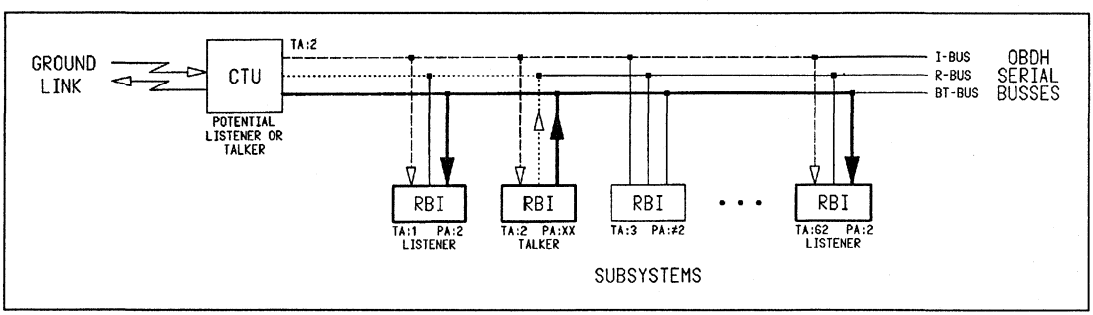


Figure 8: RBI transfer to a group of RBIs via the BT-bus. Transfers on other busses are similar.
A response will only be generated by the group's 'talker' if the BT-bus is used for transfer.

Note: For all bus selections, DMAKn must be granted to the DMA controller so that the required DMA exchange can be completed before the next data word is placed into or removed from its buffer in order to prevent a DMA Overrun condition occurring. For II, IR and OR mode transfers, this period is controlled by the CTU and may be lengthened to suit expected DMA availability.

Additionally, in OB mode, if DMA access cannot be obtained, data transmission to the BT-bus is simply inhibited (and delayed) until such access can be obtained and no DMA error is generated. This mechanism permits the OB mode output transmission rate to the BT-bus to adapt to DMA availability. Similarly, in the IB mode, data words which are missing from the BT-bus data stream will not be transferred to the RBI's DMA controller and will not hence change the address and length registers.

Validity, parity or length errors on the OBDH Interrogation bus will cause the affected Interrogation to be ignored. Mode 7 'Proceed' instructions ignored in this way will result in underrun - one (or more) data word(s) will be missing from the transferred data block. For II and OR mode transfers, there will also be no response. For OB mode transfers, there will be no BT bus activity. In all modes, underrun may be detected by sending Mode 0 'Read Address' and 'Read Length' commands and comparing the values obtained with those expected. For IR and IB mode transfers, the CTU is also able to conduct similar checks during the transfer process.

Note that either the DMA Overrun or DMA Error conditions will cause the TFRERR output pin to be raised until either a Read Status or a DMA Reset command is received. While TFRERR is high, no DMA data transfers will be permitted and no responses to Mode 7 Proceed commands will be generated.

NORMAL OPERATION

1. POWER UP

Power up resets the RBI, so the CTU must set up the RBI bus selection and direction, (and UCC, PA if required), DMA address and length before proceeding with the first transfer.

2. DMA ENABLE

The user processor must allow RBI direct memory access (DMA) during data transfers. The CTU can read the processor DMA Enable (DMAE) status via a BIL user input pin and, if necessary, send a UCC interrupt to ensure that DMA is enabled before the transfer is begun. RBI failstops if the user disables DMA during transfer.

3. HANDSHAKING

The OBDH and RBI protocols were designed for handshaking. For error-free operation, the CTU may check each response before sending the next instruction.

4. TYPICAL TRANSFER INSTRUCTION SEQUENCE

CTU instructions 'single-step' the RBI down a transfer sequence e.g. that shown in Figure 9. Additionally, the CTU may wish to check that each data block has been successfully transferred. For II mode transfers, check for a zero length response to the final 'Proceed' command; for all other modes, perform a 'Read Length' instruction and perform a similar check. Additionally, for all bus selections, perform a 'Read Status' instruction and inspect the response for DMA error or DMA overrun indications in bits 4-6.

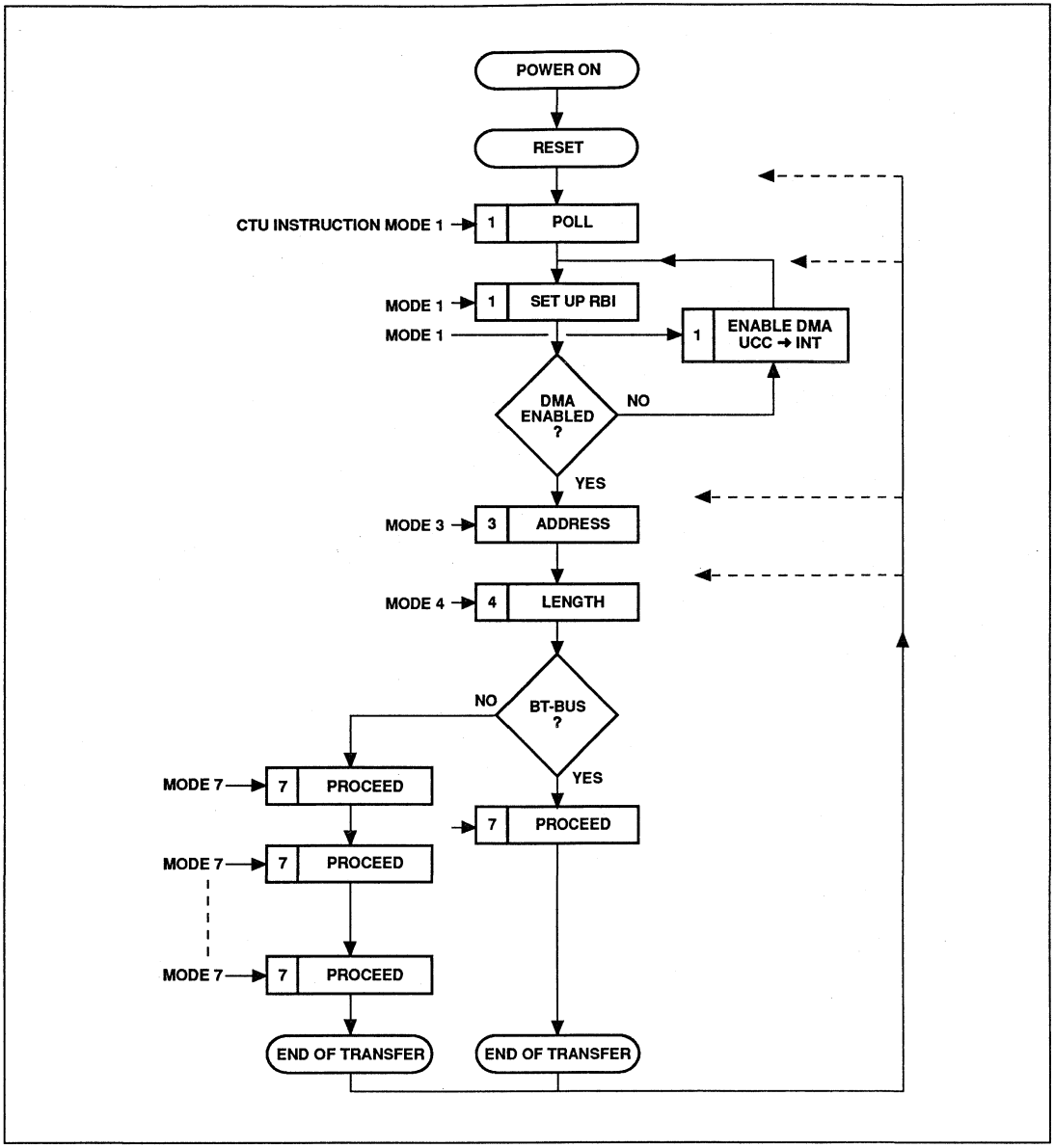


Figure 9: Flowchart Showing Typical Transfer Instruction Sequence

Interrogation Bit Number (notes 1, 2, 3) 6:11 (Basic Format) 5:11 (Extended Format)	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	**RBI Action**	**RBI Response** Bits 0-19 (note 7)
Instruction	**Mode 0**																				
TA	0	0	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Read DMA address	0000 (DMA address)
TA	0	0	0	1	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Read DMA length	00000000 (DMA length)
TA	0	0	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Read DMA bus selection and RBI/user status (note 8)	0000 (RBI/user status)
Instruction	**Mode 1** (notes 4, 5, 6)																				
TA	0	0	1	0	0	0	(Programmed Address)						(User Control Command)							Select Input from I-bus, Set PA, UCC	0000 (RBI/user status)
TA	0	0	1	0	0	1	(Programmed Address)						(User Control Command)							Select Input from R-bus, Set PA, UCC	0000 (RBI/user status)
TA	0	0	1	0	1	0	(Programmed Address)						(User Control Command)							Select Input from BT-bus, Set PA, UCC	0000 (RBI/user status)
TA	0	0	1	0	1	1	(Programmed Address)						(User Control Command)							Reset DMA, etc	0000 (RBI/user status)
TA	0	0	1	1	0	1	(Programmed Address)						(User Control Command)							Select Output to R-bus, Set PA, UCC	0000 (RBI/user status)
TA	0	0	1	1	1	0	(Programmed Address)						(User Control Command)							Select Output to BT-bus, Set PA, UCC	0000 (RBI/user status)
TA	0	0	1	1	1	1	(Programmed Address)						(User Control Command)							Set PA, UCC only	0000 (RBI/user status)
All 1s	0	0	1	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	(G.I.)	Broadcast poll given group for user Service Request state (note 9)	(Single Broadcast Poll bit)
Instruction	**Mode 3**																				
TA	0	1	1	(16 bit start address to be loaded into DMA controller)																Load DMA start address	0000 (DMA address)
Instruction	**Mode 4**																				
TA	1	0	0	x	x	x	x	(12 bit length to be loaded into DMA controller)												Load DMAC length	00000000 (DMA length)
Instruction	**Mode 7** (notes 10, 11)																			**Proceed**	
TA or PA	1	1	1	(16 bit I-bus word.....memory load data.....)																If II selected, Input word from I-bus bits 15:30 to user's memory	00000000 (DMA length)
TA or PA	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	If IR selected, Input single word from R-bus talker's response to user's memory	no response possible
TA or PA	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	If IB selected, Start input transfer from BT-bus to user's memory	0000 (RBI/user status)
TA	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	If OR selected, Output single word from user's memory to R-bus	0000 (...16 bit data word)
TA	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	If OB selected, Start output transfer from user's memory to BT-bus	0000 (RBI/user status)

Table 1: RBI Interrogation Instruction Set and Actions (see notes on page 11)

Notes for Table 1:

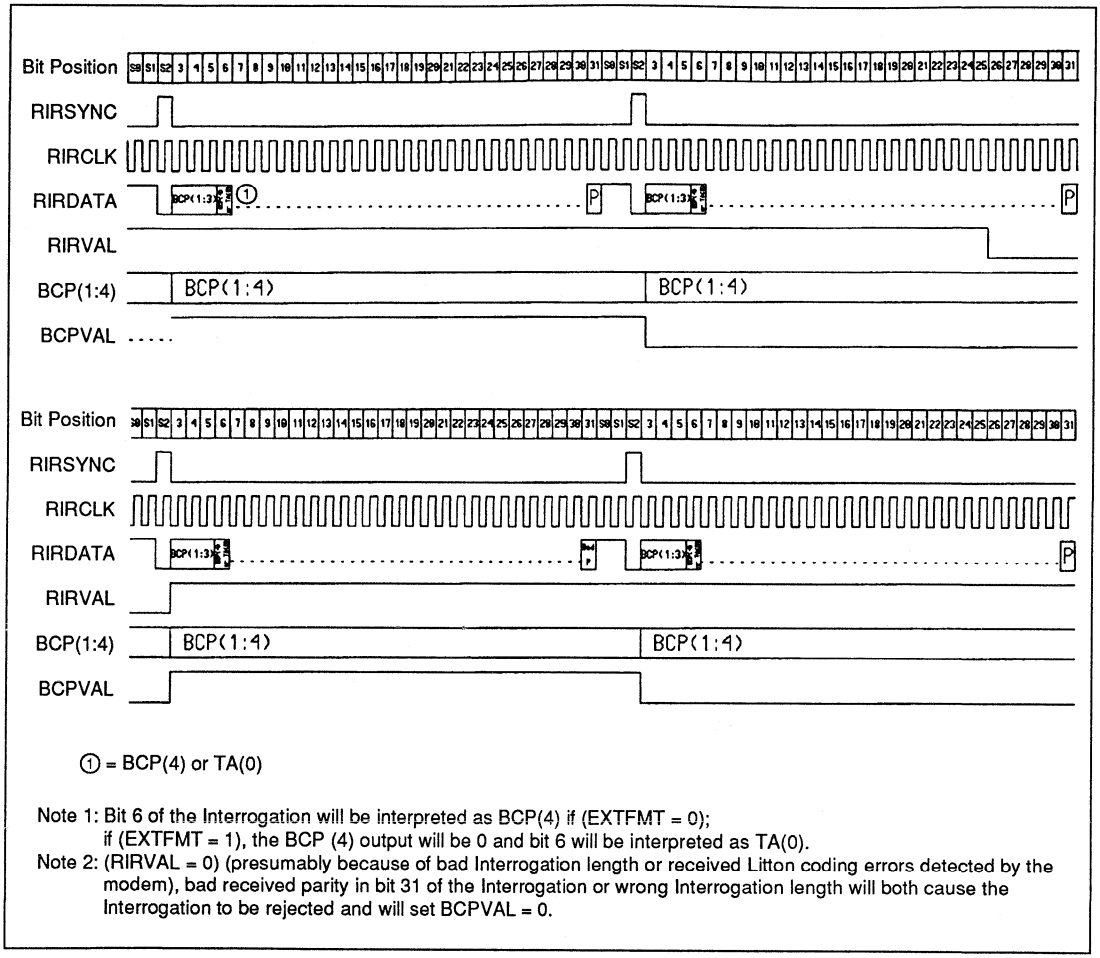
1. Interrogation bits 0:2 are the OBDH Sync pattern, bits 3:6 (Basic Addressing) or 3:5 (Extended Addressing) are BroadCast Pulses, bits 7:11 (Basic Addressing) or 6:11 (Extended Addressing) are the Terminal Address field, bits 12:14 are the Mode field, bits 15:30 are the Instruction field and bit 31 is the Parity bit.
2. An Interrogation containing validity, parity or length errors will not be decoded, will not hence be executed and will not cause a response to be generated. All unused interrogations (i.e. those not listed above, subject to use of PA and BC in Extended Addressing mode as shown in Table 3) will similarly not be decoded, not be executed or cause any response.
3. BroadCast Pulses (contained in Interrogation bits 3:6 (Basic Format) or Interrogation bits 3:5 (Extended Format)) are latched at the end of each Interrogation, regardless of status; they can be externally qualified if desired. BCPVAL indicates the validity of the last Interrogation.
4. Specifying a new Programmed Address (PA) value of 0 causes no change. Specifying 63 causes the PA to be disabled. Other values cause the new PA to be loaded.
5. Specifying a new UCC value of 0 causes the UCC(0:6) output pins to be set to zero. Specifying 127 causes no change. Other values cause the new output value to be set.
6. 'Input from I-bus' means 'write the word from the I-bus to the user at the current DMA address and respond with the new DMA length'; other bus selections should be interpreted similarly.
7. Response bits 0:3 are the Destination Address field (always 0), bits 4:19 are the 16 bit Response Data field (bits 4:7 are '0's for Length responses) and bit 20 is a Stop bit.
8. RBI/user status Response Data field format is: bus selection/direction (bits 4:6), user Service Request (SREQ) pin state (bit 7), Bi-Level status (BIL(0:5)) state (bits 8:13) and PA value (bits 14:19).
9. Broadcast Polling is enabled if the (all '1's) BroadCast address is used and Interrogation bits 29:30 match the pin-programmed Group Identifier inputs, GI(0:1). The (single bit) response is the state of the user Service Request (SREQ) pin; its position is controlled by the Poll Bit Position inputs, PBP(0:4)
10. The current DMA address is used for all Proceed instructions. Proceed instructions received after a DMA Overrun or DMA Error condition has been detected will not be executed nor generate a response until a Read Status or a Reset DMA instruction has been executed. Responses are only generated for Proceed instructions which match the TA.
11. In (IB or OB) BT-bus transfers, a status response is generated for the starting Proceed instruction only.

RBI Instruction Mode	RBI Action	Basic Addressing Mode (EXTAEN = '0') -- RBI-2 Compliant			Extended Addressing Mode (EXTAEN = '1') -- Superset of RBI-2 Access		
Interrogation Bits 12-14		Interrogation is Executed when Addressed via:			Interrogation is Executed when Addressed via:		
		TA	PA	BC	TA	PA	BC
0	Read DMA Address	Yes	No	No	Yes	No	No
	Read DMA Length	Yes	No	No	Yes	No	No
	Read DMA Status	Yes	No	No	Yes	No	No
1	Set Input from I-Bus, PA and UCC	Yes	No	No	Yes	Yes	Yes
	Set Input from R-Bus, PA and UCC	Yes	No	No	Yes	Yes	Yes
	Set Input from BT-Bus, PA and UCC	Yes	No	No	Yes	Yes	Yes
	Reset DMA	Yes	No	No	Yes	Yes	Yes
	Set Output to R-Bus, PA and UCC	Yes	No	No	Yes	No	No
	Set Output tp BT-Bus, PA and UCC	Yes	No	No	Yes	No	No
	Set PA and UCC only	Yes	No	No	Yes	Yes	Yes
	Broadcast (single-bit) Poll	No	No	Yes	No	No	Yes
3	Load DMA start Address	Yes	No	No	Yes	Yes	Yes
4	Load DMA Length	Yes	No	No	Yes	Yes	Yes
7	Proceed (if Input from I-Bus set)	Yes	Yes	No	Yes	Yes	Yes
	Proceed (if Input from R-Bus set)	Yes	Yes	No	Yes	Yes	Yes
	Proceed (if Input from BT-Bus set)	Yes	Yes	No	Yes	Yes	Yes
	Proceed (if Output to R-Bus set)	Yes	No	No	Yes	No	No
	Proceed (if Output to BT-Bus set)	Yes	No	No	Yes	No	No

Notes: TA = (5 bit or 6 bit) hard-wired Terminal Address
PA = (5 bit or 6 bit) Programmable Address, set via Terminal Address only
BC = (5 bit or 6 bit) all-'1's dedicated Broadcast Address
Setting the PA to all-'1's causes it to be considered as invalid; requesting it to be set to all-'0's causes it to remain unchanged.
All TA, PA and BC comparisons are conducted to 5 bit or 6 bit precision depending on the current choice of Standard or Extended addressing selected using the EXTFMT pin.
'Yes' indicates that an operation is valid and will be executed when addressed using that particular addressing mode.
'No' indicates that an operation is not valid and will not be executed when addressed using that particular addressing mode.

Table 2: Instruction Validity in both RBI Addressing Modes

RBI TIMING

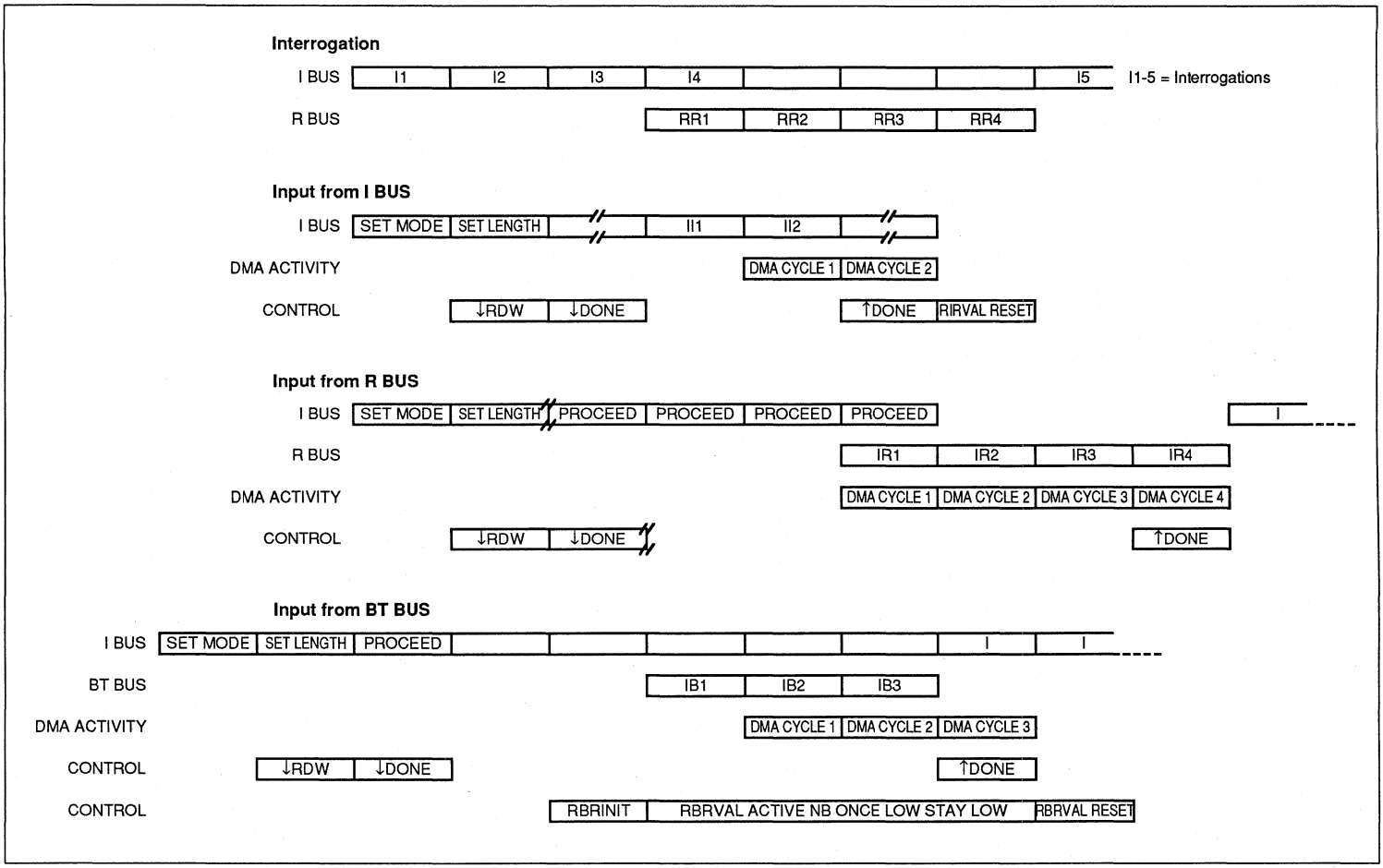


Note 1: Bit 6 of the Interrogation will be interpreted as BCP(4) if (EXTFMT = 0);
if (EXTFMT = 1), the BCP (4) output will be 0 and bit 6 will be interpreted as TA(0).
Note 2: (RIRVAL = 0) (presumably because of bad Interrogation length or received Litton coding errors detected by the modem), bad received parity in bit 31 of the Interrogation or wrong Interrogation length will both cause the Interrogation to be rejected and will set BCPVAL = 0.

Figure 10: BroadCast Pulse and BCP Validity Waveforms

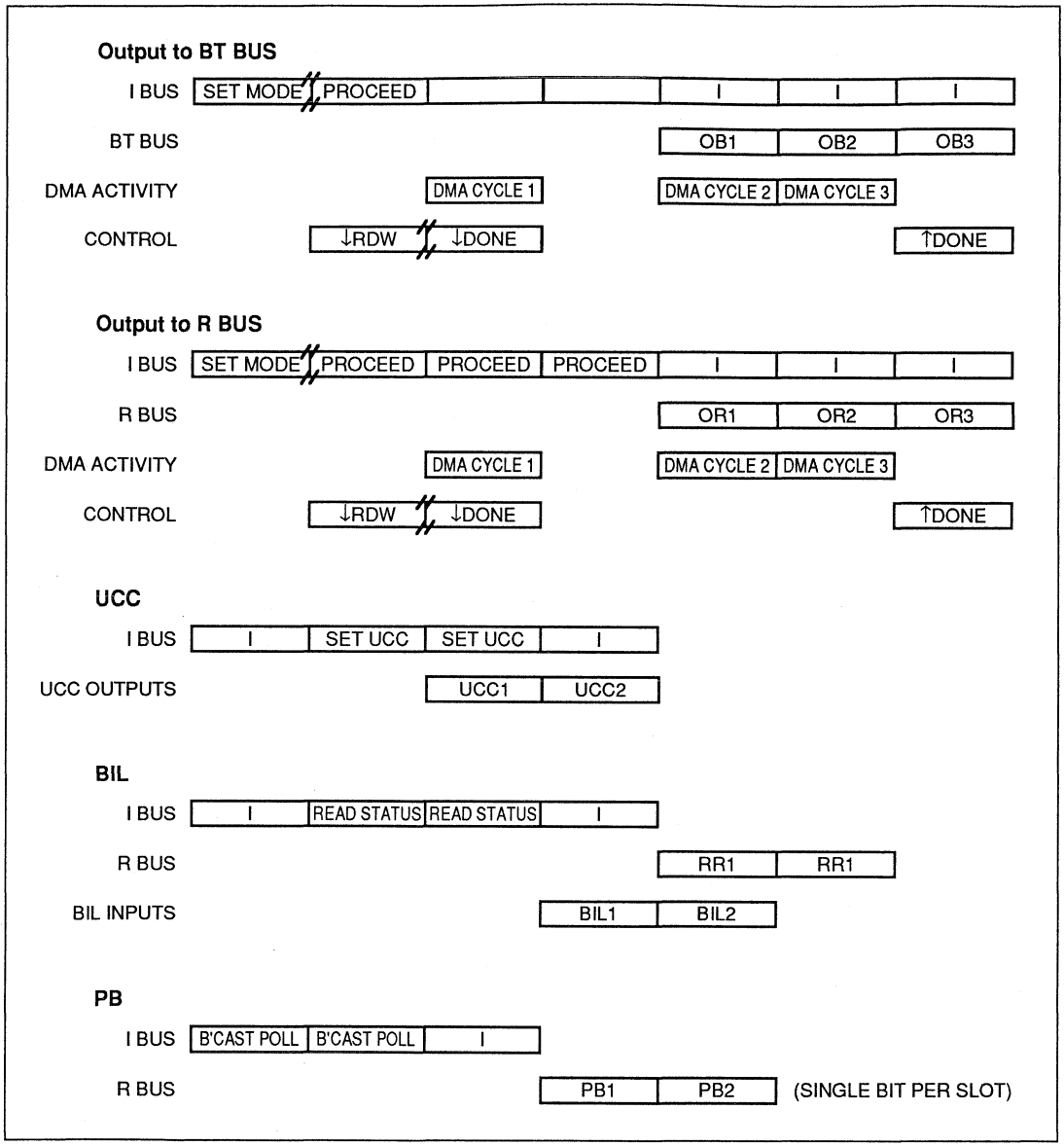
Figures 11 and 12 show 'slot'-level activity to be expected on the OnBoard Data Handling Bus DBI interface. The timing resolution shown for control signals is also shown at the 'slot' level for convenience; for more detail see Figures 13 to 18. The exact timing of DMA operations and control signals associated with them will depend upon response to the DMA Request (DMARn) signal by external circuitry (typically a microprocessor or a DMA Arbiter) and the resulting timing of the associated DMA Acknowledge (DMAKn) signal.

Note that RBI operation in general is determined by more than one clock signal - RIRCLK, RRRCLK and RBRCLK clock edges used to capture and generate all signals on the DBI interface and OSC clock edges used to determine the timing of all signals on the CPU interface.



Note 1: I = Arbitrary Interrogations

Figure 11: 'Slot'-level activity for basic interrogation and Response stream and all Input transfer modes (II, IR and IB)



Note 1: I = Arbitrary Interrogations

Figure 12: 'Slot'-level activity for all Output transfer modes (OR and OB) and for system level features (User Control Command reception, Bi-Level Status read and Broadcast Poll response)

Figures 13 to 17 show more accurate DBI 'slot'-level timings during each type of transfer (i.e. during II, IR, OR, IB and OB mode transfers). Figure 18 shows similar timings for User Control Command and Bi-Level status register and Broadcast Poll operations. More detail on the timing of CPU interface signals can be found in Figures 19 to 22.

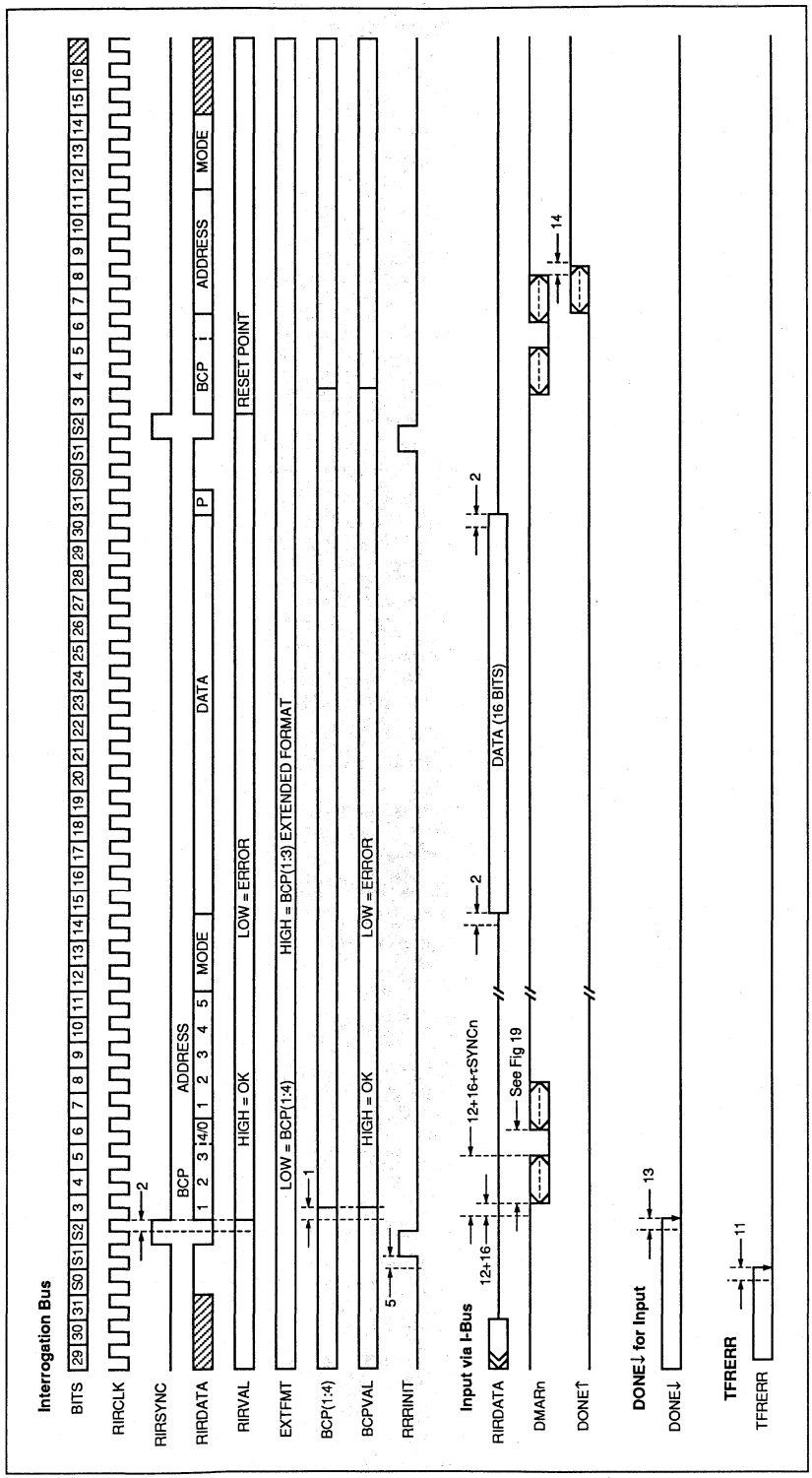


Figure 13: 'Timing diagrams for data reception from the Interrogation bus in the 'Input from I-Bus' (II) mode

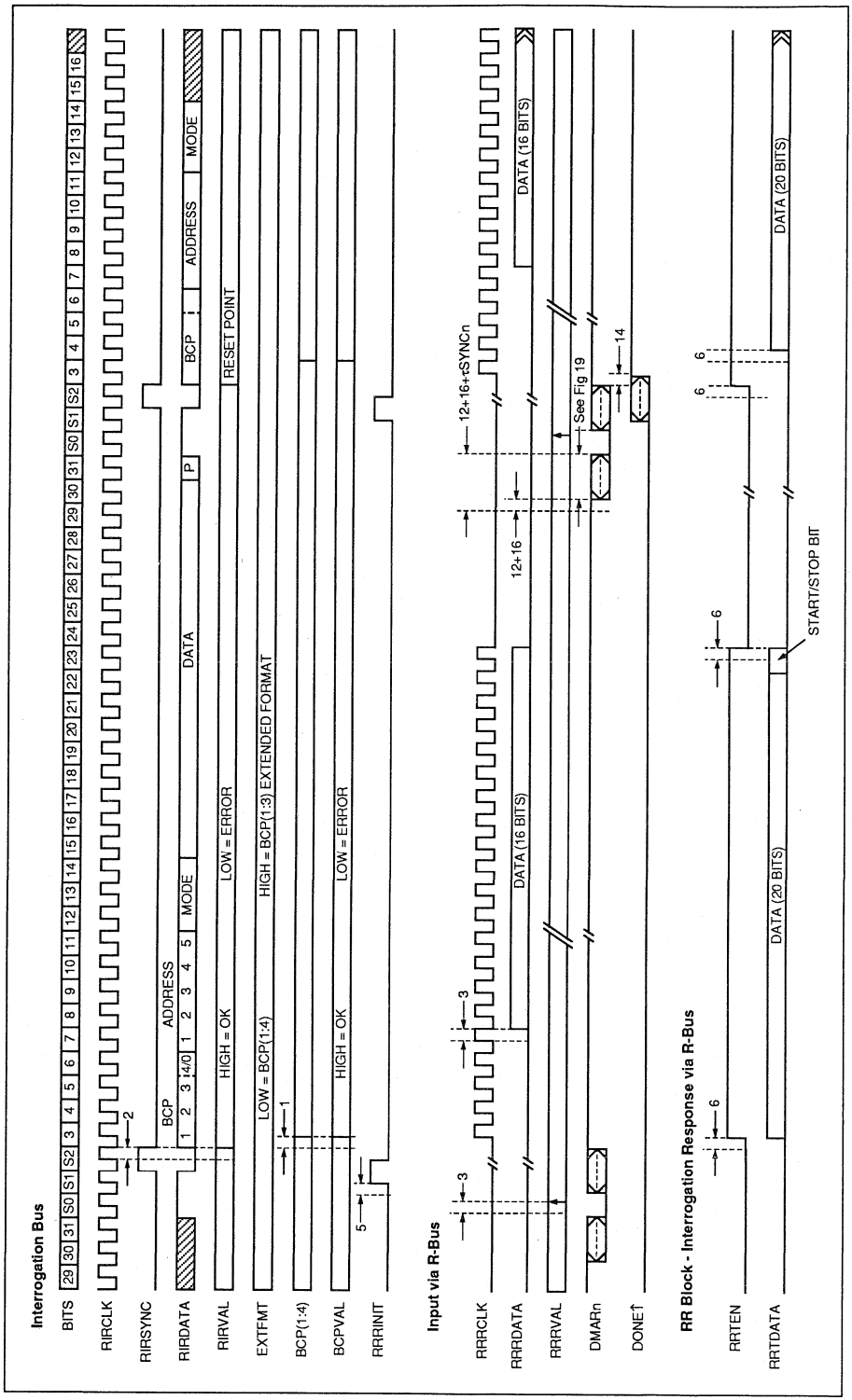


Figure 14: 'Timing diagrams for data reception from the Response bus in the 'Input from R-bus' (IR) mode

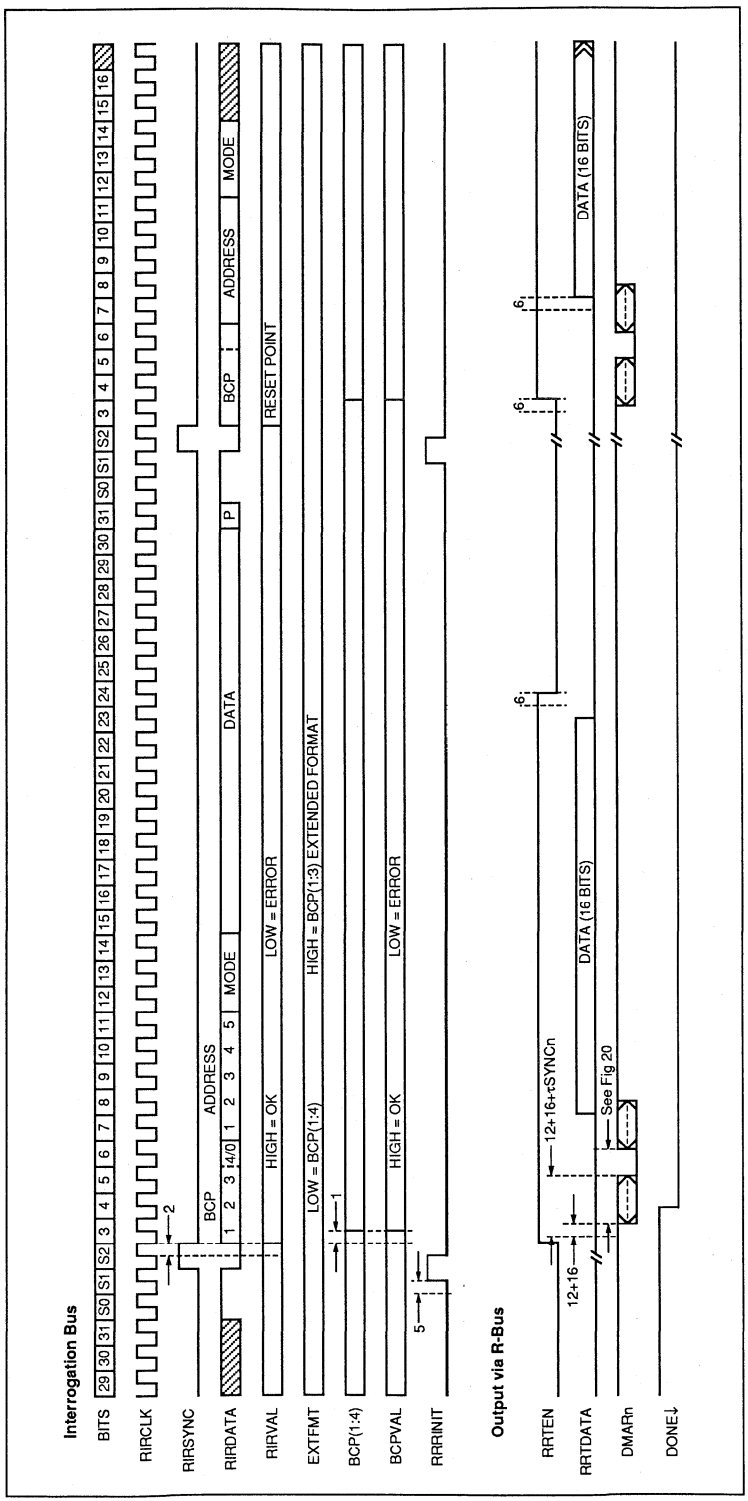


Figure 15: 'Timing diagrams for data transmission to the Response bus in the 'Output to R-bus' (OR) mode

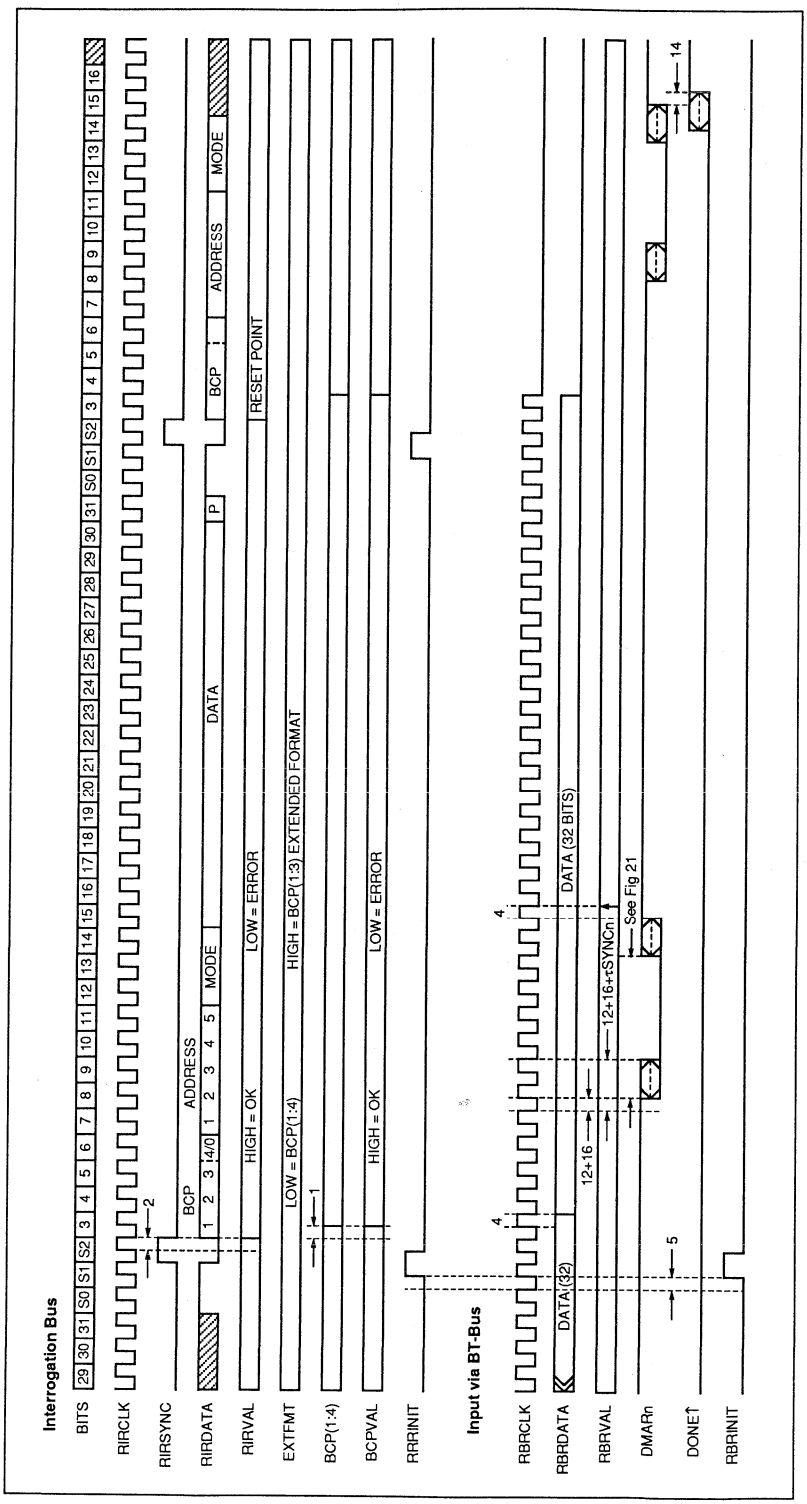


Figure 16: 'Timing diagrams for data reception from the Block Transfer bus in the 'Input from BT-bus' (IB) mode

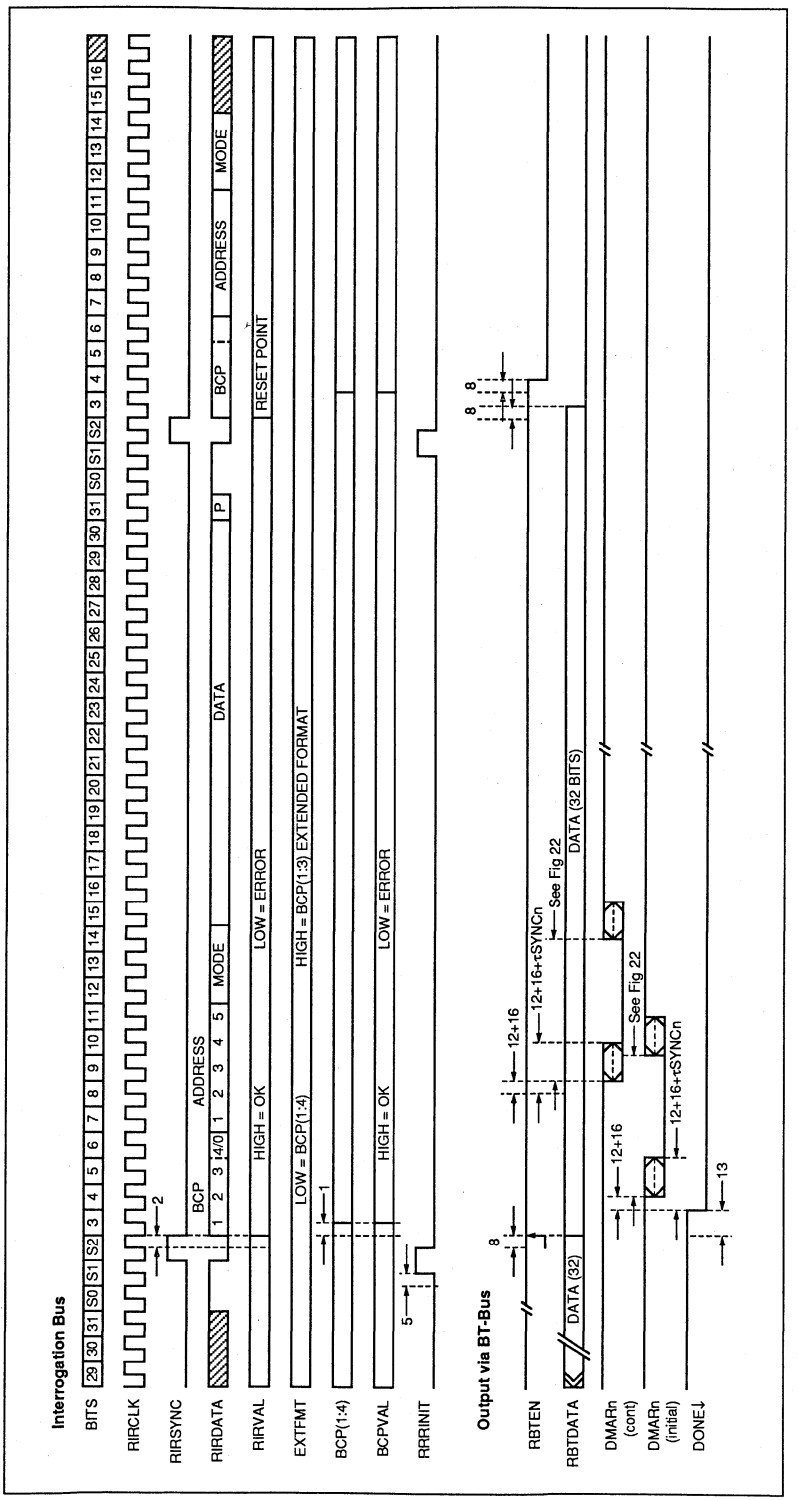


Figure 17: 'Timing diagrams for data transmission to the Block Transfer bus in the 'Output to BT-bus' (OB) mode

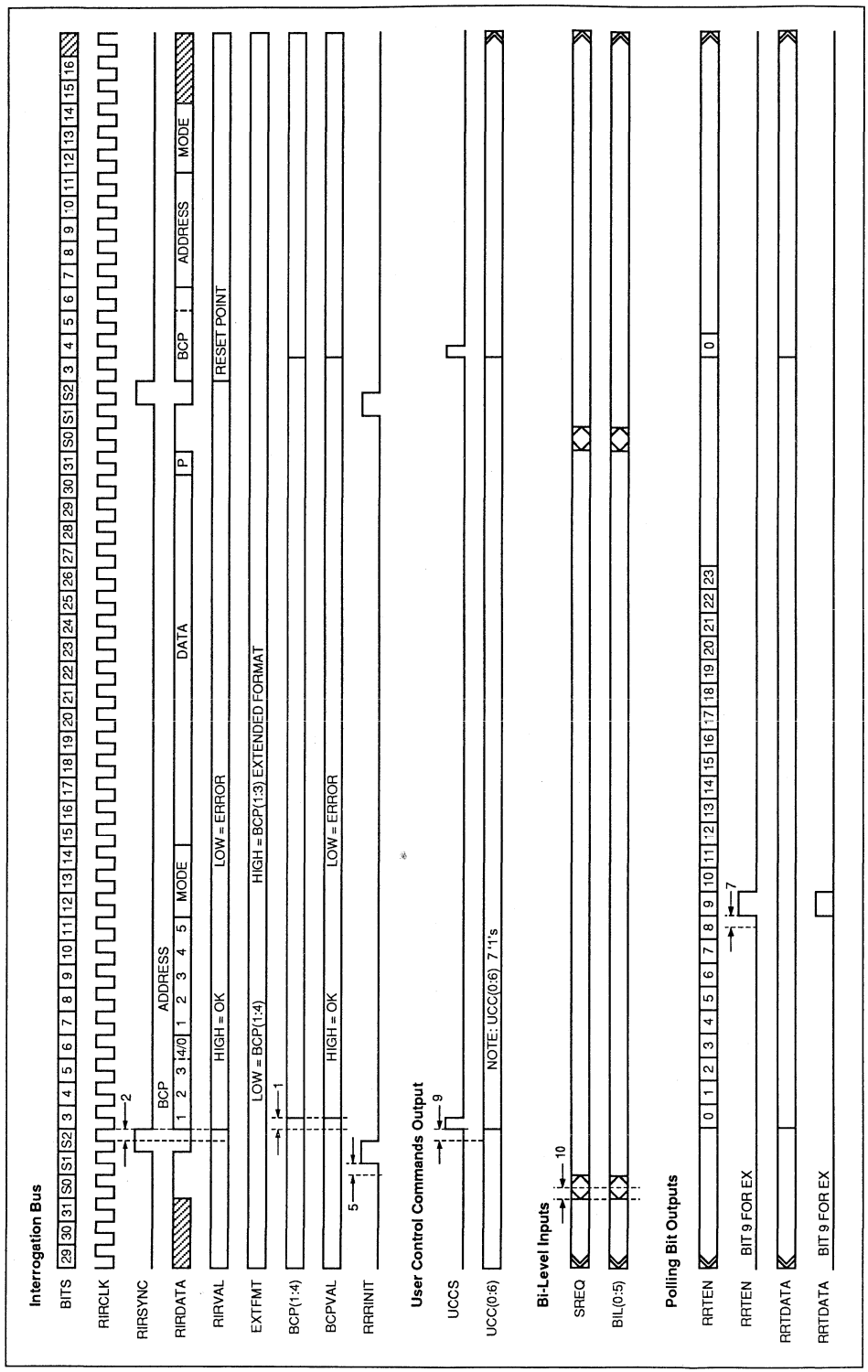


Figure 18: Timing diagrams for system level features (User Control Command reception, Bi-Level Status read and Broadcast Poll response)

The need for the RBI to perform a DMA operation is indicated to the system's DMA Arbiter by asserting the active low DMARn output pin. When DMA operations are enabled, permission to perform the DMA operation is indicated by the arbiter using a low level on the RBI's active low DMAKn input pin. Once the DMA operation has been completed, DMARn is de-asserted by the RBI; the arbiter responds by deasserting DMAKn. DMAKn is interpreted by the RBI as permission to drive the tri-state output busses; premature removal of DMAKn will cause DMA transfer errors.

Figures 19 to 22 show 16 or 32 bit read or write DMA cycles during each type of transfer (i.e. during II, IR, OR, IB and OB mode transfers) where wait states do not need to be inserted (i.e. where each machine cycle is completed in 5 OSC cycles). Figure 23 shows a 16 bit DMA write cycle (II or IR mode transfer) where 5 wait states need to be inserted.

The exact timing of the start of each DMARn pulse is determined by two clock signals - an RIRCLK edge at a specific point in the Interrogation (at which the DMA transfer is instigated) and an OSC edge (to which the generated pulse is synchronised). The exact timing of the end of each DMARn pulse is determined by the timing of DMAKn, but is also synchronised to an OSC edge. Note that the DONE signal is asserted in response to completion of the last DMA transfer.

The generation of all CPU signals is related to the OSC clock. All signals which are generated on the CPU-side of the MA28138 are intended to mimic those of an MAS281 microprocessor. In addition, provision has been made for two extra control signals:

- an active low DMA Data Direction signal (DMADDn), intended to turn-around a bidirectional buffer between the MA28138 and the system back-plane
- a system-level replacement for the SYNCn pulse (SYNDn) which should be OR-ed with SYNCn.

Note that on MAS281 systems a bus time-out fault will normally occur if the delay from DMARn↓ to DMAKn↓ exceeds 32μs.

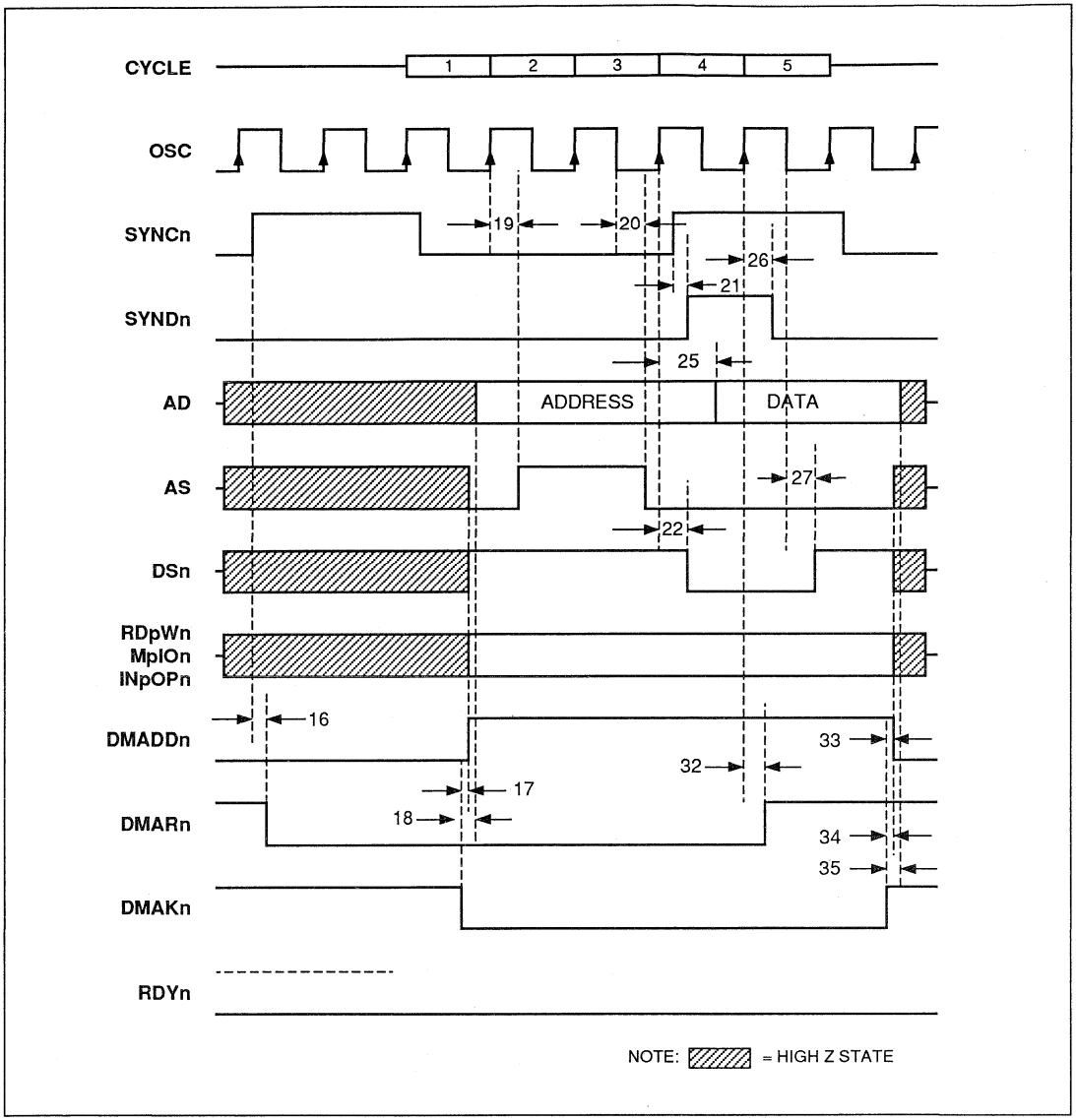


Figure 19: 'Input from I-bus' (II) and 'Input from R-bus' (IR) mode DMA Controller 16 bit write cycle (based on a 5 OSC machine cycle)

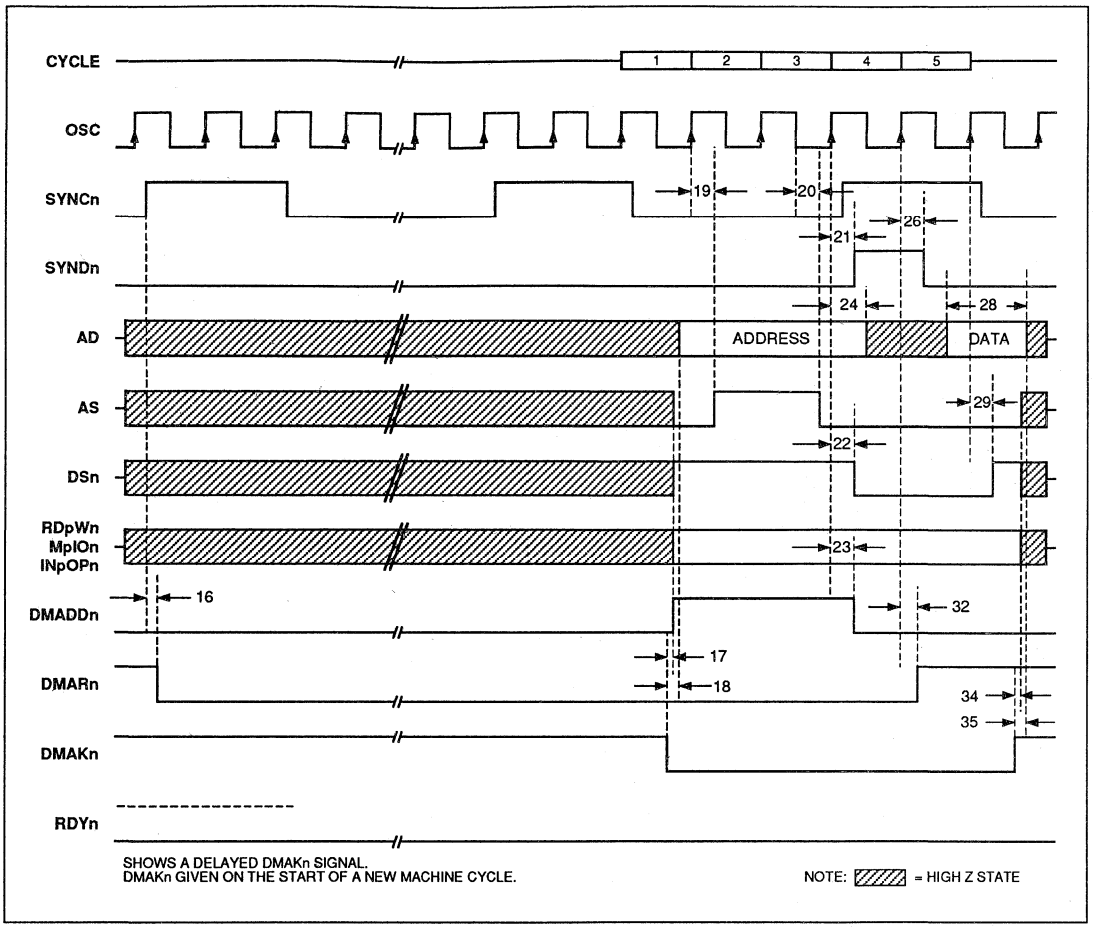


Figure 20: 'Output to R-bus' (OR) mode DMA Controller 16 bit read cycle (based on a 5 OSC machine cycle)

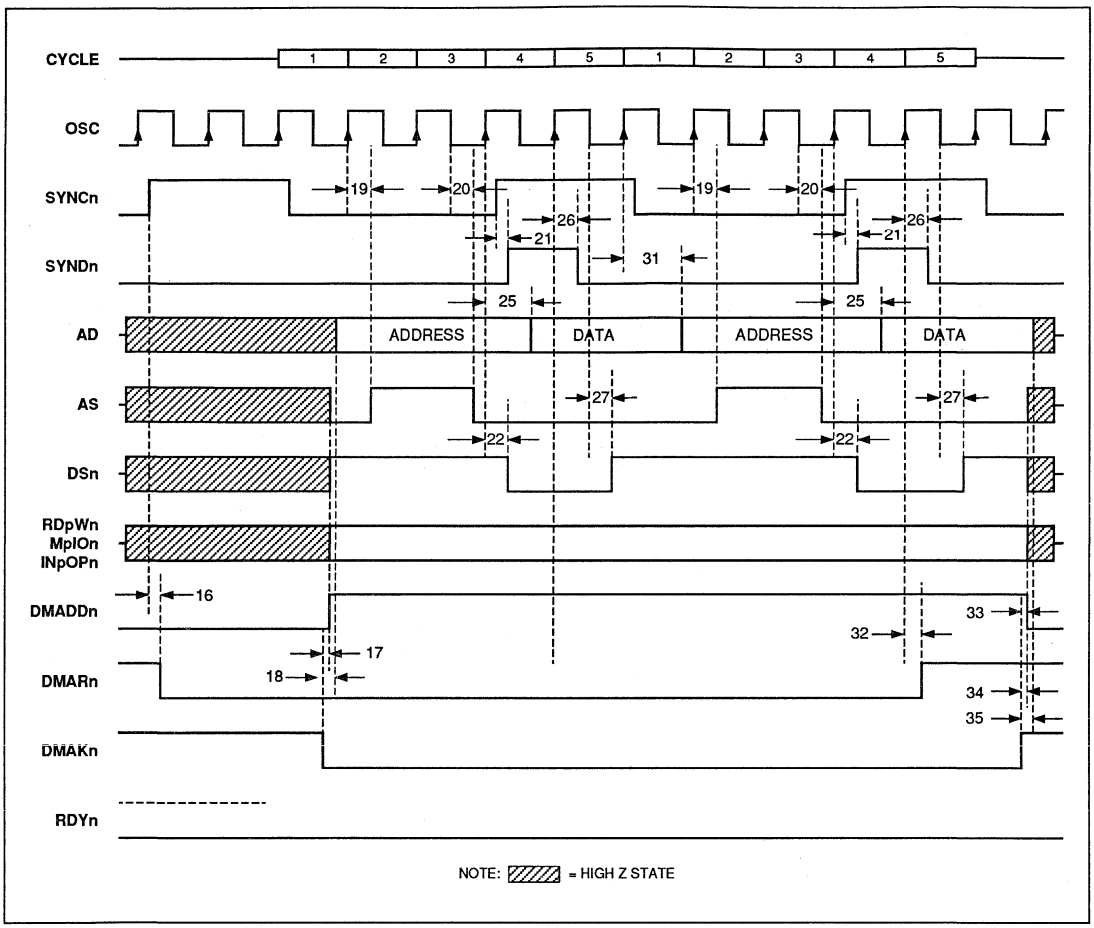


Figure 21: 'Input from BT-bus' (IB) mode DMA Controller 32 bit write cycle (based on a 5 OSC machine cycle)

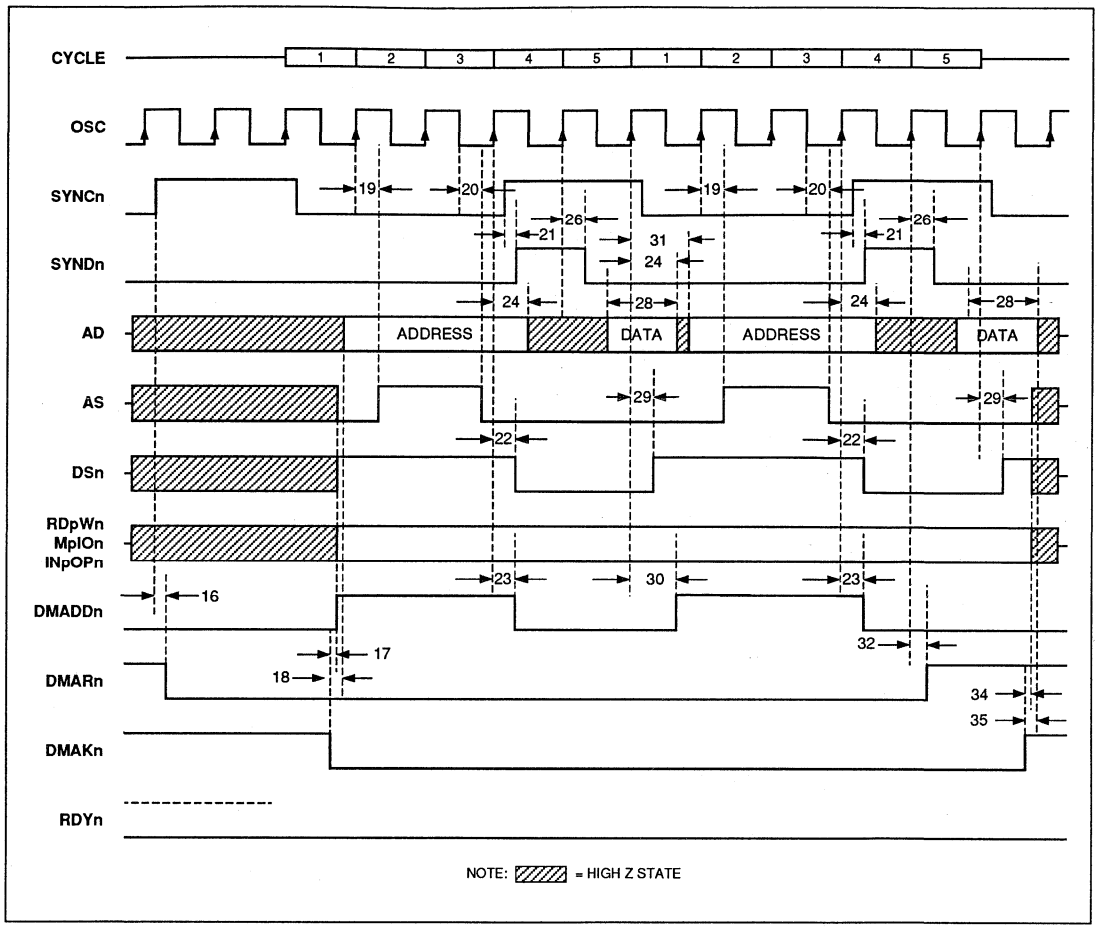


Figure 22: 'Output to BT-bus' (OB) mode DMA Controller 32 bit read cycle (based on a 5 OSC machine cycle)

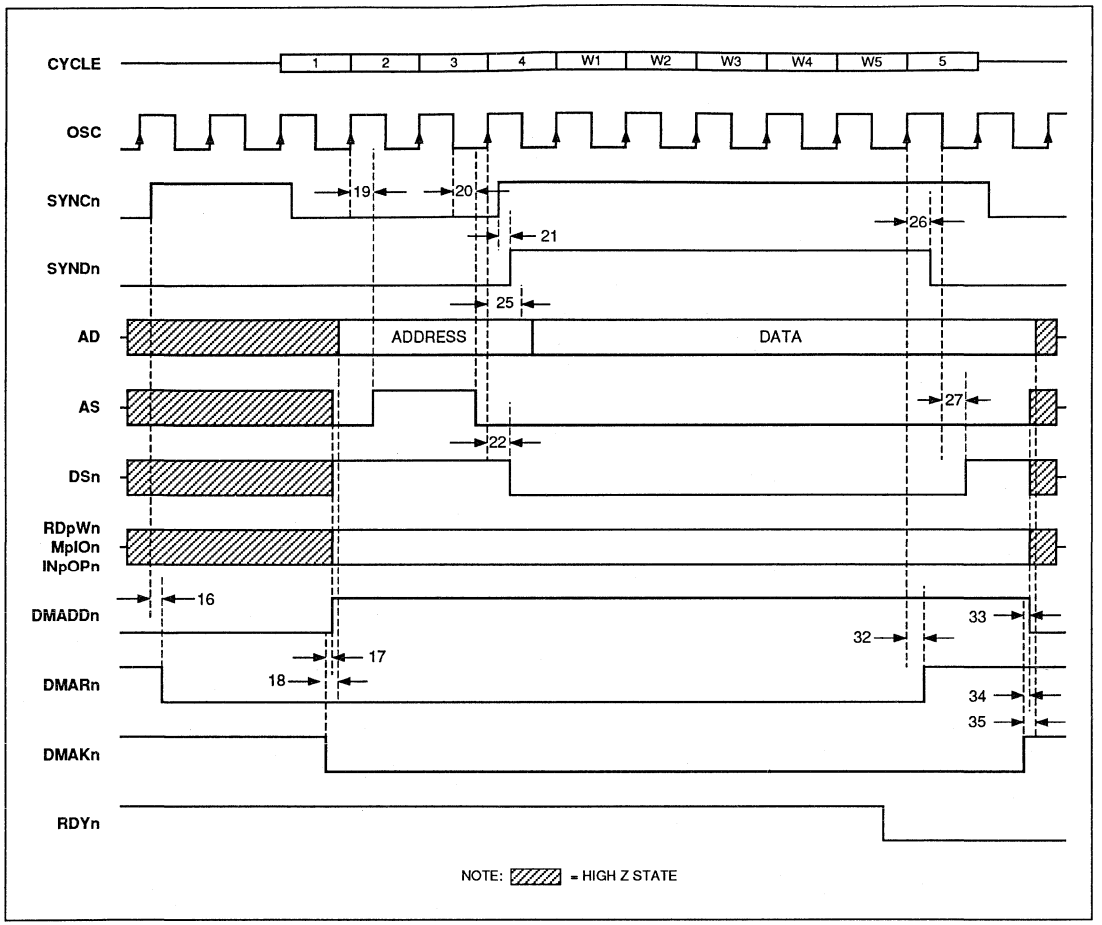


Figure 23: 'Input from I-bus' (II) and 'Input from R-bus' (IR) mode DMA Controller 16 bit write cycle (based on a 10 OSC machine cycle inserting 5 wait states)

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 3: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IHT}	TTL Input High Voltage	-	2.0	-	V_{DD}	V
V_{ILT}	TTL Input Low Voltage	-	V_{SS}	-	0.8	V
V_{IHC}	CMOS Input High Voltage	-	0.8V_{DD}	-	V_{DD}	V
V_{ILC}	CMOS Input Low Voltage	-	V_{SS}	-	0.2V_{DD}	V
V_{OH}	Output High Voltage	I_{OH} = -1mA	V_{DD}-0.5	-	-	V
V_{OL}	Output Low Voltage	I_{OL} = 4mA	-	-	0.4	V
I_{PDL}	Input Pull-down Current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-25	-	25	µA
I_{PDH}	Input Pull-down Current	V_{DD} = 5.5V, V_{IN} = V_{DD}	25	-	400	µA
I_{PUL}	Input Pull-up Current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-400	-	-25	µA
I_{PUH}	Input Pull-up Current	V_{DD} = 5.5V, V_{IN} = V_{DD}	-25	-	25	µA
I_L	Input Leakage Current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-10	-	10	µA
I_{OZL}	Output Leakage Current	V_{DD} = 5.5V, V_{OUT} = V_{SS}	-30	-	30	µA
I_{OZH}	Output Leakage Current	V_{DD} = 5.5V, V_{OUT} = V_{DD}	-30	-	30	µA
I_{DD1}	Static Power Supply Current	V_{DD} = 5.5V	-	0.02	8	mA
I_{DD2}	Dynamic Power Supply Current	f = 1MHz, V_{DD} = 5.5V	-	6	20	mA

Notes: 1. V_{DD} = 5V ±10% over full temperature range.
2. Total dose radiation not exceeding 10^5 Rads (Si).
3. Mil-Std-883, method 5005, subgroups 1, 2, 3.
4. All outputs are suitable for TTL/CMOS drive.
5. Electro-Static Discharge protection is provided for all pins.
6. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.
7. Input and I/O leakage measurements are guaranteed but not tested at -55°C.

Table 4: DC Characteristics

No.	Parameter	Min	Max	Units
T1	RIRCLK ↓ to BCP (1:4), BCPVAL valid			
T2	RIRSYNC, RIRDATA, RIRVAL to RIRCLK ↑ (setup/hold)			
T3	RRRDATA, RRRVAL to RRRCLK ↑ (setup/hold)			
T4	RBRDATA, RBRVAL to RBRCLK ↑ (setup/hold)			
T5	RIRCLK ↓ to RRRINIT, RBRINIT valid			
T6	RIRCLK ↓ to RRTEN, RRTDATA valid (Normal response data)			
T7	RIRCLK ↓ to RRTEN, RRTDATA valid (Bit Polling response)			
T8	RIRCLK ↓ to RBTEN, RBTDATA valid			
T9	RIRCLK ↓ to UCC (0:6), UCCS valid			
T10	BIL (0:5), SREQ to RIRCLK ↑ (setup/hold)			

Table 5: OBDH DBI Interface Characteristics (TBD)

No.	Parameter	Min	Max	Units
T11	RIRCLK ↓ to TFERR valid			
T12	RIRCLK ↓ to SYNCn ↑ (setup/hold)			
T13	RIRCLK ↓ to DONE ↓			
T14	DMARn ↑ to DONE ↑			
T15	RIRCLK ↓ to DONE ↑			

Table 6: DMA Interface Characteristics (TBD)

No.	Parameter	Min	Max	Units
T16	SYNCn ↑ to DMARn ↓			
T17	DMAKn ↓ to AS, DSn, RDpWn, MpIOn, INpOPn valid and DMADDn ↑			
T18	DMAKn ↓ to Address valid			
T19	OSC ↑ to AS ↑			
T20	OSC ↓ to AS ↓			
T21	SYNCn ↑ to SYNDn ↑			
T22	OSC ↑ to DSn ↓			
T23	OSC ↑ to DMADDn ↓			
T24	OSC ↑ to AD High Impedance state			
T25	OSC ↑ to Data valid			
T26	OSC ↑ to SYNDn ↓			
T27	OSC ↓ to DSn ↑			
T28	DSn ↑ to Data (setup/hold)			
T29	OSC ↑ to DSn ↑			
T30	OSC ↑ to 2nd DMADDn ↑			
T31	OSC ↑ to 2nd 16 bit Address valid			
T32	OSC ↑ to DMARn ↑			
T33	DMAKn ↑ to DMADDn ↓			
T34	DMAKn ↑ to AS, DSn, RDpWn, MpIOn, INpOPn High Impedance state			
T35	DMAKn ↑ to AD High Impedance state			
T36	RDYn ↑ to OSC ↑ (setup/hold)			

Notes: 1. V_{DD} = 5V±1-% over full temperature range.
2. Total dose radiation not exceeding 10^5Rads(Si).
3. Tables 5, 6 and 7 contain Mil-Std-883, method 5005, subgroups 9, 10 and 11.

Table 7: Microprocessor Bus Interface Characteristics (TBD)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

NOTE 1: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Table 8: Capacitance

Symbol	Parameter	Conditions
F_T	Functionality	V_{DD} = 4.5 - 5.5V, FREQ = 1 MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} = V_{OH} = V_{DD}/2$ TEMP = -55°C to +125°C, GPS Pattern Set Mil-Std-883 5005 subgroups 7, 8A, 8B

Table 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 4 at +25°C
2	Static characteristics specified in Table 4 at +125°C
3	Static characteristics specified in Table 4 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 5, 6 and 7 at +25°C
10	Switching characteristics specified in Tables 5, 6 and 7 at +125°C
11	Switching characteristics specified in Tables 5, 6 and 7 at -55°C

Table 10: Definition of Subgroups

RBI PINLIST AND DESCRIPTIONS

Pin	Signal	Type	Description	
55, 113	V_{DD}	P/S	+5 volt nominal power supply. Connect all pins	Power
14, 47, 80	V_{SS}	P/S	Power and signal ground. Connect all pins	
102	MRSTn	I (CS) (PD)	Master reset active low	RESET
37-42	TA(0-5)	I	Terminal address to match I-bits 6-11 (table 1)	POLL
43	EXTFMT	I	Extended format: when low TA0 = X	
44	EXTAEN	I (PD)	Enable use of Programmed Address and Broadcast Address with ESA RBI-2 Command Set	
90-91	GI(0-1)	I	Poll group identifier to match I-bits 29-30	
92-96	PBP(0-4)	I	Poll bit position in 24 bit response	
21-36	AD(0-15)	I/O (TTL)	µP address/data bus (5mA output)	Processor Bus
56	AS	O	Address strobe	
57	DSn	O	Data strobe	
58	RDpWn	O	Read when positive, write when negative	
59	MPIOn	O	Memory when positive, I/O when negative	
60	INpOPn	O	Instruction when positive, operand when negative	
61	DMADDn	O	DMA data direction	
62	RDYn	I (TTL) (PD)	Ready	
45	SYNCn	I (TTL)	Sync from µP	
46	OSC	I (TTL)	Oscillator from µP	
63	SYNDn	O	RBI sync during DMA. OR with system sync	
64	DMARn	O	DMA request	DMA
65	DMAKn	I (TTL) (PU)	DMA acknowledge	
88	DONE	O	DMA transfer correct and complete	
89	TFRERR	O	DMA transfer error. RBI has aborted transfer	
66	SREQ	I	User service request	User
67-72	BIL(0-5)	I	User bi-level inputs	
73-79	UCC(0-6)	O	User control commands	
87	UCCS	O	UCC strobe when UCC value changes	
97-100	BCP(1-4)	O	Broadcast pulses 1 to 4 (I-bits 3 to 6)	Broadcast
101	BCPVAL	O	Broadcast pulses valid	
103	RBTEN	O	RBI BT-bus transmitter enable	OBDH DBI
104	RBTDATA	O	RBI BT-bus transmitter data	
105	RBRINIT	O	RBI BT-bus receiver initialisation	
106	RBRVAL	I (PD)	RBI BT-bus receiver validity	
107	RBRDATA	I (PD)	RBI BT-bus receiver data	
108	RBRCLK	I (PD)	RBI BT-bus receiver clock	
109	RRTEN	O	RBI R-bus transmitter enable	
110	RRTDATA	O	RBI R-bus transmitter data	
111	RRRINIT	O	RBI R-bus receiver initialisation	
112	RRRVAL	I (PD)	RBI R-bus receiver validity	
121	RRRDATA	I (PD)	RBI R-bus receiver data	
122	RRRCLK	I (PD)	RBI R-bus receiver clock	
123	RIRVAL	I (PD)	RBI I-bus receiver validity	
124	RIRDATA	I (PD)	RBI I-bus receiver data	
125	RIRCLK	I (PD)	RBI I-bus receiver clock	
126	RIRSYNC	I (PD)	RBI I-bus receiver sync	

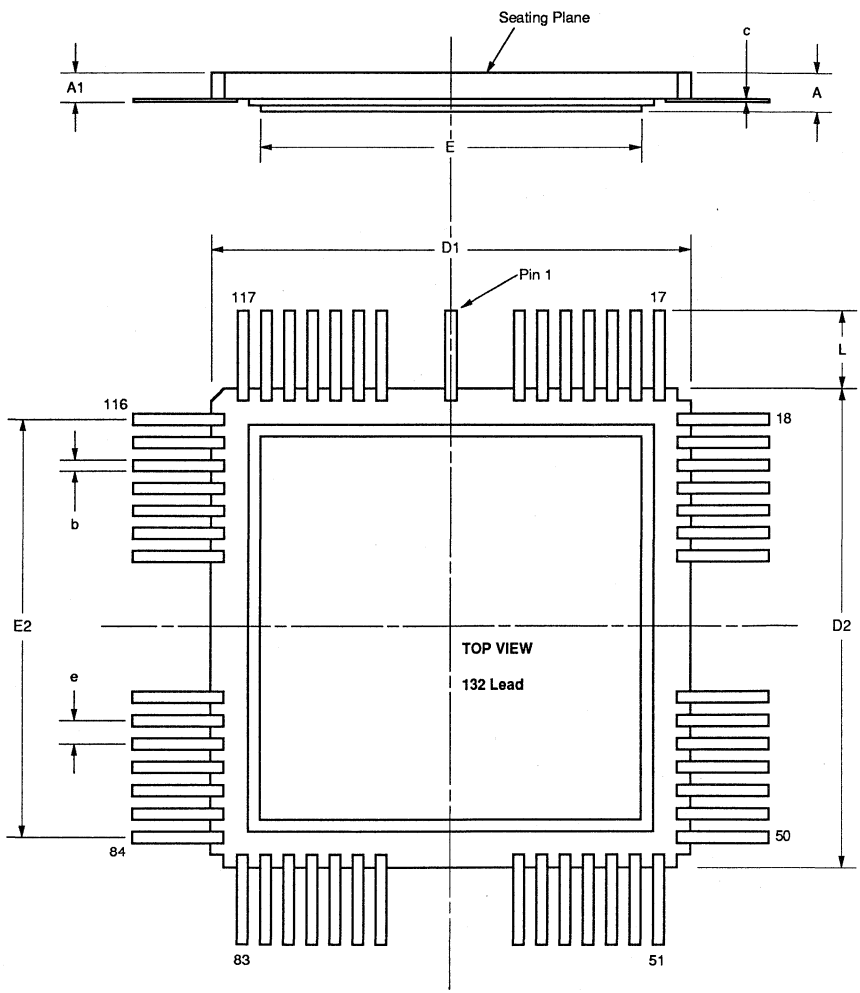
All other pins are used for test during manufacture and must be left unconnected.

Notes: 1. CS means CMOS Schmitt-trigger input.
2. TTL means TTL input levels.
3. Inputs not labelled use CMOS input levels.
4. PU means pull-up resistor.
5. PD means pull-down resistor.
6. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consulation with GPS.

PACKAGE DIMENSIONS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.59	-	-	0.102
A1	1.37	-	1.88	0.054	-	0.074
b	0.23	-	0.33	0.009	-	0.013
c	0.10	-	0.18	0.004	-	0.007
D1, D2	-	-	24.38	-	-	0.960
E	-	-	18.11	-	-	0.713
E2	-	20.32	-	-	0.800	-
e	-	0.63	-	-	0.025	-
L	6.35	-	7.11	0.250	-	0.280

XG533



RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

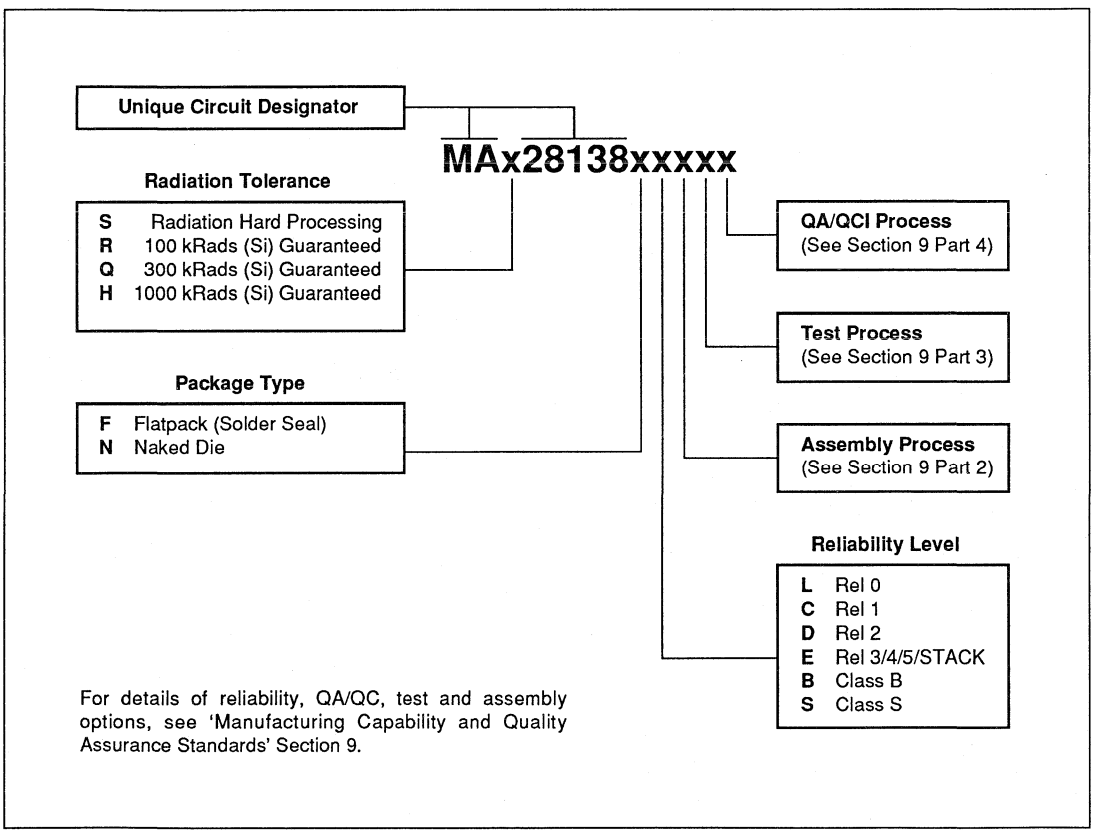
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 11: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

SYNONYMS

ASIC	Application Specific Integrated Circuit
BC	(all '1's) Broadcast Address
BT-bus	Block Transfer Bus
CBR	CTU mode, block transfer bus, receive
CBT	CTU mode, block transfer bus, transmit
CIT	CTU mode, interrogation unit, transmit
CRR	CTU mode, response bus, receive
CTU	Central terminal unit
DBI	Digital bus interface
DBU	Digital bus unit
DMA(C)	Direct Memory Access (Controller)
ESA	European Space Agency
FET	Field effect transistor
FTC	Fault tolerant computer
GPS	GEC Plessey Semiconductors
IB	Input from BT-bus
I-bus	Interrogation bus
ICU	Intelligent control unit
II	Input from I-bus
IR	Input from R-bus
IUB	Internal user bus
MA28138	Remote bus interface (RBI) ASIC
MA28139	OBDH bus terminal (OBT) ASIC
µP	Microprocessor
OB	Output to BT-bus
OBDH	On board data handling
OBT	OBDH bus terminal (MA28139)
OR	Output to R-bus
PA	Programmable Address
PIU	Payload Interface Unit
R-bus	Response bus
RBI	Remote bus interface (MA28138)
RBR	RTU mode, block transfer bus, receive
RBT	RTU mode, block transfer bus, transmit
RIR	RTU mode, interrogation bus, receive
RRR	RTU mode, response bus, receive
RRT	RTU mode, response bus, transmit
RT(U)	Remote terminal (unit)
SBC	Single board computer
TA	(hard-wired) Terminal Address
VLSI	Very large scale integration

MA28139

OBDH BUS TERMINAL

The OBT ASIC will interface any user to the ESA On Board Data Handling bus. Developed under ESA Contract, it conforms to ESA OBDH, Digital Bus Interface and Internal User Bus Standards.

The OBT has 2 separate functions. The first is a 5 channel modem which, on the bus side, provides the digital waveforms necessary to operate the Litton Bus drivers, and receives the outputs of the Litton bus detectors. On the user side, it provides an input / output at Digital Bus Interface level. The second function, internally coupled to the first, provides a multiplexing / demultiplexing function of the DBI signals down to Internal User Bus levels and vectored 16 bit serial register read and write commands (see section 7.2 of ESA standard TTC-B-01). In effect, the second function of the OBT provides the core of an RTU.

The Interrogation and Response bus data streams of the two functions may be either coupled together (in RT mode) or isolated (in CT mode). The device may hence be used as a modem only, an RTU kernel only or as a combined modem and RTU kernel. In RT mode, the Interrogation bus data stream can be observed and the Response bus data from associated devices, such as an MA28138 Remote Bus Interface, can be combined with that from the RTU kernel before being used by the modem circuits to modulate the Response bus. Bi-directional access to the Block Transfer bus is provided in either mode.

When used to interface a central terminal to the OBDH bus, the OBT should be continuously clocked in order to output timing to all users on the I-bus as dummy interrogations from the CT. Commands and telemetry are normally sent on the I and BT busses whilst responses and telemetry normally return on the R and BT busses.

FEATURES

- Radiation Hard
- Low Power Consumption
- Single CMOS-SOS ASIC Implementation
- Latch-up Free
- High SEU Immunity
- Fully Compliant with ESA OBDH, IUB, DBI and RBI Specification
- Contains OBDH Bus Modem and RTU Kernel
- Supports Bi-directional Data Transfer on Response and Block Transfer Bus

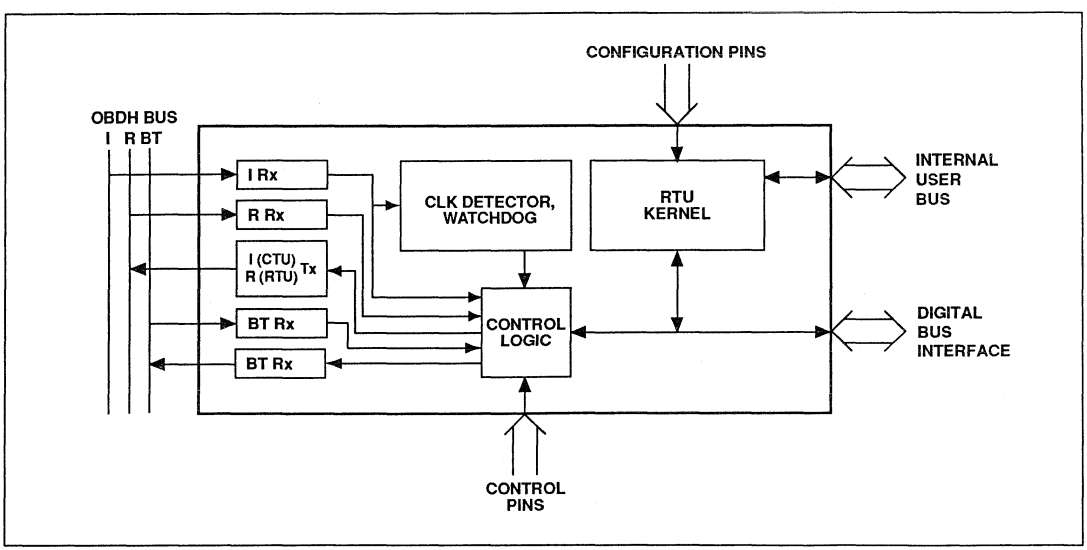


Figure 1: Block Diagram

APPLICATION

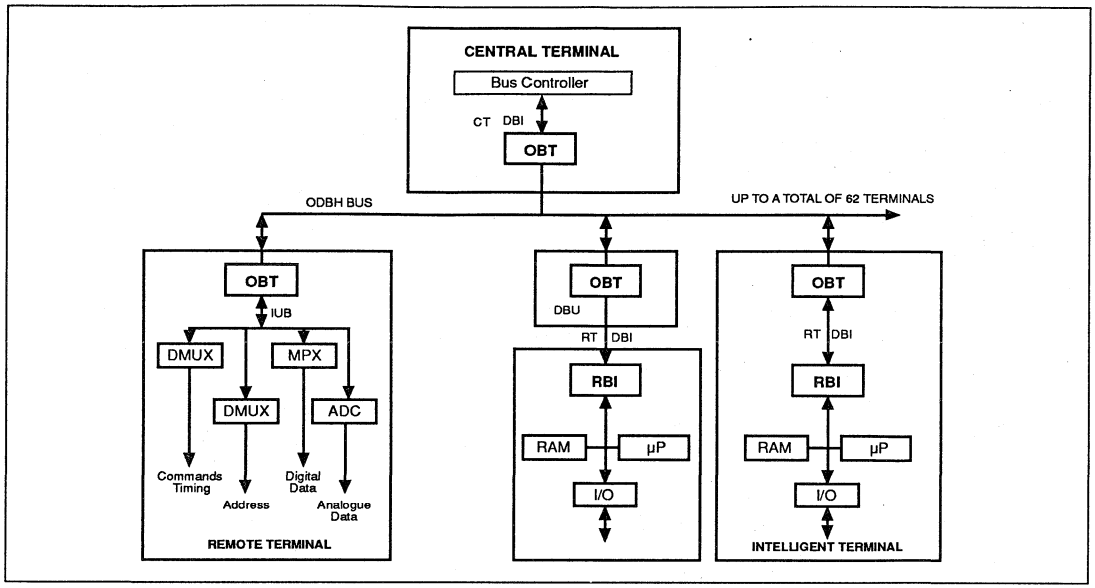


Figure 2: Application

PAYLOAD INTERFACES

The OBT converts the OBDH bus to an Internal User Bus, and a Digital Bus Interface. The OBT can connect OBDH to existing ESA standard payload interfaces such as the MSS PIU (payload interface unit), ICU (intelligent control unit), SBC (single board MIL-STD-1750 computer) or FTC (fault tolerant computer).

The OBT and analogue components/transformers can be integrated in the PIU, ICU, SBC, etc.

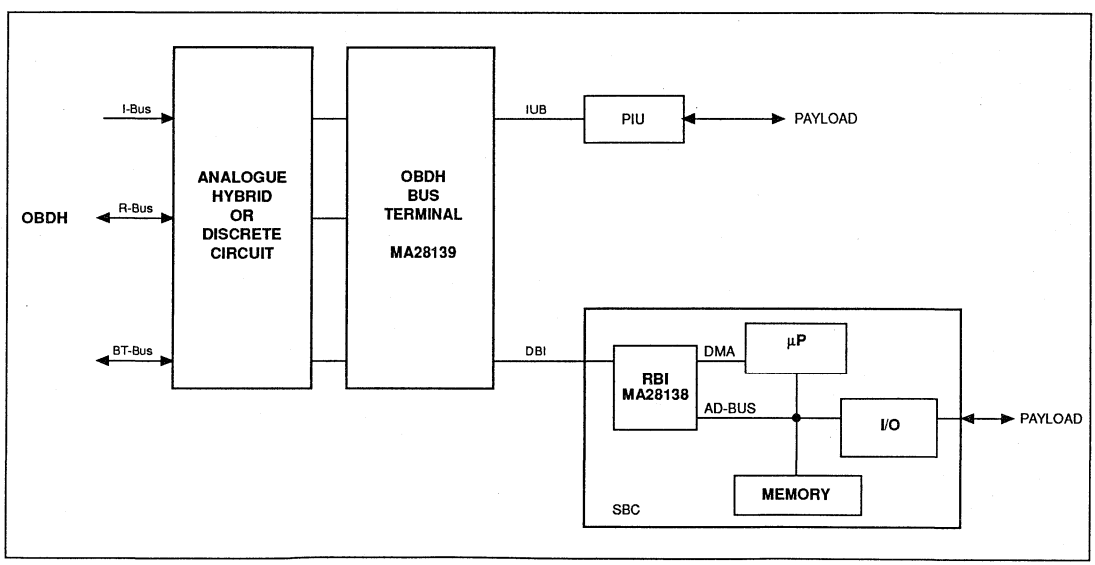


Figure 3: Payload Interface

FUNCTIONAL DESCRIPTION

In RT mode, power up resets the OBT and causes it to deselect both busses. Two watchdog counters monitor the Nominal I-bus and the Redundant I-bus. If either bus becomes active, that bus will be selected. If the selected bus stops, the OBT watchdog times out and resets both the OBT and the user. If both busses become active, the Nominal bus will be selected in preference to the Redundant one. A change in bus selection will always result in the OBT and the user being reset. Responses from the user are always returned on the selected bus. Setting 'SIMUL' high causes both BATs to drive both the Nominal and the Redundant busses irrespective of the current bus selection. The time-out period may be set to any desired number of bits by varying the 'LOSC' frequency. The OBT derives all timing from, and is synchronous with, the selected I-bus. The OBT demodulates the I-bus to the DBI and decodes commands to the IUB.

The CTpRTn mode pin causes the modem circuits and the RTU Kernel to be either cascade or isolated. If CTpRTn is low (RT mode), the RIRSYNC, CLK, DATA and VAL signals are routed to the RTU Kernel and the associated pins act as outputs; responses from the RTU Kernel are ORed with those from the external RRTDATA and RRTEN inputs and can be independently monitored on the DATARRT and ENRRT pins. In this mode any reset caused by the Clock Detector watchdogs is also combined with the power up reset input.

If CTpRTn is high (CT mode), the modem and RTU Kernel functions are isolated to permit the device to be used as either a modem within the CTU or an RTU Kernel interfacing to an external modem where the RIRSYNC, CLK, DATA and VAL pins act as inputs. The right-hand multiplexer bank is switched to the upper position so that the CT drives the OBDH via the CIT and CBT (if used) pins and receives responses/telemetry via the CRR and CBR (if used) pins. Note: in CT mode, BAT1 must be connected to the I-busses.

In RT mode, the CITSEL, MOD, CLK, SYNC and INV pins are disabled and the clocks are supplied by the I-bus BAR in response to the selected bus. In CT mode, the Clock Detector is functional and drives the TIMEOUTn pin but is unable to cause internal reset on time-out; in this mode the CT must supply all clocks and select the operational bus.

The changes depending upon selection of RT mode or CT mode with the CTpRTn pin are defined in the table below:

Functional Signal	**CT Mode Source (CTpRTn = '1')**	**RT Mode Source (CTpRTn = '0')**
BAT1, 2 modulation clock	CITMOD input pin	Recovered R2F
BAT1, 2 data clock	CITCLK input pin	Recovered RIRCLK
BAT1 data input	RRTDATA input pin	RRTDATA OR DATARRT (RTU Kernel)
BAT1 tx enable	'1'	RRTEN OR DATAEN (RTU Kernel)
BAT1 sync code tx enable	CITSYNC input pin	'0'
BAT1 bit invalidate tx enable	CITINV input Pin	'0'
BAT1, 2 bus selection	CITSEL and SIMUL input pins	Detected active bus and SIMUL input pin
BAT2 data input	RBTDATA input Pin	RBTDATA input pin
BAT2 tx enable	RBTEN input pin	RBTEN input pin
BAT1, 2, BAR1, 2, 3 reset	MRSTn input pin	TIMEOUTn AND MRSTn input pin
RIRSYNC, CLK, DATA, VAL pin direction	outputs	inputs
BAT/BAR and RTU Kernel coupling	separated	coupled

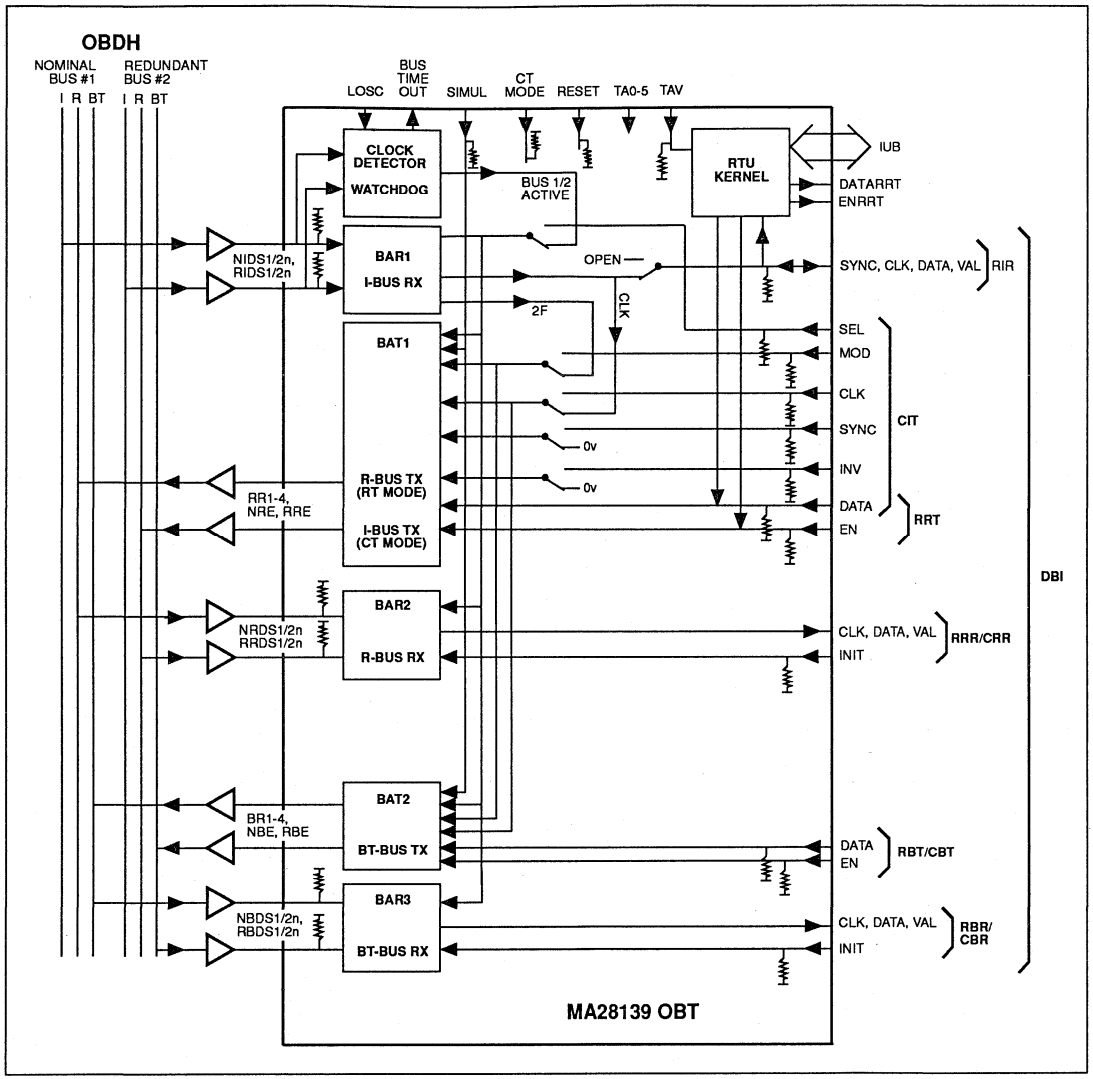
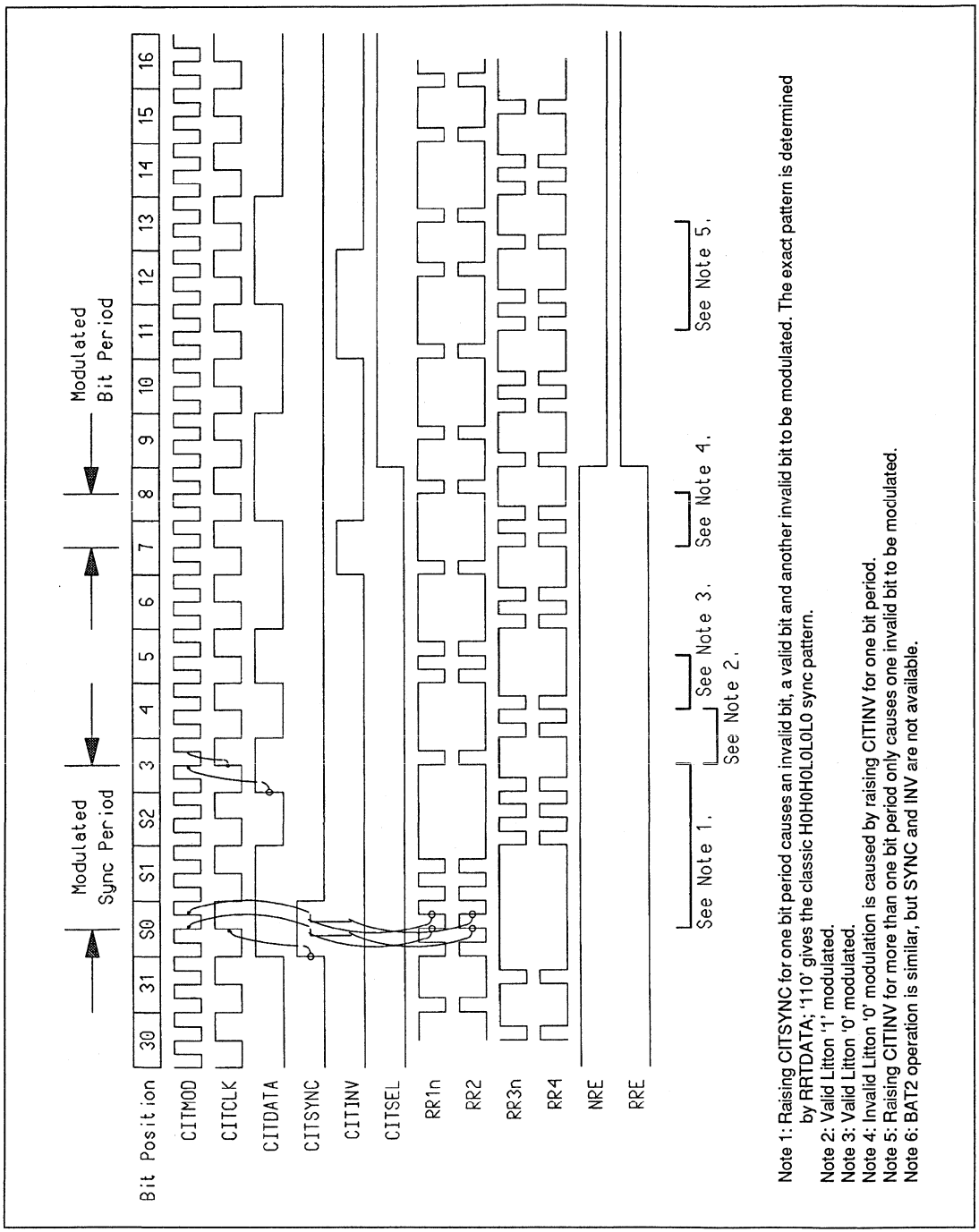


Figure 4: Architecture

Note: Switches in lower position - RT mode
Switches in upper position - CT mode

MODEM Modulation Waveforms are compliant with ESA document THB/Apo/KZ/1386/av. Waveforms indicating the operation of BAT1, 2 and BAR1, 2, 3 in both the CT and RT modes are shown in Figures 5 to 8.



Note 1: Raising CITSYNC for one bit period causes an invalid bit, a valid bit and another invalid bit to be modulated. The exact pattern is determined by RRTDATA; '110' gives the classic H0H0H0L0L0L0 sync pattern.
Note 2: Valid Litton '1' modulated.
Note 3: Valid Litton '0' modulated.
Note 4: Invalid Litton '0' modulation is caused by raising CITINV for one bit period.
Note 5: Raising CITINV for more than one bit period only causes one invalid bit to be modulated.
Note 6: BAT2 operation is similar, but SYNC and INV are not available.

Figure 5: CT Mode Bus Adaptor Transmitter Waveforms

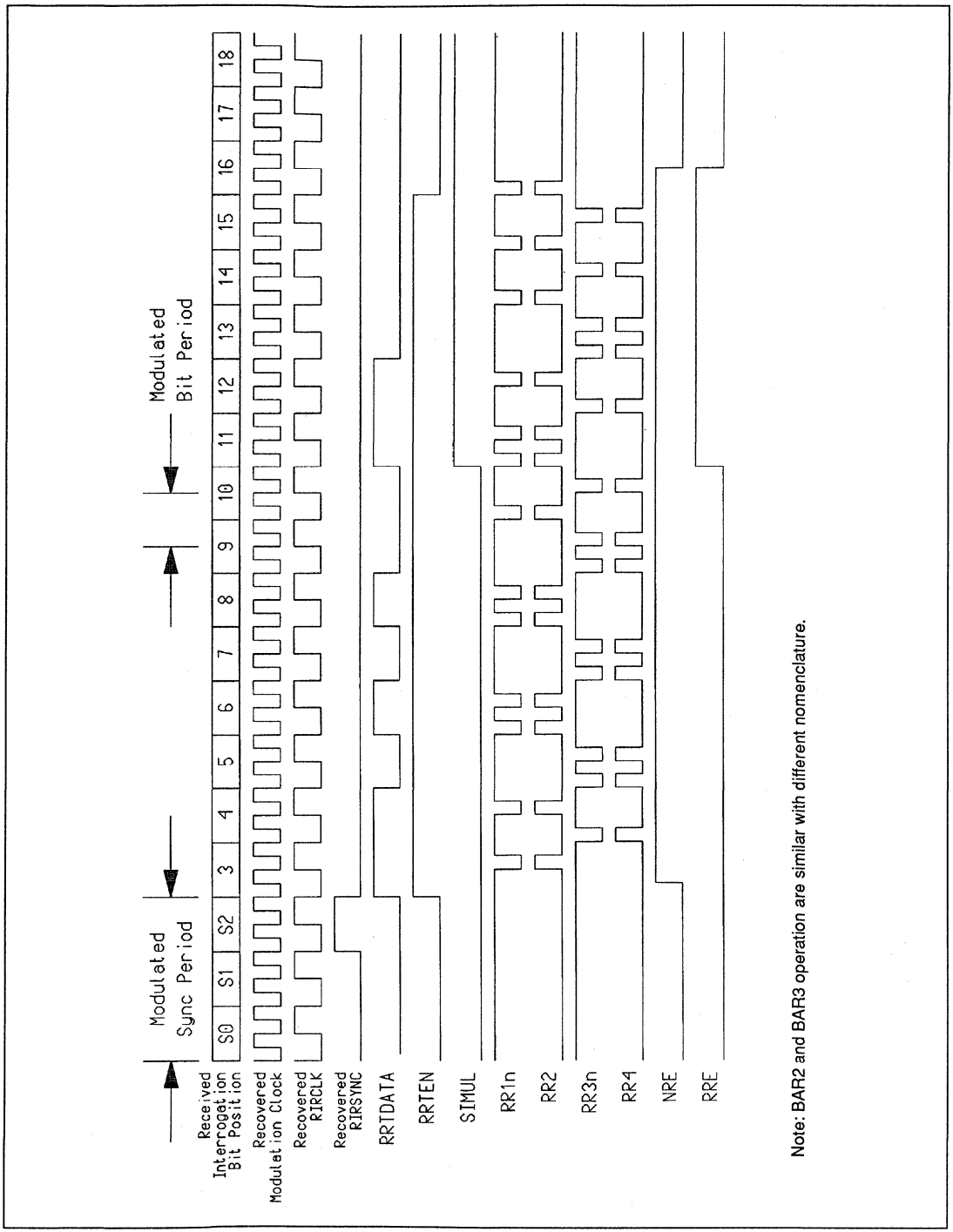
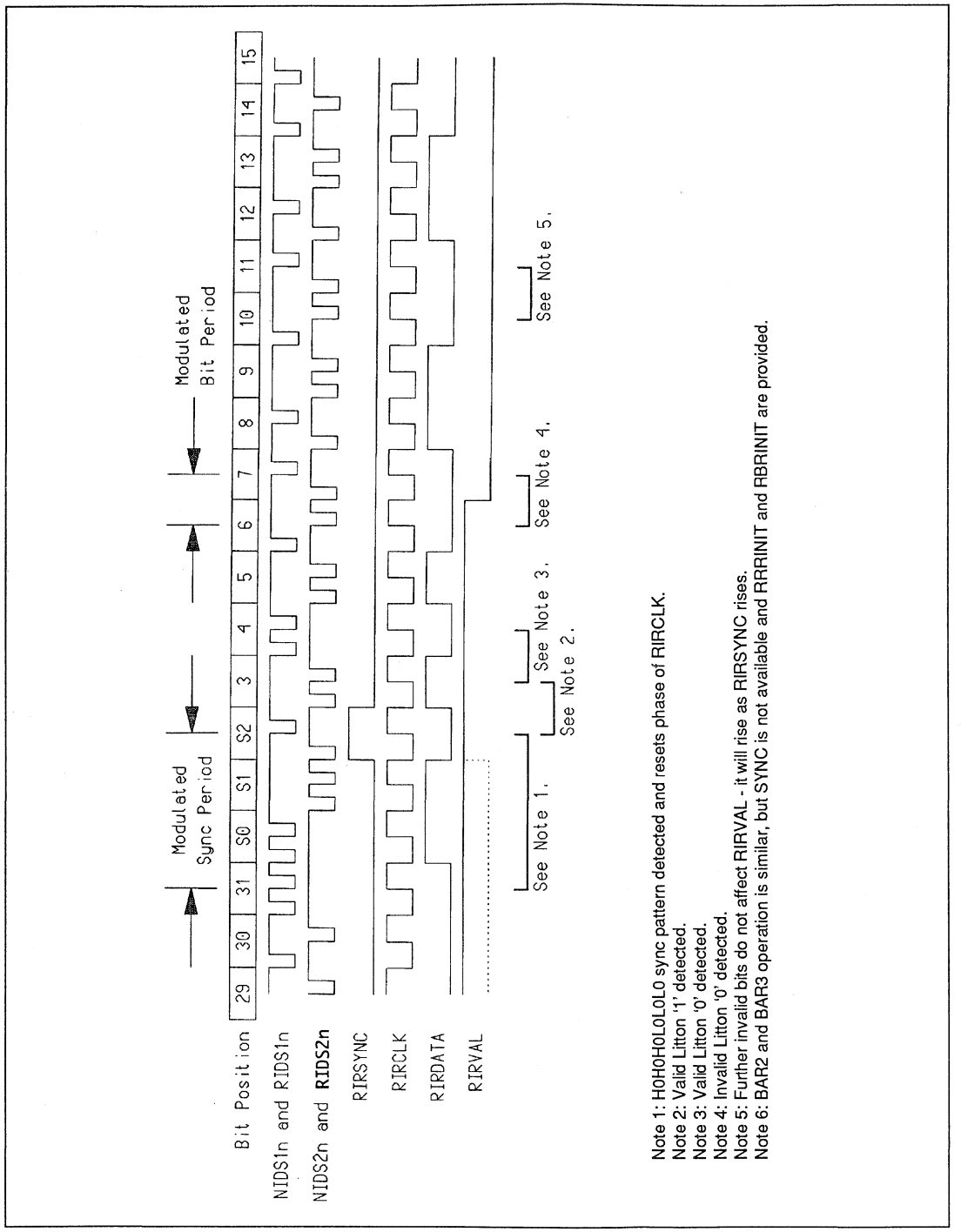
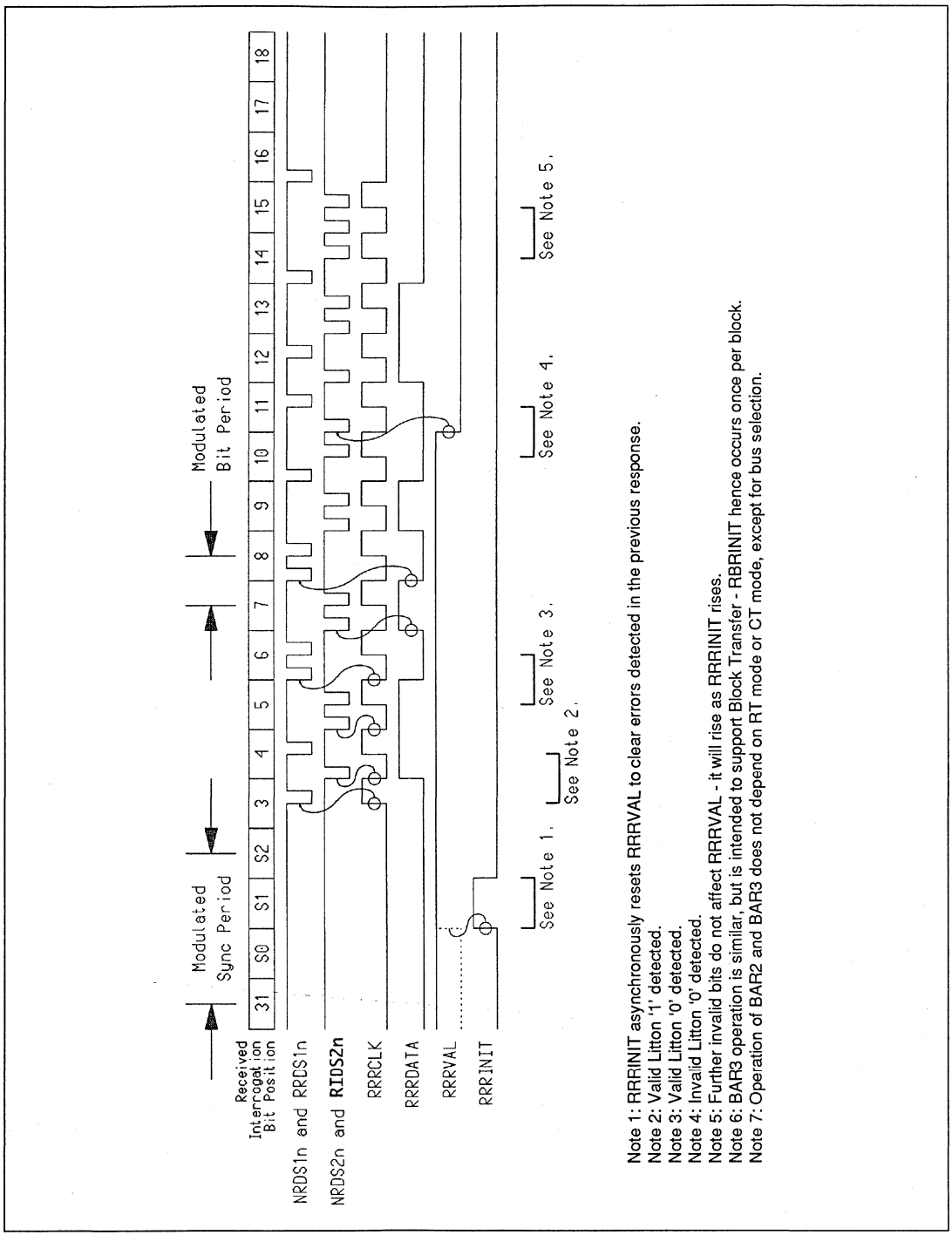


Figure 6: RT Mode Bus Adaptor Transmitter Waveforms



Note 1: H0H0H0L0L0L0 sync pattern detected and resets phase of RIRCLK.
Note 2: Valid Litton '1' detected.
Note 3: Valid Litton '0' detected.
Note 4: Invalid Litton '0' detected.
Note 5: Further invalid bits do not affect RIRVAL - it will rise as RIRSYNC rises.
Note 6: BAR2 and BAR3 operation is similar, but SYNC is not available and RRRINIT and RBRINIT are provided.

Figure 7: RT Mode Bus Adaptor Receiver Waveforms



Note 1: RRRINIT asynchronously resets RRRVAL to clear errors detected in the previous response.
Note 2: Valid Litton '1' detected.
Note 3: Valid Litton '0' detected.
Note 4: Invalid Litton '0' detected.
Note 5: Further invalid bits do not affect RRRVAL - it will rise as RRRINIT rises.
Note 6: BAR3 operation is similar, but is intended to support Block Transfer - RBRINIT hence occurs once per block.
Note 7: Operation of BAR2 and BAR3 does not depend on RT mode or CT mode, except for bus selection.

Figure 8: BAR2 Bus Adaptor Receiver Waveforms

CLOCK DETECTOR OPERATION

The Clock Detector architecture is shown in Figure 9; a separate channel is essentially provided for each of the Nominal and Redundant Interrogation busses. Associated waveforms are shown in Figure 10.

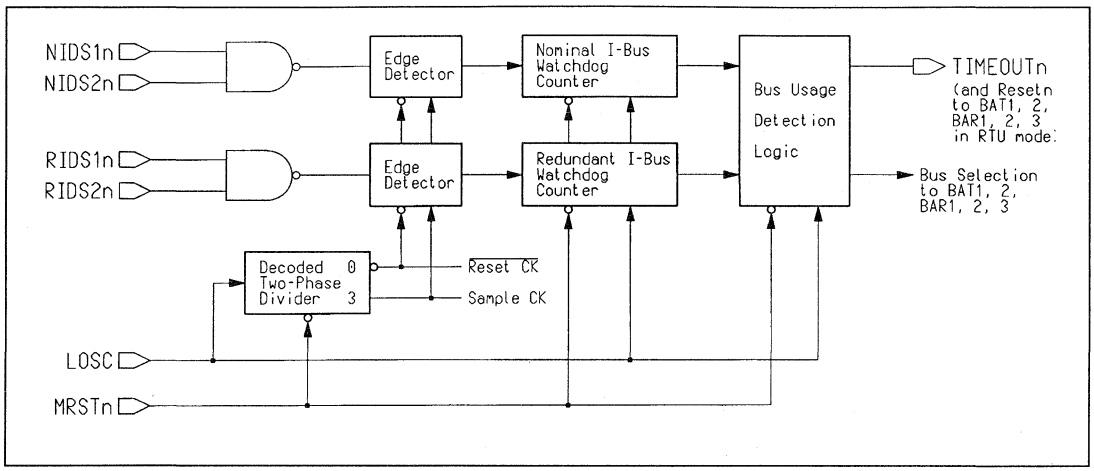


Figure 9: Clock Detector Architecture

Each channel contains an Edge Detector and a 5-bit Watchdog Counter which respond only to high-to-low transitions on their respective Interrogation bus DS1n inputs. A common Bus Usage Detection circuit is used to generate time-out pulses (used for internal and external reset) and bus selection signals from the results of the watchdogs.

The local oscillator input, LOSC, is divided and decoded to generate an active low reset and an active high sample clock. When applied to both input Edge Detectors, these signals permit input high-to-low transitions to be detected for one LOSC cycle in every two (between the reset ↓ and sample clock ↑). Once such transitions have been detected by a sample clock, the associated watchdog counter is reset. The MSB of each watchdog counter is used as an indication of its bus's status - active or inactive. Should the watchdog counter overflow (i.e. its MSB be set to 1), the associated bus will be considered inactive.

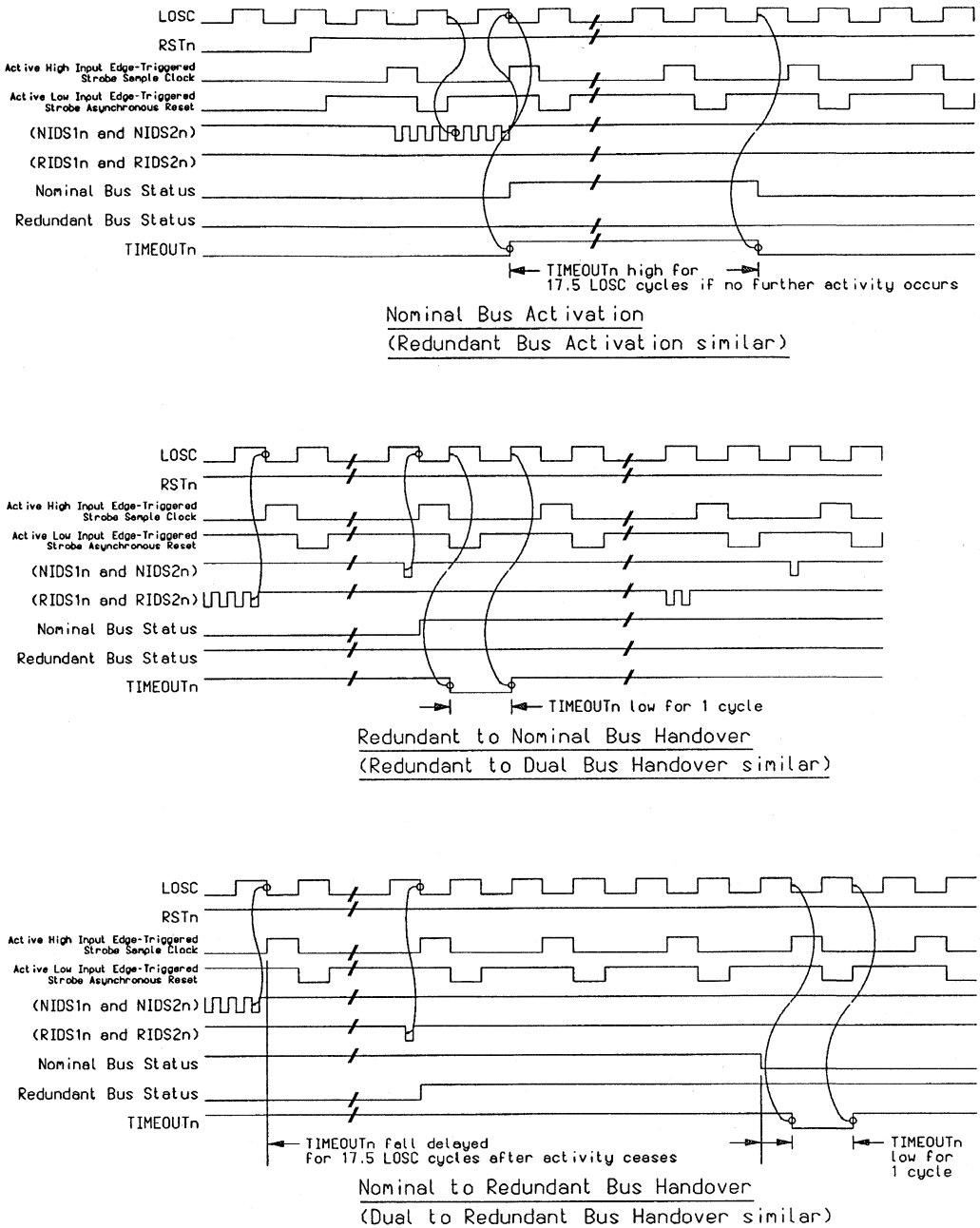
The status of the Nominal and Redundant Interrogation busses is used to determine internal bus selection for the modulation of Response and Block Transfer data in the device's RT mode. If neither bus is considered active, the TIMEOUTn pin will be held low and RT mode reception of all 3 busses will be inhibited. If one bus is considered active, RT mode reception will occur on the same set of bus circuits (redundancy) as the active Interrogation bus. If both busses are considered active, RT mode reception from the Nominal set of bus circuits will be performed. RT mode transmission will always occur on the same set of bus circuits (redundancy) as selected for reception unless the SIMUL pin is held high, in which case transmission will occur simultaneously on both the Nominal and Redundant busses.

Both watchdog counters are fully set at power up to mark both busses as inactive - in this way, a missing LOSC input will not cause inactive busses to be deemed active.

For a single detected input transition, 17.5 to 18.5 LOSC cycles will elapse before the relevant bus is considered inactive. If near-instantaneous Nominal-to-Redundant or Dual-to-Redundant bus handover occurs, the change-over will be delayed by 18 to 19 LOSC cycles, in order to preserve the priority of the Nominal bus. If near-instantaneous Redundant-to-Nominal or Redundant-to-Dual bus handover occurs, the change-over will occur after 1.5 to 2.5 LOSC cycles since the Nominal bus takes priority. In either of these cases, a 1 LOSC cycle TIMEOUTn pulse is always generated to ensure that internal reset occurs.

The frequency of the local oscillator may be varied to make the nominal time-out period of 17.5 LOSC cycles correspond to any desired number of (missing) bits on the Interrogation bus. Variation of the duty cycle does not vary the time-out period. After 16 LOSC cycles without detected input transitions, the associated watchdog times-out and is detected on the next LOSC ↑ edge; the generation of a TIMEOUTn pulse and reset are then inevitable.

For proper Clock Detector operation, (at least) one high-to-low input transition must be detected within a period of 16 LOSC cycles of the last such detection, but transitions made during alternate LOSC cycles (the phase is difficult to predict) will not be detected. Local oscillator clock signals which are harmonically-related to the modulation clock by an integer ratio are thus a cause for concern, although this problem is perhaps only likely to occur in experimental set-ups.



Note: If both busses are determined by their watchdogs to be active (as indicated above by their status), the Nominal Bus will always be used by the Bus Adaptor Transmitter and Receiver circuits instead of the Redundant Bus.

Figure 10: MA28139 Clock Detector Operation

The requirement to respect set-up and hold times for the capture of the Edge Detector outputs by the LOSC high-to-low transition means that LOSC signals which are harmonically-related to the Litton modulation clock but whose phase can not be controlled can never be guaranteed to provide reliable operation.

For asynchronous local oscillator signals, there will be no concern if we are simply able to place two or more Litton DSn high-to-low edges into each LOSC cycle, so that:

$$\tau_{MOD} \leq \tau_{LOSC} - t_{SU} - t_{HOLD}$$

and the time-out period of 16 τ_{LOSC} is hence approximately 8 bit periods or more.

However, suppose that the periods of the modulation clock and the local oscillator clock are such that the relationship between them is:

$$\tau_{MOD} = m\ \tau_{LOSC}$$

where m is a positive integer.

In order to respect the setup and hold times, t_{SU} + t_{HOLD} respectively, between the DSn ↓, and LOSC ↓ edges, it is necessary to avoid such harmonic relationships; it can be shown that around these spot frequencies it is necessary to ensure that either:

$$w\ \tau_{MOD} \geq x\ \tau_{LOSC} + t_{SU} + t_{HOLD}$$

or

$$y\ \tau_{MOD} \leq z\ \tau_{LOSC} - t_{SU} - t_{HOLD}$$

where the integer constants w, x, y and z are given in the table below.

Since two modulation clock cycles occur per bit, the time-out period at these harmonics will then be:

$16\ \tau_{LOSC} \approx 16\ \tau_{MOD} / m \approx 8 / m$ bit periods.

m	w	x	y	z	Approx. time-out period (bit periods)
1	15	15	17	17	8
2	7	15	8	15	4
3	5	15	5	15	2.67
4	3	13	4	15	2
5	3	15	3	15	1.6
6	2	13	2	11	1.33
7	1	7	1	7	1.14
8	1	9	2	15	1
9	1	9	1	9	0.88
10	1	11	1	9	0.8
11	1	11	1	11	0.73
12	1	13	1	11	0 67
13	1	13	1	13	0.62
14	1	15	1	13	0.57
15	1	15	1	15	0.53

In summary, slow local oscillator clocks which cause relatively long timeout periods ≥ 8 bit periods are not considered a problem; very long time-outs can be reliably implemented. For shorter time-out periods, however, it is necessary to avoid harmonic relationships between the Litton modulation clock and the local oscillator. The simplest practical method for avoiding such relationships would be to arrange for the ratio

$$n = \tau_{MOD} / \tau_{LOSC}$$

to have a half-integer value such that n = 0.5, 1.5, 2.5, ...using an independent crystal oscillator if necessary.

OBDH / IUB INTERFACE

The Central Terminal Unit controls timing, commands and telemetry to all subsystems on the OBDH bus. ESA TTC-B-01 specifies the OBDH to be 2 redundant sets (Nominal and Redundant) of 2 twisted pairs (Interrogation and Response bus) plus an optional redundant 3rd twisted pair (Block Transfer bus), Litton modulated (self clocking with parity on each bit), balanced transformer coupled for less than 1 error in 100 million bits on a 25 metre bus. The data rate is nominally 500K Bits/sec although the chip itself supports up to 5MBits/sec. The OBT is transformer coupled with adjustable reference and threshold levels as shown below. Litton more positive than V_{th+} makes discriminator signal NIDS1n low. Litton more negative than V_{th-} makes NIDS2n low. OBT RR1n, RR2, RR3n, RR4 control 4 switches which drive the bus with bipolar Litton code when enabled. For clarity redundancy is not shown below:

TTC-B-01 also specifies the IUB. The OBT supplies specified clocks, memory load address for ML data (or channel address for mode command) and responds on the R bus with a 13 zeroes response as acknowledgement. If the command requires data aquisition, the OBT responds with a 13 or 21 bit response containing 8 or 16 bits (respectively) of user data, controlling external ADC as required.

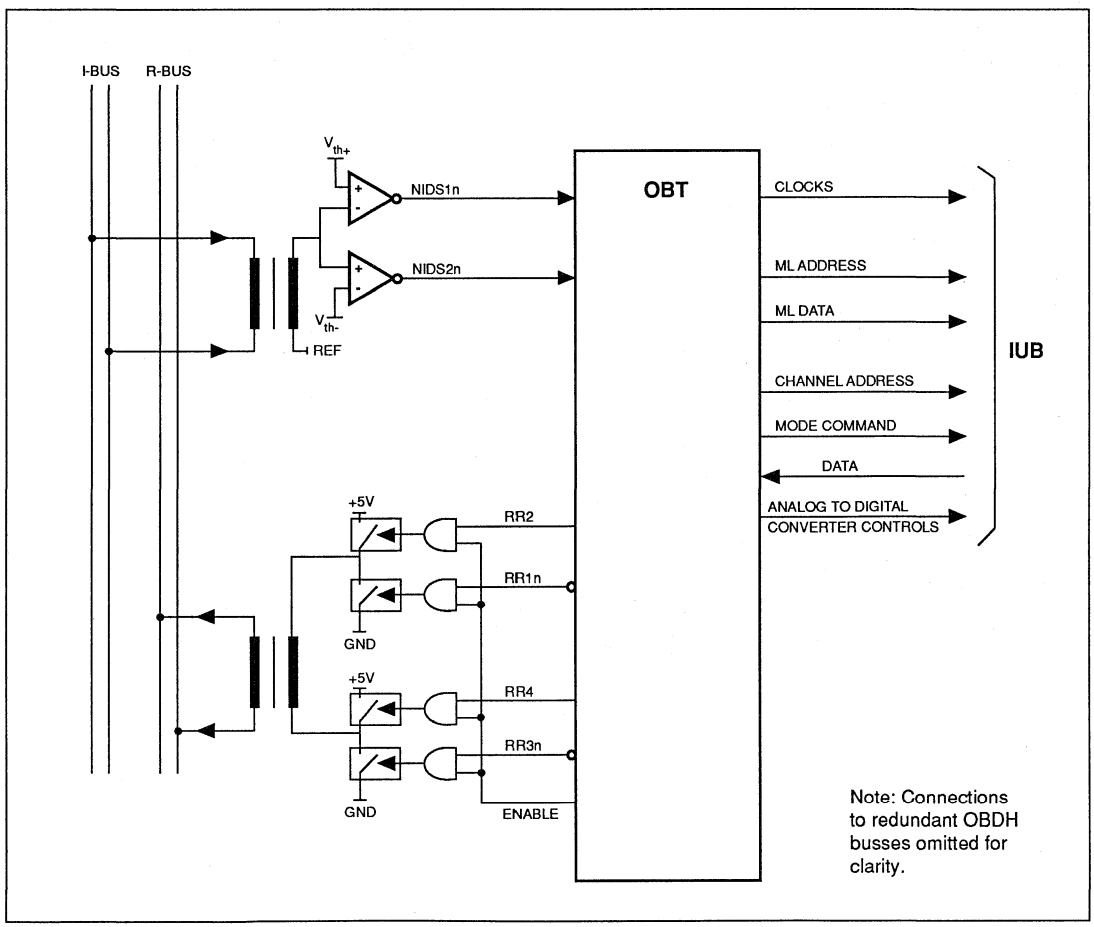


Figure 11: OBDH to IUB interface

RTU KERNEL PROTOCOL VIOLATIONS

Some commands to the RTU Kernel cannot be completed within one Interrogation period (or "slot") because of the need to provide a slow external interface as defined in ESA standard TTC-B-01. These are commands for 16-bit Digital Serial Acquisition (S16) and 16-bit Memory Load (ML). In addition, it is also possible to inhibit On/Off commands by pin configuration.

Consequently:

- a Memory Load command cannot be followed by another Memory Load command in the next Interrogation; the second command of such a sequence will be ignored,
- a 16-bit Digital Serial Acquisition (S16) cannot be followed by another acquisition or command in the next Interrogation; the second command of such a sequence will be ignored,
- a Long On/Off command will be ignored if the On/Off command Inhibit input pin, OOINH, is high.

Note that in all MODE Dependent Command and Acquisition Interrogations, bits 23 to 30 of the Interrogation are output as an 8 bit channel address on CHADD(0:7). ESA standard TTC-B-01, p.110 specifies a 7 bit channel address in bits 27 to 29, leaving bit 30 as Reserved. For complete compliance with this standard, CHADD(7) should be disregarded and CHADD(0:6) only should be used.

The signals generated by the RTU Kernel during 8-bit Single-Ended and 8-bit Double-Ended Analog Data Acquisitions are intended for connection to an 8-bit serial ADC module. The outputs PC, ANCLK, SOC and SH are intended to provide ADC power control, conversion clock, start of conversion pulse and sample/hold control respectively.

RTU Kernel BroadCast Pulse and BCP Validity Waveforms are shown in Figure 12.

RTU Kernel Memory Load Command Waveforms are shown in Figure 13.

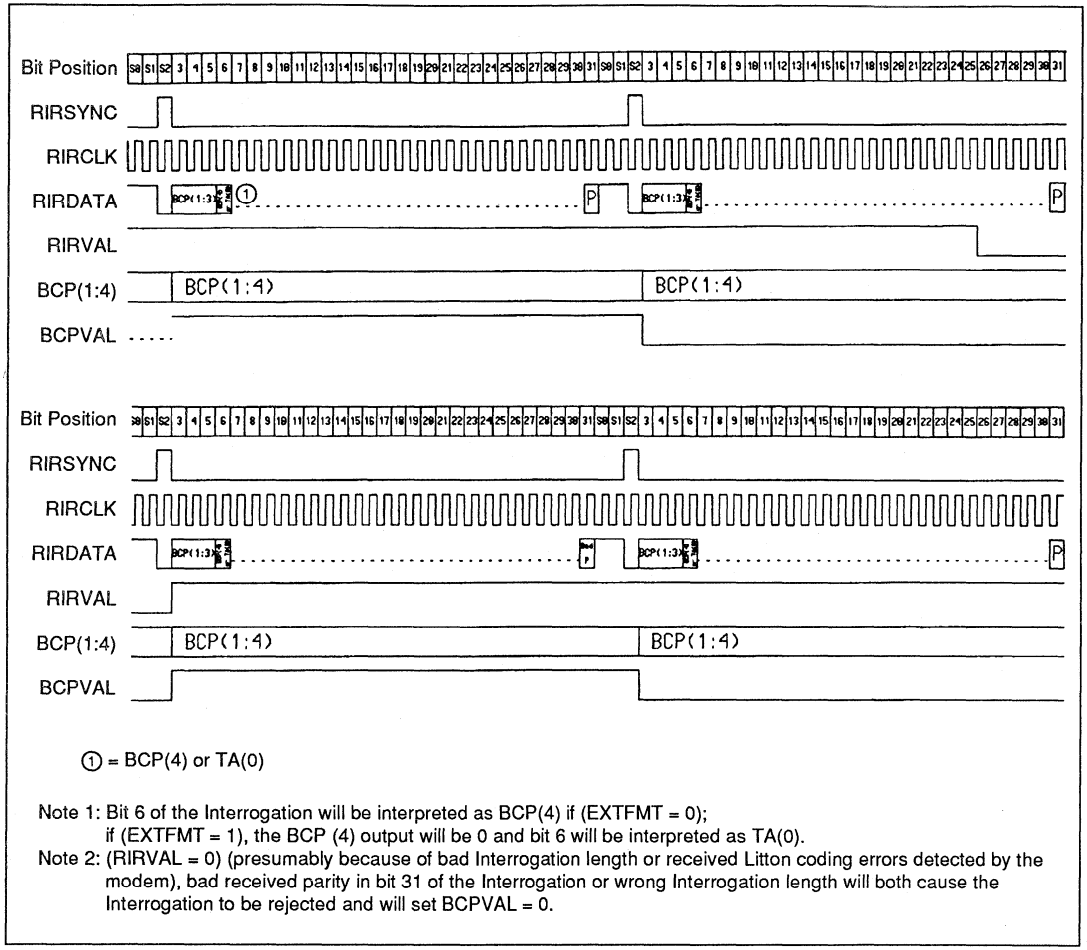
RTU Kernel MODE Dependent Command and Acquisition Waveforms are shown in Figures 14 - 17.

RTU KERNEL MODE DEFINITIONS

The mode field contained in bits 19 to 22 of the Interrogation is decoded during acquisition commands to drive one of the MOSC, MOLC, MOHL, MOBT, MODBL, MODS8, MODS16, MOANS or MOAND outputs. Mode decoding is an extension of that defined in ESA standard TTC-B-01 Table 7.1 and is shown in Table 1 below:

Mode Code					Associated
Bit 19	Bit 20	Bit 21	Bit 22	Function	Output Pin
0	0	0	0	Unused	-
0	0	0	1	Short Switch Closure On/Off Command	MOSC
0	0	1	0	Long Switch Closure On/Off Command	MOLC
0	0	1	1	High Power Switch Closure On/Off Cmd	MOHL
0	1	0	0	Unused	-
0	1	0	1	Unused	-
0	1	1	0	Unused	-
0	1	1	1	Block Transfer Command	MOBT
1	0	0	0	8-bit Digital Bi-Level Data Acquisition	MODBL
1	0	0	1	Unused	-
1	0	1	0	16-bit Serial Digital Data Acquisition	MODS16
1	0	1	1	8-bit Serial Digital Data Acquisition	MODS8
1	1	0	0	8-bit Single-Ended Analog Data Acquisition	MOANS
1	1	0	1	Unused	-
1	1	1	0	8-bit Double-Ended Analog Data Acquisition	MOAND
1	1	1	1	Unused	-

Table 1: RTU Kernel Mode Definitions

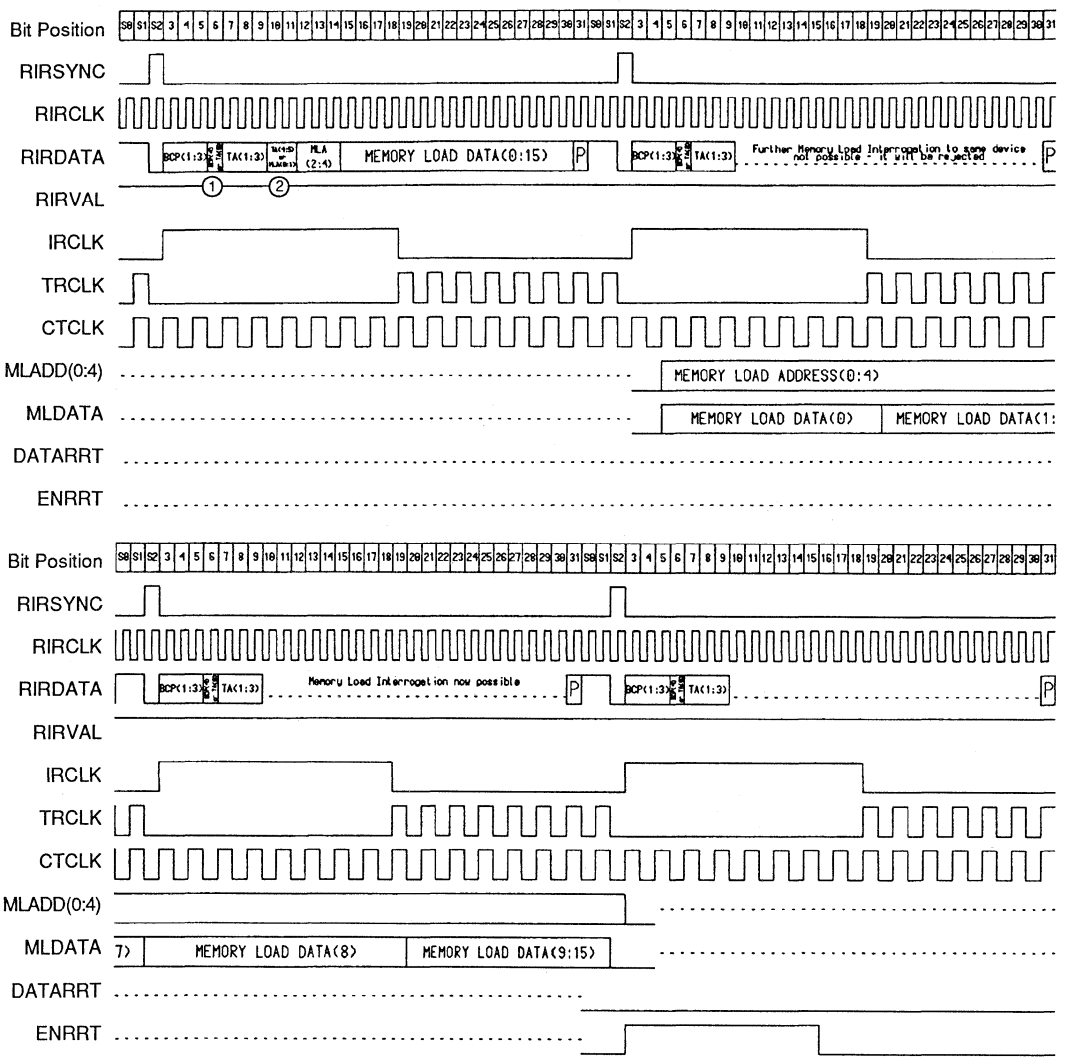


① = BCP(4) or TA(0)

Note 1: Bit 6 of the Interrogation will be interpreted as BCP(4) if (EXTFMT = 0);
if (EXTFMT = 1), the BCP (4) output will be 0 and bit 6 will be interpreted as TA(0).

Note 2: (RIRVAL = 0) (presumably because of bad Interrogation length or received Litton coding errors detected by the modem), bad received parity in bit 31 of the Interrogation or wrong Interrogation length will both cause the Interrogation to be rejected and will set BCPVAL = 0.

Figure 12: BroadCast Pulse and BCP Validity Waveforms



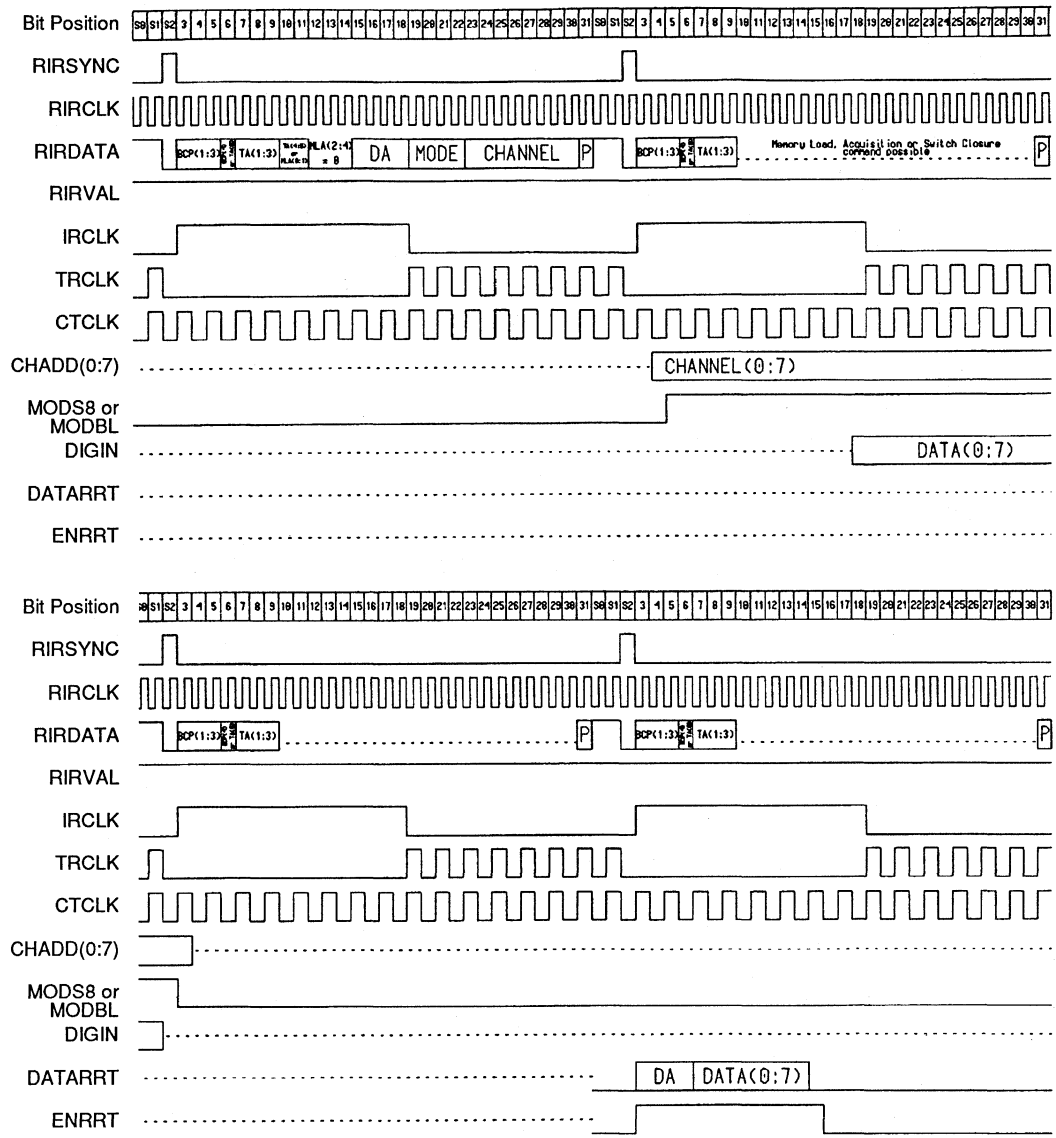
Note 1: One Memory Load command takes 2 Interrogations to complete. Consecutive Memory Load commands are hence not possible and form a protocol violation. The second Memory Load command of such a sequence will be rejected.

Note 2: For a Memory Load command to be decoded, the evaluated Memory Load Address must be non-zero. An evaluated Memory Load Address of zero implies data aquisition.

Note 3: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 4: The Memory Load command response is always 13-zeros.

Figure 13: Memory Load Command Waveforms

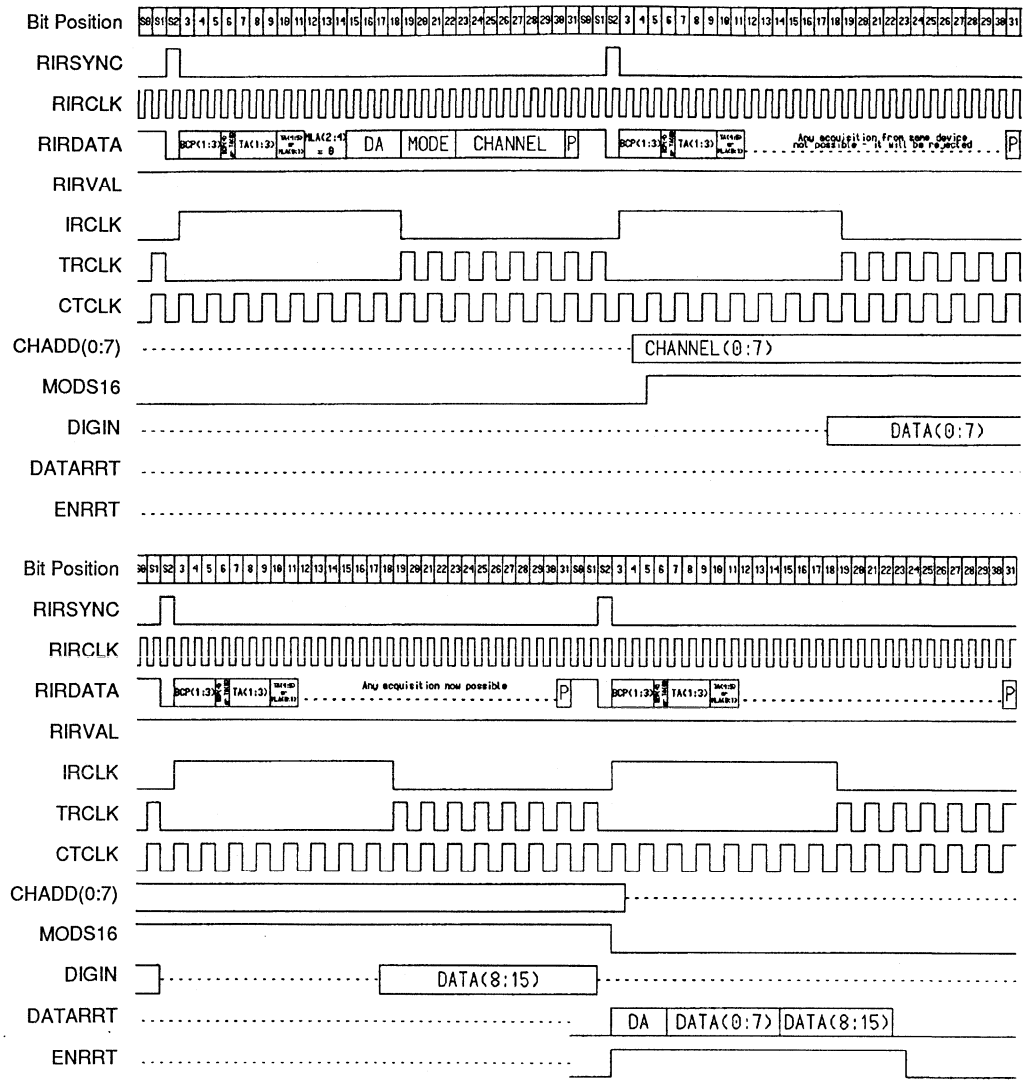


Note 1: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 2: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 3: The 8-bit Digital Serial and 8-bit Digital Bi-Level Acquisition command responses are always 13 bits in length; the Destination Address is simply copied from the Interrogation into the Response.

Figure 14: 8-Bit Digital Serial and 8-Bit Digital Bi-Level Acquisition Waveforms



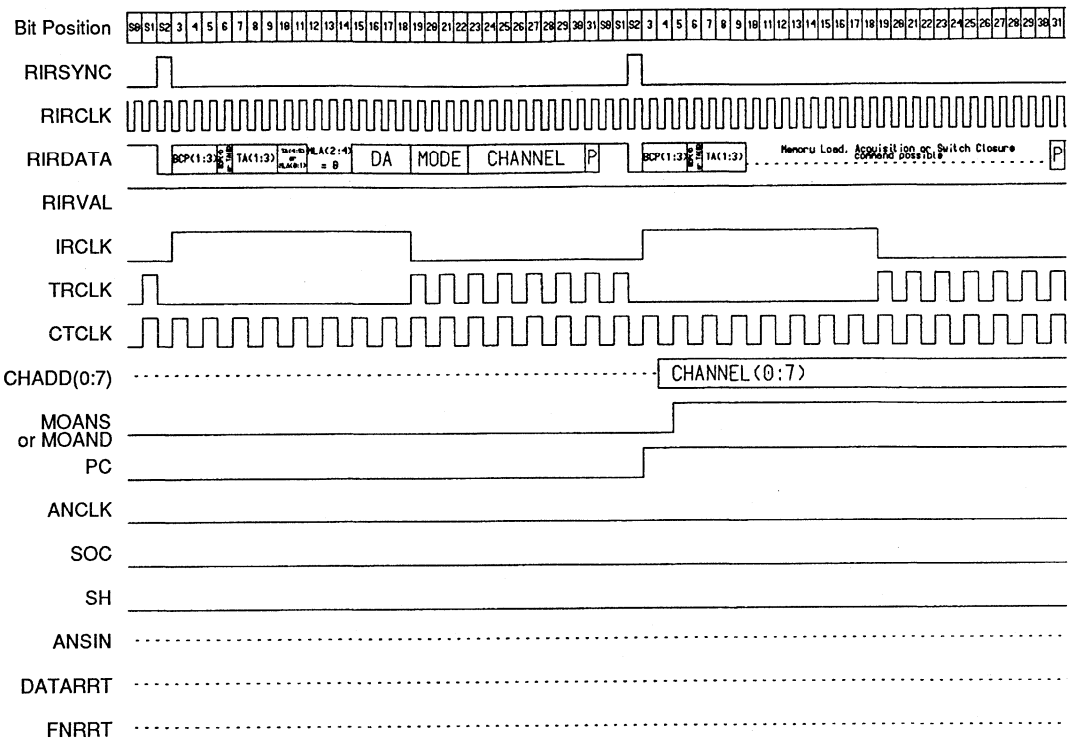
Note 1: One 16-bit Digital Serial Acquisition command takes 2 Interrogations to complete. A succeeding Acquisition or Switch Closure command of any type is hence not possible and forms a protocol violation. The second command of such a sequence will be rejected.

Note 2: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 3: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11 of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 4: The 16-bit Digital Serial Acquisition command response is always 21 bits in length; the Destination Address is simply copied from the Interrogation into the Response.

Figure 15: 16-Bit Digital Serial Acquisition Waveforms



Note 1: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 2: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 3: The 8-bit Analog Single-Ended and 8-bit Analog Double-Ended Acquisition command responses are always 13 bits in length; the Destination Address is simply copied from the Interrogation into the Response.

Figure 16: 8-Bit Analog Single-Ended and 8-Bit Analog Double-Ended (Serial) Acquisition Waveforms

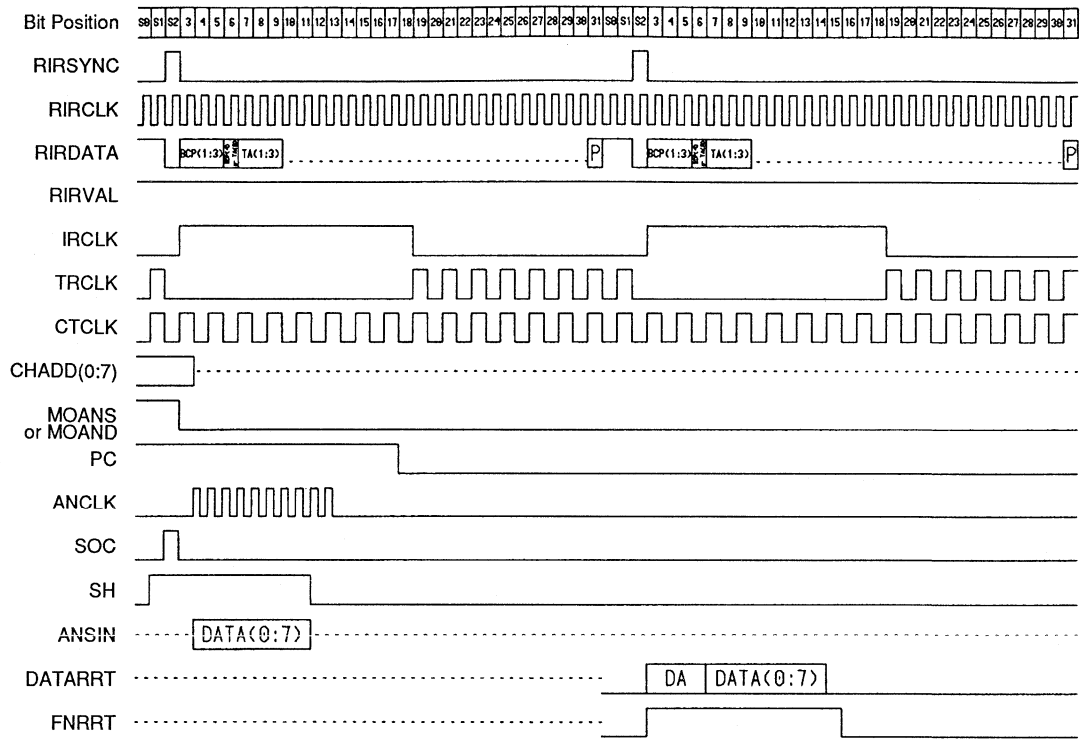
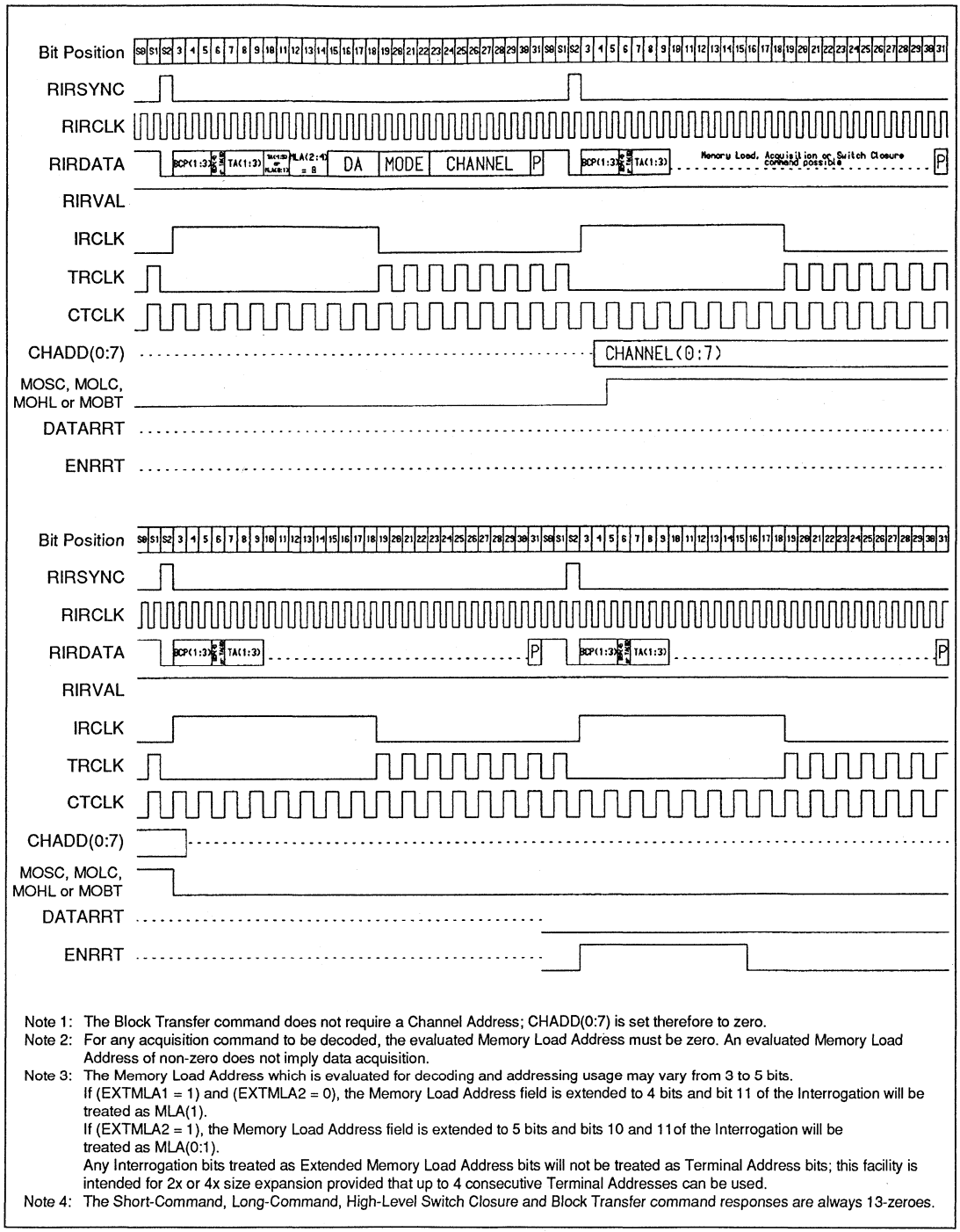


Figure 16 continued



Note 1: The Block Transfer command does not require a Channel Address; CHADD(0:7) is set therefore to zero.

Note 2: For any acquisition command to be decoded, the evaluated Memory Load Address must be zero. An evaluated Memory Load Address of non-zero does not imply data acquisition.

Note 3: The Memory Load Address which is evaluated for decoding and addressing usage may vary from 3 to 5 bits.
If (EXTMLA1 = 1) and (EXTMLA2 = 0), the Memory Load Address field is extended to 4 bits and bit 11 of the Interrogation will be treated as MLA(1).
If (EXTMLA2 = 1), the Memory Load Address field is extended to 5 bits and bits 10 and 11of the Interrogation will be treated as MLA(0:1).
Any Interrogation bits treated as Extended Memory Load Address bits will not be treated as Terminal Address bits; this facility is intended for 2x or 4x size expansion provided that up to 4 consecutive Terminal Addresses can be used.

Note 4: The Short-Command, Long-Command, High-Level Switch Closure and Block Transfer command responses are always 13-zeroes.

Figure 17: Short-Command, Long-Command and High-Level Switch Closure and Block Transfer Command Waveforms

THE ESA ON-BOARD DATA HANDLING (OBDH) BUS

The dual redundant OBDH bus is connected to the OBT bus interface via an input descriminator and an output bridge driver circuit. These convert between the bipolar LITTON code and the standard CMOS inputs and outputs of the IC.

The OBDH bus is divided into three parts:

A. INTERROGATION BUS (I BUS)

This bus is used to transfer data from the CT to the RTs, as commands of 32 bit words, each bit being modulated according to the Litton scheme shown in Figure 18. Each Interrogation (or command) "slot" comprises 3 Sync bits, 3 or 4 BroadCast Pulses, 5 or 6 Terminal Address bits, 4 Destination Address bits, 16 Data bits and a Parity bit.

B. RESPONSE BUS (R BUS)

This bus is used to send data from the RTs to the CT, (can be used by RTs to receive data). Each response word comprises the 4 Destination Address bits sent in the corresponding Interrogation, either 8 or 16 Data bits from the user (8 bits unless a 16 bit acquisition was requested and 8 zeros if no response data is required) and a single Stop bit (used to ensure data is fully clocked through bus modems and 0 by convention).

C. BLOCK TRANSFER BUS (BT BUS)

Used to transfer blocks of data between the CT and RTs, in either direction, as a contiguous block or stream of data bits.

FASTER OBDH/DBI COMPATIBLE NETWORKS

With analog components the OBT can interface any equipment to the specified ESA OBDH bus at the nominal data rate of 0.5 Mbps. Contract 5352 proved that analog components limit OBDH data rate to 2 Mbps maximum. But OBTs work to over 5 Mbps (10MHz with 2 clocks/bit Litton coded). OBTs may be directly networked via digital bus drivers/receivers, (eliminating analog components) using Litton coded 4 wire (R2/DS1 and R4/DS2) busses (see OBDH application note 1). MSS made a 3 metre optical OBDH network for the Pegasus ion source.

DBIs may be directly connected but will not be Litton coded with Parity on every bit, or exhibit modulation and demodulation delays.

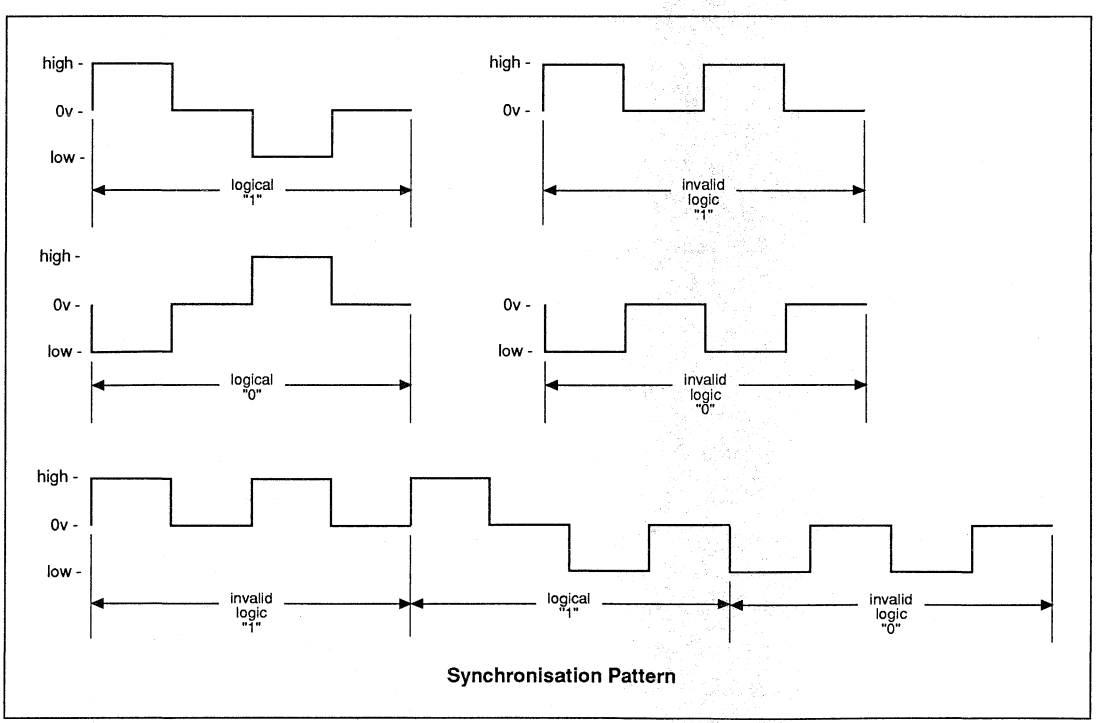
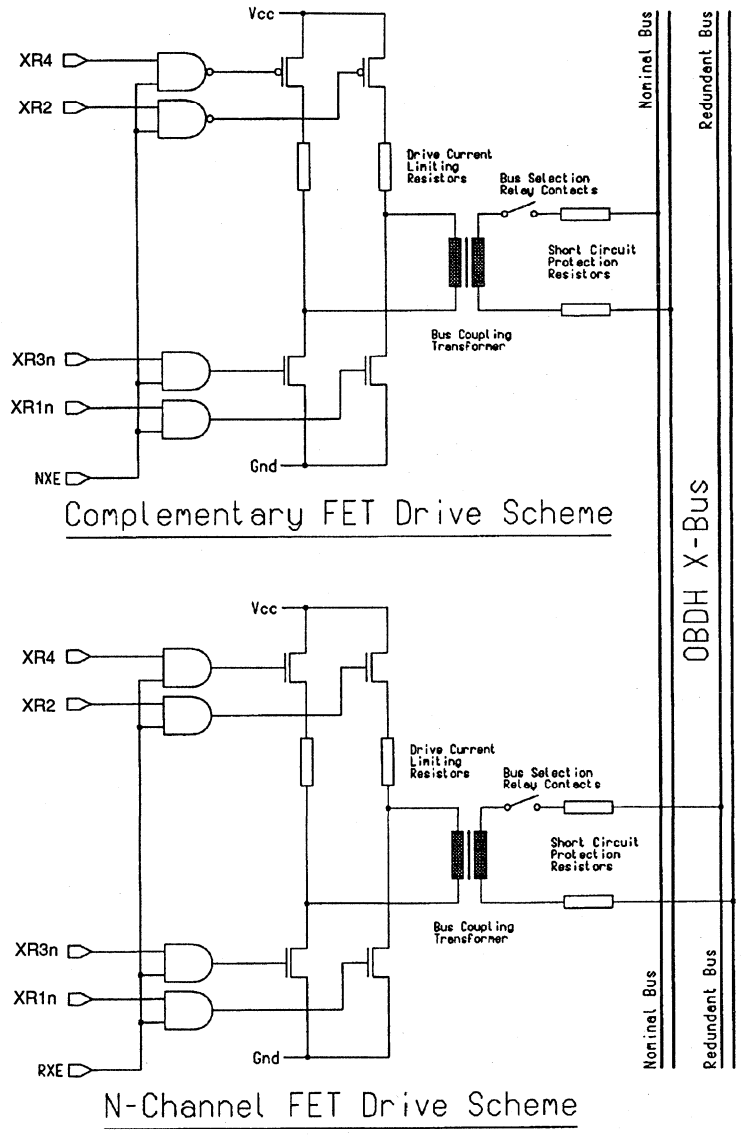


Figure 18: Litton Coded Data

CONNECTIONS TO THE OBDH I, R AND BT BUSSES (SUGGESTED SCHEMES ONLY)

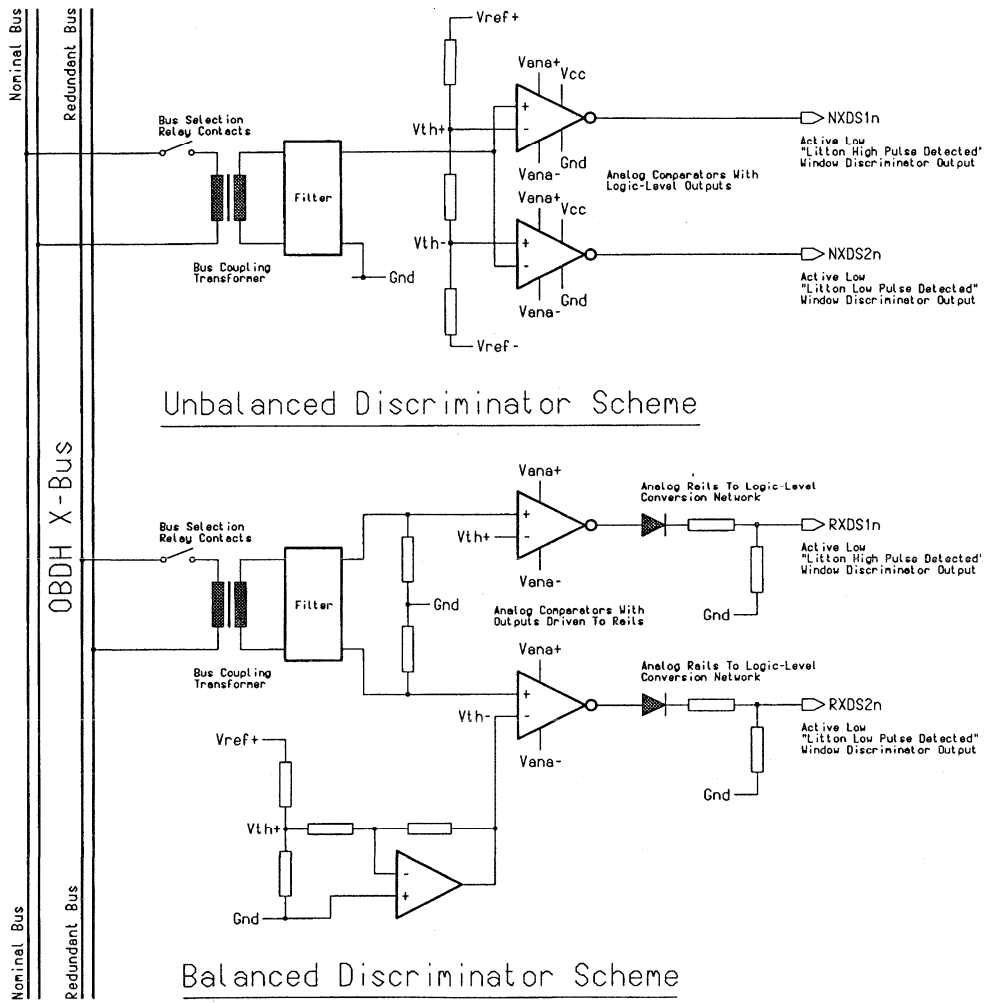
TRANSMITTER



Two OBDH bus driver schemes based on complementary and N-channel enhancement-mode FETs are shown.
Current-limiting and protection resistors may be employed to prevent damage under short-circuit.
Latching and/or non-latching relays may be used to provide isolation from the bus when a redundant circuit is unused or unpowered.
NPN and/or PNP bipolar junction transistors may also be employed in place of FETs.
Redundancy can be handled in channels (as shown) or by applying cross-strapping between the transformers and the drivers.
This implementation generates 'active ground' pulses where the transformer is shorted out (by conduction of the two lower FETs) while the bus driver is enabled to reduce ringing, bus echoes, etc.
Using XR2 in place of XR3n and XR4 in place of XR1n will not cause 'active zeros' to be driven.

Figure 19: Conceptual OBDH Bus Driver Scheme

RECEIVER



Two OBDH bus window discriminator schemes, based on balanced and unbalanced techniques are shown.
Current-limiting and protection resistors may be employed to prevent damage under short-circuit.
Latching and/or non-latching relays may be used to provide isolation from the bus when a redundant circuit is unused or unpowered.
Noise filtering and the effects of bus loading should be considered.
Redundancy can be handled in channels (as shown) or by applying cross-strapping between the transformers and the receivers.

Figure 20: Conceptual OBDH Bus Window Discriminator Scheme

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	+125	°C
Storage Temperature	-65	+150	°C

Table 2: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH}	CMOS input high voltage	-	0.8V_{DD}	-	V_{DD}	V
V_{IL}	CMOS input low voltage	-	V_{SS}	-	0.2 V_{DD}	V
V_{OH}	Output high voltage	I_{OH} = -1.0mA	V_{DD} - 0.5	-	-	V
V_{OL}	Output high voltage	I_{OL} = 4.0mA	-	-	0.4	V
I_{PDL}	Input Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-25	-	25	µA
I_{PDH}	Input Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{DD}	25	-	400	µA
I_{PUL}	Input Pull-up current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-400	-	-25	µA
I_{PUH}	Input Pull-up current	V_{DD} = 5.5V, V_{IN} = V_{DD}	-25	-	25	µA
I_L	Input leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-10	-	10	µA
I_{OZL}	Output leakage current	V_{DD} = 5.5V, V_{OUT} = V_{SS}	-30	-	30	µA
I_{OZH}	Output leakage current	V_{DD} = 5.5V, V_{OUT} = V_{DD}	25	-	400	µA
I_{DD1}	Static Power supply Current	V_{DD} = 5.5V	-	0.02	8	mA
I_{DD2}	Dynamic Power supply Current	f = 1MHz, V_{DD} = 5.5V	-	6	20	mA

Notes: 1. V_{DD} = 5V ±10% over full temperature range.
2. Total dose radiation not exceeding 10^5 Rads(Si).
3. Mil-Std-883, method 5005, subgroups 1, 2, 3.
4. All outputs are suitable for TTL/CMOS drive.
5. Electro-Static Discharge protection is provided for all pins.
6. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.
7. Input and output leakage measurements are guaranteed but not tested at -55°C.

Table 3: DC Characteristics

AC CHARACTERISICS

No.	Parameter	Condition	Min.	Max.	Units
T1	CITMOD to RR1n, RR2, RR3n, RR4, BR1n, BR2, BR3n, BR4	CTU mode	-	45	ns
T2	CITMOD to NRE, RRE, NBE, RBE	CTU mode	-	55	ns
T3/ T3a	CITSYNC, CITINV to CITCLK ↑ (setup/hold)	CTU mode	10	-	ns
T4/4a	RRTDATA to CITMOD ↓ (setup/hold)	CTU mode	10	-	ns
T5/5a	RBTDATA to CITMOD ↓ (setup/hold)	CTU mode	10	-	ns
T6/6a	RBTEN to CITMOD ↑ (setup/hold)	CTU mode	10	-	ns
T7/7a	CITCLK to CITMOD ↑ (setup/hold)	CTU mode	10	-	ns
T8	NIDS1n, NIDS2n, RIDS1n, RIDS2n to RR1n RR2, RR3n, RR4, BR1n, BR2, BR3n, BR4	RTU mode	-	55	ns
T9	NIDS1n, NIDS2n, RIDS1n, RIDS2n to NRE RRE, NBE, RBE	RTU mode	-	75	ns
T10/ T10a	RRTDATA to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (setup/hold)	RTU mode	10	-	ns
T11/ T11a	RBTDATA to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (setup/hold)	RTU mode	10	-	ns
T12	RRTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ setup	RTU mode	0	-	ns
T12a	RRTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ hold	RTU mode	35	-	ns
T13	RBTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ setup	RTU mode	0	-	ns
T13a	RBTEN to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↑ hold	RTU mode	35	-	ns

Table 4: Bus Adaptor Transmitter Characterisation

No.	Parameter	Condition	Min.	Max.	Units
T14	NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ to RIRSYNC, RIRCLK, RIRDATA, RIRVAL valid	RTU mode	-	80	ns
T15	NRDS1n, NRDS2n, RRDS1n, RRDS2n ↓ to RRRCLK, RRRDATA valid	RTU mode	-	55	ns
T16	NBDS1n, NBDS2n, RBDS1n, RBDS2n to RBRCLK, RBRDATA valid	RTU mode	-	55	ns
T17	NRDS1n, NRDS2n, RRDS1n, RRDS2n ↓ to RRRVAL ↓	RTU mode	-	55	ns
T18	NBDS1n, NBDS2n, RBDS1n, RBDS2n to RBRVAL ↓	RTU mode	-	55	ns
T19	RRRINIT to RRRVAL ↑	RTU mode	-	30	ns
T20	RBRINIT to RBRVAL ↑	RTU mode	-	30	ns
T21	NIDS1n, NIDS2n, RIDS1n, RIDS2n pulse width low (min.)	RTU mode	12	-	ns
T22	NRDS1n, NRDS2n, RRDS1n, RRDS2n pulse width low (min.)	RTU mode	12	-	ns
T23	NBDS1n, NBDS2n, RBDS1n, RBDS2n pulse width low (min.)	RTU mode	12	-	ns

Table 5: Bus Adaptor Receiver Characterisation

No.	Parameter	Condition	Min.	Max.	Units
T24	LOSC ↓ to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (hold max.)	CTU mode or RTU mode	10	-	ns
T25	LOSC ↓ to NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ (setup max.)	CTU mode or RTU mode	15	-	ns
T26	LOSC ↑↓ to TIMEOUTn valid	CTU mode or RTU mode	-	55	ns
	Timeout period = $16\tau_{LOSC}$	CTU mode or RTU mode	Guaranteed, not measured		
	Redundant to Dual or Redundant to Nominal bus changeover TIMEOUTn low reset period = τ_{LOSC}	CTU mode or RTU mode	Guaranteed, not measured		

Table 6: Clock Detector Characterisation

No.	Parameter	Condition	Min.	Max.	Units
T27	RIRCLK ↓ to BCP(1:4), BCPVAL valid	CTU mode	-	70	ns
T28	RIRCLK ↓ to MLADD(0:4)	CTU mode	-	80	ns
T29	RIRCLK ↓ to MLDATA	CTU mode	-	80	ns
T30	RIRCLK ↓ to CHADD	CTU mode	-	75	ns
T31	RIRCLK ↓ to MOSC, MOLC, MOHL, MOBT, MODBL, MODS16, MODS8, MOANS, MOAND valid	CTU mode	-	70	ns
T32	RIRCLK ↓ to IRCLK, CTCLK, TRCLK valid	CTU mode	-	70	ns
T33	RIRCLK ↓ to PC, ANCLK, SOC, SH valid	CTU mode	-	70	ns
T34	RIRCLK ↓ to DATARRT, ENRRT valid	CTU mode	-	55	ns
T35	ANSIN to RIRCLK ↑ setup	RTU mode	0	-	ms
T35a	ANSIN to RIRCLK ↑ hold	RTU mode	30	-	ns
T36	NIDS1n, NIDS2n, RIDS1n, RIDS2n ↓ to DATARRT, ENRRT	RTU mode	-	75	ns

Note 1: RTU mode timing parameters not explicitly stated will be lower than the sum of the appropriate parameters for the RTU Kernel, BAR1 and BAT2. Parameters T34 and T36 above may be used to estimate the difference in timing between CTU mode (i.e. where the RTU Kernel, BAR1 and BAT2 are not coupled together) and RTU mode usage (i.e. where those components are coupled together).

Note 2: Configuration pins such as TA(0:5), EXTFMT, EXTMLA1 and EXTMLA2 and MRSTn are not considered here because they do not need to be dynamically changed.

Note 3: V_{DD} = 5V ±10% over full temperature range. $V_{OH} = V_{OL} = V_{DD}/2$, $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, C_L = 50pF.

Note 4: Total dose radiation not exceeding 10^5 Rads (Si).

Note 5: Tables 4, 5, 6 & 7 contain Mil-Std-883, method 5005, subgroups 9, 10, 11.

Table 7: RTU Kernel Characterisation

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

Note 1: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Table 8: Capacitance

Symbol	Parameter	Conditions
F_T	Functionality	V_{DD} = 4.5 - 5.5V, FREQ = 1 MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} = V_{OH} = V_{DD}/2$ TEMP = -55°C to +125°C, GPS Pattern Set Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Table 9: Functionality

Subgroup	Definition
1	Static characteristics specified in Table 3 at +25°C
2	Static characteristics specified in Table 3 at +125°C
3	Static characteristics specified in Table 3 at -55°C
7	Functional characteristics specified in Table 9 at +25°C
8A	Functional characteristics specified in Table 9 at +125°C
8B	Functional characteristics specified in Table 9 at -55°C
9	Switching characteristics specified in Tables 4 to 7 at +25°C
10	Switching characteristics specified in Tables 4 to 7 at +125°C
11	Switching characteristics specified in Tables 4 to 7 at -55°C

Table 10: Definition of Subgroups

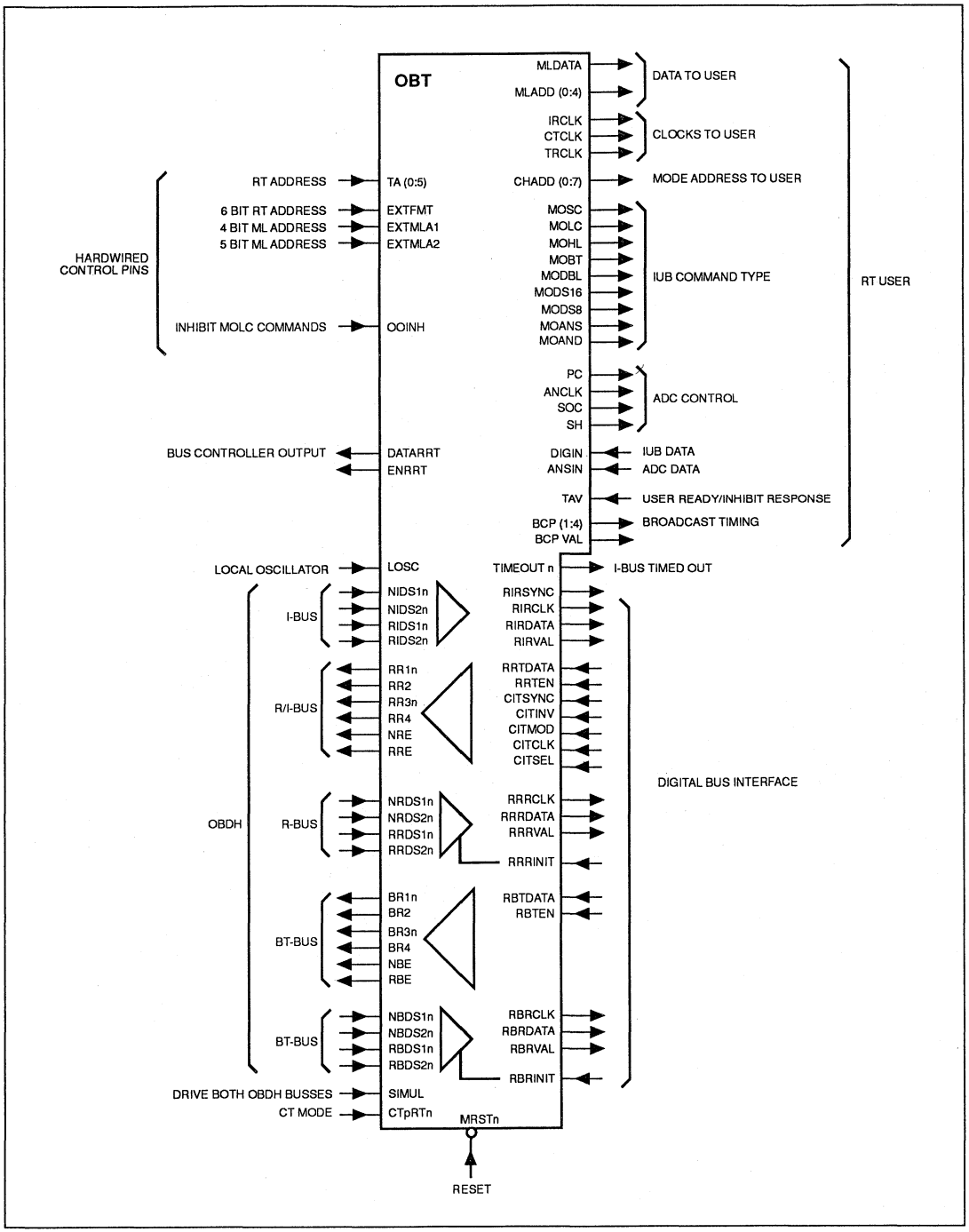


Figure 21: OBT Schematic

PIN ASSIGNMENT

OBT/IUB PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
45	IRCLK	O	Interrogation rate clock
46	CTCLK	O	Continuous clock
56	TRCLK	O	Transfer clock
79	MLDATA	O	Memory load data to user
78	MLADD0	O	Memory load address MSB (Interrogation bit 10)
77	MLADD1	O	Memory load address
76	MLADD2	O	Memory load address
75	MLADD3	O	Memory load address
74	MLADD4	O	Memory load address LSB (Interrogation bit 14)
73	CHADD0	O	Channel address 0 (Interrogation bit 23)
72	CHADD1	O	Channel address 1
71	CHADD2	O	Channel address 2
70	CHADD3	O	Channel address 3
69	CHADD4	O	Channel address 4
68	CHADD5	O	Channel address 5
67	CHADD6	O	Channel address 6
66	CHADD7	O	Channel address 7 (Interrogation bit 30)
65	MOSC	O	Mode short command (Interrogation mode bits 19/22 = 1 hex)
64	MOLC	O	Switch closure on/off command (mode 2)
63	MOHL	O	High power on/off command (mode 3)
62	MOBT	O	Mode block transfer (mode 7)
61	MODBL	O	Digital bi-level data acquisition (mode 8)
60	MODS16	O	16-bit serial digital data acquisition (mode A)
59	MODS8	O	8-bit serial digital data acquisition (mode B)
58	MOANS	O	Single ended analog data acquisition (mode C)
57	MOAND	O	Double ended analog acquisition (mode E)
131	PC	O	Power on to analog-to-digital converter
132	ANCLK	O	ADC shift clock
1	SOC	O	Start of conversion
2	SH	O	Sample/hold
42	DIGIN	I (PULL-DOWN)	Digital serial data input
43	ANSIN	I (PULL-DOWN)	Analog serial data input
3	BCP1	O	Broadcast pulse 1 (Interrogation bit 3)
4	BCP2	O	Broadcast pulse 2 (Interrogation bit 4)
5	BCP3	O	Broadcast pulse 3 (Interrogation bit 5)
6	BCP4	O	Broadcast pulse 4 (Interrogation bit 6 when extfmt = 0)
7	BCPVAL	O	Broadcast pulses valid
37	DATARRT	O	Data to RRT when used as RTU kernel
38	ENRRT	O	Enable RRT when used as RTU kernel

OBT/DBI PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
8	RIRSYNC	O/I (PULL-DOWN)	Sync from I-bus or (CT mode) input to RTU kernel
9	RIRCLK	O/I (PULL-DOWN)	Clock from I-bus or (CT mode) input to RTU kernel
10	RIRDATA	O/I (PULL-DOWN)	Data from I-bus or (CT mode) input to RTU kernel
11	RIRVAL	O/I (PULL-DOWN)	Validity from I-bus or (CT mode) input to RTU kernel
12	RRRCLK	O	Clock from R-bus
13	RRRDATA	O	Data from R-bus
21	RRRVAL	O	Validity from R-bus
22	RRRINIT	I (PULL-DOWN)	Initialise R-bus receiver
23	RRTDATA	I (PULL-DOWN)	Data to R-bus or (CT mode) to I-bus
24	RRTEN	I (PULL-DOWN)	Enable R-bus transmitter
25	CITSYNC	I (PULL-DOWN)	(CT mode) sync to I-bus
26	CITINV	I (PULL-DOWN)	(CT mode) invalid to I-bus
27	CITMOD	I (PULL-DOWN)	(CT mode) modulation to I-bus
28	CITCLK	I (PULL-DOWN)	(CT mode) clock to I-bus
29	CITSEL	I (PULL-DOWN)	(CT mode) select nominal or redundant I-bus
34	RBTDATA	I (PULL-DOWN)	Data to BT-bus
35	RBTEN	I (PULL-DOWN)	Enable BT-bus transmitter
30	RBRCLK	O	Clock from BT-bus
31	RBRDATA	O	Data from BT-bus
32	RBRVAL	O	Validity from BT-bus
33	RBRINIT	I (PULL-DOWN)	Initialise BT-bus receiver

OBT/OBDH PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
111	NIDS1n	I (PULL-UP) (CSCHMITT)	Nominal I-bus Discriminator Signal 1
110	NIDS2n	I (PULL-UP) (CSCHMITT)	Nominal I-bus Discriminator Signal 2
109	RIDS1n	I (PULL-UP) (CSCHMITT)	Redundant I-bus Discriminator Signal 1
108	RIDS2n	I (PULL-UP) (CSCHMITT)	Redundant I-bus Discriminator Signal 2
107	NRDS1n	I (PULL-UP) (CSCHMITT)	Nominal R-bus Discriminator Signal 1
106	NRDS2n	I (PULL-UP) (CSCHMITT)	Nominal R-bus Discriminator Signal 2
105	RRDS1n	I (PULL-UP) (CSCHMITT)	Redundant R-bus Discriminator Signal 1
104	RRDS2n	I (PULL-UP) (CSCHMITT)	Redundant R-bus Discriminator Signal 2
103	RR1n	O	R-bus driver 1
102	RR2	O	R-bus driver 2
101	RR3n	O	R-bus driver 3
100	RR4	O	R-bus driver 4
99	NRE	O	Nominal R-bus Enable
98	RRE	O	Redundant R-bus Enable
97	NBDS1n	I (PULL-UP) (CSCHMITT)	Nominal BT-bus Discriminator Signal 1
96	NBDS2n	I (PULL-UP) (CSCHMITT)	Nominal BT-bus Discriminator Signal 2
95	RBDS1n	I (PULL-UP) (CSCHMITT)	Redundant BT-bus Discriminator Signal 1
94	RBDS2n	I (PULL-UP) (CSCHMITT)	Redundant BT-bus Discriminator Signal 2
93	BR1n	O	BT-bus driver 1
92	BR2	O	BT-bus driver 2
91	BR3n	O	BT-bus driver 3
90	BR4	O	BT-bus driver 4
89	NBE	O	Nominal BT-bus enable
88	RBE	O	Redundant BT-bus enable

OBT CONTROL PIN LIST AND DESCRIPTIONS

No.	Name	Type	Description
121	TA0	I	Terminal Address bit 0 (MSB = I-bus bit 6)
122	TA1	I	Terminal Address bit 1
123	TA2	I	Terminal Address bit 2
124	TA3	I	Terminal Address bit 3
125	TA4	I	Terminal Address bit 4
126	TA5	I	Terminal Address bit 5
127	EXTFMT	I	Extended format Enable
128	EXTMLA1	I	Extended Memory Load Address 1 Enable
129	EXTMLA2	I	Extended Memory Load Address 2 Enable
130	OOINH	I	On/Off INHibit of MOLC commands
40	TEST	I	Tie to Ground (this input for test purposes only)
87	SIMUL	I (PULL-DOWN)	Simultaneously drive both busses
41	CTpRTn	I (PULL-UP)	CT mode when high, RT mode when low
36	MRSTn	I (PULL-DOWN) (CSCHMITT)	Master reset when low
112	LOSC	I (CSCHMITT)	Oscillator from user to drive OBT timeout
39	TIMEOUTn	O	Low when I-bus timeout
44	TAV	I (PULL-DOWN)	Terminal available (take low to disable responses from RTU kernal)

OBT POWER SUPPLY DISTRIBUTION PINS

No.	Name	Type	Description
55, 113	V_{DD}	P	Positive supply nominally +5 volts. Connect both pins.
14, 47, 80	V_{SS}	P	Power and signal ground. Connect all pins.

Notes: 1. CSCHMITT means CMOS Schmitt-trigger inputs.
2. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.59	-	-	0.102
A1	1.37	-	1.88	0.054	-	0.074
b	0.23	-	0.33	0.009	-	0.013
c	0.10	-	0.18	0.004	-	0.007
D1, D2	-	-	24.38	-	-	0.960
E	-	-	18.11	-	-	0.713
E2	-	20.32	-	-	0.800	-
e	-	0.63	-	-	0.025	-
L	6.35	-	7.11	0.250	-	0.280

XG533

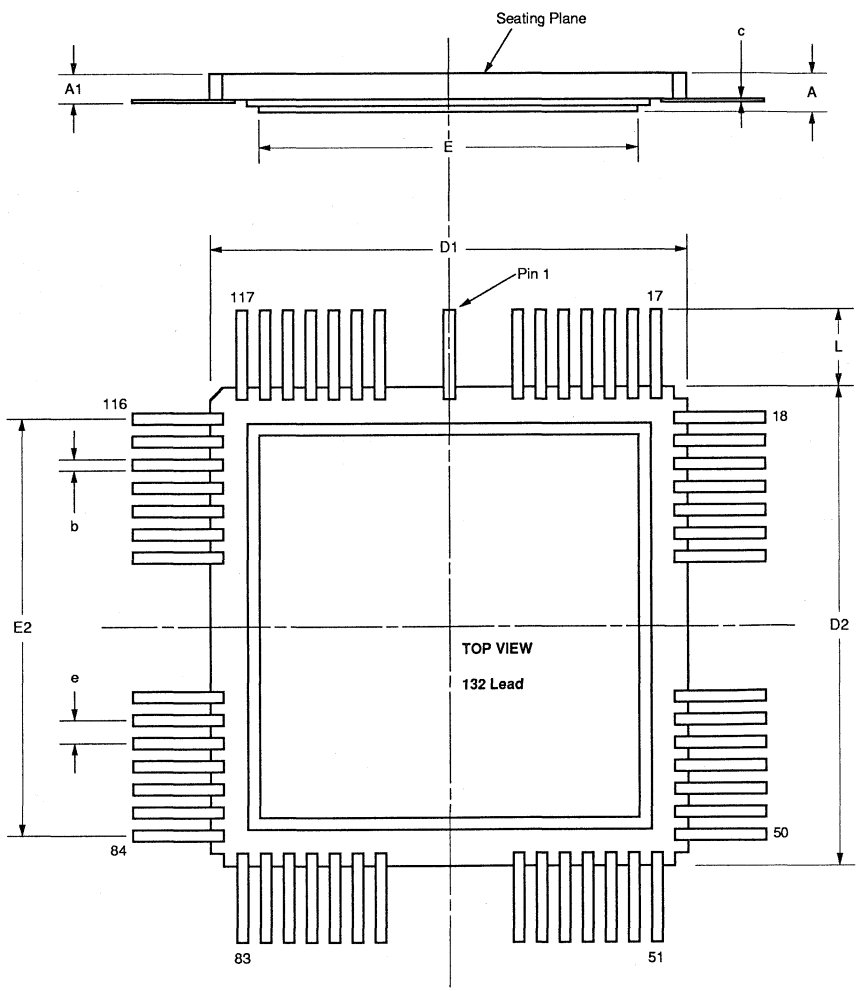


Figure 22: Package Dimensions

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 test method 1019 Ionizing Radiation (total dose).

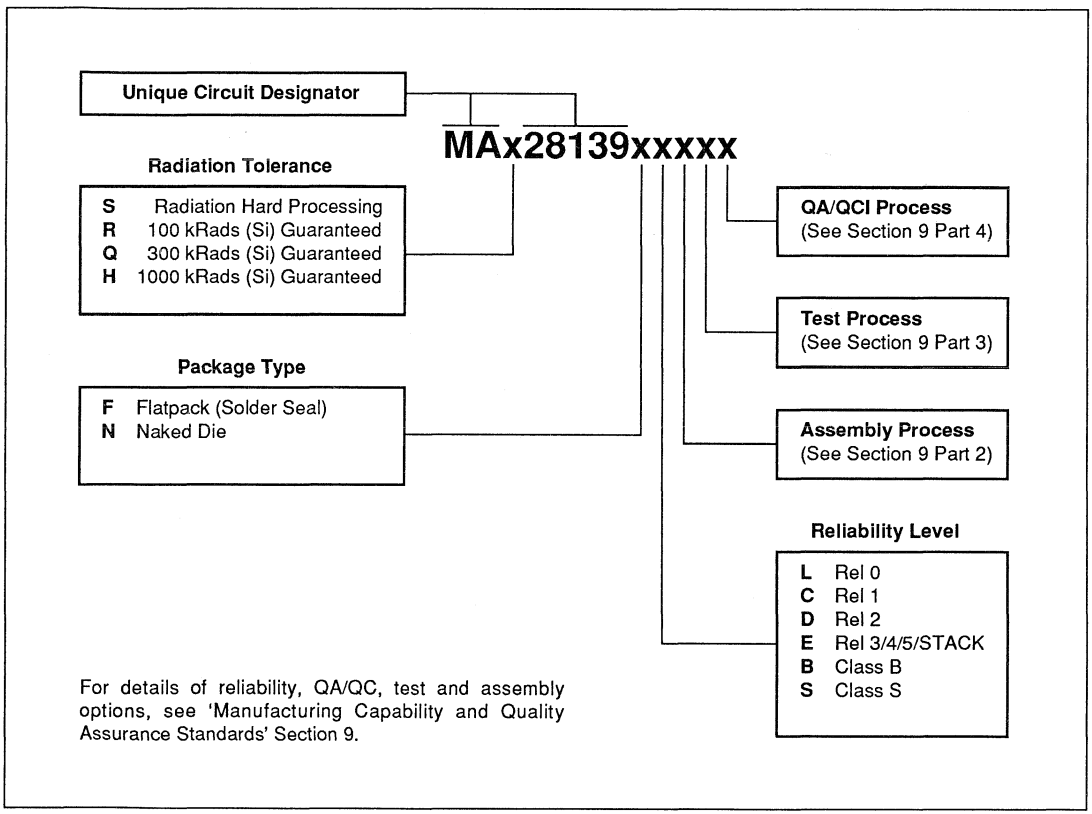
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 11: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

SYNONYMS

ASIC	Application Specific Integrated Circuit
BT-bus	Block Transfer Bus
CBR	CTU mode, block transfer bus, receive
CBT	CTU mode, block transfer bus, transmit
CIT	CTU mode, interrogation unit, transmit
CRR	CTU mode, response bus, receive
CT	Central terminal
DBI	Digital bus interface
DBU	Digital bus unit
ESA	European Space Agency
FET	Field effect transistor
FTC	Fault tolerant computer
GPS	GEC Plessey Semiconductors
I-bus	Interrogation bus
ICU	Intelligent control unit
IUB	Internal user bus
MA28138	Remote bus interface (RBI) ASIC
MA28139	OBDH bus terminal (OBT) ASIC
µP	Microprocessor
MSS	Marconi Space Systems - now Matra Marconi Space (MMS)
OBDH	On board data handling
OBT	OBDH bus terminal (MA28139)
PIU	Payload interface unit
R-bus	Response bus
RBI	Remote bus interface (MA28138)
RBR	RTU mode, block transfer bus, receive
RBT	RTU mode, block transfer bus, transmit
RIR	RTU mode, interrogation bus, receive
RRR	RTU mode, response bus, receive
RRT	RTU mode, response bus, transmit
RT	Remote terminal
SBC	Single board computer
VLSI	Very large scale integration

MA28140

PACKET TELECOMMAND DECODER

The MA28140 Packet Telecommand Decoder (PTD) is a single-chip implementation of the core part of a telecommand decoder, manufactured using GPS CMOS-SOS high performance, radiation hard, 1.5µm technology. The PTD is a full implementation of and fully compliant with the packet telecommand standard ESA PSS-04-107 and the telecommand decoder specification ESA PSS-04-151, these being derived from the corresponding CCSDS standards.

The PTD, which handles 6 NRZ TC input channels, processes the following layers:

Coding Layer

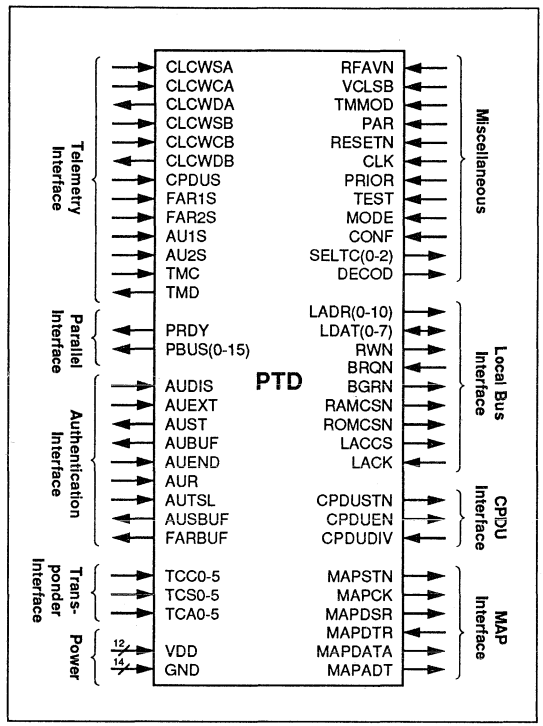
Transfer Layer

Segmentation Layer

Authentication Layer

Command Pulse Distribution

Some of these layers have a telemetry reporting mechanism. The processed TC segment can be transferred to the application either serially or in parallel.



FEATURES

- Single Chip Implementation of all TC Decoder Core Functions
- Built-in Authentication Unit
- Built-in Command Pulse Distribution Unit Core Logic
- Radiation Hard to 1MRads (Si)
- High SEU Immunity, Latch-up Free
- CMOS-SOS Technology
- Conforms to CCSDS Standards
- 6 NRZ TC Input Channels
- 50Kbps Bit Rate
- Low Power Consumption
- Single 5V Supply
- -55 to +125°C Operation

CONTENTS

REFERENCES

1. "Packet Telecommand Standard" ESA PSS-04-107, Issue 2, April 92.
2. "Telecommand Decoder Specification" ESA PSS-04-151, Issue 1, September 93.

1. INTRODUCTION

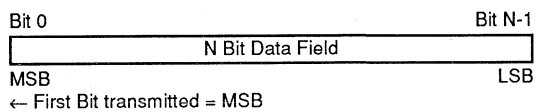
This document is the data sheet of the "Packet Telecommand Decoder", henceforth called the PTD.

The PTD is compatible with the ESA PSS-04-107 standard directly derived from the CCSDS recommendations. This standard is described in references 1 and 2. The data sheet is based on both documents for the description of the protocol. Nevertheless, it was impossible to include the whole reference documents in the data sheet, thus some specific points of the protocol or some descriptions of the recommended hardware implementation have not been included. The reader may find these points in the applicable documents.

CONVENTION

In this document the two conventions described in references 1 and 2 apply:

1. The first bit in the field to be transmitted (i.e. the most left justified bit when drawing a figure) is defined to be Bit 0. When the field is used to express a binary value, the Most Significant Bit (MSB) shall be the first transmitted bit of the field (i.e. Bit 0).



Note: Some of the external interfaces have parallel busses (LADR, LDAT, PBUS, SELTC) which have the opposite bit order specified, i.e. Bit 0 is The Least Significant Bit.

2. An 8-bit word (a byte) is called an OCTET.

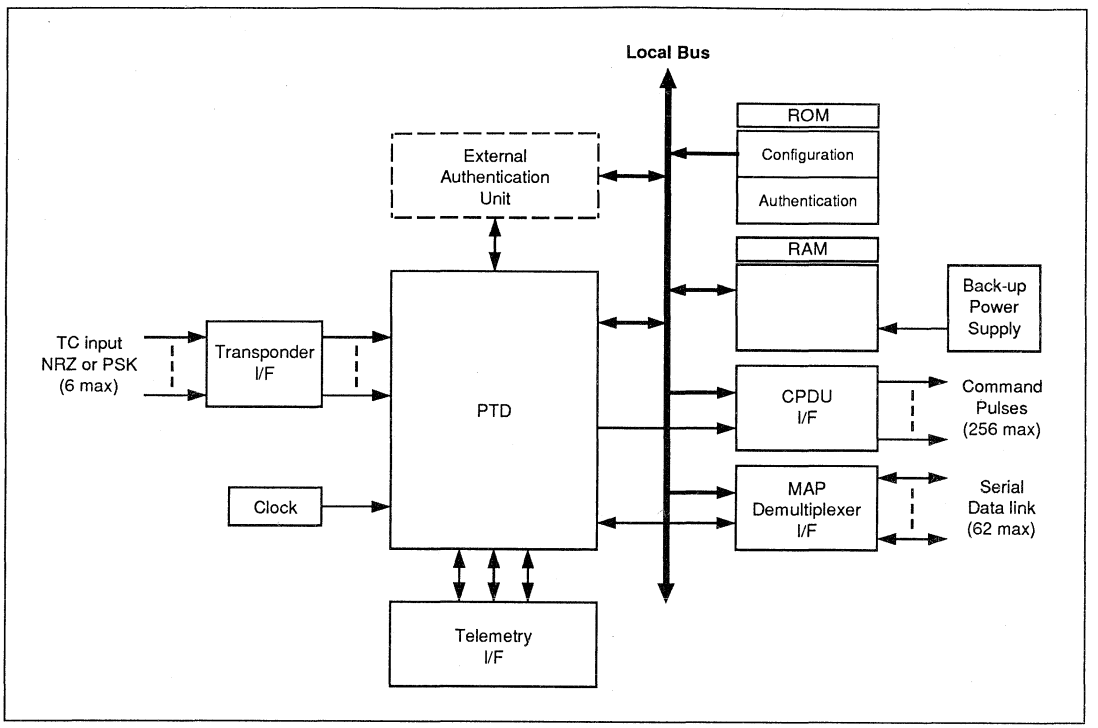


Figure 1: Block Diagram of a TC Decoder Subsystem

2. TC DECODER SUBSYSTEM OVERVIEW

An ESA/CCSDS Telecommand Decoder subsystem including the PTD and fulfilling the receiving-end functions established in the Packet Telecommand Standard (ref 1) is shown in Figure 1.

The PTD requires the following additional hardware to fulfil the requirements of the Telecommand Decoder Specification (ref 2):

- Transponder I/F including demodulators for PSK TC inputs.
- Telemetry I/F. The telemetry reporting signals can be directly connected to a Virtual Channel Multiplexer (ref 3).
- Command Pulse Distribution Unit I/F. This function performs decoding of commands present on the local bus and power amplification. The PTD ASIC associated with the CPDU I/F can manage 256 pulse outputs.
- MAP demultiplexer I/F. This interface is composed of a demultiplexer to provide the TC segment data to various Data Management System interfaces. The demultiplexer is controlled by the MAP data present on the Local Bus. The PTD ASIC can manage 62 different serial data interfaces (63 if AU is disabled).
- Memories. There are 2 different memories:
  - RAM (2Kx8) used to store the received TC data and protocol variables (programme authentication key for instance) and eventually to store the TC segment available for further processing by the Data Management System. If this memory is used to store the recovery LAC counter (Authentication function), it must be a non-volatile memory.
  - ROM (1Kx8) divided in two parts:
    - Configuration part, used to provide the Mission Specific Data.
    - Authentication part, used to provide the fixed Authentication key.
- External Authentication Unit (optional). Although an AU is implemented in the PTD, it is also possible to use an external AU if the mission requires a different authentication algorithm. This external unit accesses the RAM in order to authenticate a TC segment.

3. PTD ARCHITECTURAL OVERVIEW

Figure 2 describes the PTD functional architecture which features 7 major blocks described below. Figure 3 shows the CCSDS protocol layer architecture. The PTD deals with the Coding Layer, the Transfer Layer, the Authentication Layer, the Segmentation Layer and a part of the Packetisation Layer of the CCSDS protocol.

CODING LAYER BLOCK

The coding layer block multiplexes the 6 physical TC channel inputs and fulfils the coding layer function described in section 5 of ref.1.

The main tasks performed by the PTD at this level are:

- Start sequence detection and selection of the first active TC input.
- Codeblock error detection and correction.
- Valid codeblock transfer to the above layer.
- Generation of part of the FAR and CLCW status.

TRANSFER LAYER BLOCK

This level is concerned with the processing of the frames received from the coding layer and fulfils the transfer layer function described in section 6 of ref.1.

At this level, the PTD performs the following tasks:

- Clean frame validation.
- Legal frame validation.
- Frame analysis report mechanism.
- Reporting word (16 bit CLCW and part of 32 bit FAR) generation.

AUTHENTICATION UNIT BLOCK

This block (which is optional and can be disabled permanently or during flight) is concerned with the segment data protection, it enables the spacecraft to authenticate the received data. The authentication concept is the "plain text with appended signature" approach, described in Section 8 of ref. 2.

In the PTD architecture this function is implemented on chip. However, a specific interface allows authentication to be performed externally - if another coding algorithm is to be used, the on-chip block can be disabled and an external authentication system can be used.

The block generates a reporting word (Authentication Status = 80 bits) and part of the 32 bit FAR.

SEGMENTATION LAYER BLOCK

This block implements only some of the segmentation layer functions described in section 7 of ref.1. Its purpose is to manage the back-end buffer shared with the FARM-1 block of the transfer layer and to implement the MAP interface in order to demultiplex (with external hardware) the segments dedicated to the different spacecraft applications.

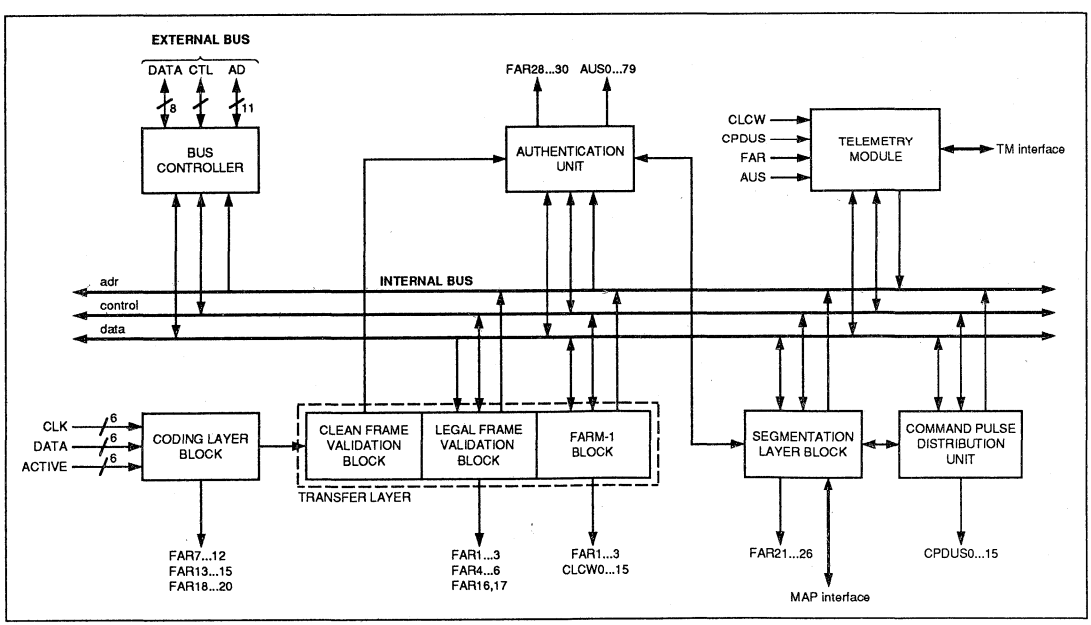


Figure 2: PTD Internal Architecture

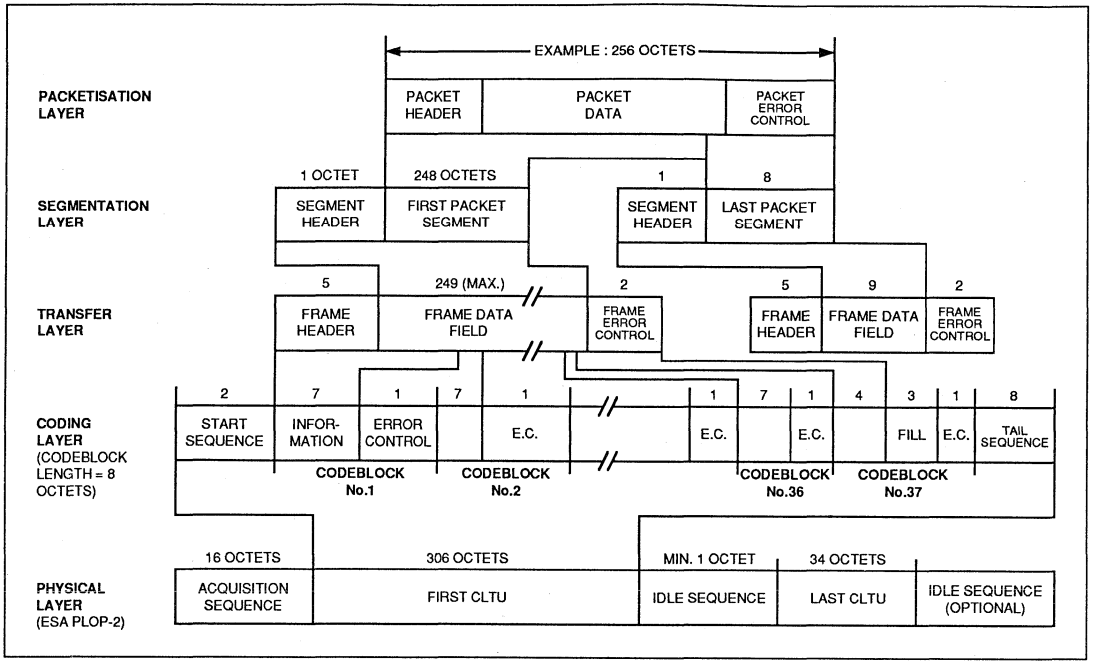


Figure 3: CCSDS Protocol Layer Architecture

COMMAND PULSE DISTRIBUTION UNIT

The CPDU is integrated into the PTD ensuring higher reliability for this critical function (direct telecommand for spacecraft reconfiguration) than if implemented in an external chip. The critical commands executed by the CPDU are received in specific packets. The CPDU responds to the MAP identifier 0, and to a mission dependent application process identifier (stored in ROM). No segmentation is accepted, the commands must be contained in an unsegmented package. The unit generates a reporting word (CPDU Status = 16 bits).

BUS CONTROLLER

This block is the interface between external memories and on chip modules. Its different functions are:

- address decoding.
- internal and external bus access arbitration.

TELEMETRY MODULE

This block is the interface with the telemetry subsystem. It manages the data report storage using double buffered registers.

4. PTD FUNCTIONAL DESCRIPTION

4.1 CODING LAYER

Overview of the Layer

The coding layer provides the forward error correction capability and synchronisation services used by the Transfer layer. Each Transfer Frame is encoded/embedded in one CLTU (Command Link Transmission Unit), which is the protocol-data unit of the coding layer. At the receiving end of the Coding Layer, a "dirty" symbol stream (plus control information on whether the physical channel is active or inactive) is received from the layer below. Searching for the Start Sequence, the coding layer finds the beginning of a CLTU and decodes the TC Codeblocks. As long as no errors are detected, or errors are detected and corrected, the coding layer passes "clean" octets of data to the Transfer layer. Should any codeblock contain an uncorrectable error, this Codeblock is abandoned and considered as Tail Sequence, no further data is passed to the layer above and the Coding Layer returns to a Start Sequence searching mode until it detects one. The coding layer also generates part of the CLCW and FAR status.

The PTD can handle up to 6 TC input interfaces, the data bit rate on these inputs should not exceed 50 Kbits per second when using the Authentication Unit. If the Authenication unit is not used the symbol rate could exceed 200kBits/sec (not guaranteed).

Standard Data Structures Within the Layer

A CLTU is made up of three distinct protocol data elements:

- one 16-bit Start Sequence,
- one or more TC Codeblocks of a fixed length of 8 octets to encode the protocol data unit from the layer above,
- one Tail Sequence of length equal to that of the TC Codeblock, i.e. 8 octets.

Start Sequence	First Codeblock	.....	Last Codeblock	Tail Sequence
16 Bits	Variable Number of Codeblocks			8 Octets

The Start Sequence marks the beginning of the TC Codeblock field within a CLTU. It consists of a 16-bit synchronisation pattern represented in hexadecimal as EB90, where the first transmitted octet is EB.

The TC Codeblock field consists of one or more TC Codeblocks. The codeblock length of received data is fixed and set to 8 octets (information field: 7 octets).

	P0 (MSB) P6	P7 (LSB)
Information Field	Error Control Field 7 parity bits	Filler Bit
7 Octets	1 Octet	

The Tail Sequence marks the end of the TC Codeblock Field within a CLTU. The length of the Tail Sequence is that of a TC Codeblock. Reference 1 specifies that its pattern should be alternating "zeros" and "ones", ending with a "one" (55 .... 55 in hexadecimal), but any double error codeblock, or single error codeblock with filler bit equal to 1 will be interpreted as Tail Sequence by the PTD.

Standard Procedures Within the Layer

Synchronization and TC Input Selection

Synchronization is performed by the start sequence detection simultaneously on all active TC inputs.

The start sequence detection allows one bit error anywhere in the pattern. Furthermore, due to NRZ coding ambiguity, it is possible to detect the complemented start sequence pattern in order to choose between positive or negative representation for further NRZ data processing. If an inverted pattern is detected, the following bit stream is inverted until the tail sequence.

TC inputs selection locks the selection multiplexer on the first TC channel where the start sequence is found. The selection mechanism is restarted once a tail sequence or a codeblock rejection has been detected. Furthermore, in order not to remain locked on a TC channel selection in case of RF receiver breakdown, a timeout mechanism is provided - if the TC channel clock is not detected after a certain time, the TC selection mechanism is reactivated in order not to remain locked on an inactive channel.

The time-out value between two successive edges of the TC channel clock is as follows (Tck is the PTD clock period): 3932160 Tck < TC clock timeout < 4587520 Tck. With a system clock frequency Fck of 4 MHz: 0.983 s < TC clock timeout < 1.147 s.

Priority Mode

Two different modes are provided to perform the TC channel selection selectable with a configuration input called PRIOR:

- No priority mode (PRIOR=0)

The 6 channels 0-5 have the same priority. The search for a Start Sequence is performed on all active TC channels simultaneously.

- Priority mode (PRIOR=1)

Two inputs have priority. The selection is compliant with the following rule:

TC0 > TC1 > TC2 = TC3 = TC4 = TC5

Priority mode means that the rules of the no priority mode apply when:

- As soon as the TC active signal of TC0 is true, the TC input mechanism is locked on this input even if another input was already selected (this means that the 5 other channels are inhibited). The TC0 input remains selected until:

a1 - its TC active signal becomes inactive or
b1 - its bit clock has not been received for a period = TC clock timeout or,
c1 - no valid synchronization pattern has been detected for a period = TC active timeout or,
d1 - a tail sequence or a codeblock rejection has occurred.

Upon events (a1) and (d1), the selection logic returns to the search state.

Upon events (b1) and (c1), the selection logic ignores the TC0 input until the event (a1) occurs.

- As soon as the TC active signal of TC1 is true, this input is selected, even if another lower priority input was already selected (not including TC0). The TC1 input remains selected until:

a2 - its TC active signal becomes inactive or,
b2 - its bit clock has not been received for a period = TC clock timeout or,
c2 - no valid synchronization pattern has been detected for a period = TC active timeout or,
d2 - a tail sequence or a codeblock rejection has occurred or,
e2 - the occurrence of TC0 active signal.

Upon events (a2) and (d2), the selection logic returns to the search state.

Upon event (e2) the TC1 input is ignored and the TC0 input is selected as mentioned previously.

Upon events (b2) and (c2), the selection logic ignores the TC1 input until the event (a2) occurs.

The TC clock time-out value between two successive edges of the TC channel clock shall be as follows (Tck is the PTD clock period):

3932160 Tck < TC clock timeout < 4587520 Tck

With a system clock frequency fck of 4 MHz:

0.983 s < TC clock timeout < 1.147 s.

The TC active time-out value between two successive synchronization patterns being detected is as follows (Tck is the PTD clock period):

334233600 Tck < TC active timeout < 335399960 Tck

With a system clock frequency Fck of 4 MHz:

83.558 s < TC active timeout < 83.850 s.

Codeblock Decoding

Codeblock decoding is performed for each received codeblock. At the sending end, a systematic block coding procedure processing 56 bits per Codeblock and generating 7 parity check bits per Codeblock is used. The parity check bits are then complemented and placed into the codeblocks: P0 (MSB) through P6 are located in the first seven bits (MSBs) of the last octet of the codeblock. The last bit of the last octet, P7 (LSB), is a filler bit appended to complete the 8-bit Error Control Field. This Filler Bit should normally be a zero, except for the Tail Sequence. The code is a (63,56) modified Bose-Chaudhuri-Hocquenghem (BCH), based on the following polynomial generator: $g(x)=x^7+x^6+x^2+1$. A single error correction & double error detection mode is provided by using this code.

The following table describes the Decoding Strategy of the codeblocks:

ERRORS DETECTED	FILLER BIT VALUE	DECISION
no errors	ignored	codeblock accepted
even number of errors	ignored	codeblock rejected
odd number of errors with a binary syndrome value equal to all zeros	ignored	codeblock rejected
odd number of errors with a binary syndrome value different from all zeros	0	codeblock accepted correction of a single error
odd number of errors with a binary syndrome value different from all zeros	1	codeblock rejected

CLTU Management

CLTU decoding consists of the states and events summarized in the following table and state diagram:

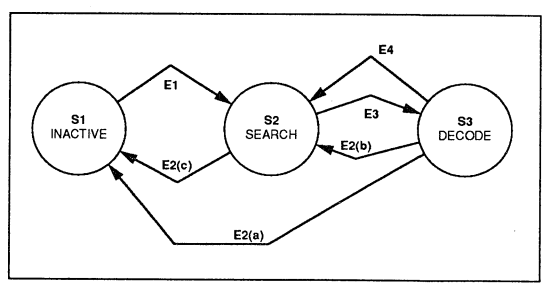


Figure 4: CLTU Decoder State Diagram

State Number	State Name	State Definition
S1	INACTIVE	All telecommand channels are inactive (no bit lock is achieved) or no bit modulation is detected.
S2	SEARCH	Incoming bit stream is searched, bit by bit, for the Start Sequence pattern.
S3	DECODE	Codeblocks, which are either free of error or which can be corrected, are received and decoded, and their information octets are transferred to the layer above

Event Number	Event Name	Event Definition
E1	CHANNEL ACTIVATION	Bit modulation is detected and bit lock is achieved: telecommand bit stream is present
E2 (a) (c)	CHANNEL DEACTIVATION	Deactivation of the TC Active Signal
(b)	CLTU ERROR	More than 37 codeblocks accepted in the CLTU or Timeout on the TC Clock signal or Activity on a channel having higher priority in priority mode
E3	START SEQUENCE FOUND	The Start Sequence pattern has been detected, signalling the beginning of the first codeblock of the CLTU
E4	CODEBLOCK REJECTION	A codeblock is found uncorrectable (erroneous codeblock or tail sequence). No information octet from this codeblock is transferred to the layer above

Codeblock transfer is performed in a serial way to the above layer (Transfer layer). Two indication signals are provided to the above layer - one indicating the whole frame duration, the other asserted each time a 7 octets block is being transferred.

The following rules apply to the data transfer between the Coding Layer and the Transfer Layer:

• When the first Candidate Codeblock is affected by an event E4 or by an event E2, the CLTU is abandoned. No Candidate Frame is transferred to the Transfer Layer.

• When the first Candidate Codeblock is found to be error free, or if it contained one error which has been corrected, its information octets (i.e. 7 octets) are transferred to the Transfer Layer. The decoding of the CLTU continues until one of the following events occurs:

1- when an event E4 (codeblock rejection) occurs for any of the 37 possible Candidate Codeblocks the decoder returns to the search state S2 with the following actions:
- The codeblock is abandoned
- No information from that codeblock is transferred to the layer above
- The Coding Layer indicates to the Transfer Layer the end of transfer of the Candidate Frame.

2- when an event E2 (channel deactivation) occurs the decoder returns to the inactive state (for the channel) with the following actions:
- The CLTU is aborted,
- The CLTU is reported as abandoned,
- A signal is sent to the Transfer Layer to indicate that the entire block of octets making up the Candidate Frame must be erased.

3- When an event E2(b) (CLTU error) occurs, the decoder returns to the search state with the following actions:
- The CLTU is aborted,
- The CLTU is reported as abandoned,
- A signal is sent to the Transfer Layer to indicate that the entire block of octets making up the Candidate Frame must be erased.

A CLTU error occurs in the following cases:
- More than 37 codeblocks have been accepted in the CLTU,
- A timeout on the TC clock signal occurs,
- Activity on a channel having higher priority is detected in priority mode.

The DECOD output is activated when the CLTU decoder state is S3.

4.2 TRANSFER LAYER

Overview of the Layer

The Transfer Layer implements the following sublayers:
- The Frame Error Control Sublayer which ensures that only "clean" frames are transferred to the sublayer above by using a CRC error syndrome verification.
- The Frame Header Sublayer verifies the conformity of the relevant frame header fields by using the Legal Frame Validation process before passing the frame to the FARM1.
- The "Frame Acceptance and Reporting Mechanism One" or FARM1 ensures that frames are processed in the correct sequence.

There are three types of TC transfer frames:
- two types for the Sequence-Controlled Service: AD and BC frames
- one type for the Expedited Service: BD frames

The Sequence-Controlled Service is used for normal spacecraft communications. It concerns essentially TC Transfer Frames carrying TC segments: the AD frames. To configure the AD machine, special control frames are used called BC frames.

The Expedited Service is used for recovery in the absence of the telemetry downlink or during unexpected situations. It is only concerned with TC transfer frames carrying TC segments: the BD frames.

Standard Data Structures Within the Layer

The major fields of the TC Transfer Frame are shown below:

5 octets	1 to 249 octets	2 octets
Frame Header	Frame Data Field	Frame Error Control Field

Frame Header

The structure of the frame header is given below:

2 octets					1 octet		1 octet	1 octet
version number	bypass flag	control command flag	reserved field A	spacecraft ID	virtual channel ID	reserved field B	frame length	frame sequence number
2	1	1	2	10	6	2	8	8

A description of the fields of the frame header is given below:

• Version number, Reserved field A and Reserved field B should always be 00 (ref 1).

• Bypass flag and control command flags. Their values are given in the next table:

Bypass Flag	Control Command Flag	Interpretation
0	0	AD frames
0	1	ILLEGAL
1	0	BD frames
1	1	BC frames

• Spacecraft identifier. This field provides the identification of the spacecraft being commanded.

• Virtual channel identifier. It is used as a spacecraft sub-identifier. It can provide an identification of the spacecraft telecommand chain selected for operating the spacecraft.

• Frame length. This field specifies the number of octets contained within the entire TC transfer frame:
Field Value = (Total number of octets) - 1

• Frame sequence number. This number is denoted as N(S). It is set to different values:
- for AD frames it should be set to the Transmitter Frame Sequence Number and it is compared to the Receiver Frame Sequence Number V(R) stored in the PTD, to control the transfer of a sequence of frames (see the FARM-1 process)
- for BC and BD frames it should be set to all zeros.

Except for the bypass and control command flags, the values of the first three header octets are programmed in the external ROM.

In the abbreviations AD, BD and BC, A stands for Acceptance check of N(S), B stands for Bypass of A, C stands for Control and D stands for Data. AC is an illegal combination because Control Commands cannot reliably use a transfer service which they are meant to modify.

Frame Data Field

The frame data field is of variable length from a minimum of 1 octet to a maximum of 249 octets. When the frame is a data frame (type AD or BD), it contains a TC segment. When the frame is a BC frame, this field can contain 2 control commands to configure the FARM-1 process:

• the UNLOCK command. The FARM-1 has a built in mechanism which will go into a Lockout state whenever it receives a type-AD frame containing a frame sequence number N(S) outside the limits of the FARM-1 Sliding Window. The UNLOCK command provides a mechanism to reset the Lockout condition. The UNLOCK command is encoded as a single octet with the value: 00000000.

• The SET V(R) command. The SET V(R) command allows V(R) to be preset to any desired value. The SET V(R) command is encoded as three octets with the values:

10000010 00000000 XXXXXXXX

The value to be set into V(R) is stored in the third octet.

Frame Error Field

The frame error field is a mandatory 16-bit field which occupies the two trailing octets of the TC Transfer Frame. It is a cyclic redundant code (CRC) generated with the polynom $X^{16}+X^{12}+X^5+1$ with the shift register being initialised to all ones before processing each frame (refer to ref 2 for a complete description of this field). The CRC is only used for error detection by the frame and not for error correction.

Standard Procedures Within the Layer

The Clean Frame Validation Process

On receiving a new frame, the Clean Frame Validation process performs the following tasks:

- the number of octets in the frame is checked to be greater than 7 octets,
- the transfer frame is assumed to be a version 1 frame,
- the frame length field is checked to be compliant with the real number of octets of the frame,
- the number of fill octets is verified to be minimum zero and maximum six,
- the fill octets are removed,
- the CRC error syndrome verification is carried out.

All candidate frames passing all the preceding validation checks are declared clean and transferred immediately to the Legal Frame Validation process. Frames failing any of the preceding tests are declared dirty and are erased.

The Legal Frame Validation Process

On receiving a clean frame, the Legal Frame Validation process performs the following validation checks:

- the version number is checked to be as defined in the ROM,
- the reserved fields A and B are checked to be as defined in the ROM,
- the value of the spacecraft ID is checked to be as defined in the ROM,
- the value of the Virtual Channel ID is checked to be as defined in the ROM and by the VCLSB input,
- the Bypass and Control Command flags must combine legally,
- the BC frames must contain a valid control command (either UNLOCK or SET V(R)),
- for a BC or BD frame the Frame Sequence Number field must be set to all zeros.

The LSB of the VC ID is indirectly defined from a dedicated pin VCLSB; it allows easy configuring of a pair of redundant TC decoders.

- VCLSB = 1: The VC ID LSB read from the ROM is inverted.
- VCLSB = 0: The VC ID LSB read from the ROM is not inverted.

All candidate frames passing all the preceding validation checks are declared legal and transferred immediately to the FARM-1 process. Frames failing any of the preceding tests are declared illegal and erased.

The FARM-1 Process

THE FARM-1 VARIABLES

The Frame Acceptance and Reporting mechanism (FARM-1) is described by a finite state machine represented by the FARM-1 state table. The FARM-1 maintains a set of variables which are described below:

• The State. This may be one of the following:

- Open (S1)
- Wait (S2)
- Lockout (S3)

This variable represents the state of the FARM-1 automaton. In Open State, the FARM-1 accepts frames and passes them to the above layer. In Wait State, there is no buffer space available in which to place any further received data of type AD. The protocols leaves the Wait State upon receipt of a buffer release signal from the Higher Layer. Lockout is entered if the protocol machine detects an error. It is a safe state in that no user data (AD frames) will be accepted or transferred to the Higher Layer. The only accepted data frames are the BD frames, but even in this case the protocol machine remains in lockout state. The protocol machine leaves the Lockout State upon receipt of an UNLOCK control command.

• The Lockout Flag. This is set to 1 whenever the protocol is in the Lockout State.

• The Wait Flag. This is set to 1 whenever the protocol is in Wait State.

• The Retransmit Flag. This is set to 1 whenever the protocol machine knows that an AD frame has been lost in transmission or has been discarded because there was no buffer space available. This flag is reset to 0 upon the successful receipt of a frame with N(S)=V(R), the receipt of a SET V(R) control command (unless in Lockout State) or receipt of an UNLOCK control command.

• FARM B counter. This is incremented whenever a valid BD or BC frame arrives. This counter is a 2 bit wraparound counter.

• Receiver Frame Sequence Number V(R). This records the value of N(S) expected to be seen in the next AD frame.

• The buffer management variable. The PTD maintains a flag indicating the number of the back end buffer. The AUBUF output pin provides the value of this flag (the back end and front end buffers are represented in Figure 6). The number of the TC channel on which the data stored in the back-end buffer has been received is provided on the output pins (SELTC2-0).

• FARM Sliding window variables. The purpose of these are to protect FARM-1 against the unauthorised transfer of a sequence of frames such that the Frame Sequence Number N(S) of one or more of these frames will exceed the current value of the V(R) counter. The FARM Sliding Window concept applies only to AD frames.

The FARM Sliding Window is defined in terms of two variables:

- the width of the positive part referred to as PW
- the width of the negative part referred to as NW

The FARM Positive window area starts with V(R) and extends PW frames in the positive direction. The FARM Negative window starts at V(R) - 1 and extends NW frames in the negative direction.

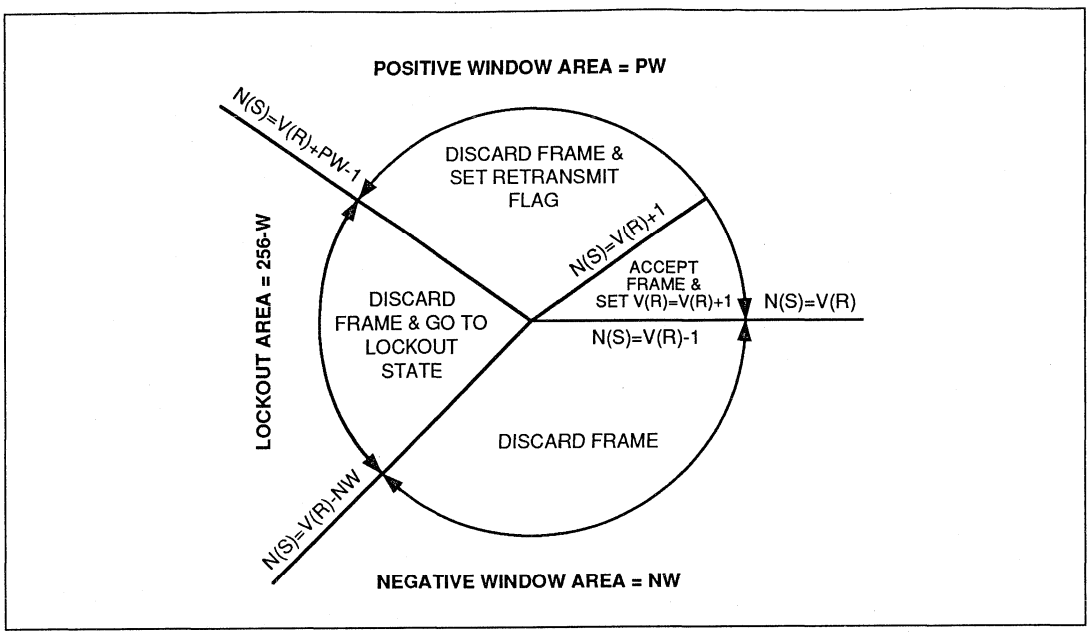


Figure 5: The FARM Sliding Window Concept

A Frame Sequence Number N(S) falls outside the FARM Sliding Window i.e. in the Lockout Area when:

$$N(S)>V(R)+PW-1$$
$$N(S)<V(R)-NW$$

In this case, the Lockout flag is set.

When N(S) falls inside the FARM Sliding Window, one of the following three cases can occur:

• First case

$$N(S)=V(R)$$

The frame is accepted

• Second Case

$$N(S)>V(R) \text{ and } N(S)\leq V(R)+PW-1$$

The frame is in the positive window and does not contain the expected Frame Sequence Number. The Frame is discarded and the retransmit Flag is set.

• Third Case

$$N(S)<V(R) \text{ and } N(S)\geq V(R)-NW$$

The frame is in the negative window and is discarded without any other action being taken.

THE FARM-1 PROCESS DESCRIPTION

At the user end of the FARM-1 process the TC segments are delivered as a buffer of accepted data. No distinction is made between a TC segment delivered by means of an AD frame and one delivered by a BD frame. However, the management of the common FARM-1 back end buffer is affected as follows:

• BD Frames:
When a frame of this type is accepted by the FARM-1, the TC segment it contains shall be placed in the back end buffer of the FARM-1 even if this buffer still contains data (partially read or not) in which case this data will be erased, an abort signal sent to the Segment Layer to signal the erasure and the new data signalled as arrived. This implies an Event E10.

• AD frames:
When a frame of this type is accepted by the FARM-1, the TC segment it contains is placed in the back end buffer of the FARM- 1 only when the buffer is available (empty). If the buffer still contains data, the newly arrived frame is discarded (erased) as shown by the FARM-1 state table (Event E2 in table 1).

The definitions used in the FARM-1 State Table are listed below:

• "Valid frame arrives" means that the Legal Frame Validation Sublayer has placed a legal frame in the front-end buffer. If the frame is a data frame (AD or BD) and if the FARM-1 accepts it, the back end buffer is allocated for the data.

• "Accept" for an AD frame is subject to a buffer available signal. When no back end buffer is available (Event E2) the frame is discarded. The data is then made available for the Authentication Layer, or the Segmentation Layer if Authentication is disabled.

• "Accept" for a BD frame means that the TC segment is placed in the back end buffer even when this buffer still contains data, in which case this previous data is erased (event E10). The Wait concept does not apply to BD frames. The data is available for the Authentication Layer, or the Segmentation Layer if Authentication is disabled.

State Name				OPEN	WAIT	LOCKOUT
Main Feature of State				Normal state to accept frames	Wait Flag is on	Lockout Flag is on
State Number				(S1)	S(2)	S(3)
Event	**Conditions**		**Event Number**	**OPEN**	**WAIT**	**LOCKOUT**
Valid AD frame arrives	N(S)=V(R)	A buffer is available for this frame	E1	Accept frame, V(R):=V(R)+1 Retransmit Flag:=0 (S1)	Not applicable	Discard (S3)
	N(S)=V(R)	No buffer is available for this frame	E2	Discard, Retransmit Flag:=1, Wait Flag:=1 (S2)	Discard (S2)	Discard (S3)
	N(S)>V(R) N(S)≤V(R) i.e. inside part of sliding N(S)<	and +PW-1 positive window and >V(R)	E3	Discard, Retransmit Flag:=1 (S1)	Discard (S2)	Discard (S3)

Table 1: The FARM-1 State Table

Event	Conditions	Event Number	OPEN	WAIT	LOCKOUT
(Cont') Valid AD frame arrives	N(S)<V(R) and N(S)≥ V(R)-NW i.e. inside negative part of sliding window	E4	Discard (S1)	Discard (S2)	Discard (S3)
	N(S)>V(R)+PW-1 and N(S)<V(R)-NW i.e. outside sliding window	E5	Discard Lockout Flag:=1 (S3)	Discard Lockout Flag:=1 (S3)	Discard (S3)
Valid BD frame arrives*		E6	Accept, Increment FARM-B Counter (S1)	Accept, Increment FARM-B Counter (S2)	Accept, Increment FARM-B Counter (S3)
Valid Unlock BC frame arrives		E7	Increment FARM-B Counter, Retransmit Flag:=0 (S1)	Increment FARM-B Counter, Retransmit Flag:=0, Wait Flag:=0 (S1)	Increment FARM-B Counter, Retransmit Flag:=0, Wait Flag:=0, Lockout Flag:=0 (S1)
Valid Set V(R) to V*(R) BC frame arrives		E8	Increment FARM-B Counter, Retransmit Flag:=0 V(R):=V*(R) (S1)	Increment FARM-B Counter, Retransmit Flag:=0 Wait Flag:=0 V(R):=V*(R) (S1)	Increment FARM-B Counter, (S3)
Invalid frame arrives		E9	Discard (S1)	Discard (S1)	Discard (S3)
Buffer release signal		E10	Ignore (S1)	Wait Flag:=0 (S1)	Wait Flag:=0 (S3)
CLCW report time		E11	Report value of: V(R), Lockout Flag, Wait Flag, Retransmit Flag, FARM-B Counter (S1)	Report value of: V(R), Lockout Flag, Wait Flag, Retransmit Flag, FARM-B Counter (S2)	Report value of: V(R), Lockout Flag, Wait Flag, Retransmit Flag, FARM-B Counter (S3)

* Note: Event E6 implies that Event E10 also occurs. When in state S2, an event E6 will lead to state S1.

Table 1: The FARM-1 State Table (continued)

Buffer Management

Once the data is validated (Clean, Legal and Frame Validation processes passed), it is transferred from the front-end buffer to the back-end buffer for use by the segmentation layer. Only one back-end buffer is managed by the PTD. This mechanism is depicted in figure 6 below:

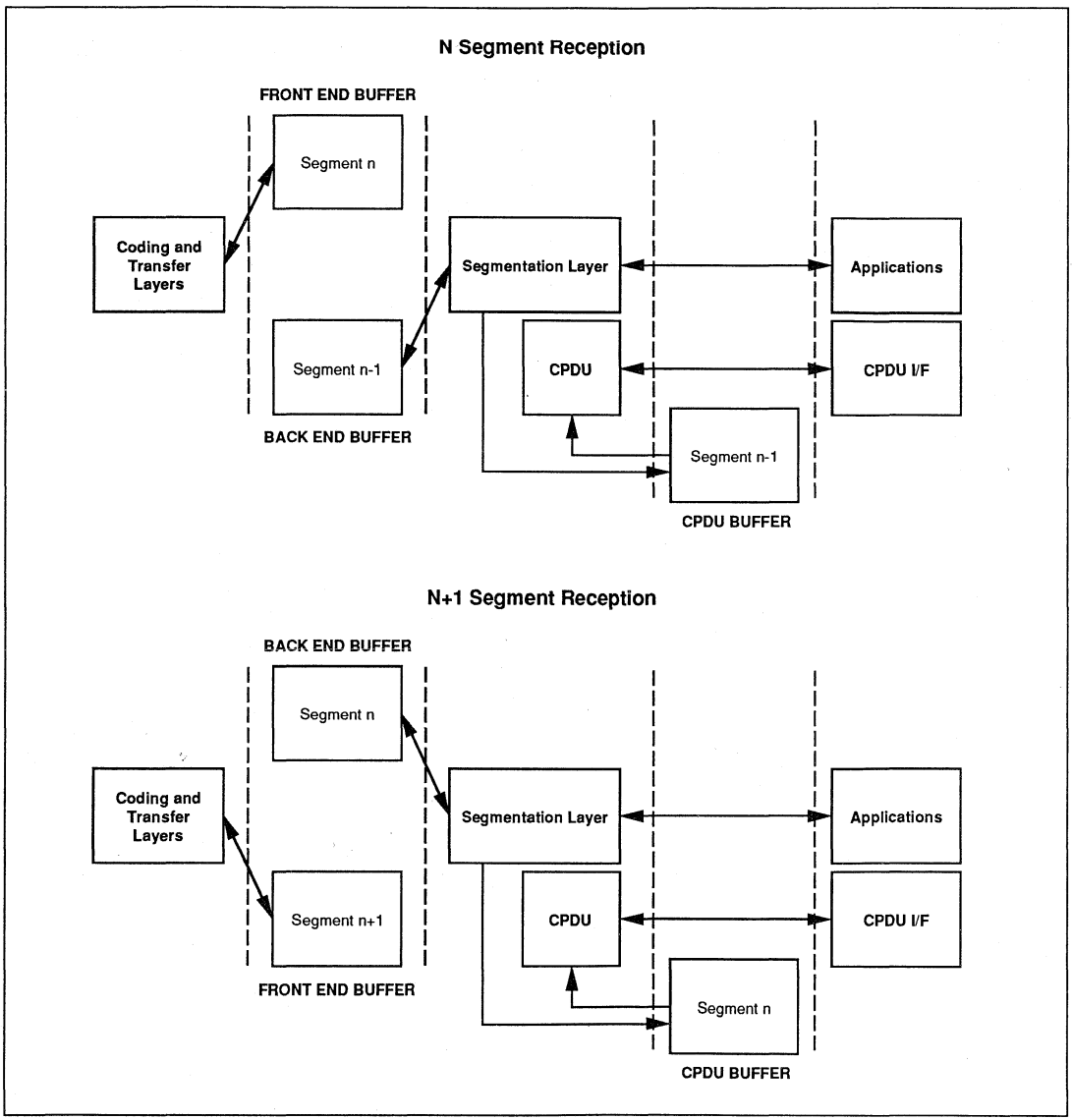


Figure 6: Buffer Management

4.3 AUTHENTICATION LAYER

Structure of the Authenticated Segments

The TC segment is the protocol data unit of the Segmentation Layer. The general format of an authenticated TC Segment is specified in Section 10 of ref.1. The particular format of an authenticated TC segment for the PTD is the following:

(a) The length of the signature field of the Authentication Tail is 5 octets.

(b) The length of the Authentication Tail is 9 octets (5 octets for the signature + 4 octets for the LAC); the maximum length of the TC Segment is 249 octets (Segment Header (1 octet) + Segment Data Field (239 octets) + Authentication Tail (9 octets)), and its minimum length 10 octets (Segment Header (1 octet) + Authentication Tail (9 octets)).

SEGMENT HEADER		SEGMENT DATA FIELD	SEGMENT TRAILER
Sequence Flags	MAP Identifier		(optional)
2 bits	6 bits	variable	9 octets

<----------1 octet ----------><----- from 9 to 248 octets ------>

The segment trailer is optional and has a fixed length of 9 octets. The following table summarizes the management of the Segment Trailer.

Type of Authentication	Type of Frame	Segment Trailer
Internal AU	Authenticated frame	segment trailer (9 octets length)
	Not authenticated frame	no segment trailer
External AU	Authenticated frame	segment trailer (9 octets length) if AuTsI=0, no segment trailer if AuTsI=1
	Not authenticated frame	no segment trailer
AU disable	All	no segment trailer

The selection of MAPs that are deemed to carry authenticated TC segments takes into account the possibility to associate MAP IDs in pairs when packet re-assembly is required. Therefore, authenticated MAPs are selected by pairs, using the 5 LSBs of the MAP identifier field of the Segment Header. The selection mechanism is such that it will point at the last pair of MAP identifiers (counting upwards from MAP 0) that carries authenticated segments. The value identifying this particular pair of identifiers is called the Authenticated MAP ID Pointer and is stored in ROM.

For example, selecting MAP 4 (i.e. Authenticated MAP ID Pointer = 4) means that the first 5 pairs of MAPs (i.e. MAP 0 and 32, MAP 1 and 33, MAP 2 and 34, MAP 3 and 35, MAP 4 and 36) are expected to carry authenticated TC segments.

Overview of the Layer

This optional layer is implemented on-chip but a connection to an external Authentication Unit is also implemented in case another implementation is desired. The choice of the AU is done by means of a dedicated configuration input AUEXT:

- AUEXT = 1: the internal AU is disabled and the external AU is used,
- AUEXT = 0: the internal AU is used and the external AU is disabled.

MAP 63 is reserved for AU configuration commands when authentication is disabled. It is possible to bypass this layer (when no authentication is required) by means of a dedicated configuration input AUDIS. In this case, segments are passed directly to the segmentation layer .The values of the AUDIS pin are:

- AUDIS = 1: the internal or external AU is disabled,
- AUDIS = 0: the internal or external AU is enabled.

When the AU is disabled, the TC segment does not have an AU tail (the last nine octets are not deleted), the Authenticated MAP ID Pointer has no meaning and MAP 63 is considered as a standard MAP (the data is output on MAP number 63 without removing the AU tail).

An 80 bit length status, AUS, is generated by this block and fetched by the telemetry system in order to send it back to the ground segment.

The Authentication Processor

The authentication method specified in references 1 and 2 consists of generating a 40-bit digital signature using a transformation under a secret key applied to the TC Segment. This authentication signature is appended to the TC segment and guarantees to the recipient that the TC Segment is authentic with respect to its sender and its contents.

An incoming TC Segment is authenticated by performing the same transformation made by the transmitting end, and by comparing the received signature with the onboard-generated one. A functional diagram of the Authentication Processor is shown below. There are four main parts:

- the Hashing Function;
- the Hard Knapsack;
- the Deletion Box;
- the Signature Comparator.

They are described in the next four subsections. Not apparent on the functional diagram of Figure 7 is the organisation of the secret Authentication Keys stored in the Authentication Processor. This is described in the section on AU Control Commands on page 18.

THE HASHING FUNCTION

One purpose of the Hashing Function is to compress the variable amount of data bits constituted by the extended message x into a pre-signature P of fixed length (60 bits). The device realising the Hashing Function is a 60-bit linear feedback shift register (LFSR), as shown in Figure 8. The 60 feedback coefficients C0, C1,.....,C59 are part of the Authentication Key.

The LFSR is initialised to the 60-bit value P' = 1000....000 (where Bit P0 = 1) before the process of each authenticated TC Segment begins. P will be the value in the LFSR after the last bit of the variable-length extended message x has been shifted in. The extended message x (x = [m,l,z]) consists of the following data elements, placed one after the other in that order:

- the received message m, i.e., the TC Segment (variable from 1 to 240 octets) without the Authentication Tail;
- the received LAC value l, i.e., 4 octets (2 bits of LAC ID, plus 30 bits of LAC Count);
- three octets of virtual fill z, consisting of 24 zeros.

The purpose of the 24 bits of virtual fill is to ensure that the Hashing Function is provided with a minimum of data bits. The 24 bits of virtual fill z are generated by the PTD. Note that since m (the TC Segment) cannot be equal to zero, the total length of an authenticated TC Segment (i.e., [m,l,s]) cannot be smaller than 10 octets (Segment Header (1 octet) + Authentication tail (9 octets)). Anything smaller than 10 octets is rejected as being too short.

THE HARD KNAPSACK

The purpose of the Hard Knapsack is to ensure that it is not possible to deduce the presignature P from the signature S. The Hard Knapsack is based on the concept of the modular knapsack. It consists of 60 weights (numbered from W0 to W59, each weight being 48 bits long) and is defined by the following transformation:

$$S' = \left(\sum_{j=0}^{j=59} P_j W_j\right) \bmod 2^{48}$$

where the bits Pj of the presignature P select the corresponding weights W_j of the knapsack.

The result is the 48-bit knapsack sum S'. The most significant bit of the sum is called S'0.

THE DELETION BOX

The Deletion Box deletes the 8 least significant bits of the 48-bit knapsack sum S', i.e., bits S'40 through S'47. The result is the 40-bit authentication signature S (numbered from Bit 0 to Bit 39, as for signature s).

THE SIGNATURE COMPARATOR

The Signature Comparator compares the received 40-bit signature s with the onboard generated 40-bit signature S.

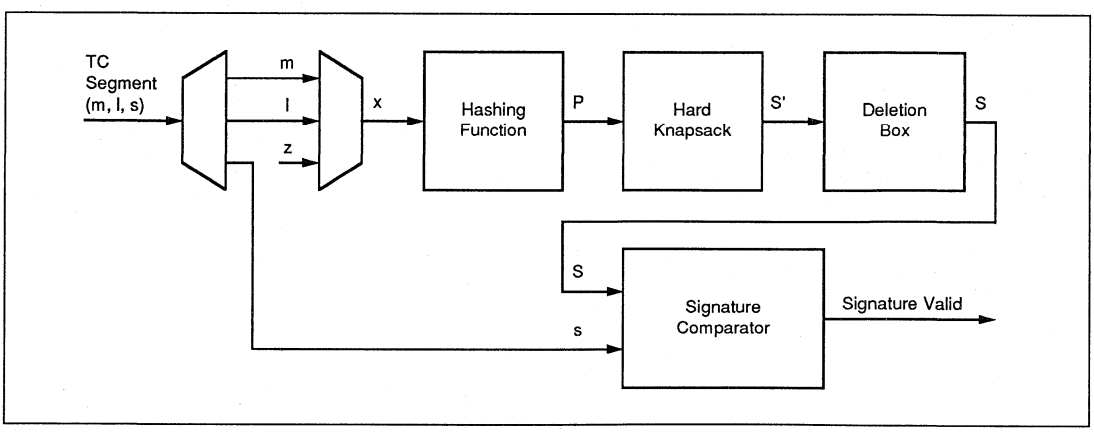


Figure 7: Functional Diagram of the Authentication Processor

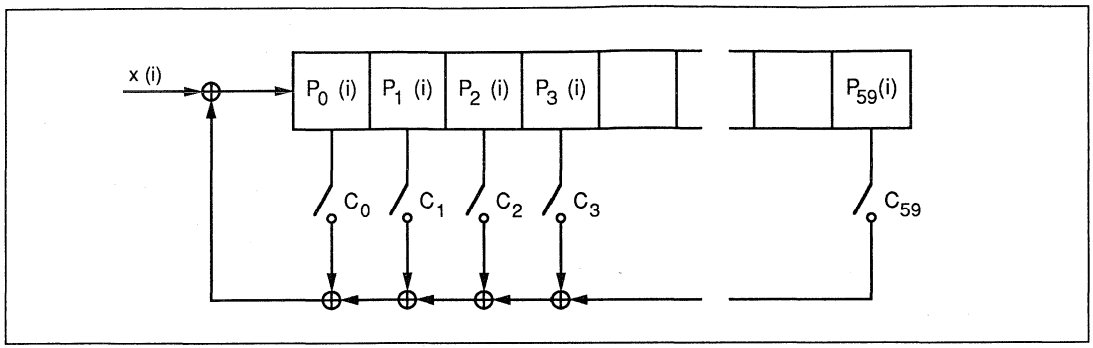


Figure 8: Realisation of the Hashing Function

THE AUTHENTICATION KEY

The Authentication Key consists of:

60 x 48-bit Hard Knapsack Weights =	2880 bits =	360 octets
60 x 1-bit Hashing Function coefficients =	60 bits =	8 octets
Full Authentication Key =	2940 bits =	368 octets

The system includes two such 2940-bit keys:

- a fixed, mission-unique Authentication Key, called the Fixed Key;
- an in-flight programmable Authentication Key, called the Programmable Key.

(a) Fixed Key

The Fixed Key is required for start-up and emergency (recovery) operations. The Fixed Key is stored in the external ROM as part of the Mission-Specific Data.

(b) Programmable Key

The Programmable Key is required for all normal operations. The contents of the Programmable Key reside in the RAM where it can be modified by means of Authentication Control Commands specifically defined for that purpose. The format of these Change Programmable Key Block Control Commands, which are specified in the section on AU Control Commands (page 18), allows any 5-octet block to be modified starting at any of the 368 octet boundaries.

The Supervisor

The Supervisor consists of four main parts:

- the Logical Authentication Channel (LAC) Registers;
- the Final Authorisation Function;
- the Control Command Processor;
- the Deletion Function.

They are briefly described in the next four subsections.

THE LAC COUNTERS

A LAC Counter is basically a 30-bit counter which is used to associate every TC segment with an authentication sequence number. The purpose of this number is to protect the system against attacks by ensuring that identical TC segments will not have the same signature except at very large intervals of time. The LAC counter is incremented by one every time a TC segment is successfully authenticated (and only then). The LAC counter value used for authenticating each TC segment is uplinked with each signature.

Three LAC Registers are provided:

- one Principal LAC register (LAC ID = 00);
- one Auxiliary LAC register (LAC ID = 01);
- one Recovery LAC register (LAC ID = 10).

Bits 0 and 1 of the LAC are fixed in order to select the LAC Register to be used for the final authorisation of a TC Segment. For what concerns the 30 bits of LAC Count (Bits 2 through 31, where the LSB is Bit 31), they are implemented as follows:

- The Principal and Auxiliary LAC counters have 30 bits.
- The Recovery LAC counter has 8 bits (the LSBs 24-31) whereas the remaining 22 bits (2-23) are permanently set to 1.

THE FINAL AUTHORISATION FUNCTION

When the received signature s of a TC Segment compares with the onboard-generated signature S, the contents of the received LAC Count field is compared with the contents of the indicated LAC Register. If both contents are found equal, there are two cases:

- The TC Segment was transferred on a MAP to be authenticated with a MAP ID lower or equal to the MAP ID pointer. In this case, the TC Segment is authorised for transfer to the Segmentation Layer.

- The TC Segment was transferred on MAP 63 (i.e., MAP 111111), which is dedicated to the transfer of Authentication Control Commands. In this case, the Control Command Processor is authorised to further process the TC Segment, which will never be transferred to the Segmentation Layer.

In both cases, the contents of the indicated LAC Register is incremented by one.

THE CONTROL COMMAND PROCESSOR

The function of the Control Command Processor is to execute the special TC Segments called Authentication Control Commands after being authorised by the Final Authorisation Function. The formats of the various Authentication Control Commands are specified in the section on AU Control Commands next. Any TC Segment not conforming to the specified formats (i.e., both in length and in contents) are rejected and reported as not executable.

THE DELETION FUNCTION

The Deletion Function deletes the Authentication Tail of all TC Segments authorised by the Final Authorisation Function. The complete authentication process is meant to be transparent to an observer placed at the receiving end of the Segmentation Layer.

AU Control Commands

It is necessary to differentiate TC Segments containing the Authentication Control Commands required to reconfigure the AU. This is done by allocating the TC Segment Header contents "all ones" to these particular segments, i.e.:

- Sequence Flags set to 11 (Unsegmented)
- MAP ID set to 111111 (MAP63)

TC Segments containing the Authentication Control Commands shall always be authenticated. The formats of the Authentication Control Commands are organised in three groups as follows:

- One octet of TC Segment Header for all three groups.
- One octet following the Segment Header to specify the Control Command Identifier
- Zero, four or eight octets of Control Command Data Field, depending on the group.

Table 2 gives the complete list of Authentication Control Commands, with Group numbers, Control Command IDs and Command Names. Table 3 shows the format of the TC Segment for each Group, complete with Authentication Tail. Each Control Command is specified in the next subsections.

DUMMY CONTROL COMMAND

The purpose of this command is to serve as NOP (No Operation) for testing purposes. After being authenticated, this Control Command will have no effect. However, since the AU has authenticated the Dummy Segment, the contents of the LAC Register used during the authorisation process have been incremented and a telemetry report prepared accordingly.

SELECT KEY CONTROL COMMANDS

(a) Select Fixed Key

The AU selects the Fixed Key prior to authenticating the TC Segment:

- If authentication is successful, the Fixed Key remains selected.
- If authentication is unsuccessful, the key previously in use remains selected.

(b) Select Programmable Key

The AU selects the Programmable Key for authentication of the TC Segment:

- If authentication is successful, the Programmable Key remains selected.
- If authentication is unsuccessful, the key previously in use remains selected.

LOAD FIXED KEY IN PROGRAMMABLE KEY MEMORY CONTROL COMMAND

This command reloads the Fixed Key set in the Programmable Key memory with a single command instruction. The key used for authenticating the TC Segment containing the Control Command will be whatever key was selected in the AU at the time the command was transmitted.

SET NEW LAC COUNT VALUE CONTROL COMMAND

The purpose of this Control Command is to set the value of one of the three programmable LAC Counters: Principal, Auxiliary or Recovery with LAC Identifiers 00, 01 and 10 respectively. If the LAC Identifier is set to 11, the command is not executed and reported as not executable. As soon as the TC Segment is authorised by the authentication process, the specified LAC Count value is forced into the selected LAC Register. Note that the 22 MSBs of the 30-bit Recovery LAC Register are permanently set to all ones, therefore those same bits in a Set New Recovery LAC Count Value Control Command are ignored by the AU. The key used for authenticating the TC Segment containing the Control Command will be whatever key was selected in the AU at the time the command was transmitted.

GROUP	CONTROL COMMAND IDENTIFIER (8 BITS)	COMMAND NAME
GROUP 1	0000 0000	DUMMY
	0000 0101	SELECT FIXED KEY
	0000 0110	SELECT PROGRAMMABLE KEY
	0000 0111	LOAD FIXED KEY IN PROGRAMMABLE KEY MEMORY
GROUP 2	0000 1001	SET NEW LAC COUNT VALUE
GROUP 3	0000 1010	CHANGE PROGRAMMABLE KEY BLOCK A
	0000 1011	CHANGE PROGRAMMABLE KEY BLOCK B

Table 2: List of Authentication Control Commands

1 octet	1 octet	9 octets
Segment Header	Control Command Identifier	Authentication Tail
11111111	00000***	LAC+Signature

Group 1 Control Command, 11 Octets

1 octet	1 octet	4 octets		9 octets
Segment Header	Control Command Identifier	LAC value to be set		Authentication Tail
11111111	00001001	LAC ID 2 bits	LAC Count 30 bits	LAC + Signature

Group 2 Control Command, 15 Octets

1 octet	1 octet	1 octet	7 octets	9 octets
Segment Header	Control Command Identifier	Start Address of new 40 bit Keyblock	Key specific pattern to be encoded	Authentication Tail
11111111	0000101*			LAC+Signature

Group 3 Control Command, 19 Octets

Table 3: Formats of Authentication Control Commands (Full TC Segment)

CHANGE PROGRAMMABLE KEY BLOCK CONTROL COMMANDS A AND B

Two such Control Commands are provided to cover the full size of the Programmable Key:

- Command A concerns the first 256 octet boundaries.
- Command B concerns the last 112 octet boundaries.

It is possible to load a 5-octet (40 bits) block starting from any of the 368 octet boundaries. Any transmission using the unused boundaries of Command B (from 113 to 255) is ignored and reported as non-executable. The key used for authenticating the TC Segment containing one of these Control Commands will be whatever key was selected in the AU at the time each Control Command was received. Once the TC Segment has been authorized by the authentication process, the TC Segment, minus the 40-bit signature s (i.e. [m,l]) is complemented and passed once more through the signature-building process, i.e. through the Authentication Processor. The 24 bits of virtual fill z are inserted as before, i.e., they are not complemented, but remain all zeros. The result of the process is a 40-bit pseudo-signature which, instead of being sent to the Signature Comparator, is loaded in the Programmable Key memory, starting at the octet location indicated by the start address field, as follows:

- Bits 32 through 39 of pseudo-signature at the indicated octet location;
- Bits 24 through 31 of pseudo-signature at the next location (start address + 1);
- And so on, until Bits 0 through 7 are loaded at location start address + 4.

Any arbitary procedure can be used for changing the key, starting from any of the 368 octet boundaries.

RAM Mapping		Address provided in the Control command (decimal)			
200	Bank A	000	40	W0 (40 to 47)	47
201		001	32	W0 (32 to 39)	39
202		002	24	W0 (24 to 31)	31
203		003	16	W0 (16 to 23)	23
204		004	8	W0 (8 to 15)	15
205		005	0	W0 (0 to 7)	7
206		006	40	W1 (40 to 47)	47
207		007	32	W1 (32 to 39)	39
2FF		255	16	W42 (16 to 23)	23
300	Bank B	000	8	W42 (8 to 15)	15
367		103	0	W59 (0 to 7)	7
368		104	59	C (59 to 56)	56
369		105	55	C (55 to 48)	48
36A		106	47	C (47 to 40)	40
36B		107	39	C (39 to 32)	32
36C		108	31	C (31 to 24)	24
36D		109	23	C (23 to 16)	16
36E		110	15	C (15 to 8)	8
36F		111	7	C (7 to 0)	0

Note: Bit 0 is the MSB

Figure 9: Organisation of the Programmable Key Memory

4.4 SEGMENTATION LAYER

Overview of the Layer

The segmentation layer provides the means to distribute several distinct streams of variable-length data units (e.g. the TC packets) to different applications by providing a number of service access points called the Multiple Access Points (MAPs). The data flow on each stream can be controlled by the receiving application using handshake control.

A TC segment consists of three distinct protocol data elements:

- an 8-bit segment header, the purpose of which is to identify the MAP connection and flag the sequential position of the segment relative to the complete TC Packet,

- a segment data field, of maximum length 248 octets, which contains all or a portion of a TC Packet,

- the 9-octet Segment Trailer specific to authenticated segments is removed by the authentication layer.

Standard Data Structures Within the Layer

The structure of the TC segment is given below:

SEGMENT HEADER		SEGMENT DATA FIELD
Sequence Flags 2 bits	MAP Identifier 6 bits	variable

<---------- 1 octet ----------><- from 0 to 248 octets ->

Segment Header

The Segment Header is the first octet (octet 0) of the TC segment structure. The Segment Header is divided into two major fields as follows:

- Sequence Flags (bits 0 & 1): this field is used by the segmentation protocol to indicate the sequential position of the segment relative to the complete data unit (e.g. the TC Packet). The flags are interpreted as follows:

Bit 0 (MSB)	Bit 1	Interpretation
0	1	First segment
0	0	Continuation segment
1	0	Last segment
1	1	Unsegmented

When the flags are set to 11 this means that the TC Segment Data Field contains an entire TC Packet. Except for the CPDU described in section 4.5, these flags are ignored by the PTD.

- Multiplexed Access Point (MAP) Identifier: this 6-bit field enables up to 64 MAP connection addresses to be associated with a single Virtual Channel. The PTD supports MAP 1 to 63 as externally available MAPs. MAP 0 is dedicated to the CPDU. MAP 63, when AU is enabled, is reserved for AU commands; when the AU is disabled, MAP 63 is processed by the segment layer like a standard MAP (see section 4.3).

Segment Data Field

The segment data field may vary from 0 to 248 octets maximum. When the optional Segment Trailer is used, the maximum length of the segment data field will be reduced by 9 octets.

Standard Procedures Within the Layer

The following segmentation layer functions are implemented in the PTD:

- the back-end buffer for the accepted TC segment. The back-end buffer is shared between the Transfer Layer and the Segmentation Layer.

- the MAP interface.

Upon reception of a new segment the Segment Layer performs the following operations:

- Checks whether the segment is authenticated or not.

- Starts the AU process if the segment is authenticated and if the AU is not disabled. The Segment Layer waits for the completion of the AU process (internal or external). A security mechanism is implemented, in case of AU locking mechanism the user can stop the AU process by activating the AU disable signal. In this case, the segment layer stops waiting for the AU completion process and the content of the back end buffer is lost.

- Checks if the frame is a CPDU command (MAP 0). In this case, the CPDU layer is activated and no data is output on the MAP interface.

- Checks if the frame is an AU command (MAP 63) and the AU is not disabled. In this case no data is output on the MAP interface.

- For a MAP 1 to 62 and for MAP 63 if the AU is disabled, the data is provided in serial or in parallel via the MAP interface. The MAP output frequency for serial MAP is selectable by reading a value associated with each MAP in the external ROM (see section 5.2).

4.5 COMMAND PULSE DISTRIBUTION UNIT

General Requirements

The CPDU is a simple unit that is solely accessible from ground. The aim of this unit is to generate pulses to drive certain actuators (e.g. relays). The CPDU is identified by the Application Process Identifier placed in the TC Packet Header. The Application Identifier of the CPDU is programmable in ROM at addresses 006 and 007.

Functional Description

The CPDU receives TC segments, each segment containing a complete TC Packet. TC segments having a MAP equal to zero are carrying CPDU commands. It must be noted that if the internal AU is enabled, MAP0 segments are always authenticated. When a new segment carrying CPDU commands has arrived, two cases are possible:

- the CPDU is still executing previous CPDU commands. In this case, the incoming TC segment is ignored, whether it was transferred in an AD or BD transfer frame.

- the CPDU is idle. The incoming TC segment is copied from the back end buffer to the CPDU buffer for checking and execution by the CPDU.

An important point must be noted: there is no packetisation layer abort command associated with the CPDU. Once it has accepted a TC Packet, the CPDU cannot release it until all command instructions specified in that packet have been executed.

The CPDU performs first the clean validation process which verifies the complete packet (CRC, packet length, segmentation flags). If the clean validation process is successful, the CPDU performs the legal validation process, which checks the content of the Packet Headers. The result of the two previous verifications is reported in the 16 bits CPDU status. For a dirty or illegal CPDU Packet, the CPDU buffer is erased. The execution of the CPDU commands is possible only if all the verifications succeed.

A short description of the fields of the CPDU Packet is given below:

- version number: 3-bit field occupying the 3 MSBs of the packet header. To be compliant with ref.1, these 3 bits should be 000.

- type bit: this bit identifies if the Packet is telemetry type (type bit = 0) or telecommand type (type bit = 1). To be compliant with ref 1, this bit should be set to 1.

- data field header flag: this indicates the presence (data field header flag = 1) or absence (data field header flag = 0) of a data field header within the packet data field. To be compliant with ref 1, this bit should be set to 0.

- application process identifier: this field identifies the particular process to which the CPDU Packet is sent.

- sequence flags: this two-bit field indicates if the packet is a first, last or intermediate component of a higher layer data structure. For CPDU Packets, these two bits shall be equal to 11.

- packet sequence count: this 14-bit field allows a particular TC Packet to be identified with respect to others occurring within a telecommand session. This field is reported in the CPDU status for clean and legal CPDU packets.

- packet length: this field specifies the number of octets contained within the packet data field, by indicating the number of octets in data field minus 1.

- packet data field: this field contains the CPDU commands and the CRC for packet error control.

Checking the CPDU-Specific TC Packet

The CPDU Packet format is shown below:

PACKET HEADER (48 bits)							**PACKET DATA FIELD** (variable)		
PACKET IDENTIFICATION				**PACKET SEQUENCE CONTROL**		PACKET LENGTH	DATA FIELD HEADER	APPLIC-ATION DATA	PACKET ERROR CON-TROL
version number	type	data field header flag	applicat-ion process ID	Sequence Flags	Packet Name or Sequence Count				
3	1	1	11	2	14				
16				16		16	variable	variable	16

The CPDU Packet is checked in two steps: the clean validation process and the legal validation process. The clean verification process performs the following tests:

- correct CRC (last two octets of the Packet contain a 16-bit CRC calculated using the same algorithm as used for the TC transfer frame, see section on transfer frame) to verify that there is no error in the Packet.

- the TC Segment Segmentation Flags (in Segment Header) are equal to 11.

- the CPDU Packet length is checked to be an even number of octets, greater than or equal to 10 octets and less than or equal to 248 octets: 10 octets ≤ TC Packet length = even number of octets ≤ 248 octets. The CPDU Packet length is read from Packet Header octets 5 and 6.

- consistency between the actual number of octets making up the CPDU Packet and the Packet length field. To achieve this, the Packet Header octet 5 is checked to be zero and the Packet Header octet 6 is checked to be consistent with the effective packet length.

At this level, if the packet is found to be error-free, it is declared clean and the process continues. Otherwise, the complete CPDU packet is erased.

The legal verification process performs the lollowing tests on the Packet Header (see ref 1, Section 8):

- the first octet of the Packet Header (version number & type bit & data fields header flag & 3 MSBs of Application Process Identifier) is compared with the value programmed in ROM at address 006.

- the second octet (8 LSBs of Application Process Identifier) is compared with the value programmed in ROM at address 007.

- in the third octet (sequence flags & 6 MSBs of packet name or sequence count), only the sequence flags field is checked by the PTD to be equal to 11. The packet name or sequence count is not verified, it is only reported in the CPDU status.

- the fourth octet (8 LSBs of packet name or sequence count) is not tested since the packet name or sequence count is not verified. It is only reported in the CPDU Status.

If the above check succeeds, the TC Packet is declared legal and its Application Data (command instructions) read out and executed as described in the next subsection. If the check fails, the Packet is erased.

Processing the Application Data

The CPDU receives a segment from the segment layer and stores it for further processing in the CPDU buffer provided in RAM. At the same time, the clean process is performed. This segment duplication is necessary due to delayed command execution. The duration of the transfer is equal to:

$$Td = Nb * Tacc$$

where Nb is the number of octets of the TC segment (including AU tail), and Tacc is the duration of three RAM accesses Read - Write - Read (the last read is used for computing the CRC with data effectively stored in RAM). Tacc can be estimated to 20*Tck (5 µs for a clock frequency of 4 MHz).

The application data of the CPDU packet should consist of at least one command instruction in the form of one double octet, or several of such double-octet command instructions, up to the maximum capacity.

Each double octet should be formatted as follows:

• first octet: specifies one of 256 Command Pulse outputs. The command distribution shall be made by an external demultiplexer (256 possible command pulse outputs).

• Second octet: specifies the duration of the Command Pulse to be issued on the specified output as follows:
  - the 5 MSBs are ignored by the CPDU,
  - the 3 LSBs specify the duration of the Command Pulse, which is equal to about 2^X multiplied by D where X is the value of the 3 LSBs and
    D = 40960 clock periods for CPDUDIV=0,
    D = 8192 clock periods for CPDUDIV=1.
    (see section 5.5 for exact figures.)

When there is more than one command instruction in the CPDU Packet, each instruction is executed one after the other in the same sequence as in the packet.

The maximum capacity of the CPDU packet is:

• 248 octets corresponding to 120 command instructions if the Internal or External Authentication Unit is disabled (AUDIS=1) or if the External Authentication Unit is enabled (AUEXT=1 and AUDIS=0) and AUTSL=1.

• 238 octets corresponding to 115 command instructions if the Internal Authentication Unit is enabled (AUEXT=0 and AUDIS=0) or if the External Authentication Unit is enabled (AUEXT=1 and AUDIS=0) and AUTSL=0.

For the calibrated pulses being output on the CPDUEN pin, the pulse amplification shall be made by external hardware. The CPDU provides a 16 bit status, CPDUS, that can be fetched by the telemetry system. The different fields of the CPDU status are detailed later.

4.6 TELEMETRY REPORTING

General Description

Telemetry reporting is essential to the normal operation of the telecommand data communication system.

Data Reports are not modified during telemetry readout. In particular they are not affected by the arrival of new report data. If the telemetry interface sampling rate is slower than the rate at which new data reports are generated, a double register mechanism ensures that the complete data report is read out.

CLCW Status Report

The Command Link Control Word (CLCW) is a standard reporting data structure of the Packet Telecommand System. It is a four-octet word generated by the spacecraft, the PTD generating only the 2 least significant octets of this CLCW which are described hereafter.

Bits	Value	Meaning
0 (MSB)		No RF Available
1		No Bit Lock
2		Lock Out
3		Wait
4		Retransmit
5,6		FARM B Counter
7	0	Report Type
8 - 15 (LSB)		Report Value

Each CLCW field is specified in the next paragraphs:

- No RF Available. This field is dedicated to the Physical Layer, i.e. the RF Transponders. When this field is 1, the RF physical connection is not available through any of the spacecraft transponders. When it is 0, the RF connection is available through at least one of the spacecraft transponders. This information is provided to the PTD by an input pin called RFAVN.

- No Bit Lock. This field is dedicated to the Physical layers, and monitors the presence of the spacecraft demodulation. When this field is 1, all the TC Active Signals (0 to 5) are zero at the PTD input pins. When it is 0, at least one of the TC Active signals is set to 1.

- Lockout Flag. If 1, this field indicates that the FARM- 1 is in the Lockout state.

- Wait Flag. If 1, this field indicates that the FARM- 1 is in a Wait state.

- Retransmit Flag. If 1, this field indicates that an AD frame has been lost in transmission or has been discarded because there was no buffer space available.

- FARM B counter. This 2 bit field contains a wraparound up-counter (modulo 4) of each TC frame of type BC or BD declared valid by the Legal Frame Validation process, and therefore acceptable by the FARM-1.

- Report Type. In the PTD it is always 0 in accordance with reference 1.

- Report Value. This field is maintained by the FARM-1 and contains the next expected frame sequence number V(R).

The first bit to be read in serial mode is Bit 0 (MSB). The interface for reading the CLCW status is specified in section 5.3.

CPDU Status Report

The CPDU Status report consists of 16 bits of status data formatted as follows:

Bits	Value	Meaning
0,1	00	Cold Start
	01	Last TC Packet accepted legal
	10	Last TC Packet accepted clean, but erased as not legal
	11	Last TC Packet erased as not clean
2 - 15 (LSB)	all 1	Cold Start
	all other values	Packet Sequence Count (or Name) of last legal CPDU Packet

The first bit to be read out in serial mode is Bit 0 (MSB). Legal and Clean concepts are defined previously. The telemetry interface used to read out the CPDU Status Report is fully described in section 5.3.

AU Status Report

The AU Status Report consists of 80 bits (i.e. 10 octets) of status data formatted as follows:

Bits	Value	Meaning
0,1	00	Permanently set to 00
2 - 31		Current value of the contents of the Principal LAC counter. The LSB of the LAC counter value is in bit 31
32,33	01	Permanently set to 01
34 - 63		Current value of the contents of the auxiliary LAC counter. The LSB of the LAC counter value is in bit 63
64		Key in use by AU: 0 fixed key in use 1 Programmable key in use
65 - 71	0000000	Permanently set to 0 (reserved for future use)
72 - 79 (LSB)		Current value of the 8 LSBs of the recovery LAC counter. The LSB of the LAC counter value is in bit 79.

The first bit to be read in serial mode is bit 0 (MSB).

The AU Status report is implemented by using a double register mechanism located in the external RAM. In the case of external AU, the external AU can write the AU Status in RAM. The number of the buffer is given by the AUS pin and the toggling mechanism of the AU Status buffer is locked by the PTD when the signal AUST (External AU Start) is high. The telemetry interface used to read the AU status report is described in section 5.3.

Frame Analysis Report

The FAR is required for proper testing and check-out of the TC Decoder. The FAR consists of 32 bits of survey data formatted as follows:

BITS	VALUE	MEANING
0 (MSB)		STATUS OF SURVEY DATA
	0	New survey data (or Cold Start)
	1	Old survey data
1,2,3		FRAME ANALYSIS Note: The report of the lowest rank (i.e. of lowest 3-bit value) has precedence in case of conflicting states.
	000	Abandoned CLTU (see Note 1)
	001	Frame declared dirty
	010	Frame declared illegal for one reason
	011	Frame declared illegal for multiple reasons
	100	Frame (AD) discarded because of LOCKOUT
	101	Frame (AD) discarded because of WAIT
	110	Frame (AD) discarded because of N(S) or V(R)
	111	Frame (AD, BD or BC) Accepted by FARM-1
4,5,6		LEGAL/ILLEGAL FRAME QUALIFIER **Note:** When a frame is declared ILLEGAL for multiple reasons, only the reason of the first rank (i.e. of lowest 3-bit value) is reported. The fields mentioned are those of the frame header.
	000	No illegal report (or Cold Start)
	001	Error in fixed fields (Version & Reserved)
	010	Illegal combination (AC) of Bypass & Control Command Flags
	011	Wrong Spacecraft ID
	100	Wrong VC ID (because of Bits 0 to 4 of ID)
	101	Wrong VC ID (because of Bit 5 of ID)
	110	N(S) of BC or BD frame not set to all 0
	111	Wrong BC frame data format (not executable)
7 - 12		COUNT OF ACCEPTED CODE BLOCKS PER CLTU
	xxxxxx	Straight 6-bit binary count of correct or single-error-corrected codeblocks in one CLTU; (Cold Start value: 000000)
13,14,15		COUNT OF SINGLE-ERROR CORRECTIONS PER CLTU
	xxx	Straight 3-bit binary count, saturates at maximum value, no roll over. (Cold Start value:000)
16,17		LEGAL FRAME QUALIFIER (4 STATES)
	00	AD frame
	01	No report on legal frame (or Cold Start)
	10	BD frame
	11	BC frame
18,19,20		SELECTED CHANNEL INPUT (MAXIMUM CAPABILITY : 6 INPUTS)
	xxx	(Cold Start value : 111)
21 - 26		LAST MAP ADDRESSED (64 MAPS)
	xxxxxx	(Cold Start value : 111111)
27	0	RESERVED BY ESA (set to 0)
28,29,30		AUTHENTICATION PROCESS ANALYSIS
	000	No authentication report (or Cold Start)
		AUTHORISED SEGMENT QUALIFIER
	001	Authorised data segment
	010	Authorised (and executable) Authentication Control Command
	011	Authorised dummy segment received

BITS	VALUE	MEANING
		REJECTED SEGMENT QUALIFIER
	100	Error in Signature
	101	Error in LAC
	110	Wrong format (not executable) of authorised Authentication Control Command (includes Segment Header)
	111	Wrong length of TC Segment prior to being authenticated (authorised), i.e. length shorter than 10 octets
31 (LSB)	0	set to 0

A few specific points need to be detailed:

Note 1: The abandoned CLTU state (000) is used to indicate:

- the Cold Start
- a first TC codeblock of CLTU was abandoned (erased) because of event 4 or event 2
- an event E2(a) channel deactivation occurs (see section 4.1)
- an event E2(b) CLTU error occurs (see section 4.1)

In the case of an Abandoned CLTU the Legal/Illegal Frame Qualifier (bits 4, 5, 6) is set to 000 and the Legal Frame Qualifier (bits 16, 17) is set to No Report on Legal Frame (01).

Note 2: The rejected segment qualifier in the Authentication process analysis has the following prioritisation:

- 111 Too short TC segment has the highest precedence, followed by
- 100 Error in Signature, followed by
- 101 Error in LAC, followed by
- 110 Wrong format of AU command or segmentation flags.

The FAR is sampled and read by a telemetry interface described in section 5.3.

5. PTD INTERFACES

5.1 PHYSICAL CHANNEL INTERFACE

Each TC channel consists of 3 input lines:

- TCC_i : symbol clock input
- TCS_i : symbol stream input (NRZ-L)
- TCA_i : channel active indication input

The maximum symbol rate with guaranteed operation (using the internal AU) on these channels is 50 kbps. For higher frequency, an incomplete AU process may occur resulting in wrong signature calculation and thus rejected frames. Without AU the symbol rate could be 200 kbps (not guaranteed). At higher frequency, incorrect processing may occur due to insufficient time to perform memory accesses. The interface is composed of 6 TC channels. Figure 10 below gives the timing associated with one of these 6 channels. For unused channels, the TCA_i signal should be connected to V_{SS}, and the TCC_i and TCS_i signals to V_{DD}.

The DECOD output is activated when the CLTU decoder state machine is in the decode state (see section 4.1). This output goes high following the detection of a start sequence, and goes low following a codeblock rejection or CLTU error.

5.2 MAP INTERFACE

The MAP interface allows the PTD to provide the on-board applications with the TC segments stored in the back-end buffer in the RAM. It is possible to transfer full TC segments (including segment header and packet segment) with various lengths, from 1 octet to 249 octets. The first data output is the TC segment header. It is possible for an application to use either a serial or parallel interface to read this TC data. The choice between serial or parallel interface is made with the configuration input pin PAR as follows:

- PAR = 1; the parallel MAP interface is used (section 5.4)
- PAR = 0; the serial MAP interface is used

The serial MAP interface consists of 5 signals.

- MAPDSR, data set ready output,
- MAPDTR, data terminal ready input,
- MAPCK, MAP clock output,
- MAPDATA, segment data output,
- MAPADT, aborted data transfer output.

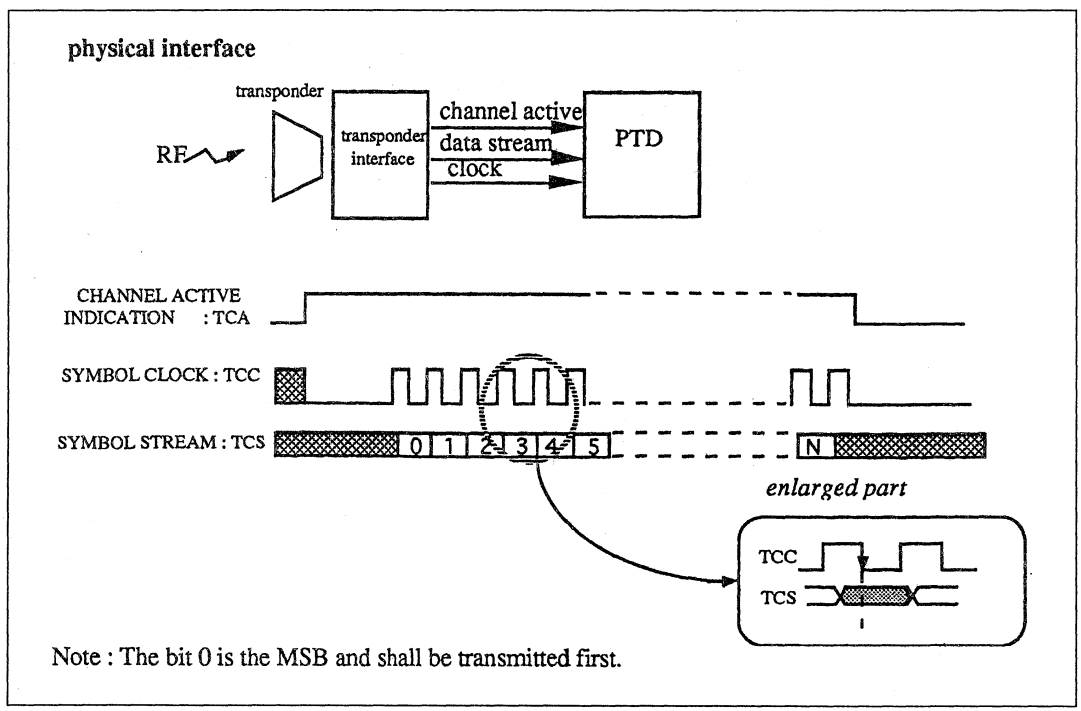
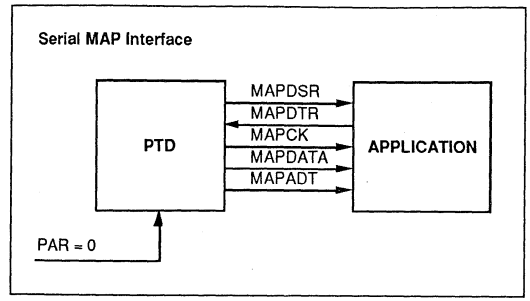


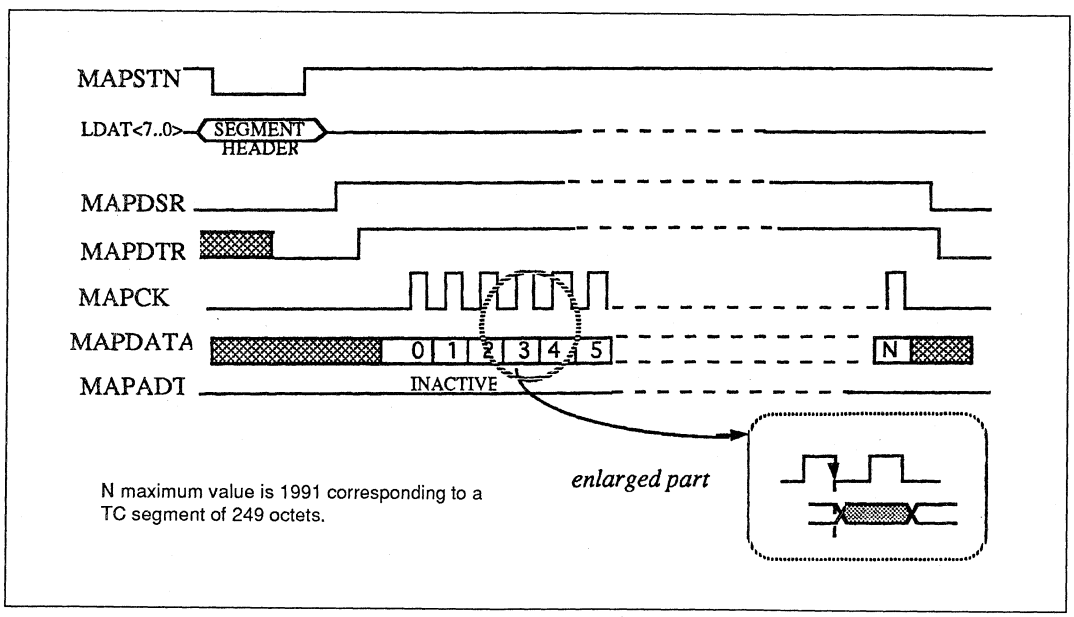
Figure 10: TC Channel Input Timing

In addition, the MAP interface provides the output signal MAPSTN, in order to save the MAP identifier present on the local data bus (LDAT<7..0>) in an external latch. This MAP identifier is used to demultiplex the segment data toward the selected application. The MAPSTN signal can be controlled by the LACK signal. MAPDSR has no effect when MAPDTR output is deasserted.

The output frequency for each MAP is programmable and is defined in ROM. For MAP number n, the address of the value X defining the MAP frequency is (hex) 100+n. The MAP output frequency is given by $F=f_{ck}/[2^X]$, (X is coded on the 4 LSBs and its value varies from 1 to 13; for other values, the output frequency is $F = f_{ck}/2$). For example for a PTD clock frequency of 4 MHz, setting the ROM value to 4 will generate a MAP frequency of 250 kHz. With a system clock frequency fck of 4 MHz, the MAPCK frequency can vary from 488 Hz (X=13) to 2 MHz (X=1). The use of a too low MAP frequency compared to the TC clock frequency may lead to the activation of the WAIT flag if the MAP output of a previous frame is not finished when a new segment arrives. As a rule of thumb, in order to avoid the Wait flag being asserted, the MAP frequency should be at least the TC input bit rate multiplied by 10 when fully variable segment size (by 2 if fixed length).

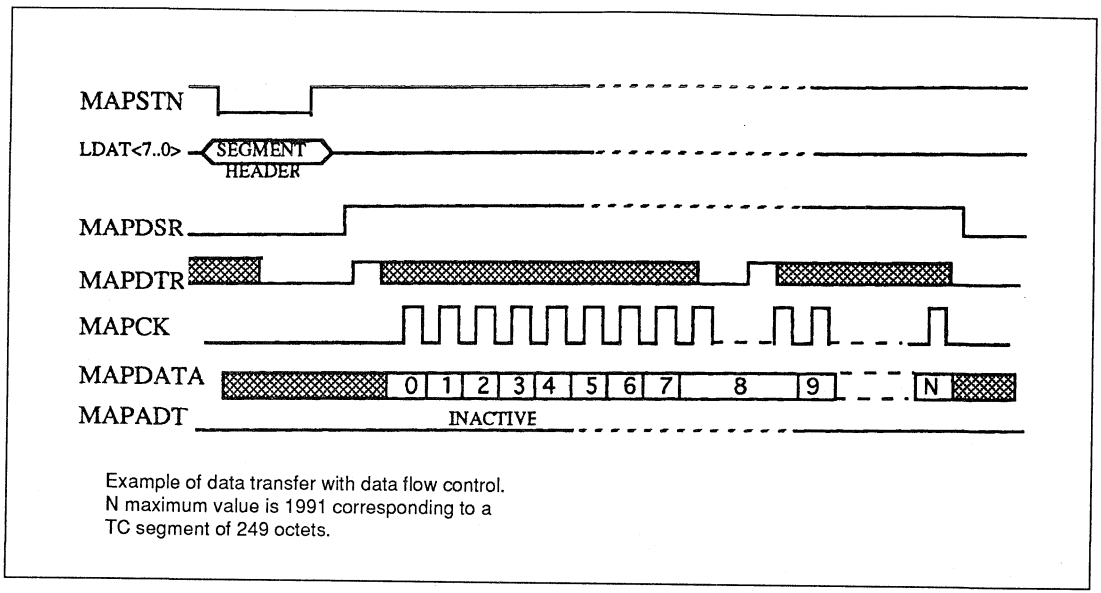
Figure 11 describes the serial interface in three different transfer situations.





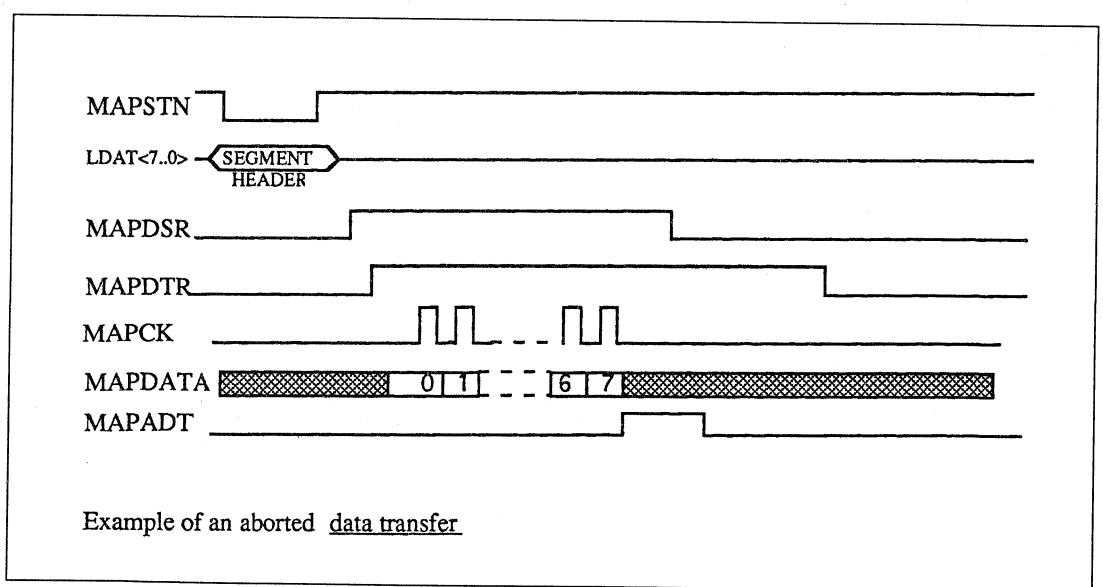
Note: The bit 0 is the MSB and shall be transmitted first.

Figure 11: Serial MAP Interface



Example of data transfer with data flow control.
N maximum value is 1991 corresponding to a
TC segment of 249 octets.

Note: For each MAPDTR pulse one octet is transferred.



Example of an aborted data transfer

Note: The MAPADT signal is asserted on octet boundaries of the MAP data being transferred.

Figure 11: Serial MAP Interface (continued)

5.3 TELEMETRY INTERFACE

The Telemetry interface allows four different reporting words to be retrieved.

- the Command Link Control Word (CLCW),
- the Command Pulse Distribution Unit Status (CPDUS),
- the Frame Analysis Report (FAR),
- the Authentication Unit Status (AUS).

It is possible for an application to use either a serial or parallel interface to read these reports. The selection between serial or parallel interface is made with the configuration input pin PAR as follows:

- PAR = 1; the parallel TM interface is used
- PAR = 0; the serial TM interface is used

The parallel interface is described in section 5.4. The parallel interface is useful for integrating subsystems comprising both the TC decoder and a processor, without cross-coupling after the TC decoders. The CLCW has its own serial telemetry interface which is redundant in serial mode.

The other three reports (CPDUS, FAR, AUS) can be fetched through a common serial interface (clock and data lines) using two or five different sample signals. The selection between using two or five sample signals is made with the configuration input pin TMMOD as follows:

- TMMOD = 0; the status (CPDUS, FAR, AUS) reports are fetched with 5 sample signals.
- TMMOD = 1; the status (CPDUS, FAR, AUS) reports are fetched with 2 sample signals.

Both interfaces use the same TMC and TMD signals. When the parallel interface is selected it is not possible to use the TM (and MAP) serial interface, except for the CLCWB interface which can be used in a serial mode even if the PAR signal is set to 1. The protocol for the serial interface is fully compliant with section 4.3 of TTC-B-01 (serial 16 bit digital channel).

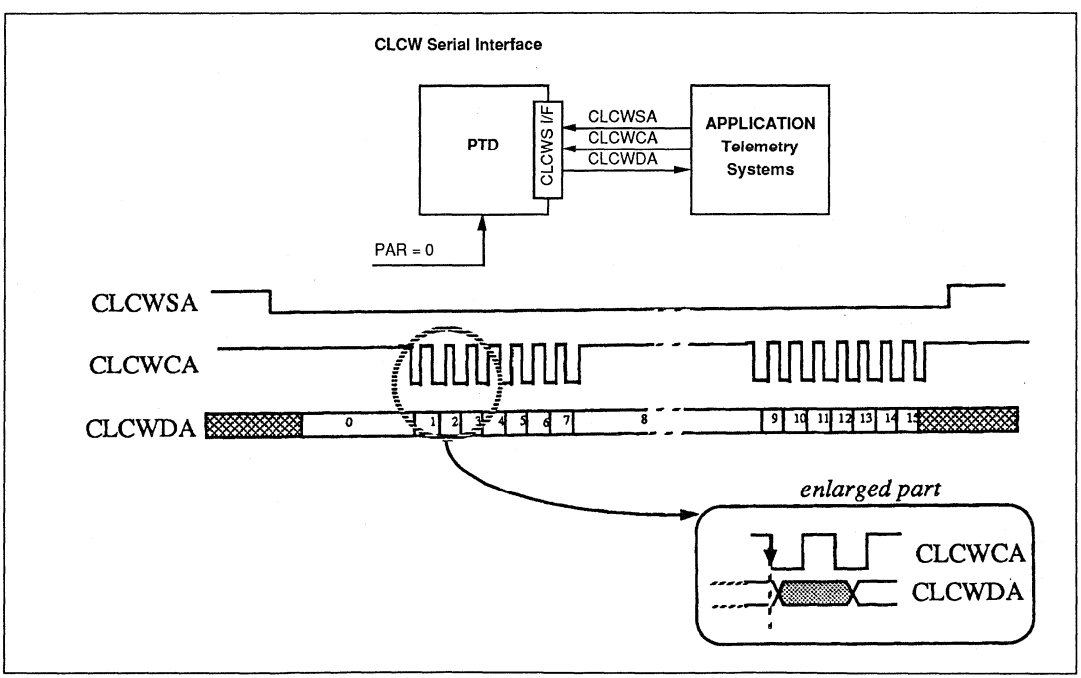
Serial CLCW Interface

The 16 bit Command Link Control Word (CLCW) can be retrieved through this interface. The serial CLCW interface is redundant in order to allow two separate redundant TM encoders to be connected to each TC decoder. Figure 12 shows the serial CLCW telemetry interface. The serial interface is implemented with 3 signal lines:

- CLCWSA: status sample input,
- CLCWCA: status clock input,
- CLCWDA: status data output.

The redundant serial CLCW interface is identical with the nominal serial CLCW interface using the 3 signals:

- CLCWSB: status sample input,
- CLCWCB: status clock input,
- CLCWDB: status data output.



Note: The 0 bit is the MSB and is transmitted first.

Figure 12: Serial CLCW Telemetry Interface

The sample signal CLCWSA should be activated only once to fetch the entire CLCW word. The serial CLCW interface has been designed to allow the VCM device specified in reference 3 to automatically retrieve the CLCWs without any additional components being required. If one of the CLCW interfaces is not used, the following signals CLCWSx and CLCWCx should be connected to V_{DD}. Activating the CLCWCA (CLCWCB) signal when CLCWSA (or CLCWSB) is deasserted, will generate invalid data output on CLCWDA (or CLCWDB).

CPDU Status Report Interface in 5 Samples Mode

The 16 bit Command Pulse Distribution Unit Status report can be retrieved through this interface. It is possible for an application to use either a serial or a parallel interface to read out this status report. The serial or parallel mode is selected with the PAR configuration pin of the PTD (see section 5.4). The serial interface in 5 samples mode uses 3 signal lines:

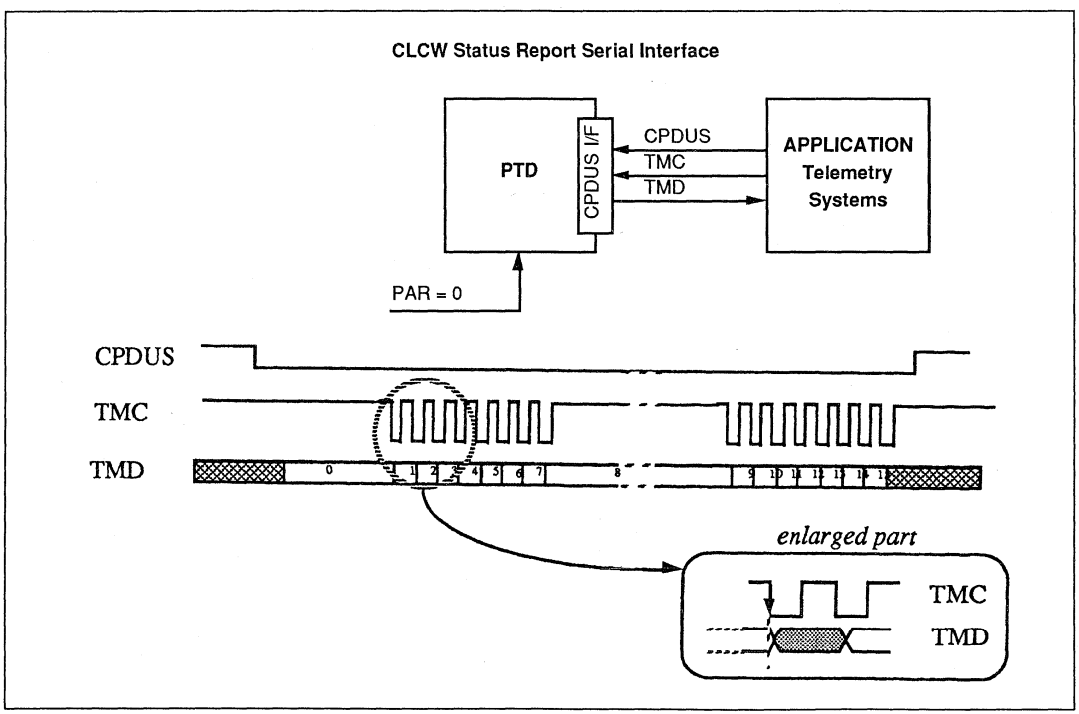
- CPDUS: status sample input.
- TMC: status clock input, is also used for FAR and AUS.
- TMD: status data output, is also used for FAR and AUS.

The sample signal CPDUS needs to be activated only once to fetch the entire CPDUS word. CPDUS, FAR1S, FAR2S, AUS1S and AU2S cannot be asserted simultaneously. If CPDUS, FAR1S, FAR2S, AUS1S and AU2S are not asserted, activating the TMC signal will generate invalid data on the TMD output. If the CPDU status report interface is not used, the CPDUS signal should be connected to V_{DD}. Figure 13 below describes the CPDU telemetry serial interface.

Serial FAR Status Report Interface in 5 Samples Mode

The 32 bit Frame Analysis Report can be retrieved through this interface. It is possible for an application to use either a serial or a parallel interface to read out this status report. The serial or parallel mode is selected with the PAR configuration pin of the PTD (see section 5.4). The serial interface in 5 samples mode uses 4 signal lines:

- FAR1S: first status sample input,
- FAR2S: second status sample input,
- TMC: status clock input, is also used for CPDUS and AUS,
- TMD: status data output, is also used for CPDUS and AUS.



Note: The 0 bit is the MSB and is transmitted first.

Figure 13: CPDU Telemetry Serial Interface

The sample signals FAR1S and FAR2S should be asserted to fetch the 32 bits of FAR. CPDUS, FAR1S, FAR2S, AUS1S and AU2S cannot be asserted simultaneously. If CPDUS, FAR1S, FAR2S, AUS1S and AU2S are not asserted, activating the TMC signal will generate invalid data on the TMD output. If the FAR status report interface is not used, the FAR1S and FAR2S signals should be connected to V_{DD}.

Figure 14 describes the FAR telemetry serial interface.

Serial AU Status Interface in 5 Samples Mode

The 80 bit Authentication Unit Status report can be retrieved through this interface. It is possible for an application to use either a serial or a parallel interface to read out this status report. The serial or parallel mode is selected with the PAR configuration pin of the PTD (ee section 5.4). The serial interface in 5 samples mode is implemented with 4 signal lines:

- AU1S: first status sample input,
- AU2S: second status sample input,
- TMC: status clock input, is also used for CPDUS and FAR.
- TMD: status data output, is also used for CPDUS and FAR.

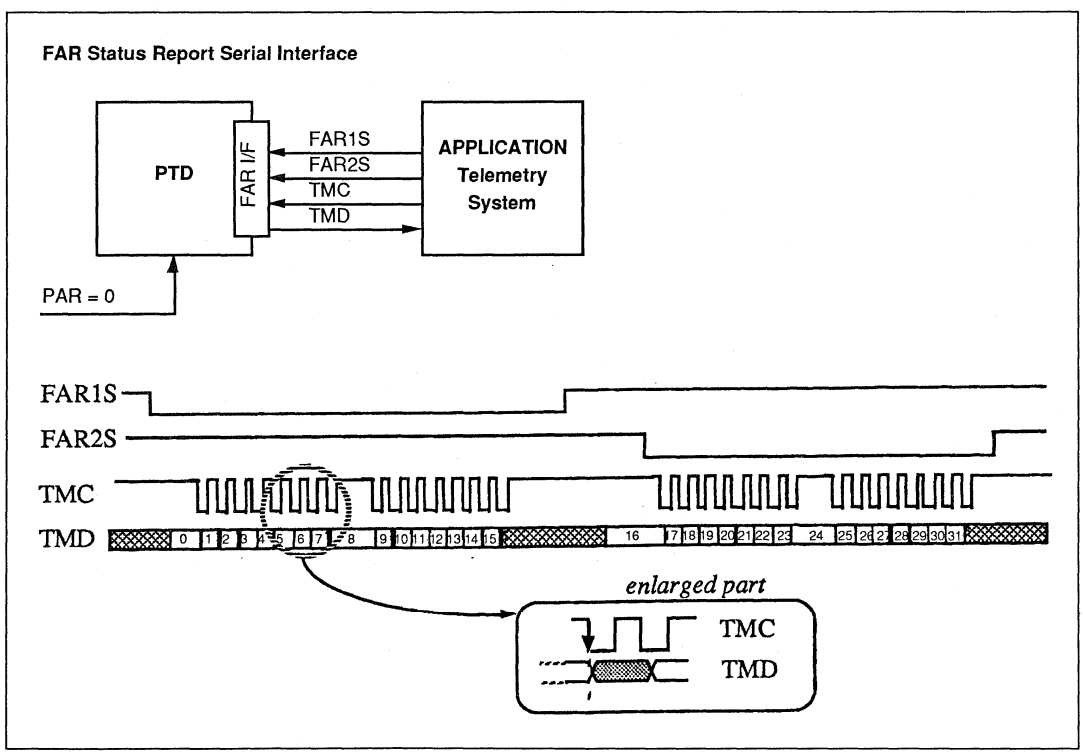
When AU1S is asserted, the pointer for reading out data with AU2S is reset to the second octet of the report. The sample signals AU1S and AU2S should be asserted as described in Figure 15 to fetch the 80 bits of AUS report. CPDUS, FAR1S, FAR2S, AUS1S and AU2S cannot be asserted simultaneously. If CPDUS, FAR1S, FAR2S, AUS1S and AU2S are not asserted, activating the TMC signal will generate invalid data on the TMD output. If the AU status report interface is not used, the AU1S and AU2S signals should be connected to V_{DD}.

Figure 15 describes the AUS telemetry serial interface.

Serial CPDU, FAR, AU Status Interface in 2 Samples Mode

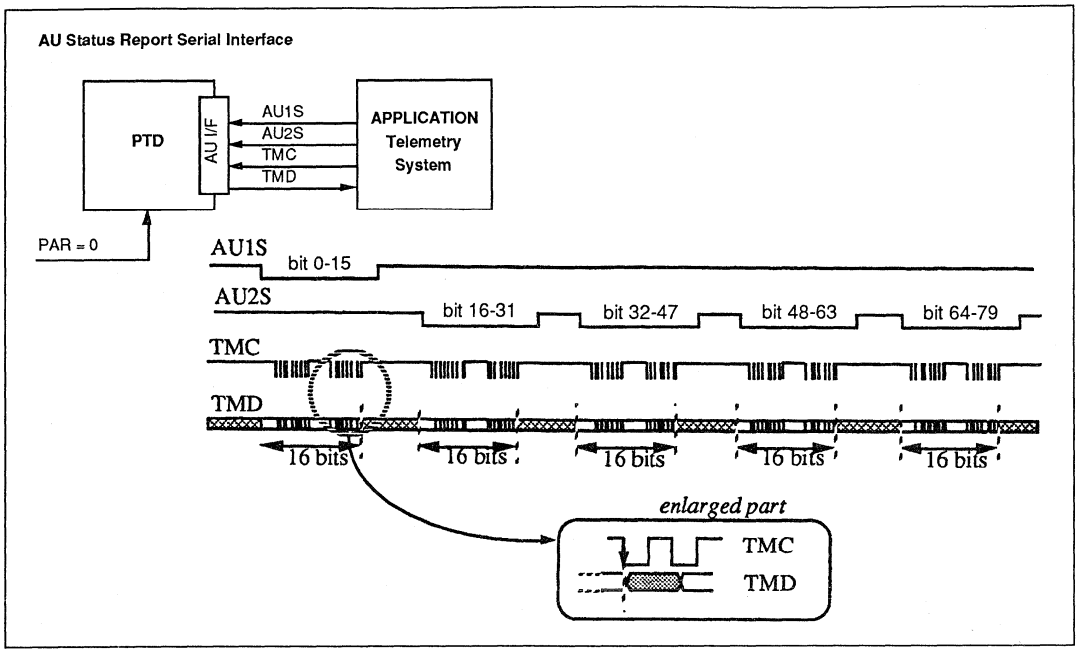
The 16 bit Command Pulse Distribution Unit status report, the 32 bit Frame Analysis report and the 80 bit Authentication Unit status report can be retrieved through this interface. The serial interface in 2 samples mode is implemented with 4 signal lines:

- CPDUS: first status sample input,
- FAR1S: second status sample input,
- TMC: status clock input,
- TMD: status data output.



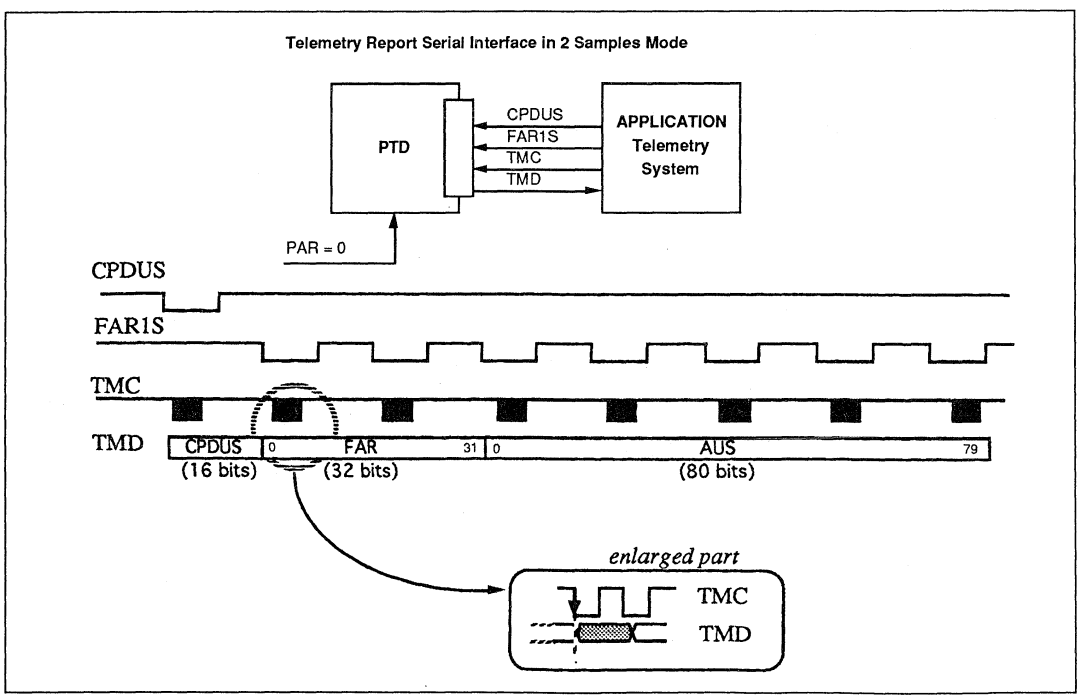
Note: The 0 bit is the MSB and is transmitted first.

Figure 14: FAR Telemetry Serial Interface



Note: The 0 bit is the MSB and is transmitted first.

Figure 15: AUS Telemetry Serial Interface



Note: The 0 bit is the MSB and is transmitted first.

Figure 16: Telemetry Serial Interface in 2 Sample Mode

When CPDUS is asserted, the pointer for reading out data with FAR1S is reset to the first octet of the FAR. The samples CPDUS and FAR1S should be activated as described in Figure 16 to fetch the 128 bits of status words. The first 16 bits are those of the CPDU status word, to be acquired by asserting the CPDUS signal line. The next 32 bits are those of the FAR status word, to be acquired by signalling on the FAR1S signal line (2 x 16 bits). The last 80 bits are those of the AU status word, to be acquired by additional assertions (5 x 16 bits) of the FAR1S signal line. It is possible to read out only the first 48 bits (CPDU and FAR), e.g. if the AU is not used.

FAR1S, AU1S and AU2S do not have any impact in this mode, but should be connected to V_{DD}.

5.4 PARALLEL INTERFACE

A parallel interface is provided on the PTD to access the TC segment and the four reporting words: CLCW, CPDUS, FAR and AUS. The parallel mode is selected with the PAR configuration pin of the PTD (the parallel mode is selected when PAR is set to 1). The parallel interface is implemented with the following signals:

- PCSN: parallel bus chip select input,
- PAD<2..0>: parallel address bus (input),
- PRDY: data validation output,
- PBUS<15..0>: parallel data bus (output),
- MAPDSR: MAP data set ready output,
- MAPADT: MAP aborted data transfer output.

The PCSN, PAD2, PAD1 and PAD0 signal lines use respectively the CPDUS, FAR1S, FAR2S and AU1S input pins of the serial interface. The application acquires the TC segment and the four reporting words by read cycles. The addressing of these words is as follows:

PAD2	PAD1	PAD0	read word
0	0	0	MAP segment
0	0	1	CPDU status
0	1	0	CLCW status
0	1	1	MAP status
1	0	0	FAR1 status
1	0	1	FAR2 status
1	1	0	AU1 status
1	1	1	AU2 status

When the AU1 status is read, the pointer for reading out data with AU2S is reset. The MAP TC segment is read as described in Figure 17.

A TC segment is read by consecutive accesses to <000>. Data read when MAPDSR is not asserted is not valid. The TC segment data octet of even rank is output on the 8 MSB of PBUS (the first octet is 00 and therefore even). The TC segment data octet of odd rank is output on the 8 LSB of PBUS. In the case of a TC segment with an odd number of octets, the last 16 bits word output on PBUS contains the last TC segment data octet on the 8 MSB and a non significant octet (all bits set to 0) on the 8 LSB. For example, if the TC segment to be output is (hexadecimal) AABBCC, the first word read is AABB and the second one is CC00.

After a PCSN assertion, the PRDY output is activated when the data is available on the PBUS output. The PRDY is released when the PCSN signal is deasserted. The PRDY signal will not be asserted if PCSN is asserted and PAD = 000 (MAP segment read) when MAPDSR is inactive. When PCSN is deasserted the PBUS bus is tristated. The MAP status word can be read at any time. The access to this word is identical to the telemetry status word accesses as described in Figure 18. It contains the following information:

- PBUS<0>: MAPDSR information (identical to MAP data set ready signal line).
- PBUS<1>: ODD/EVEN segment length information (Odd: 1, Even: 0).
- PBUS<15..2>: not used (value : 00000000000000).

NOTE: only TC segments appearing on MAP 1 to 62 and on MAP 63 when AU is disabled, can be read out using this parallel interface. MAP 0 is not affected by this parallel interface since it is directly connected to the CPDU. The telemetry status word is read as described in Figure 18.

The CLCW status word is read using one read cycle where PAD = 010.

The CPDU status word is read using one read cycle where PAD = 001.

The FAR status words are read with two read cycles:

- One read cycle with PAD = 100 for the first 16 bits (FAR1)
- One read cycle with PAD = 101 for the last 16 bits (FAR2).

The AU status words are read using five read cycles:

- One read cycle with PAD = 110 for the first 16 bits (AU1)
- Four read cycles with PAD = 111 for the last 64 bits (AU2): bits 16-31, bits 32-47, bits 48-63 and bits 64-79.

When the AU1 Status report is read, the pointer for reading out data with AU2 is reset to the second octet of the AU report. The Status of Survey bit is set when FAR2 is read. The following pins have no influence in parallel mode:

- MAPDTR (should be connected to V_{SS}),
- CLCWSA, CLCWCA (should be connected to V_{DD}),
- AU2S (should be connected to V_{DD}),
- TMC (should be connected to V_{DD}),
- TMMOD (should be connected to V_{SS}),

The reports and TC segments cannot be read out in an arbitrary order. The following constraints apply: A FAR2 read out shall not be separated from the previous FAR1 read out by AU1 or AU2 read out. An AU2 read out shall not be separated from a previous AU1 or a previous AU2 read out by FAR1 or FAR2 read out.

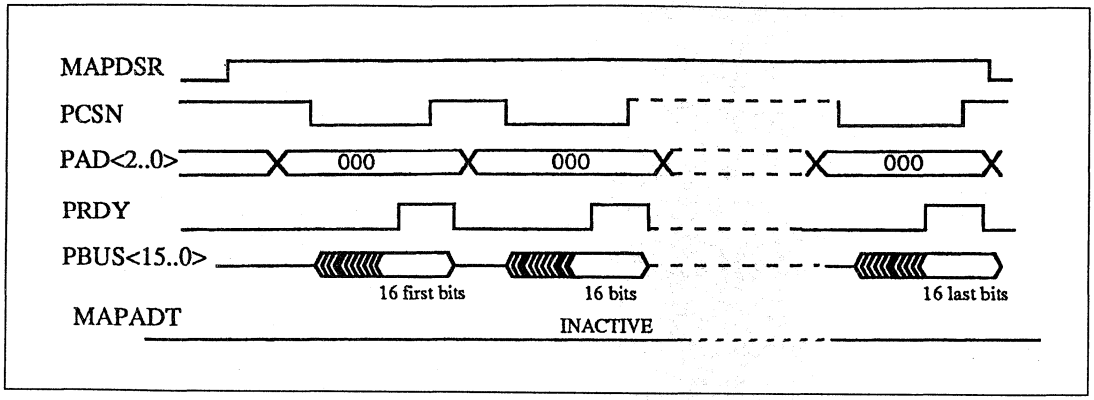


Figure 17: Parallel MAP Interface

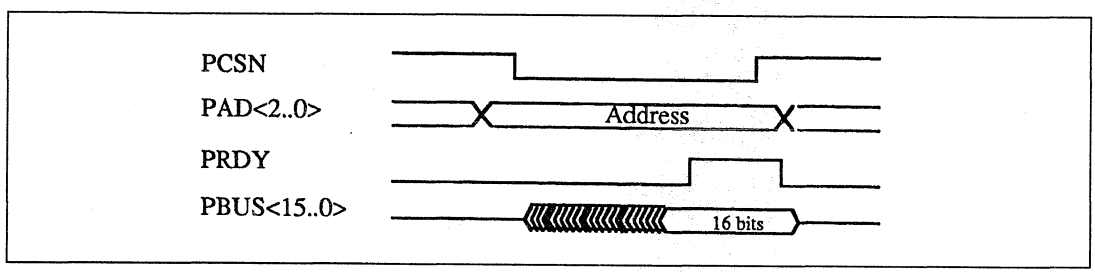


Figure 18: Parallel Telemetry Read Cycle

5.5 CPDU INTERFACE

This interface consists of 3 signal lines:

- CPDUSTN: CPDU address strobe output,
- CPDUEN: CPDU enable output,
- CPDUDIV: CPDU frequency divider input.

The CPDU interface provides the output signal CPDUSTN in order to save the CPDU physical channel identifier present on the local data bus LDAT<7..0> in an external latch (no specific LADR address is associated with this data). This CPDU identifier is used to demultiplex the command pulse toward the selected CPDU output. The CPDUSTN signal can be controlled by the LACK input. The CPDUEN signal is representative of the command pulse as far as duration is concerned. The pulse amplification should be made after demultiplexing with external circuitry. The CPDUDIV signal allows division of the pulse length specified in ref 2 by a factor of 5, in order to get a better accuracy. Alternatively, this allows the PTD to be used with a 1MHz clock frequency, instead of a 4 MHz clock.

For a 4 MHz clock, the duration D is 10.24 ms if CPDUDIV=0 and 2.048 ms if CPDUDIV=1. The maximum duration (=128xD) is about 1.31 s if CPDUDIV=0, and 262 ms if CPDUDIV=1. The delay between the time at which the packet has been declared Legal and the execution of the command instruction (rising edge of CPDUEN) can be any value between 0.5 D and 1.5 D. The duration between two instructions placed one after the other in the same CPDU packet (from falling edge to rising edge of CPDUEN) corresponds to about D.

COMMAND	PULSE LENGTH (CLOCKS) (CPUDIV=0)	PULSE LENGTH (CLOCKS) (CPUDIV= 1)
000	40961	8193
001	81921	16385
010	163841	32769
011	327681	65537
100	655361	131073
101	1310721	262145
110	2621441	524289
111	5242881	1048577

Table 4: CPDU Pulse Lengths

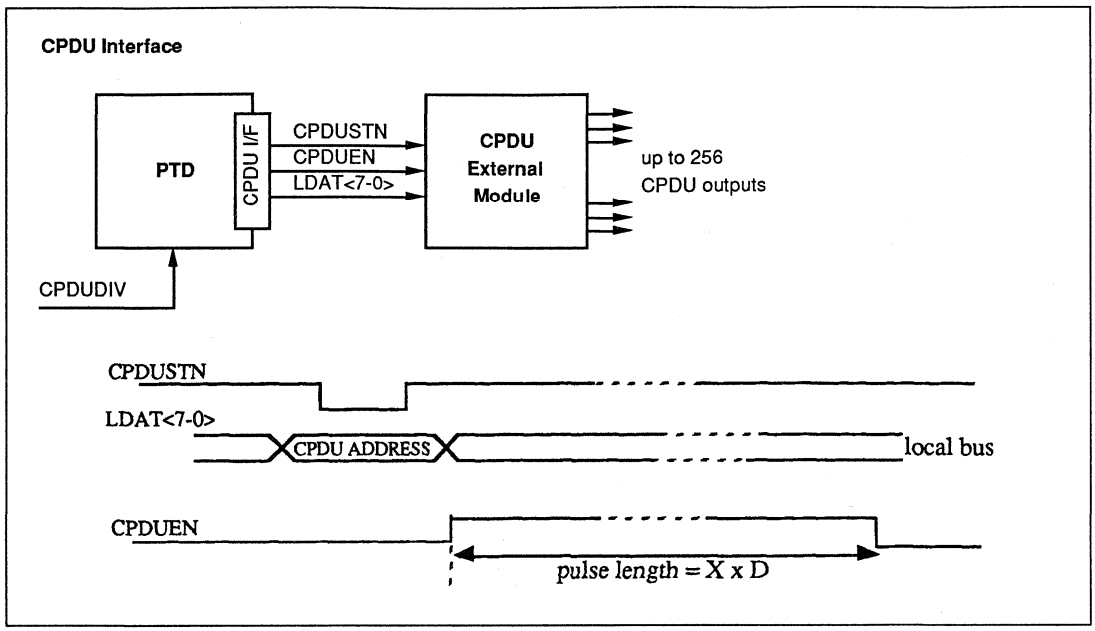


Figure 19: CPDU Interface

5.6 LOCAL BUS INTERFACE

This interface is used to access the external memory map. It consists of the following signals:

- LADR<10..0>: address bus (output),
- LDAT<7..0>: data bus (input/output),
- RWN: read write output,
- LACK: memory acknowledge input,
- RAMCSN: RAM chip select output,
- ROMCSN: ROM chip select output,
- LACCS: chip select output asserted for recovery LAC counter access.

The Local bus cycle is started by asserting the RWN and CSN signals and activating the LADR signal. It is ended by asserting LACK signal. If extended access times are not required, LACK can be permanently asserted. This interface provides a bus fault timer which is enabled when CSN signals are active and reset when LACK signal is active. If a reset doesn't occur within a minimum of 32 Tck (8 us for a 4 MHz clock frequency) and a maximum of 64 Tck (16 us for a 4 MHz clock frequency), the current Local bus cycle is aborted by forcing CSN inactive. The functional timings corresponding to the local bus interface are given in section 8.2.

5.7 MEMORIES

The PTD manages two types of memory:

- RAM to temporarily store the received TC data and all protocol variables (counter values, programmable key, ...). The RAM is organized in 2K words of 8 bits. In the case when it is used to store the eight bits of the recovery LAC counter, it should be non volatile.
- ROM (1Kx8) to store the mission specific data and the fixed Authentication key.

In order to allow the use of slow memories, an acknowledge signal (LACK) is used to indicate when the memory access is completed.

In order to save the 8 LSBs of recovery LAC counter in a device different from the RAM, two different chip select signals (RAMCSN and LACCS) are provided for the recovery LAC counter access. Two different modes are provided to manage the LAC counter select signals, these modes are selectable with a configuration pin called AUTSL as follows:

- AUTSL = 1: The recovery LAC counter is stored in RAM. The PTD asserts the RAMCSN signal when it performs the recovery LAC counter access.
- AUTSL = 0: The recovery LAC counter is stored in a device different from the RAM. The PTD asserts the LACCS signal when it performs the recovery LAC counter access. This non volatile memory could be for example an EEPROM for low radiation requirements or relays for radiation hardened recovery LACs.

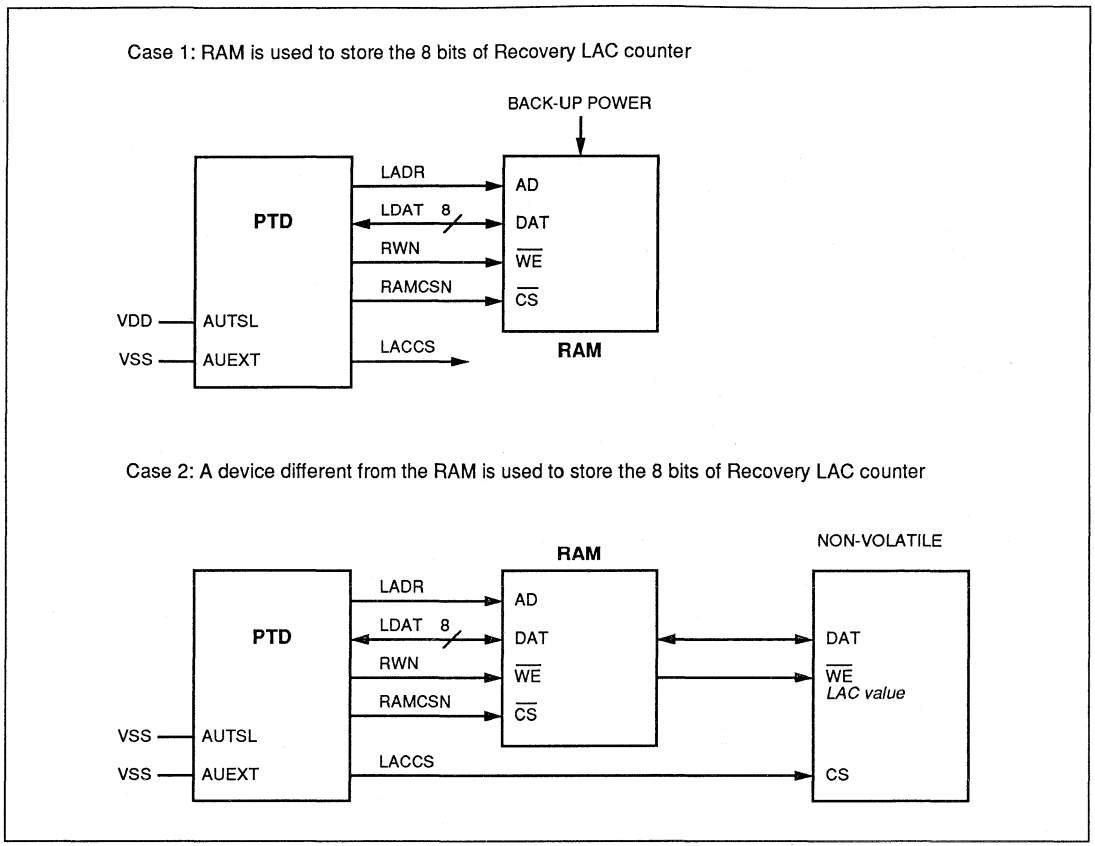


Figure 20: Recovery LAC Value Storage

A diagram of two possible implementations is given in Figure 20.

The RAM mapping is organized in such a way that the PTD is able to use the following external RAM buffers:

- two buffers working in a flip-flop mode between transfer and segmentation layer, respectively called Front End and Back End buffer.
- one buffer used by the CPDU interface

The buffer management is described in section 4.2. The memory mapping is defined in tables 5 and 6.

RAM	Start Address	End Address
Buffer0-(front end/back end) (see note 1)	000	0FF
Buffer1-(back end/front end) (see note 1)	100	1FF
Programmable key - Knapsack	200	367
Programmable key - Hashing	368	36F
Internal use (reserved)	370	373
Free	374	3FF
8 LSB of Recovery LAC	400	400
Internal use (reserved)	401	401
Auxiliary LAC Counter - octet 4 LSB	402	402
Auxiliary LAC Counter - octet 3	403	403
Auxiliary LAC Counter - octet 2	404	404
Auxiliary LAC Counter - octet 1 MSB	405	405
Principal LAC Counter - octet 4 LSB	406	406
Principal LAC Counter - octet 3	407	407
Principal LAC Counter - octet 2	408	408
Principal LAC Counter - octet 1 MSB	409	409
Free	40A	40F
AUS octet 10 - buffer 0	410	410
AUS octet 9 - buffer 0	411	411
AUS octet 8 - buffer 0	412	412
AUS octet 7 - buffer 0	413	413
AUS octet 6 - buffer 0	414	414
AUS octet 5 - buffer 0	415	415
AUS octet 4 - buffer 0	416	416
AUS octet 3 - buffer 0	417	417
AUS octet 2 - buffer 0	418	418
AUS octet 1 - buffer 0	419	419
FAR octet 4 - buffer 0	41A	41A
FAR octet 3 - buffer 0	41B	41B
FAR octet 2 - buffer 0	41C	41C
FAR octet 1 - buffer 0	41D	41D
Free	41E	42F
AUS octet 10 - buffer 1	430	430
AUS octet 9 - buffer 1	431	431
AUS octet 8 - buffer 1	432	432
AUS octet 7 - buffer 1	433	433
AUS octet 6 - buffer 1	434	434
AUS octet 5 - buffer 1	435	435
AUS octet 4 - buffer 1	436	436
AUS octet 3 - buffer 1	437	437
AUS octet 2 - buffer 1	438	438
AUS octet 1 - buffer I	439	439
FAR octet 4 - buffer 1	43A	43A
FAR octet 3 - buffer 1	43B	43B
FAR octet 2 - buffer 1	43C	43C
FAR octet 1 - buffer 1	43D	43D
Free	43E	5FF
CPDU buffer (see note 2)	600	6FF
Free	700	7FF

Note 1: The addresses 000 and 100 contain the buffer length (X) and the first word of the frame are stored at address X and 100+X respectively; the last word is stored at address 001 and 101 respectively.
Note 2: The address 600 contains the CPDU buffer length (X) and the first word of the frame is stored at address 600+X, the last word is stored at address 601.

Table 5: RAM Mapping

ROM	Start Address	End Address
Frame Header octet 1 (see note 3)	000	000
Frame Header octet 2 (see note 3)	001	001
Frame Header octet 3 (see note 3)	002	002
FARM PW' = PW - 1 (see note 4)	003	003
FARM NW' = 256 - NW (see note 4)	004	004
Authenticated MAP ID pointer (see note 5)	005	005
CPDU Packet Header octet 1 and 2 (see note 6)	006	007
Free	008	0FF
MAP frequency table defined in section 5.2	100	13F
Free	140	1FF
Fixed key - Knapsack (see note 7)	200	367
Fixed key - Hashing (see note 8)	368	36F
Free	370	3FF

Note 3: These 3 octets contain all the fields of the Frame Header including reserved bits and version bits. Bypass and Control flags (in Frame Header octet 1) form the only field that is not a fixed value: the value of these 2 bits in ROM has no influence on the PTD operation (default value = 00).
Note 4: In order to facilitate the implementation of the FARM Sliding Window Concept in the PTD, the values stored in the ROM are not PW and NW but:
- PW' = PW - 1
- NW' = 256 - NW

The PW' and NW' numbers can be any value between 0 and 255.
Note 5: Bits 7 and 6 are not used.
Note 6: These 2 octets contain all the field of the Packet Header including version and type bits.
Note 7: The Knapsack key mapping is given in Figure 9. Address 200 contains the least significant octet of the first Knapsack coefficient W0. Address 201 contains octet 1 of the first Knapsack coefficient W0, (see example below).
Note 8: The Hashing key mapping is given in Figure 9. Address 368 contains the 4 LSBs of the Hashing key stored at the right of the memory octet in the reverse order. Address 369 contains the 8 following bits in the reverse order. **Caution:** if the Hashing key is read bit by bit starting from the MSB, the memory must be filled from right to left, (see example below).

Table 6: ROM Mapping

Example

An example of ROM programming is given here for a fictitious spacecraft.
Note: In the following example 16# indicates hexadecimal, 10# indicates decimal, 2# indicates binary.

The value of the spacecraft ID is : 16#301
The value of the virtual channel ID is : 16#20
The value of the Application Process ID is : 16#456
For the FARM-1 process, the values of PW and NW are : 10#100 and 10#100
The Authenication MAP ID Pointer is : 16#15
For the CPDU, the Application Process Identifier is : 16#456

Frame Header octet 1 contains the following fields:
- Version number : 2#00 in accordance with ref 1
- Bypass flag : 0 or 1 (no influence): 0 for example
- Control Comrnand flag : 0 or 1 (no influence): 0 for example
- Reserved field A : 2#00 in accordance with ref 1
- Spacecraft ID (2 MSBs) : 2#11

The value of the ROM at address 000 is: 16#03

Frame Header octet 2 contains the following field:
- Spacecraft ID (8 LSBs) : 2#00000001

The value of the ROM at address 001 is: 16#01

Frame Header octet 3 contains the following fields:
- Virtual Channel ID : 2#100000
- Reserved field B : 2#00 in accordance with ref 1

The value of the ROM at address 002 is: 16#80

The calculation of PW' gives: PW' = PW - 1 = 100 - 1 = 99—> 16#63
The value of the ROM at address 003 is: 16#63

The calculation of NW' gives: NW' = 256 - NW = 256 - 100 = 156—> 16#9C
The value of the ROM at address 004 is: 16#9B

The authenticated MAP ID is 5 bits long. The 5 LSBs of the ROM value @ address 05 correspond to the authenticated MAP ID, the 3 MSBs can be either 0 or 1 (0 for example).
The value of the ROM at address 005 is: 16#15
CPDU Packet Header octet 1 contains the following fields:

Version number	: 2#000 in accordance with ref 1
Type	: 1 for CPDU
Data Fields Header flag	: 0 for CPDU
Application Process ID (3 MSBs)	: 2#100

The value of the ROM at address 006 is: 16#14

CPDU Packet Header octet 2 contains the following field:

Application Process ID (8 LSBs)	: 2#01010110

The value of the ROM at address 007 is: 16#56

The ROM will be programmed as follows:

Address	Data
000	03
001	01
002	80
003	63
004	9C
005	15
006	14
007	56

Knapsack and Hashing Key

If the Knapsack key is (example from ref.2 appendix B2)

W0 : 00 01 02 03 04 05
W1 : 06 07 08 09 0A 0B

W59 : 62 63 64 65 66 67

And if the Hashing Key is : C0...C59 A AA AA AA AA AA AA AA
MSB

The ROM will be programmed as follows:

Address	Data
200	05
201	04
202	03
203	02
204	01
205	00
206	0B
207	0A
etc	etc
367	62
368	05
369	55
370	55
etc	55
36E	55
36F	55

5.8 EXTERNAL AUTHENTICATION INTERFACE

This interface is provided to connect the PTD with an external Authentication Unit. The PTD allows the external AU to access the data buffer (described in section 5.7) of the RAM in order to process a TC segment which is to be authenticated. The interface is composed of the following signals:

- AUDIS: (input) This signal functions as for the internal AU, disabling the authentication unit.
- AUEXT: (input) This signal indicates the use of an external authentication unit.
- AUST: (output) This signal indicates that a TC frame has been received and must be authenticated. In this case, AUST is activated a few clock periods after the deactivation of the DECOD output indicating the end of the tail sequence of the frame.
- AUBUF: (output) This signal indicates to the external AU which RAM buffer is the back-end buffer containing the TC segment to be authenticated.
- BRQN: (input) This signal is the bus request to read or write the buffer from the external AU. It is activated for each external access to memory.
- BGRN: (output) This signal is the acknowledge of the PTD to BRQN; the PTD will then tristate its signals connected to the RAM (RAMCSN, ROMCSN, LACCS, RWN, LADR and LDAT). The LACK input has no effect when BGRN output is asserted.
- AUEND: (input) AU result validation. This signal indicates the end of the external authentication process and validates the AUR signal.
- AUR: (input) AU result signal. This signal indicates that the received TC frame is authorized or non authorized at the rising edge of AUEND.
- AUTSL: (input) AU tail length select signal. This signal allows definition of the length of the AU tail as follows:
  - AUTSL = 0: The length of the AU tail shall be 9 octets. In this case the 9 last octets of the segment authenticated by the external AU will be deleted by the PTD before transferring the segment to the application.
  - AUTSL = 1: The length of the AU tail shall be 0 octets. In this case all octets of the segment authenticated by the external AU shall be transfered to the application.
- AUSBUF: (output) This signal indicates which AU Status buffer the external AU must update.
- FARBUF: (output) This signal indicates which FAR status buffer the external AU must update (the external AU shall update only the bits 28 through 30 of the FAR status).

The external AU process starts upon receipt of the rising edge of the AUST signal, which is asserted by the PTD until the AUEND input is asserted indicating that the external AU process is finished. The result of the external authentication is given by the AUR signal (set to 1 for a valid authentication). The total duration of the external AU process plus the duration of the MAP output (if it exists) must be smaller than the duration of the next frame to arrive, measured from the start of the frame to the end of the last valid codeblock. A longer duration may lead to a rise of the FARMB WAIT flag. The result must be given to the PTD before the end of the last valid codeblock of the next frame to arrive, so as not to lock the back-end/front-end buffer toggling mechanism, and the FAR buffer management of the next frame.

The external AU can also write the AUS status in the local RAM, in the buffer number given by the AUSBUF output. The PTD locks the toggling mechanism of the AU status buffer while AUST is high in order to prevent data corruption. The external AU can also write bits 28 to 30 of the FAR status by writing the fourth octet of the FAR status in the local RAM, in the buffer number indicated by the FARBUF output. A similar mechanism locks the toggling of the FAR buffer when the AUST output is high. The AUS and FAR buffer update can start when the PTD activates the AUST output and shall be completed when the application asserts the AUEND signal. The local memory interface provides a bus arbiter fault timer. This timer is enabled when BGRN signal is active and reset when BRQN signal is inactive. If a reset does not occur within a minimum of 32 Tck and a maximum of 64 Tck (8 to 16 µs at 4 MHz), the BGRN signal is forced to inactive state. The functional timings corresponding to this interface are given in section 8.2.

6. STATE AFTER RESET

Asserting the RESETN signal asynchronously forces the local bus interface to avoid bus contention. The master clock should be started before RESETN deassertion. After 2 master clock cycles, the PTD is in a stable state and all its outputs take their cold start value. Deasserting the RESETN signal starts the initialisation phase. After this phase, the PTD registers are initialised.

PTD Outputs After the Assertion of RESETN Input

- LADR<10..0> —> 000
- LDAT<7..0> —> ZZ
- RWN —> 1
- RAMCSN —> 1
- ROMCSN —> 1
- LACCS —> 0
- all other outputs at unknown state

PTD Outputs After the Reset Sequence

- LADR<10..0> —> 000
- LDAT<7..0> —> ZZ
- RWN —> 1
- BGRN —> 1
- RAMCSN —> 1
- ROMCSN —> 1
- LACCS —> 0
- MAPSTN —> 1
- MAPCK —> 0
- MAPDSR —> 0
- MAPDATA —> 0
- MAPADT —> 0
- CPDUSTN —> 1
- CPDUEN —> 0
- CLCWDA —> 0
- TMD —> 0
- CLCWDB —> 0
- PRDY —> 0
- PBUS<15..0> —> ZZZZ
- AUST —> 0
- AUBUF —> 1
- AUSBUF —> 0
- FARBUF —> 0 after Reset, 1 after initialization (FAR write)
- SELTC<2..0> —> 111
- DECOD —> 0

PTD Outputs After the Initialisation Phase

CODING LAYER:
The coding layer is ready to receive a frame after the reset.

TRANSFER LAYER:
The transfer layer initialisation state after reset is the following:

- FARM-1 state : lockout
- FARMB counter : 11
- V(R) counter : 00000000

The cold start value of the CLCW (2 octets) is X000 (where X can be hexadecimal 2, 6, A or E).
The value of the MSB (No RF available) depends on the value of the RFAVN pin. The value of the second MSB (No Bit Lock) depends on the activation of the Tca signals (see section 4.6).

AUTHENTICATION LAYER:
The cold start initialisation state for the AU layer can be summarized as follows if AUDis = 0 and AUExt = 0:

- Key in use : fixed key
- Contents of programmable key : undefined
- Contents of Principal and Auxiliary LAC Registers : all ones
- Contents of the Recovery LAC counter : unchanged by the PTD

The cold start value of the AU Status (10 octets) takes the following value if AUDis = 0 and AUExt = 0:

3FFFFFFF 7FFFFFFF 00XX in hexadecimal

The value of the last octet corresponds to that of the 8 LSBs of the recovery LAC, which should be maintained even in the event of loss of power. Thus, this value shall be defined during the system implementation.

SEGMENT LAYER:

The segment layer is ready to receive a new segment. The MAP outputs are inactive. The cold start value of the FAR (4 octets) is the following: 00007FE0 in hexidecimal.

CPDU LAYER:

The CPDU layer is ready to receive a new CPDU. The CPDUEN output is inactive. The cold start value of the CPDU status (2 octets) is: 3FFF in hexadecimal.

7. SIGNAL DESCRIPTION

In this pin description, first the name of the pin is given, then its type (input (I) or output (O)), and then a brief description.

Total input pins : 47
Total output pins : 51
Total I/O pins : 8
Total number of Input, Output and I/O pins : 106

Note: Bit numbering convention: for busses, the bit number 0 is considered as the Least Significant Bit (LSB). For strobe signals, it is indicated in the text if they are active on low or high level.

Transponder Interface

TCC0-TCC5	I	Symbol Clock signals. These signals are only recognised while Channel Active Indication input is asserted. These signals can be asynchronous.
TCS0-TCS5	I	Symbol Stream signals. The data should be valid at the falling edge of the TCCi signals. These signals can be asynchronous w.r.t. system clock, but not w.r.t. symbol clock signals.
TCA0-TCA5	I	Channel Active Indication signals. These signals serve as enable signals for the Symbol Stream signals. Active high. These signals can be asynchronous.

Local Bus Interface

LADR<10..0>	O	Local Address Bus . This bus is unidirectional and is tristated when the BGRN signal is asserted. LADR<0> is the LSB.
LDAT<7..0>	I/O	Data Bus - This 8 bit data bus is driven as outputs during write cycles and as inputs during read cycles. This bus is tristated when the BGRN signal is asserted. LDAT<0> is the LSB.
RWN	O	Read/Write signal. This signal indicates the direction of the data transfer on the Local Bus and is tristated when the BGRN signal is asserted. RWN = 1: read mode. RWN = 0: write mode.
LACK	I	Memory acknowledge signal. This signal allows wait state cycles to be inserted for memory (RAM, ROM or LAC) read and write access and for CPDUSTN and MAPSTN outputs. LACK=0 inserts wait states. LACK can be permanently connected to 1 when no wait states are required. This signal can be asynchronous. Active high.
BRQN	I	Bus request signal. This signal is asserted by an external unit to request the Local Bus (external Authentication Unit for instance). Active low. This signal can be asynchronous.
BGRN	O	Bus grant signal. This signal is asserted to allow an external unit to use the Local Bus. Active low.
RAMCSN	O	Ram chip select signal. This signal is asserted during RAM access and is tristated when the BGRN signal is asserted. It is affected by the LACK input. Active low.
ROMCSN	O	Configuration Rom chip select signal. This signal is asserted during Configuration Rom access and is tristated when the BGRN signal is asserted. It is affected by the LACK input. Active low.
LACCS	O	Non volatile memory select signal. This signal is asserted during recovery LAC counter access and is tristated when BGRN signal is asserted. It is affected by the LACK input. Active high.

Map Interface

MAPSTN	O	MAP address strobe signal. This signal allows the MAP Demultiplexer circuitry to latch the MAP identifier present on the local data bus. It is affected by the LACK input. Active low.
MAPCK	O	MAP clockout signal. This signal is only activated when both MAPDSR and MAPDTR signals are active.
MAPDSR	O	MAP data set ready signal. This output indicates that a TC segment is available for transfer. Active high.
MAPDTR	I	MAP data terminal ready signal. This signal indicates that the receiving device is ready to clock in the segment data in serial mode or a segment data sample in parallel mode. Active high. This signal can be asynchronous.
MAPDATA	O	MAP segment data serial line. The segment data is clocked out on the falling edge of the MAPCK signal.
MAPADT	O	MAP abort data transfer signal. This output is asserted when the PTD has aborted the transfer of a TC segment. Active high.

CPDU Interface

CPDUSTN	O	CPDU address strobe signal. This signal allows the CPDU interface to latch the CPDU output address present on the local data bus LDAT<7..0>. It is affected by the LACK input. Active low.
CPDUEN	O	CPDU enable signal. This signal provides the command pulse with the appropriate duration. Active high.
CPDUDIV	I	CPDU clock division selection input. CPDUDIV = 0: the CPDU base clock (corresponding to D) is the system clock CLK divided by 40960. CPDUDIV = 1: the CPDU base clock (corresponding to D) is the system clock CLK divided by 8192.

CLCW Interface

CLCWSA	I	Nominal CLCW status sample. This signal indicates that the CLCW status is sampled by the telemetry interface. Active low. This signal can be asynchronous
CLCWCA	I	Nominal CLCW status clockout signal. This signal is provided to the PTD when CLCWSA signal is active. This signal can be asynchronous
CLCWDA	O	Nominal CLCW status data line (serial mode). The data is provided either on the falling edge of CLCWSA or on the falling edge of CLCWCA.
CLCWSB	I	Redundant CLCW status sample. Active low. This signal can be asynchronous
CLCWCB	I	Redundant CLCW status clockout signal. This signal can be asynchronous
CLCWDB	O	Redundant CLCW status data line (serial mode). The data is provided on the falling edge of CLCWSB or on the falling edge of CLCWCB.

Telemetry Interface

CPDUS/PCSN	I	CPDU status report sample. This signal indicates that the CPDU status report is sampled by the telemetry interface in serial mode. Active low . This signal has the function parallel bus chip select (PCSN) in parallel mode. This signal can be asynchronous
FAR1S/PAD2	I	FAR status report first sample. This signal indicates that the first 16 bits of FAR are sampled in serial mode. Active low. This signal has the function bit 2 of parallel address bus (PAD2) in parallel mode. This signal can be asynchronous
FAR2S/PAD1	I	FAR status report second sample. This signal indicates that the last 16 bits of FAR are sampled in serial mode. Active low. This signal has the function bit 1 of parallel address bus (PAD1) in parallel mode. This signal can be asynchronous
AU1S/PAD0	I	AUS status report first sample. This signal indicates that the first 16 bits of AUS are sampled in serial mode. Active low. This signal has the function bit 0 of parallel address bus (PAD0) in parallel mode. This signal can be asynchronous.
AU2S	I	AUS status report second sample. This signal is used to read out the last 4 bits of the AU staus report by asserting it four times. Active low. This signal can be asynchronous.
TMC	I	Common status clockout line used for CPDU, FAR and AUS (serial mode). This signal can be asynchronous.
TMD	O	Common status data line for CPDU, FAR and AUS (serial mode). The data is provided on the falling edge of CPDUS, FAR1S, FAR2S, AU1S or AU2S, or after the falling edge of TMC.

Parallel Interface

PRDY	O	Parallel interface control line. This output is asserted when the data selected by PAD<2...0> is available in parallel mode. Active low.
PBUS<15..0>	O	Parallel interface data bus PBUS<15..0> (PBUS0 being the LSB). PBUS tristate is controlled by the PCSN input. When PCSN is deasserted PBUS is tristated.

External Authentication Unit Interface

AUDIS	I	Internal AU disable signal. This signal allows bypassing of the internal or external authentication unit. The internal and external AU are disabled when AUDIS is high. This signal can be asynchronous
AUEXT	I	External AU select signal. This signal indicates the use of an external authentication unit. The PTD uses the external AU when AUEXT is high and the internal AU when AUEXT is low. This signal can be asynchronous
AUST	O	AU start signal. This signal indicates that a TC frame is received and must be authenticated. It remains active as long as the external AU is working; it is deasserted after the activation of the AUEND input. Active high.
AUBUF	O	Buffer indication signal. This signal indicates which back-end buffer contains the TC segment to be authenticated. AUBUF=0: buffer 0 is used AUBUF=1: buffer 1 is used.
AUEND	I	AU result validation signal. This signal validates the authentication process result given on pin AUR, and indicates the end of the authentication process. This signal can be asynchronous
AUR	I	AU result signal. This signal indicates that the received TC frame is authorized or not authorized. AUR=0 indicates a bad authentication result, AUR=1 indicates a valid authentication. This signal can be asynchronous.
AUTSL	I	AU tail length select signal. This signal indicates the length of the tail for segments authenticated with the external AU. - AUTSL = 0: the length of the AU tail is 9 octets - AUTSL = 1: the length of the AU tail is 0 octets. If the internal AU is selected (AUEXT = 0), this signal defines the implementation of the Recovery LAC counter: - AUTSL = 0: the Recovery LAC counter is stored outside the RAM - AUTSL = 1: the Recovery LAC counter is stored in the RAM.
AUSBUF	O	AU Status buffer. This output indicates which AU status buffer that the external AU should update. - AUSBUF = 0: AU status buffer 0 - AUSBUF = 1: AU status buffer 1.
FARBUF	O	FAR buffer. This output indicates which FAR status buffer that the external AU should update. - FARBUF = 0: FAR status buffer 0 - FARBUF = 1: FAR status buffer 1.

Miscellaneous

RFAVN	I	Incoming signal from physical layer, used to generate CLCW report. Active low. Asynchronous.
VCLSB	I	Virtual Channel Identifier LSB (static input). This bit enables differentiation between nominal and redundant decoder, even when using the same Configuration ROM for both decoders. - VCLSB = 1: The 'VC ID' LSB read from the ROM is inverted - VCLSB = 0: The 'VC ID' LSB read from the ROM is not inverted.
SELTC<2..0>	O	Selected TC channel signals. These outputs indicate the last selected TC channel on which the data present in the back-end buffer was received, it does not concern the CLTUs being input. SELTC<0> is the LSB.
DECOD	O	Decode state signal. This signal indicates that the PTD is in the Decode state (active for all bits after the start sequence until and including the tail sequence); it can be used for a scrambler.
TMMOD	I	TM mode signal. This static signal allows selection of the telemetry serial mode. - TMMOD = 0: the status (CPDUS, FAR, AUS) words are fetched with 5 samples - TMMOD = 1: the status (CPDUS, FAR, AUS) words are fetched with 2 samples.
RESETN	I	Reset signal. This signal allows the initialization of the PTD. Active low.
PAR	I	Parallel or serial interface selecting pin. This static input allows selection of the parallel or serial interface for MAP data and TM data. - PAR = 1: parallel mode is selected - PAR = 0: serial mode is selected.
MODE	I	Reserved pin. This static input shall be connected to ground.
CONF	I	Reserved pin. This static input shall be connected to ground.
PRIOR	I	Priority mode configuration pin. When this static input is set to 1, the priority mode (TC channels selection) is selected.
TEST	I	Test pin for production test only. This static input shall be connected to ground in functional mode.
CLK	I	System Clock signal.
VDD	I	+5V (12 pins).
VSS	I	Ground (14 pins).

8. ELECTRICAL CHARACTERISTICS AND RATINGS

8.1 DC PARAMETERS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 7: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IHC}	CMOS input high voltage	-	0.8 V_{DD}	-	V_{DD}	V
V_{ILC}	CMOS input low voltage	-	V_{SS}	-	0.2 V_{DD}	V
V_{IHT}	TTL input high voltage	-	2	-	-	V
V_{ILT}	TTL input low voltage	-	-	-	0.8	V
V_{OH}	Output high voltage	I_{OH} = -3.2mA	0.9 V_{DD}	-	-	V
V_{OL}	Output high voltage	I_{OL} = 5.0mA	-	-	0.1 V_{DD}	V
I_{PDL}	Input Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-30	-	30	µA
I_{PDH}	Input Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{DD}	-30	-	150	µA
I_{PUL}	Input Pull-up current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-150	-	30	µA
I_{PUH}	Input Pull-up current	V_{DD} = 5.5V, V_{IN} = V_{DD}	-30	-	30	µA
I_L	Input leakage current	V_{DD} = 5.5V, V_{IN} = V_{SS} or V_{DD}	-10	-	10	µA
I_{OZL}	Output leakage current	V_{DD} = 5.5V, V_{OUT} = V_{SS}	-50	-	50	µA
I_{OZH}	Output leakage current	V_{DD} = 5.5V, V_{OUT} = V_{DD}	-50	-	50	µA
I_{OPDL}	Output Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{SS}	-50	-	50	µA
I_{OPDH}	Output Pull-down current	V_{DD} = 5.5V, V_{IN} = V_{DD}	-50	-	150	µA
I_{DD1}	Static Power supply Current	V_{DD} = 5.5V	-	0.5	20	mA
I_{DD2}	Dynamic Power supply Current	f = 4MHz, V_{DD} = 5.5V	-	20	40	mA

Notes: 1. V_{DD} = 5V ±10% over full temperature range.
2. Total dose radiation not exceeding 10^5 Rads(Si).
3. Mil-Std-883, method 5005, subgroups 1, 2, 3.
4. All outputs are suitable for TTL/CMOS drive.
5. Electro-Static Discharge protection is provided for all pins.
6. Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.
7. Input and output leakage measurements are guaranteed but not tested at -55°C.

Table 8: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	V_I = 0V	-	3	5	pF
C_{OUT}	Output Capacitance	$V_{I/O}$ = 0V	-	5	7	pF

NOTE 1: T_A = 25°C and f = 1MHz. Data obtained by characterisation or analysis; not routinely measured.

Table 9: Capacitance

8.2 AC CHARACTERISTICS

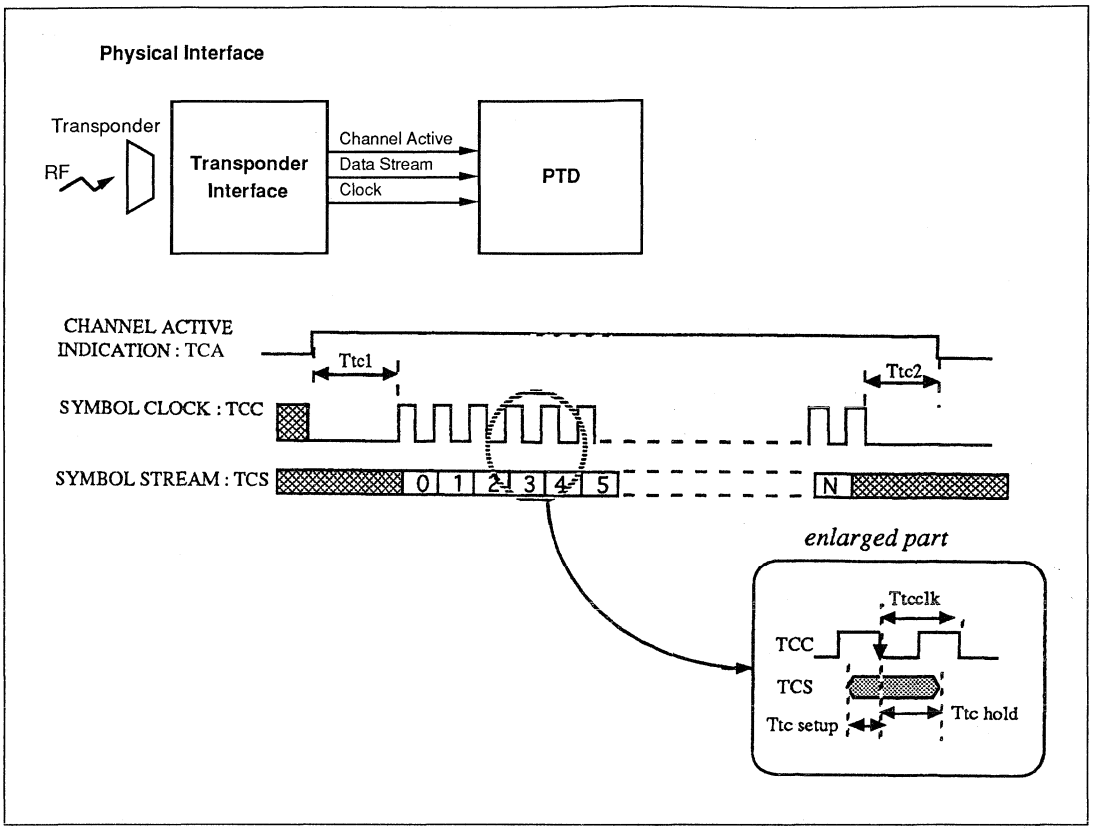
Symbol	Parameter	Conditions
F_T	Functionality	V_{DD} = 4.5 - 5.5V, FREQ = 4MHz $V_{IL} = V_{SS}$, $V_{IH} = V_{DD}$, $V_{OL} = V_{OH} = V_{DD}/2$ Temp. = -55°C to +125°C, GPS Pattern Set MIL-STD-883 5005 subgroups 7, 8A, 8B

Table 10: Functionality

Symbol	Parameter	Min.	Typ.	Max.	Units
Fck	Clock frequency	-	-	4	MHz
Tck	Clock period	-	1/Fck	-	-
Tcl	Clock low pulse width	100	-	-	ns
Tch	Clock high pulse width	100	-	-	ns

NOTES.
1. T_{CK} will be used as a reference for the timings.
2. For timings specified as a number of clock cycles, it should be noted that there is a variance of ±10ns caused by the hold time (for inputs only) and different delays for rising and falling signals.
3. It should be noted that a half clock cycle can mean either the longer or shorter time for a clock not having a duty cycle of 50%.
4. V_{DD} = 5V±10% over full temperature range.
5. Total dose radiation not exceeding 10^5 Rads (sec).
6. Input pulse = V_{SS} to 4V.
7. Measurement reference level = 1.5V.
8. Output load 1 TTL gate and C_L = 50pF.
9. Tables 11-25 contain Mil-Std-883, method 5005, subgroups 9, 10, 11.

Table 11: Clock Timings

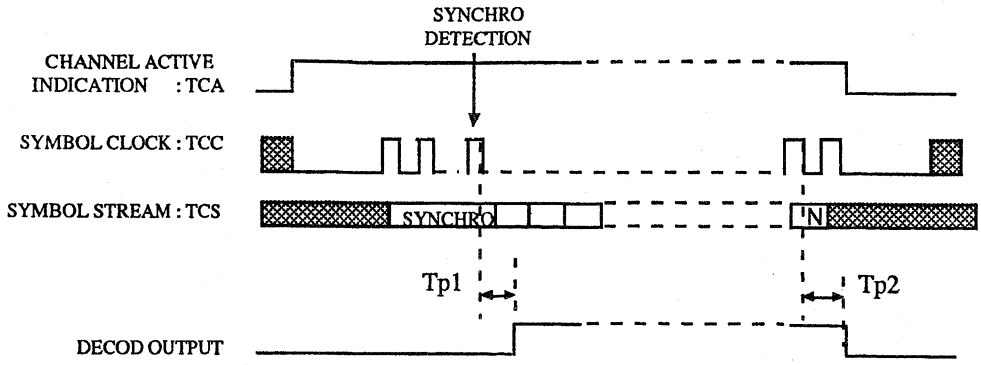


TIMING	Description	min	typ	max
Ttc1 *	TCA high to first TCC rising	4 Tck		
Ttc2 *	Last TCC falling to TCA low	4 Tck		
Ttcclk	TCC period	20 µs		
Ttc setup	TCS setup to TCC falling	0 ns		
Ttc hold	TCS hold after TCC falling	4 Tck		

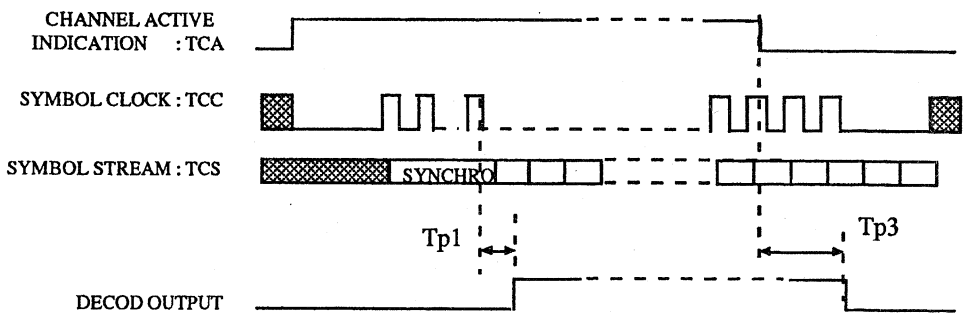
* NOTE: if the required timing is not fulfilled on Ttc1 and Ttc2, there is a risk of loss of the first or last bits.

Table 12: Physical Interface Timings

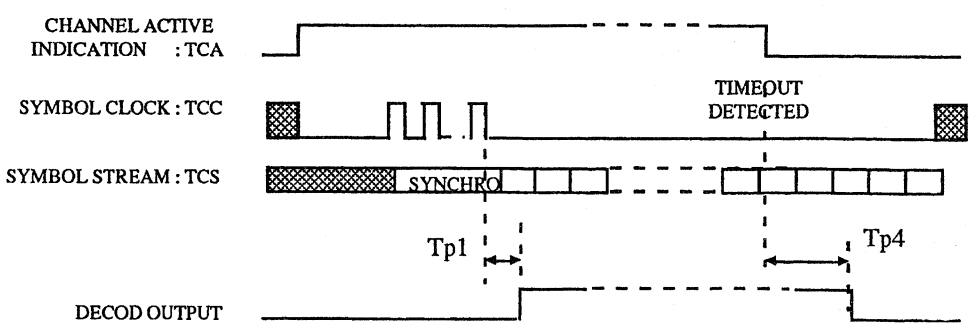
Decod Output



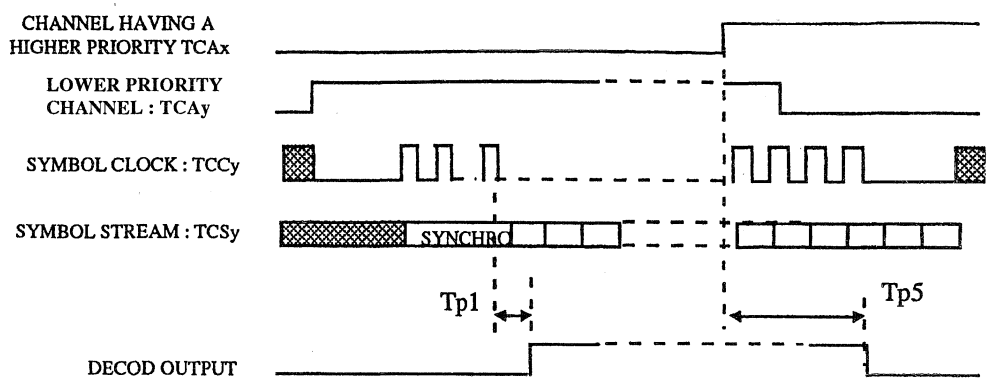
Case 1 : Codeblock Rejection or more than 37 codeblocks accepted



Case 2 : TCA deactivation



Case 3 : Timeout on TCC detected

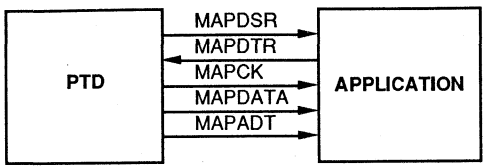


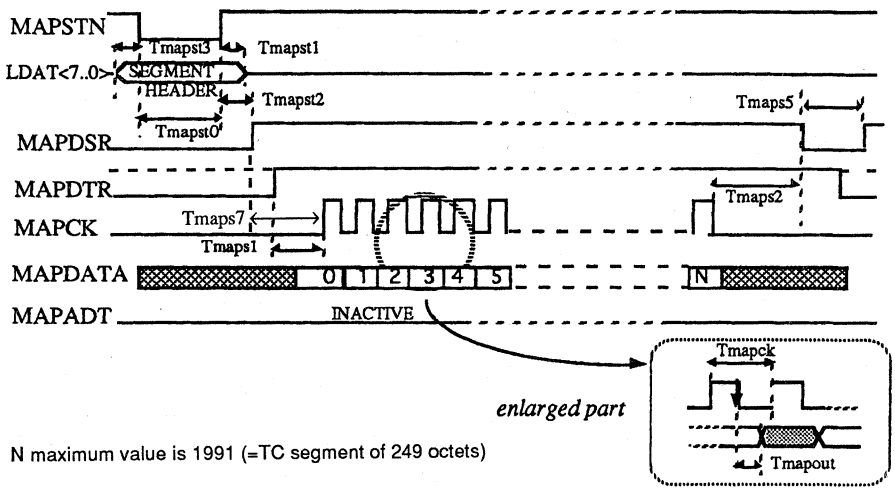
Case 4 : Activity on a channel having a higher priority detected in priority mode

Timing	Description	Min	Typ	Max
Tp1	TCC falling of the last synchro bit to DECOD rising			3 Tck
Tp2	TCC falling of the last bit of the rejected codeblock or of the last bit of codeblock number 38 to DECOD falling			3 Tck
Tp3	TCA deactivated to DECOD falling			3 Tck
Tp4	Timeout on TCC detected to DECOD falling			3 Tck
Tp5	TCA rising on the channel with higher priority to DECOD falling			3 Tck

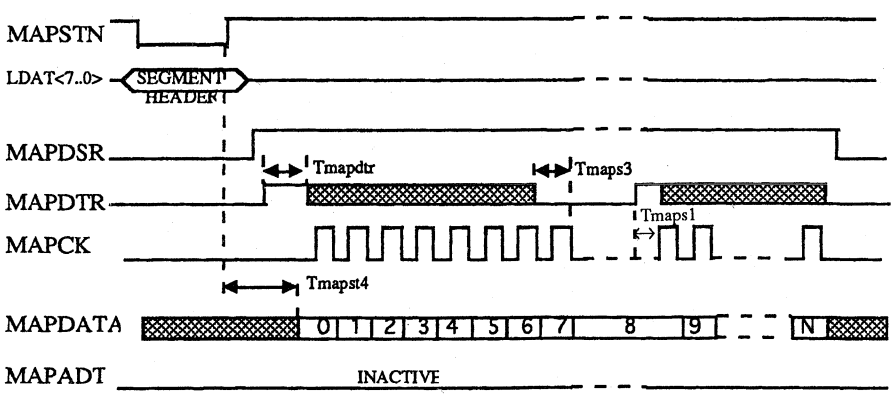
Table 13: DECOD Output Timings

Serial MAP Interface

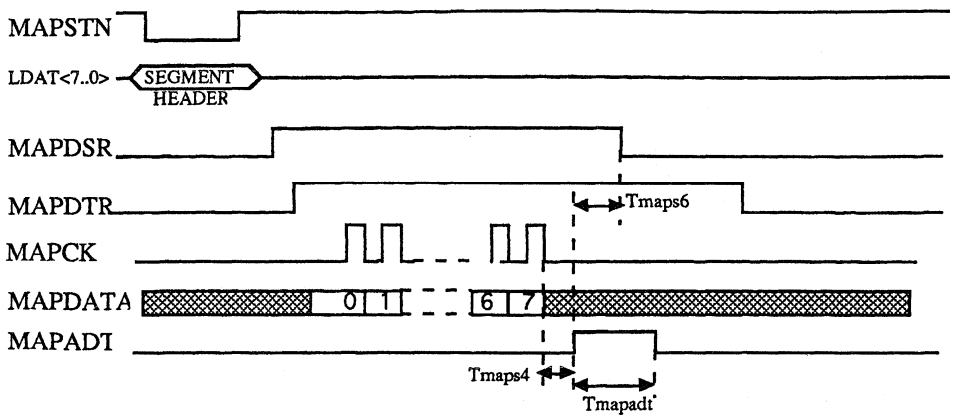




N maximum value is 1991 (=TC segment of 249 octets)



Example of data transfer with data flow control
for each MAPDTR pulse one octet is being transferred
N maximum value is 1991 (=TC segment of 249 octets)



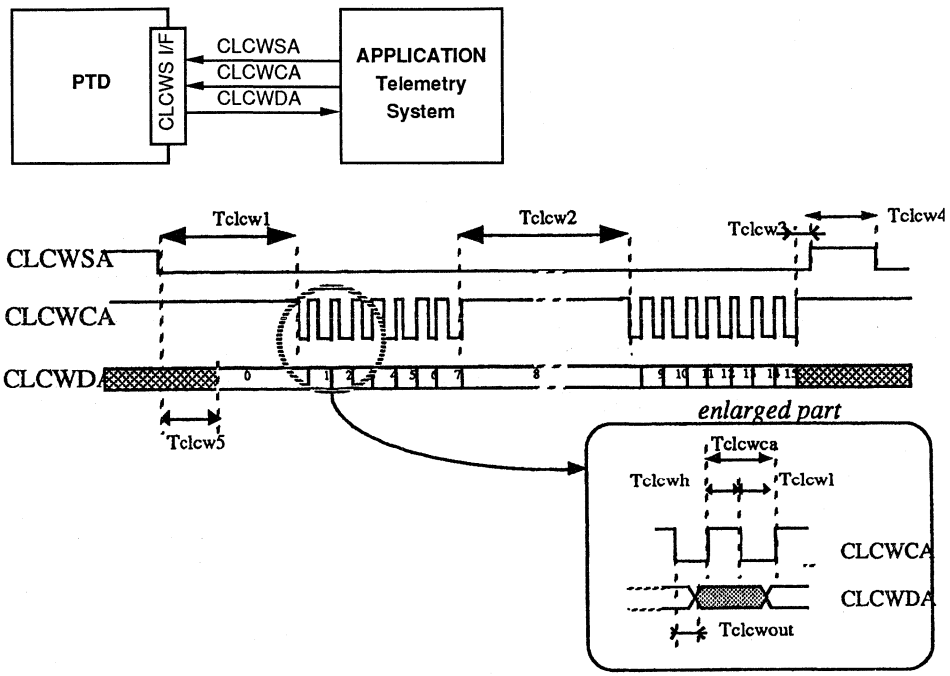
Example of an aborted data transfer.

Timing	Description	Min	Typ	Max
Tmapst0 (1) (3)	MAPSTN low pulse width		1 Tck	
Tmapst1	LDAT hold after MAPSTN rising	0.5 Tck		
Tmapst2	MAPST rising to MADSR rising	2 Tck		1 Tmapck + 2 Tck
Tmapst3	LDAT setup to MAPSTN falling	0.5 Tck		
Tmapst4	MAPSTN rising to MAPDATA valid	2 Tck		1 Tmapck + 2 Tck
Tmaps1	MAPDTR high to MAPCK rising	0.5 Tmapck		1.5 Tmapck + 1 Tck
Tmaps2 (3)	MAPCK falling to MAPDSR falling		1 Tmapck	
Tmaps3	MAPDTR setup to MAPCK falling	2 Tck		
Tmapck (2)	MAPCK period	2 Tck		$[2^{13}]$ Tck
Tmapout	MAPCK falling to MAPDATA valid	-5 ns		10 ns
Tmapdtr	MAPDTR high pulse width	2 Tck		
Tmapadt (3)	MAPADT high pulse width		2 Tmapck	
Tmaps4 (3)	MAPCK falling to MAPADT rising		1 Tmapck	
Tmaps5	MAPDSR falling to MAPDSR rising	56 Tck		
Tmaps6 (3)	MAPADT rising to MAPDSR falling		1 Tmapck	
Tmaps7 (4)	MAPDSR rising to MAPCK rising	0.5 Tmapck		1.5 Tmapck

Note (1): This timing is specified with no wait state configuration (LACK permanently asserted). The asserting of this signal is identical with the asserting of the RAMCSN signal in a write cycle.
Note (2): Tmapck period is programmable as defined in section 5.2.
Note (3): These timings are exact with a variance of -10ns to +10ns.
Note (4): This timing is for a data transfer with MAPDTR permanently asserted.

Table 14: Serial MAP Interface Timings

CLCW Serial Interface

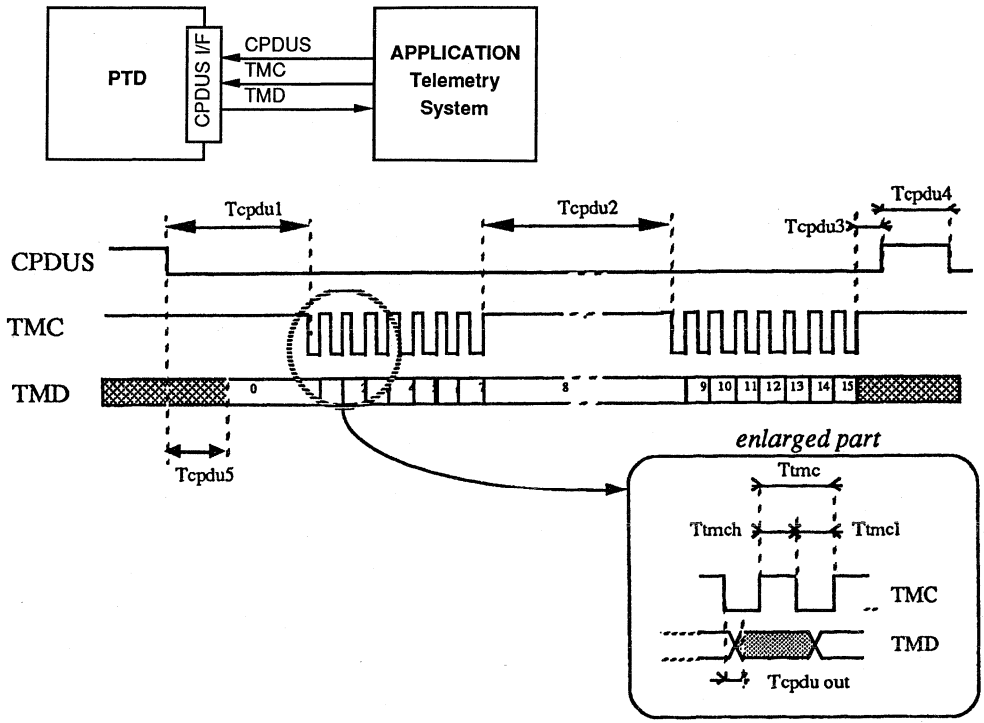


Timing	Description	Min	Typ	Max
Tclcw1	CLCWSA falling to CLCWCA falling	5 Tck		
Tclcw2	CLCWCA high pulse width between octets	2 Tck		
Tclcw3	CLCWCA setup to CLCWSA	0 ns		
Tclcw4	CLCWSA high pulse width	3 Tck		
Tclcw5	CLCWSA falling to CLCWDA valid (bit 0)	4 Tck		
Tclcwh	CLCWCA high pulse width	Tck		
Tclcwl	CLCWCA low pulse width	Tck		
Tclcwca	CLCWCA period	4 Tck		
Tclcwout	CLCWCA falling to CLCWDA valid	1 Tck		2 Tck

Note: The same timings apply for the redundant CLCW status telemetry interface, which is composed of CLCWSB, CLCWCB, CLCWDB signals.

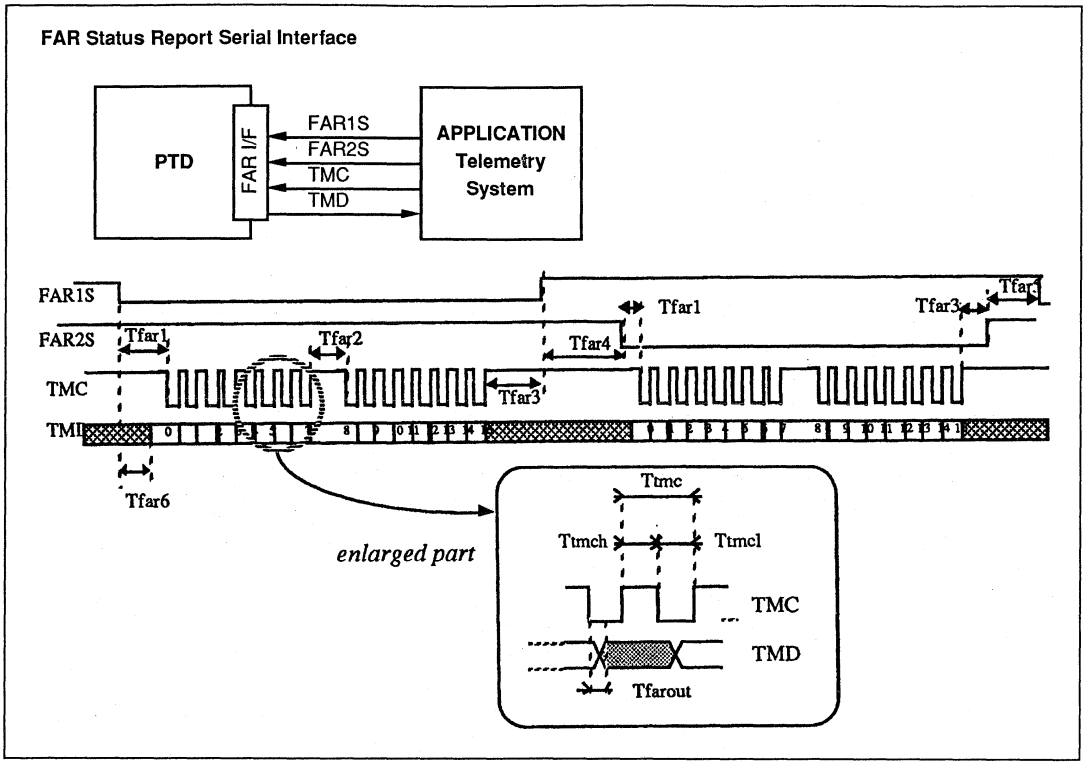
Table 15: CLCW Serial Interface Timings

CPDU Status Report Serial Interface



Timing	Description	Min	Typ	Max
Tcpdu1	CPDUS falling to TMC falling	6 Tck		
Tcpdu2	TMC high pulse width between octets	2 Tck		
Tcpdu3	TMC setup to CPDUS	0 ns		
Tcpdu4	CPDUS high pulse width	3 Tck		
Tcpdu5	CPDUS falling to TMD valid (bit 0)	5 Tck		
Ttmch	TMC high pulse width	Tck		
Ttmcl	TMC low pulse width	Tck		
Ttmc	TMC period	4 Tck		
Tcpduout	TMC falling to TMD valid	1 Tck		2 Tck

Table 16: CPDUS Serial Interface Timings

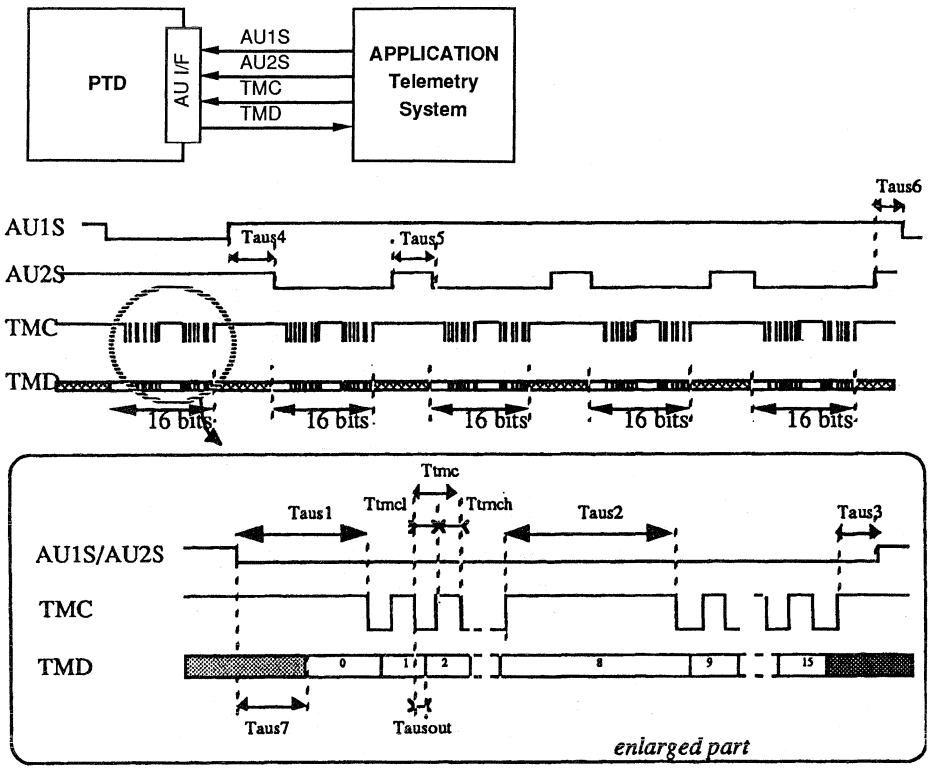


Timing	Description	Min	Typ	Max
Tfar1 (1)	FARS falling to TMC falling	16 Tck		
Tfar2	TMC high pulse width between octets	2 Tck		
Tfar3	TMC setup to FARS	0 ns		
Tfar4	FAR1S rising to FAR2S falling	2 Tck		
Tfar5	FAR2S rising to FAR1S falling	4 Tck		
Tfar6 (1)	FARS falling to TMD valid (bit 0)	15 Tck		
Ttmch	TMC high pulse width	Tck		
Ttmcl	TMC low pulse width	Tck		
Ttmc	TMC period	4 Tck		
Tfarout	TMC falling to TMD valid	1 Tck		2 Tck

Note (1): These timings are guaranteed when there is no request for the local bus through the BRQN input. In addition when using slow memories, the local memory accesses may be delayed by using the LACK input of duration d_L (defined by the user). In this case Tfar1 and Tfar6 become Tfar1+2d_L and Tfar6+2d_L.

Table 17: FAR Status Report Serial Interface Timings

AU Status Report Serial Interface

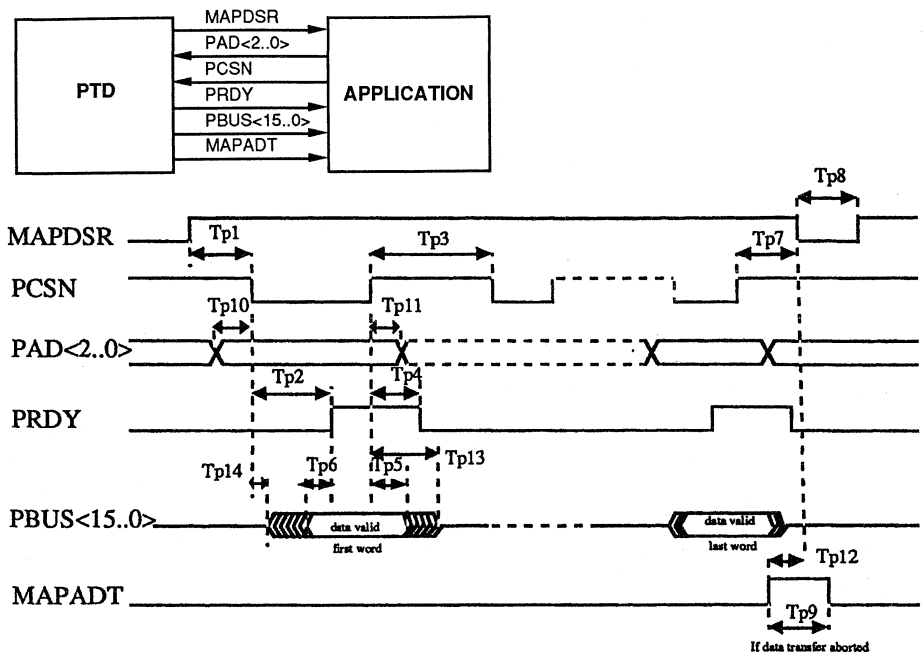


Timing	Description	Min	Typ	Max
Taus1 (1)	AUS falling to TMC falling	16 Tck		
Taus2	TMC high pulse width between octets	2 Tck		
Taus3	TMC setup to AUS	0 ns		
Taus4	AU1S rising to AU2S falling	2 Tck		
Taus5	AU2S rising to AU2S falling	2 Tck		
Taus6	AU2S rising to AU1S falling	4 Tck		
Taus7 (1)	AUS falling to TMD valid (bit 0)	15 Tck		
Ttmch	TMC high pulse width	Tck		
Ttmcl	TMC low pulse width	Tck		
Ttmc	TMC period	4 Tck		
Tausout	TMC falling to TMD valid	1 Tck		2 Tck

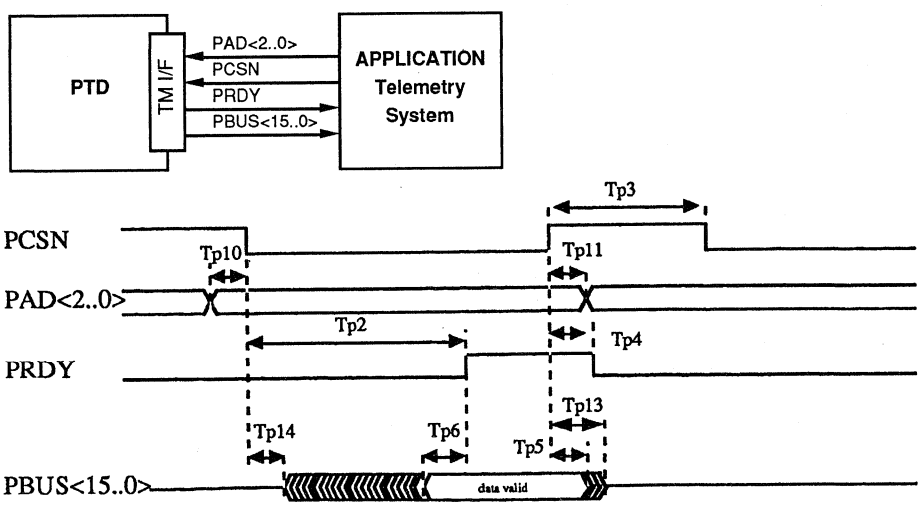
Note (1): These timings are guaranteed when there is no request for the local bus through the BRQN input. In addition when using slow memories, the local memory accesses may be delayed by using the LACK input of duration d_L (defined by the user). In this case Taus1 and Taus6 become Taus1+2d_L and Taus7+2d_L.

Table 18: AU Status Report Serial Interface Timings

Parallel MAP Interface



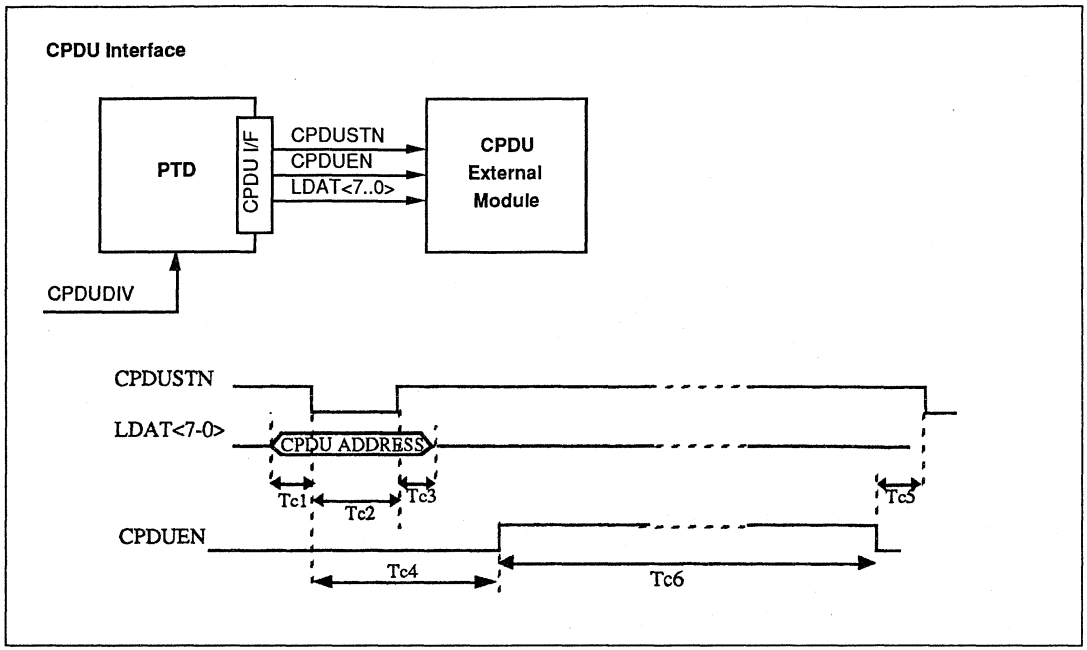
Status Report Telemetry Parallel Interface



Timing	Description	Min	Typ	Max
Tp1	MAPDSR rising to PCSN falling	0 ns		
Tp2 (1)	PCSN falling to PRDY rising - for MAP word (1) - for CLCW word - for CPDU status word - for AU and FAR status word (1)	2 Tck		17 Tck 5 Tck 7 Tck 13 Tck
Tp3	PCSN high width	Tck		
Tp4	PCSN rising to PRDY falling			39 ns
Tp5	PBUS hold after PCSN rising	0 ns		
Tp6	PBUS valid before PRDY	Tck		
Tp7	PCSN rising to MAPDSR falling	3 Tck		4 Tck
Tp8	MAPDSR low pulse width	40 Tck		
Tp9 (2)	MAPADT high pulse width		2 Tck	
Tp10	PAD setup to PCSN falling	Tck		
Tp11	PAD hold after PCSN rising	Tck		
Tp12 (2)	MAPADT rising to MAPDSR falling		Tck	
Tp13	PCSN rising to PBUS tristate			31 ns
Tp14	PCSN falling to PBUS asserted	0 ns		55 ns

Note (1): These timings are guaranteed when there is no request for the local bus through the BRQN input. In addition when using slow memories, the local memory accesses may be delayed by using the LACK input, two extra delays shall be added to Tp2.
Note (2): These timings are exact with a variance of -10ns to +10ns.

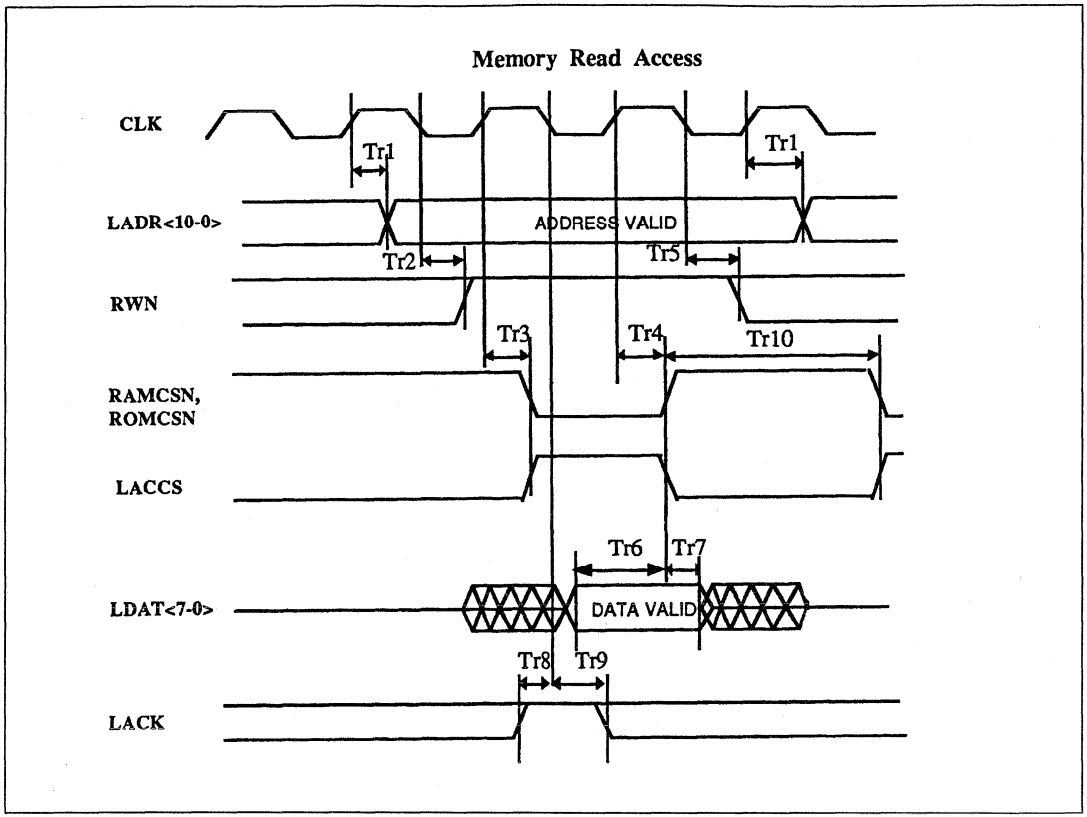
Table 19: Parallel MAP Interface Timings



Timing	Description	Min	Typ	Max
Tc1	LDAT setup to CPDUSTN falling	0.5 Tck		
Tc2 (1) (2)	CPDUSTN low pulse width		1 Tck	
Tc3	LDAT hold after CPDUSTN rising	0.5 Tck		
Tc4	CPDUSTN falling to CPDUEN rising			D/2 - 3 Tck
Tc5 (2)	CPDUEN falling to CPDUSTN falling		D/2 + 1 Tck	
Tc6	CPDUEN high pulse width	D + Tck	$[2^X]$xD + Tck	128D + Tck
D (1)	CPDUDIV = 0		40960 Tck	
D (1)	CPDUDIV = 1		8192 Tck	

Note (1): This timing is specified with no wait state configuration (LACK permanently asserted). The asserting of this signal is identical with the asserting of the RAMCSN signal in a write cycle.
Note (2): These timings are exact with a variance of -10ns to +10ns.

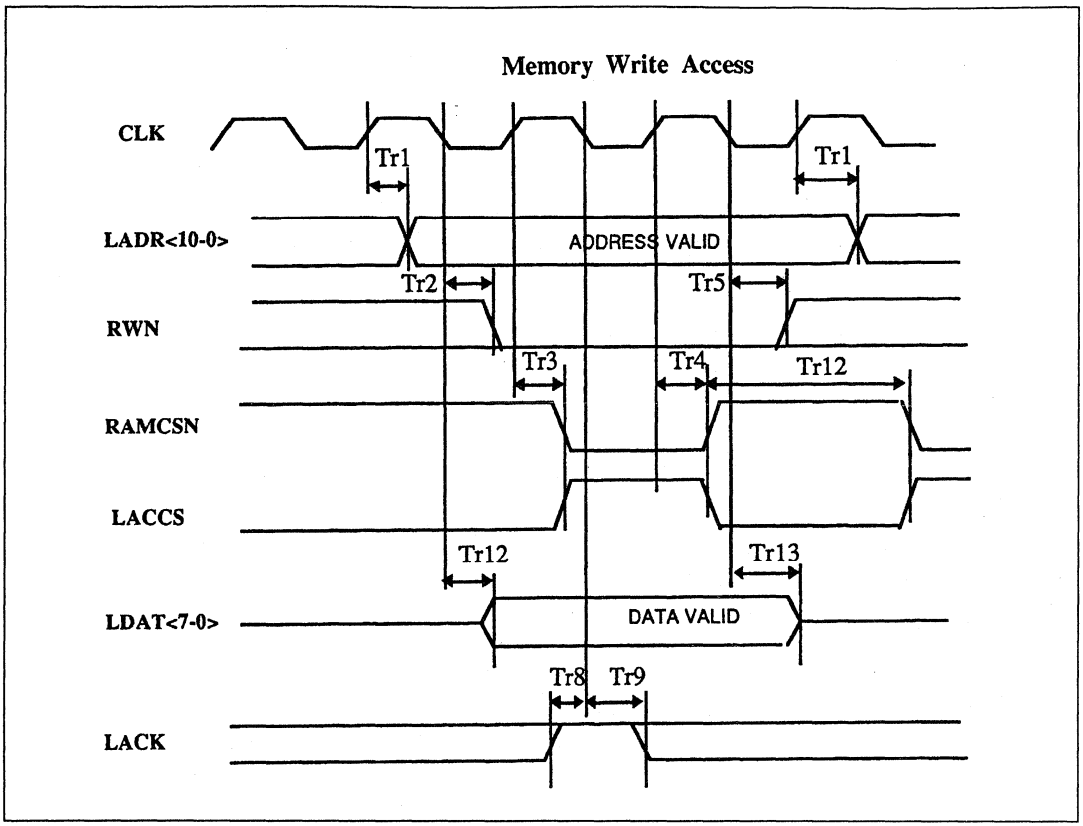
Table 20: CPDU Interface Timings



Timing	Description	Min	Typ	Max
Tr1	CLK rising to LADR valid	0 ns		150 ns
Tr2	CLK falling to RWN valid	0 ns		57 ns
Tr3	CLK rising to CSN asserted	0 ns		67 ns
Tr4	CLK rising to CSN deasserted	0 ns		68 ns
Tr5	CLK falling to RWN invalid	0 ns		57 ns
Tr6	LDAT setup to CSN deasserted	100 ns		
Tr7	LDAT hold after CSN deasserted	0 ns		
Tr8 (1)	LACK setup to CLK falling	20 ns		
Tr9 (1)	LACK hold after CLK falling	20 ns		
Tr10	CSN pulse width deasserted	2 Tck		

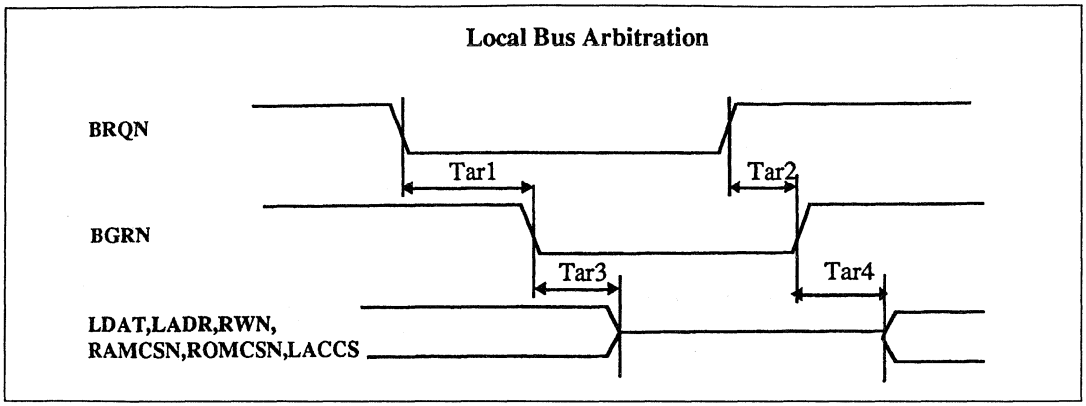
Note (1): Violation will lead to uncertainty about the number of wait states inserted.

Table 21: Memory Read Timings



Timing	Description	Min	Typ	Max
Tr12	CLK falling to LDAT valid	0 ns		62 ns
Tr13	CLK falling to LDAT hi-Z	0 ns		40 ns

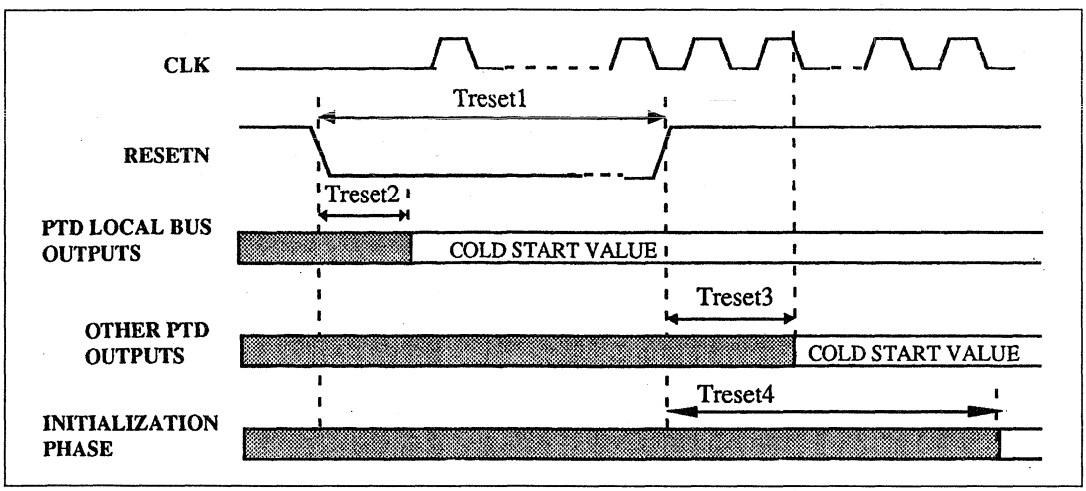
Table 22: Memory Write Timings



Timing	Description	Min	Typ	Max
Tar1 (1)	BRQN falling to BGRN falling	1.5 Tck		2.5 Tck
Tar2	BRQN rising to BGRN rising	1.5 Tck		2.5 Tck
Tar3	BGRN falling to Local Bus hi-Z			20 ns
Tar4	BGRN rising to Local Bus driven			20 ns

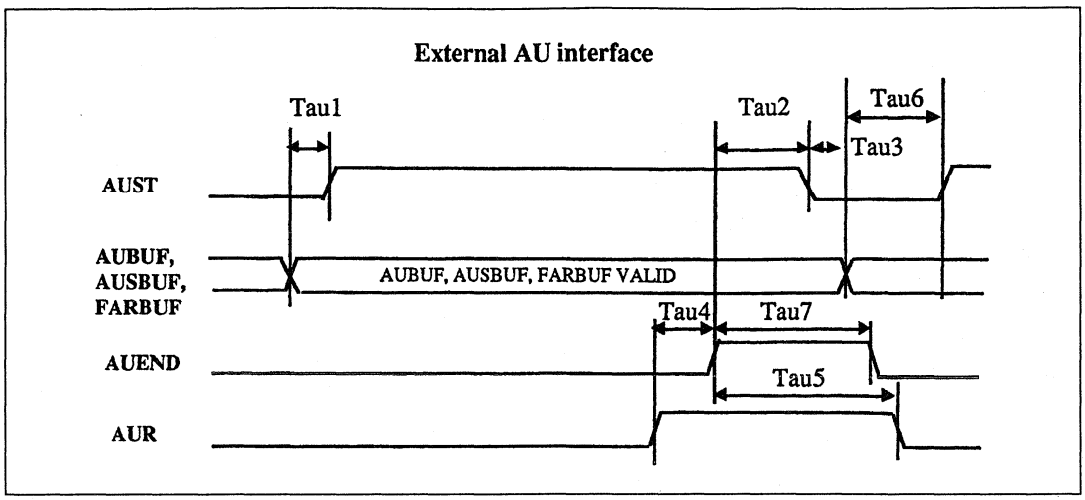
Note (1): This timing is dependent on the activity on the local bus. It is defined here for the case when the PTD does not use the local bus.

Table 23: Local Bus Arbitration Timings



Timing	Description	Min	Typ	Max
Treset1	ResetN low pulse width	5 Tck		
Treset2	ResetN asserted to local bus outputs at cold start values (0,1;Z)			60 ns
Treset3	ResetN deasserted to PTD outputs at cold start values (0,1;Z)			2 Tck
Treset4	ResetN deasserted to end of initialisation phase: PTD functional			200 Tck

Table 24: Reset Timings



Note: In order to use the external authentication unit, the AUDIS and AUEX signals should be set to 0 and 1 respectively.

Timing	Description	Min	Typ	Max
Tau1	AUBUF or AUSBUF or FARBUF setup to AUST rising	2 Tck		
Tau2	AUEND rising to AUST falling	2 Tck		3 Tck
Tau3	AUBUF or AUSBUF or FARBUF hold after AUST	0 ns		
Tau4	AUR setup to AUEND rising	2 Tck		
Tau5	AUR hold after AUEND rising	2 Tck		
Tau6	AUST pulse width deasserted	2 Tck		
Tau7	AUEND pulse width asserted	2 Tck		

Table 25: External AU Interface Timings

Subgroup	Definition
1	Static characteristics specified in Table 8 at +25°C
2	Static characteristics specified in Table 8 at +125°C
3	Static characteristics specified in Table 8 at -55°C
7	Functional characteristics specified in Table 10 at +25°C
8A	Functional characteristics specified in Table 10 at +125°C
8B	Functional characteristics specified in Table 10 at -55°C
9	Switching characteristics specified in Tables 11 to 25 at +25°C
10	Switching characteristics specified in Tables 11 to 25 at +125°C
11	Switching characteristics specified in Tables 11 to 25 at -55°C

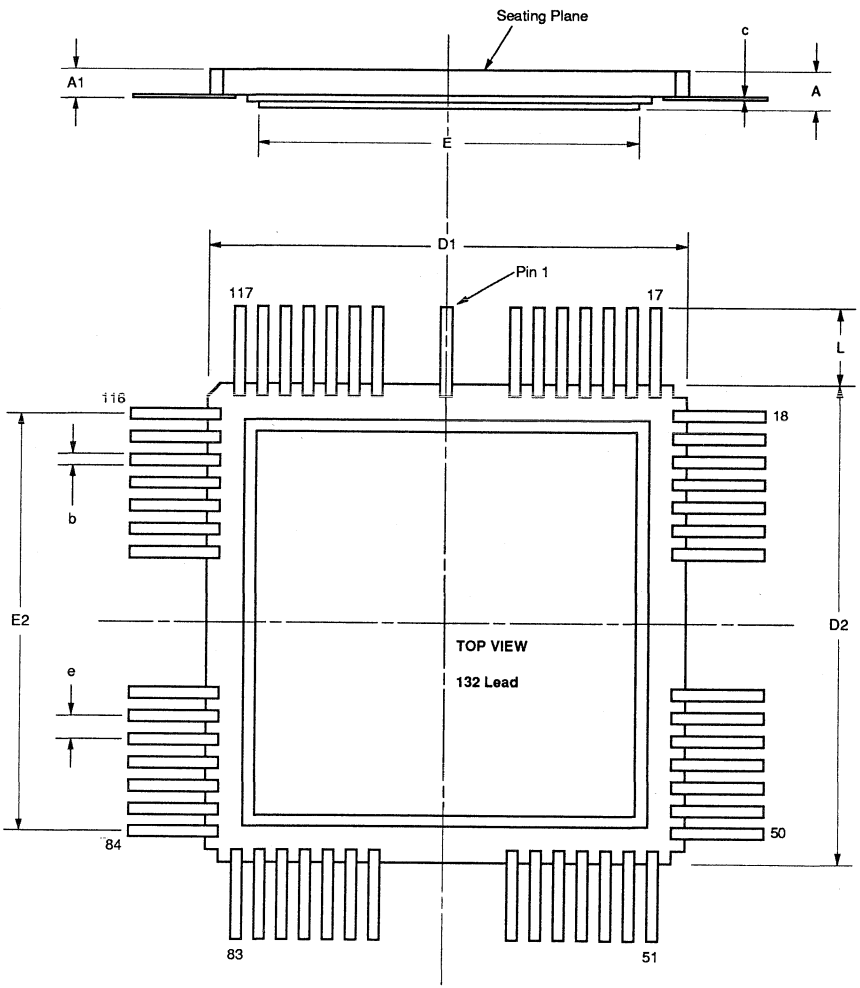
Table 26: Definition of Subgroups

9. PACKAGE DETAILS

9.1 DIMENSIONS

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.59	-	-	0.102
A1	1.37	-	1.88	0.054	-	0.074
b	0.23	-	0.33	0.009	-	0.013
c	0.10	-	0.18	0.004	-	0.007
D1, D2	-	-	24.38	-	-	0.960
E	-	-	18.11	-	-	0.713
E2	-	20.32	-	-	0.800	-
e	-	0.63	-	-	0.025	-
L	6.35	-	7.11	0.250	-	0.280

XG533



9.2 PIN ASSIGNMENT

The "type" field gives the type of buffer used in the PTD:

CMOS	for CMOS input
TTL	for TTL input
3STA	for tri-state output
TTL/CMOS	for TTL/CMOS output
TTL + 3STA	for a bidirectional TTL input associated with a tri-state output

The "buffer" field gives the name of the GPS MA9000a buffer used in the PTD:

CMOSIP	for input CMOS buffer
TTLIP	for input TTL buffer
BOP	for TTL/CMOS output buffer
TRIOUT	for output tristate buffer
CSCHMITT	for input CMOS buffer with Schmitt trigger

The "pu/pd" field indicates if an internal pull up or pull down is present in the buffer.

Note: Internal pull-up or pull-down resistors should not be relied upon for proper operation and/or termination of input levels under all operating conditions without prior consultation with GPS.

Transponder Interface

signal	pin	I/O	type	pu/pd	buffer	comments
TCC0	82	I	CMOS	PU	CSCHMITT	Symbol Clock signal
TCC1	79	I	CMOS	PU	CSCHMITT	" " "
TCC2	75	I	CMOS	PU	CSCHMITT	" " "
TCC3	72	I	CMOS	PU	CSCHMITT	" " "
TCC4	68	I	CMOS	PU	CSCHMITT	" " "
TCC5	65	I	CMOS	PU	CSCHMITT	" " "
TCS0	81	I	CMOS	PU	CSCHMITT	Symbol Stream signal
TCS1	78	I	CMOS	PU	CSCHMITT	" " "
TCS2	74	I	CMOS	PU	CSCHMITT	" " "
TCS3	71	I	CMOS	PU	CSCHMITT	" " "
TCS4	67	I	CMOS	PU	CSCHMITT	" " "
TCS5	64	I	CMOS	PU	CSCHMITT	" " "
TCA0	80	I	CMOS	PD	CSCHMITT	Channel Active Indication
TCA1	77	I	CMOS	PD	CSCHMITT	" " "
TCA2	73	I	CMOS	PD	CSCHMITT	" " "
TCA3	70	I	CMOS	PD	CSCHMITT	" " "
TCA4	66	I	CMOS	PD	CSCHMITT	" " "
TCA5	63	I	CMOS	PD	CSCHMITT	" " "

Local Bus Interface

signal	pin	I/O	type	pu/pd	buffer	comments
LADR<0>	5	O	3STA		TRIOUT	Address bus
LADR<1>	4	O	3STA		TRIOUT	" "
LADR<2>	3	O	3STA		TRIOUT	" "
LADR<3>	2	O	3STA		TRIOUT	" "
LADR<4>	1	O	3STA		TRIOUT	" "
LADR<5>	132	O	3STA		TRIOUT	" "
LADR<6>	130	O	3STA		TRIOUT	" "
LADR<7>	129	O	3STA		TRIOUT	" "
LADR<8>	128	O	3STA		TRIOUT	" "
LADR<9>	127	O	3STA		TRIOUT	" "
LADR<10>	126	O	3STA		TRIOUT	" "
LDAT<0>	16	I/O	TTL+3STA	PD	TTLIP+TRIOUT	Data bus
LDAT<1>	15	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<2>	14	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<3>	13	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<4>	11	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<5>	10	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<6>	9	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
LDAT<7>	8	I/O	TTL+3STA	PD	TTLIP+TRIOUT	" "
RWN	119	O	3STA		TRIOUT	Read/Write
BRQN	116	I	CMOS	PU	CMOSIP	Bus Request
BGRN	125	O	TTL/CMOS		BOP	Bus Grant
RAMCSN	120	O	3STA		TRIOUT	Chip Select RAM
ROMCSN	121	O	3STA		TRIOUT	Chip Select ROM
LACCS	122	O	3STA		TRIOUT	Recovery LAC access
LACK	115	I	CMOS	PU	CSCHMITT	Acknowledge

Map Interface

signal	pin	I/O	type	pu/pd	buffer	comments
MAPSTN	22	O	TTL/CMOS		BOP	MAP strobe
MAPCK	25	O	TTL/CMOS		BOP	MAP clockout
MAPDSR	26	O	TTL/CMOS		BOP	MAP data set ready
MAPDTR	36	I	CMOS	PU	CSCHMITT	MAP data term. ready
MAPDATA	28	O	TTL/CMOS		BOP	MAP serial data
MAPADT	23	O	TTL/CMOS		BOP	MAP abort data

CPDU Interface

signal	pin	I/O	type	pu/pd	buffer	comments
CPDUSTN	29	O	TTL/CMOS		BOP	Strobe signal
CPDUEN	30	O	TTL/CMOS		BOP	Pulse output
CPDUDIV	54	I	CMOS	PD	CMOSIP	Clock dividing

Telemetry Interface

signal	pin	I/O	type	pu/pd	buffer	comments
CLCWSA	47	I	CMOS	PU	CSCHMITT	CLCW status sample
CLCWCA	46	I	CMOS	PU	CSCHMITT	CLCW status clkout
CLCWDA	32	O	TTL/CMOS		BOP	CLCW status data
CLCWSB	45	I	CMOS	PU	CSCHMITT	Redundant CLCW
CLCWCB	44	I	CMOS	PU	CSCHMITT	Redundant CLCW
CLCWDB	31	O	TTL/CMOS		BOP	Redundant CLCW
CPDUS	43	I	CMOS	PU	CSCHMITT	CPDU status sample
FAR1S	42	I	CMOS	PU	CSCHMITT	FAR status first sample
FAR2S	40	I	CMOS	PU	CSCHMITT	FAR status last sample
AU1S	39	I	CMOS	PU	CSCHMITT	AU status first sample
AU2S	38	I	CMOS	PU	CSCHMITT	AU status second sample
TMC	37	I	CMOS	PU	CSCHMITT	CPDU/FAR/AU status clk
TMD	33	O	TTL/CMOS		BOP	CPDU/FAR/AU status data

Parallel Interface

signal	pin	I/O	type	pu/pd	buffer	comments
PRDY	86	O	TTL/CMOS		BOP	Parallel interface control line
PBUS<0>	106	O	3STA		TRIOUT	Parallel interface databus
PBUS<1>	105	O	3STA		TRIOUT	Parallel interface databus
PBUS<2>	104	O	3STA		TRIOUT	Parallel interface databus
PBUS<3>	103	O	3STA		TRIOUT	Parallel interface databus
PBUS<4>	101	O	3STA		TRIOUT	Parallel interface databus
PBUS<5>	100	O	3STA		TRIOUT	Parallel interface databus
PBUS<6>	99	O	3STA		TRIOUT	Parallel interface databus
PBUS<7>	98	O	3STA		TRIOUT	Parallel interface databus
PBUS<8>	96	O	3STA		TRIOUT	Parallel interface databus
PBUS<9>	95	O	3STA		TRIOUT	Parallel interface databus
PBUS<10>	94	O	3STA		TRIOUT	Parallel interface databus
PBUS<11>	93	O	3STA		TRIOUT	Parallel interface databus
PBUS<12>	91	O	3STA		TRIOUT	Parallel interface databus
PBUS<13>	90	O	3STA		TRIOUT	Parallel interface databus
PBUS<14>	89	O	3STA		TRIOUT	Parallel interface databus
PBUS<15>	88	O	3STA		TRIOUT	Parallel interface databus

Authentication Interface

signal	pin	I/O	type	pu/pd	buffer	comments
AUDIS	109	I	CMOS	PU	CMOSIP	Internal AU bypass signal
AUEXT	113	I	CMOS	PD	CMOSIP	External AU selection
AUST	84	O	TTL/CMOS		BOP	AU Start signal
AUBUF	85	O	TTL/CMOS		BOP	AU buffer signal
AUEND	112	I	CMOS	PD	CMOSIP	AU end validation signal
AUR	111	I	CMOS	PD	CMOSIP	AU result signal
AUTSL	110	I	CMOS	PU	CMOSIP	AU tail length select
AUSBUF	50	O	TTL/CMOS		BOP	AU Status Buffer
FARBUF	49	O	TTL/CMOS		BOP	FAR buffer

Miscellaneous

signal	pin	I/O	type	pu/pd	buffer	comments
RFAVN	61	I	CMOS	PU	CSCHMITT	Physical interface status
VCLSB	60	I	CMOS	PD	CMOSIP	VCld differentiation
TMMOD	58	I	CMOS	PD	CMOSIP	TM mode select
PAR	51	I	CMOS	PD	CMOSIP	Parallel/serial selection
RESETN	52	I	CMOS	PU	CSCHMITT	Reset
CLK	53	I	CMOS	PU	CSCHMITT	Clock
PRIOR	59	I	CMOS	PD	CMOSIP	Priority mode
TEST	114	I	CMOS	PD	CMOSIP	To be connected to VSS
MODE	57	I	CMOS	PD	CMOSIP	To be connected to VSS
CONF	56	I	CMOS	PD	CMOSIP	To be connected to VSS
SELTC<0>	21	O	TTL/CMOS		BOP	Selected Channel
SELTC<1>	20	O	TTL/CMOS		BOP	Selected Channel
SELTC<2>	19	O	TTL/CMOS		BOP	Selected Channel
DECOD	27	O	TTL/CMOS		BOP	Decode state

Power Supply

signal	pin	I/O	type	pu/pd	buffer	comments
VDD	6					VDD power supply
VDD	12					VDD power supply
VDD	18					VDD power supply
VDD	35					VDD power supply
VDD	48					VDD power supply
VDD	62					VDD power supply
VDD	76					VDD power supply
VDD	87					VDD power supply
VDD	97					VDD power supply
VDD	107					VDD power supply
VDD	117					VDD power supply
VDD	124					VDD power supply
VSS	7					VSS power supply
VSS	17					VSS power supply
VSS	24					VSS power supply
VSS	34					VSS power supply
VSS	41					VSS power supply
VSS	55					VSS power supply
VSS	69					VSS power supply
VSS	83					VSS power supply
VSS	92					VSS power supply
VSS	102					VSS power supply
VSS	108					VSS power supply
VSS	118					VSS power supply
VSS	123					VSS power supply
VSS	131					VSS power supply

10. RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

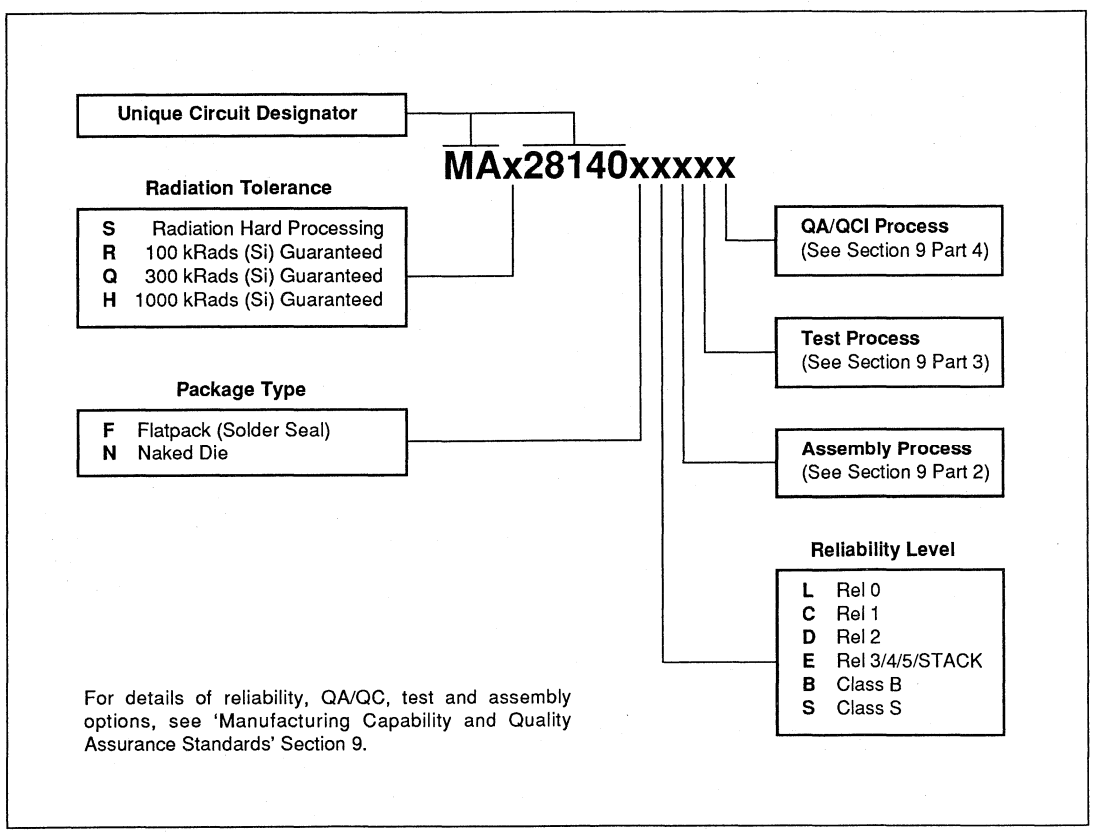
Total Dose (Function to specification)*	$1x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 27: Radiation Hardness Parameters

11. ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

12. SYNONYMS

AD	Accepted Data Frame (accepted by the FARM)
ASIC	Application Specific Integrated Circuit
AU(S)	Authentication Unit (Status)
BC	Bypass Control Frame
BD	Bypass Data Frame
CCSDS	Consultative Committee for Space Data Systems
CLCW	Command Link Control Word
CLTU	Command Link Transmission Unit
CPDU(S)	Command Pulse Distribution Unit (Status)
CRC	Cyclic Redundant Code
ESA	European Space Agency
FAR	Frame Analysis Report
FARM	Frame Acceptance and Reporting Mechanism
GPS	GEC Plessey Semiconductors
ID	Identifier
LAC	Logical Authentication Channel
LFSR	Linear Feedback Shift Register
LSB	Least Significant Bit
MAP	Multiplexed Access Point
MSB	Most Significant Bit
NOP	No Operation
NRZ(-L)	Non Return to Zero (Level)
N(S)	Frame Sequence Number of a transmitted TC Frame
NW	Negative Window
PLOP	Physical Layer Operation Procedure
PSK	Phase Shift Keying
PSS	Procedures, Specification and Standards
PTD	Packet Telecommand Decoder
PW	Positive Window
RAM	Random Access Memory
RF	Radio Frequency
ROM	Read Only Memory
EEPROM	Electrically Erasable Programmable ROM
SEU	Single Event Upset
SOS	Silicon On Sapphire
TC	Telecommand
TM	Telemetry
VC	Virtual Channel
VCM	Virtual Channel Multiplexer
V(R)	The next expected TC frame sequence number
W	FARM Sliding Window Width (variable of the FARM)

Section 6
Logic

GEC PLESSEY
SEMICONDUCTORS

15HSC Series

RADIATION HARD HIGH SPEED CMOS/SOS LOGIC

The 15HSC Series offer the conbined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and high level of radiation hardness of Silicon on Sapphire technology.

The 15HSC Series of CMOS/SOS devices are pin compatible with the 54LS Series and the 54HSC Series, but with a higher speed capability.

Further device types to those listed will be available shortly. Please contact GPS for further information.

FEATURES

- Radiation Hard to 1.5µm CMOS/SOS Technology
- High SEU Immunity
- Latch Up Free
- Low Power CMOS/SOS Technology
- Plug In Replacement for 54/74LS, HC and HCT
- Dual In Line or Flatpack Packages
- High Speed (Toggle Rate 100MHz)

DEVICE TYPES

15HSC138	3-Line to 8-Line Decoder/Multiplexer
15HSC163	Synchronous 4-Bit Counter

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	10	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-25	+25	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 1: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	HST Input High Voltage	-	2.0	-	-	V
V_{IL1}	HST Input Low Voltage	-	-	-	0.8	V
V_{IH2}	HSC Input High Voltage	-	3.5	-	-	V
V_{IL2}	HSC Input Low Voltage	-	-	-	1.5	V
V_{OH}	Output High Voltage	$V_{IN} = V_{IH}$ or V_{IL}				
		I_{OH} = -20µA*	V_{DD}-0.1	-	-	V
		I_{OH} = -6.0mA*	3.7	-	-	V
		I_{OH} = -11.0mA	2.5	-	-	V
V_{OL}	Output Low Voltage	$V_{IN} = V_{IH}$ or V_{IL}				
		I_{OL} = 20µA*	-	-	0.1	V
		I_{OL} = 6.0mA*	-	-	0.2	V
		I_{OL} = 9.0mA	-	-	0.4	V
I_{IL}	Input Leakage Current	$V_{IN} = V_{DD}$ or V_{SS} All inputs	-	-	±10	µA
I_{OL}	Output Leakage Current	$V_{OUT} = V_{DD}$ or V_{SS} Outputs disabled	-	-	50	µA
I_{DD}	Quiescent Current	$V_{IN} = V_{DD}$ Outputs unloaded	-	-	1	mA

V_{DD} = 5V±10%, over full operating temperature range.
* = Guaranteed but not tested.

Figure 2: Electrical Characteristics

15HSC138 : 3-Line to 8-Line Decoder/Multiplexer

Enable Inputs			Select Inputs			Outputs							
G_1	GN_{2A}	GN_{2B}	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 3: Function Table

Symbol	Parameter	Spice Simulation	Max.	Units
t_{PLH}	Propagation delay. Address to Output	7.6	15	ns
t_{PHL}	Propagation delay. Address to Output.	7.4	15	ns
t_{PLH}	Propagation delay. G to Output	9.3	15	ns
t_{PHL}	Propagation delay. G to Output	8.8	15	ns

Figure 4: Switching Characteristics

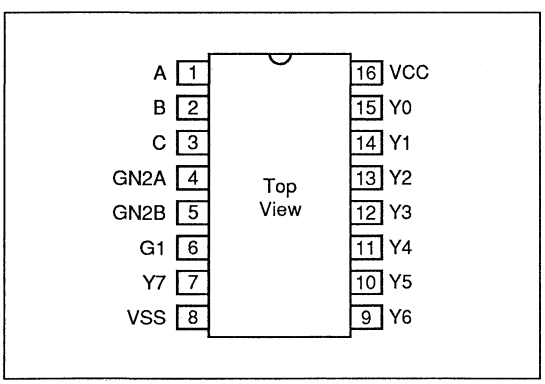


Figure 5: DIL Pin Out

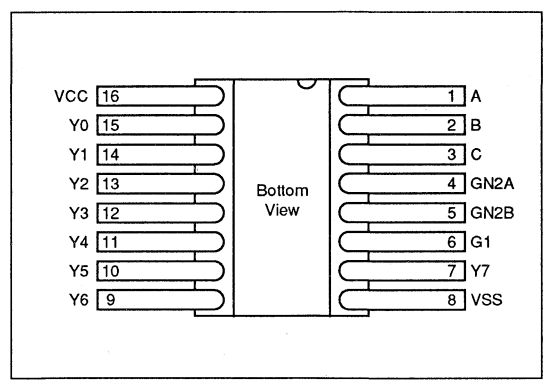


Figure 6: Flatpack Pin Out

15HSC163 : 4-Bit Counter with Synchronous Clear

Symbol	Parameter	Spice Simulation	Max.	Units
t_{PLH}	Propagation delay. Clock to RCO	11.5	15	ns
t_{PHL}	Propagation delay. Clock to RCO	11.4	15	ns
t_{PLH}	Propagation delay. Clock to any Q	9.4	15	ns
t_{PHL}	Propagation delay. Clock to any Q	9.6	15	ns
t_{PLH}	Propagation delay. ENT to RCO	8.5	15	ns
t_{PHL}	Propagation delay. ENT to RCO	8.4	15	ns

Figure 7: Switching Characteristics

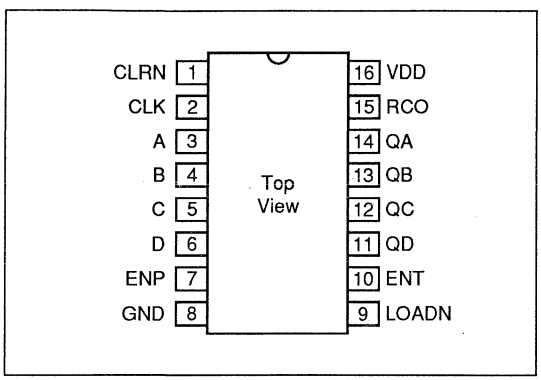


Figure 8: DIL Pin Out

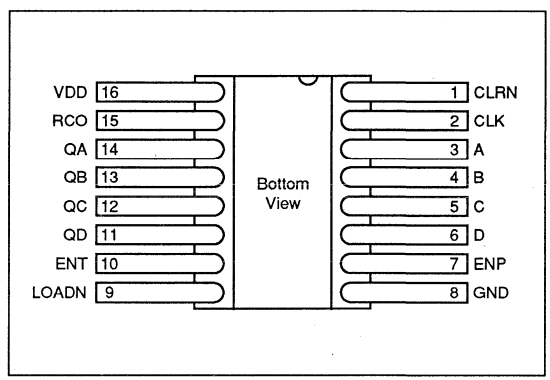


Figure 9: Flatpack Pin Out

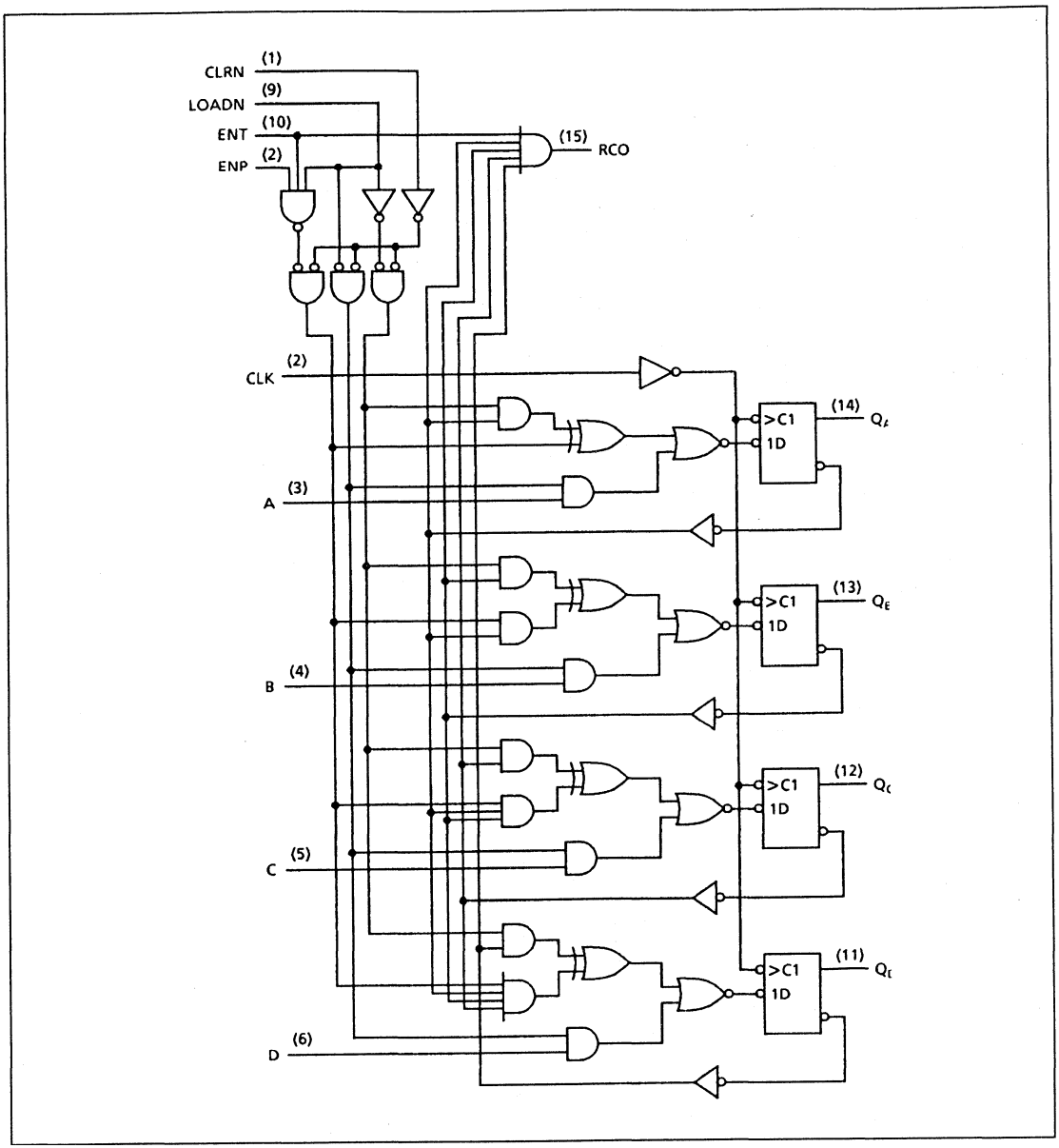


Figure 10: Logic Diagram

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.60	-	-	0.220
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	20.58	-	-	0.810
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	7.62 Typ.	-	-	0.300 Typ.	-
H	4.45	-	5.38	0.175	-	0.212
Me	-	-	8.30	-	-	0.326
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG402

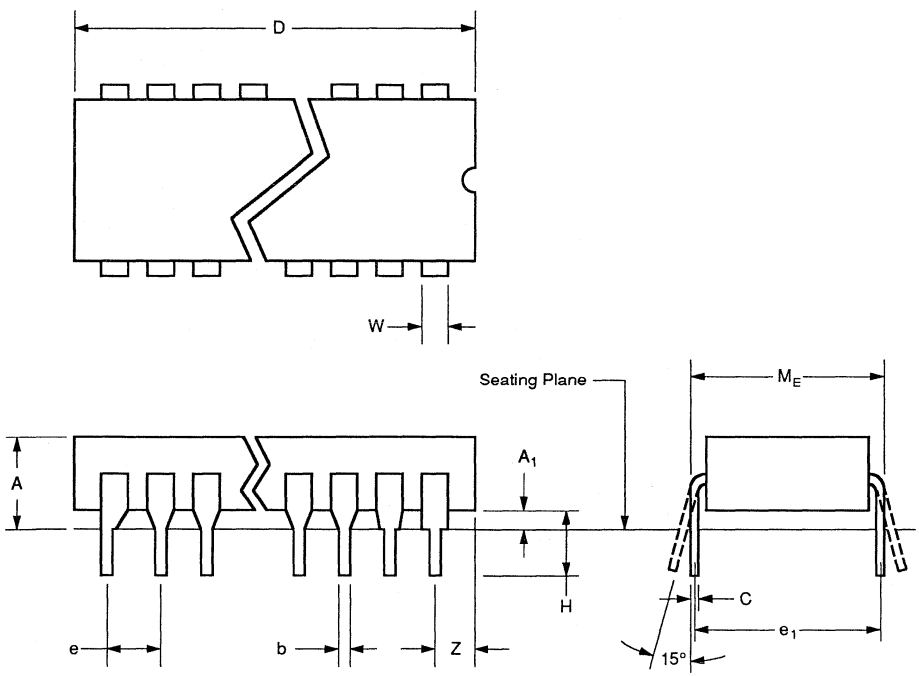


Figure 11: 16-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Inches		
	Min.	Nom.	Max.
A	-	-	0.103
A1	0.026	-	-
b	0.015	-	0.019
c	0.004	-	0.006
D	0.392	-	0.408
e	-	0.050	-
L	0.250	-	0.305
M	0.264	-	0.276
E2	0.184	-	0.196
Z	0.005	-	-

XG534

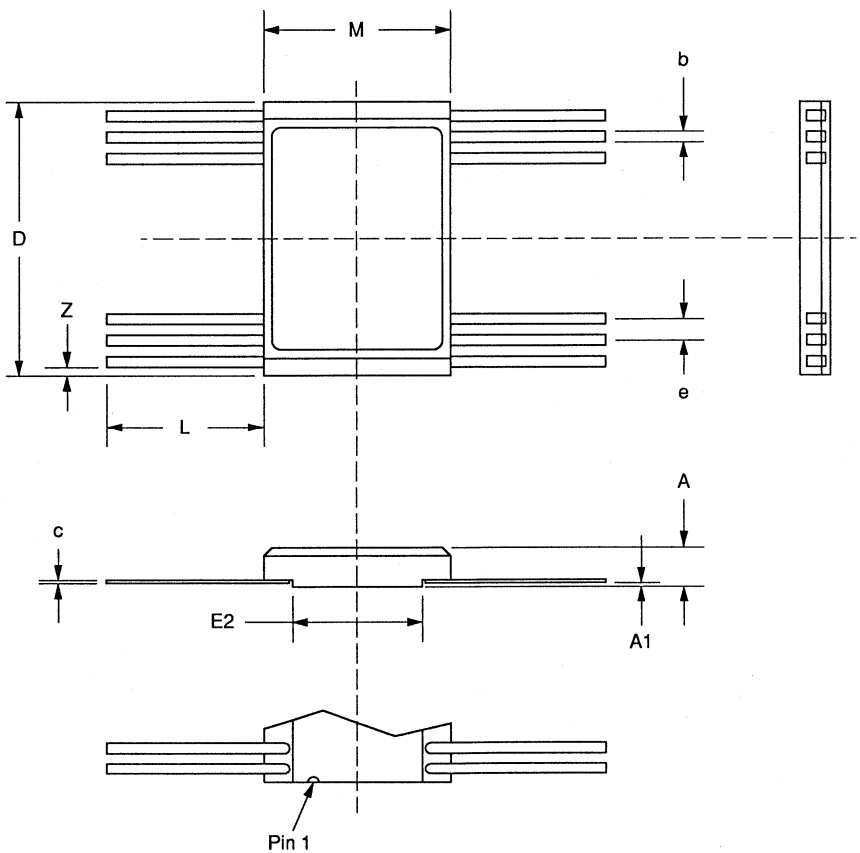


Figure 12: 16-Lead Bottom Braize Flatpack (Solder Seal) - Package Style F

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

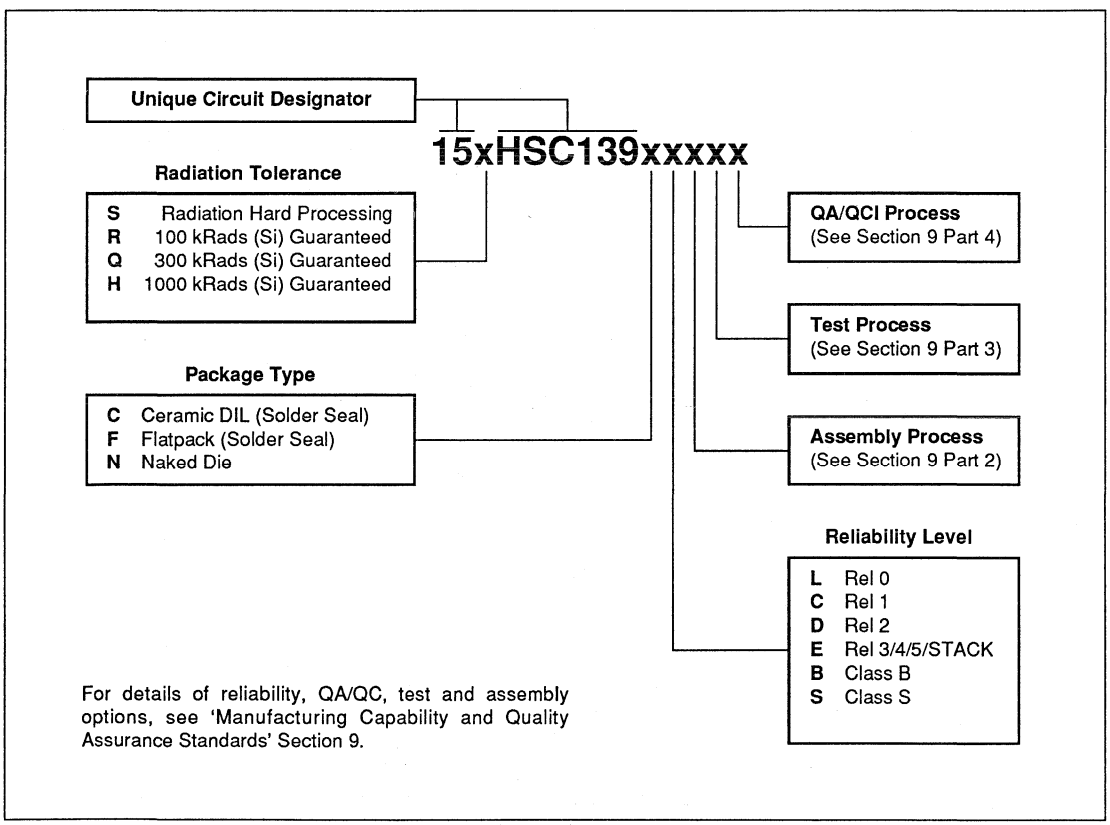
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 13: Radiation Hardness Parameters

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3594-3.3

54HSC/T Series

RADIATION HARD HIGH SPEED CMOS/SOS LOGIC

The CMOS/SOS HSC/T Series offer the combined benefits of low power, high speed CMOS with the inherent latch up immunity, Single Event Upset (SEU) immunity and the high level of radiation hardness of Silicon on Sapphire technology. The 54HSC/T Series of circuits are pin for pin compatible with the 54LS series range.

HSC and HST devices have CMOS and TTL compatible inputs/outputs respectively.

FEATURES

- Radiation Hard to 1MRad (Si)
- High SEU Immunity, Latch Up Free
- Low Power CMOS/SOS Technology
- Plug In Replacement for 54/74LS, HC and HCT
- Dual In Line or Flatpack Packages

Gates and Buffers

54HSC/T00	Quadruple 2-input positive NAND gates
54HSC/T02	Quadruple 2-input positive NOR gates
54HSC/TO3	Quadruple 2-input positive NAND gates with open collector outputs
54HSC/T04	Hex Inverters
54HSC/T08	Quadruple 2-input positive AND gates
54HSC/T10	Triple 3-input positive NAND gates
54HSC14	Hex schmitt-trigger inverters
54HSC/T21	Dual 4-input positive AND gates
54HSC/T27	Triple 3-input positive NOR gates
54HSC/T32	Quadruple 2-input positive OR gates
54HSC/T86	Quadruple 2-input Exclusive OR gates
54HSC/T125	Quadruple bus buffer gates with tri-state outputs (Active low enable)
54HSC/T126	Quadruple bus buffer gates wlth tri-state outputs (Active high enable)

Flip-Flops

54HSC/T74	Dual D-type flip-flops wlth preset and clear
54HSC/T109	Dual J-KB flip-flop with preset and clear
54HSC/T273	Octal D-type flip-flops
54HSC/T374	Octal D-type edge triggered flip-flops
54HSC/T574	Octal D-type edge triggered flip-flops

Adders

54HSC/T283	4-bit binary full adders with fast carry

Counters

54HSC/T161	4-bit synchronous binary counter
54HSC/T163	Synchronous 4-bit counter
54HSC/T191	Synchronous 4-bit counter

Decoders/Demultiplexers

54HSC/T138	3-line to 8-line decoder/multiplexer
54HSC/T139	Dual 2 to 4 decoders/multiplexers
54HSC/T148	8-line to 3-line octal priority encoders
54HSC/T151	1 of 8 data selectors/multiplexers
54HSC/T154	4 to 16-line decoders/demultiplexers
54HSC/T157	Quad 2-line to 1-line data selectors/multiplexers
54HSC/T238	3 to 8 decoder/demultiplexer
54HSC/T253	Dual 4 to 1 data selectors/multiplexers

Registers

54HSC/T164	8-bit parallel output serial shift register
54HSC/T165	Parallel load 8-bit shift register
54H5C/T166	8-bit shift register

Comparators

54HSC/T521	8-bit magnitude comparator

Line Drivers

54HSC/T240	Octal 3-state driver inverting
54HSC/T241	Octal 3-state driver complementary enable
54HSC/T244	Octal 3-state driver
54HSC/T540	Octal 3-state driver/buffer inverting
54HSC/T541	Octal 3-state driver/buffer

Transceivers

54HSC/T245	Octal bus transceiver

Latches

54HSC/T373	Octal transparent latch, 3-state outputs
54HSC/T573	Octal transparent latch, 3-state outputs

Miscellaneous

54HSC/T670	4 x 4 register files with tri-state outputs

DC CHARACTERISTICS AND RATINGS

Parameter	Min.	Max.	Units
Supply Voltage	-0.5	10	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-25	+25	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Figure 1: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min.	Typ.	Max.	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	HST Input High Voltage	-	2.0	-	-	V
V_{IL1}	HST Input Low Voltage	-	-	-	0.8	V
V_{IH2}	HSC Input High Voltage	-	3.5	-	-	V
V_{IL2}	HSC Input Low Voltage	-	-	-	1.5	V
V_{OH}	Output High Voltage	V_{IN} = V_{IH} or V_{IL}				
		I_{OH} = -20µA*	V_{DD}-0.1	-	-	V
		I_{OH} = 6mA*	3.7	-	-	V
		I_{OH} = -11mA	2.5	-	-	V
V_{OL}	Output Low Voltage	V_{IN} = V_{IH} or V_{IL}				
		I_{OL} = -20µA*	-	-	0.1	V
		I_{OL} = 6mA*	-	-	0.2	V
		I_{OL} = 9mA	-	-	0.4	V
I_{IL}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS} All inputs	-	1	5	µA
I_{OL}	Output Leakage Current	V_{OUT} = V_{DD} or V_{SS} Outputs disabled	-	20	50	µA
I_{DD}	Quiescent Current	V_{IN} = V_{DD} Outputs unloaded	-	†	†	µA

V_{DD} = 5V±10%, over full operating temperature range.
* Guaranteed but not tested.
† Refer to individual device types (-55°C / +125°C).

Figure 2: Electrical Characteristics

54HSC/T00 : Quadruple 2-Input Positive NAND Gates

The 54HSC/T00 is a Quadruple 2-Input Positive NAND gate.

Inputs		Outputs
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

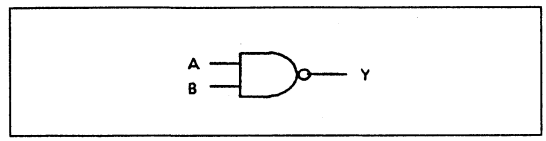


Figure 2: Logic Diagram

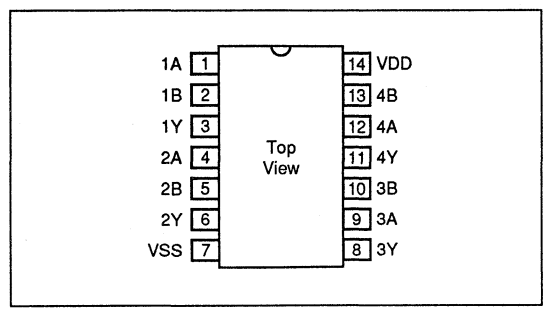


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T02 : Quadruple 2-Input Positive NOR Gates

The 54HSC/T02 is a Quadruple 2-Input Positive NOR gate.

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = high level, L = low level

Figure 1: Function Table

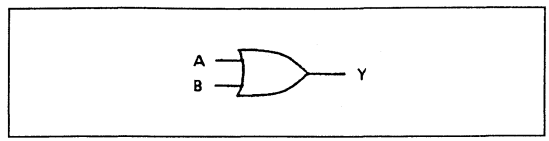


Figure 2: Logic Diagram

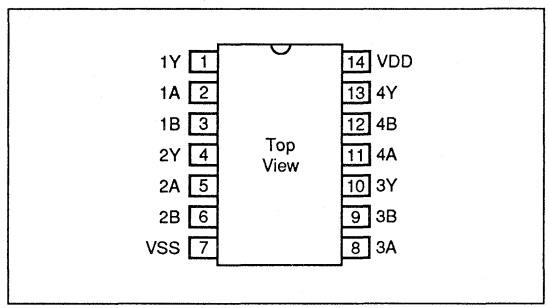


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T03 : Quadruple 2-Input Positive NAND Gates With Open Collector Outputs

The 54HSC/T03 is a Quadruple 2-Input Positive NAND gate with open collector output.

Inputs		Outputs
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

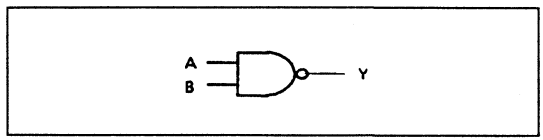


Figure 2: Logic Diagram

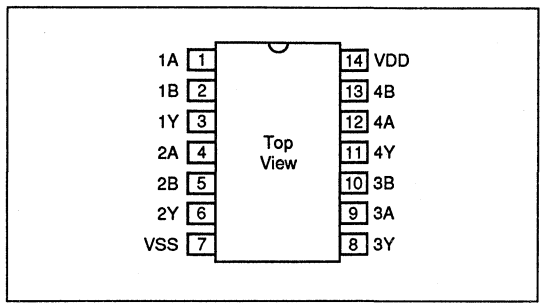


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±0.5	µA

Figure 5: DC Characteristics

54HSC/T04 : Hex Inverters

The 54HSC/T04 consists of six Hex Inverters.

Inputs	Outputs
A	Y
H	L
L	H

H = high level, L = low level

Figure 1: Function Table

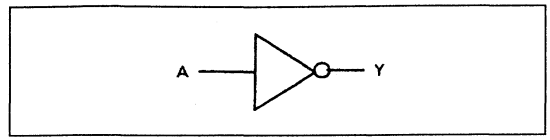


Figure 2: Logic Diagram

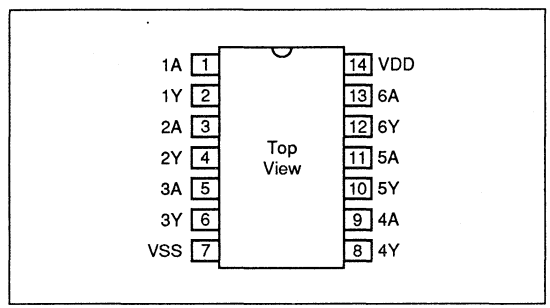


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T08 : Quadruple 2-Input Positive AND Gates

The 54HSC/T08 is a Quadruple 2-Input Positive AND gate.

Inputs		Outputs
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = high level, L = low level

Figure 1: Function Table

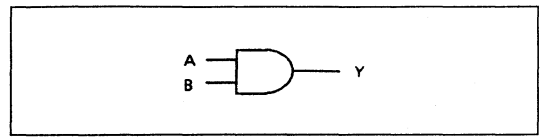


Figure 2: Logic Diagram

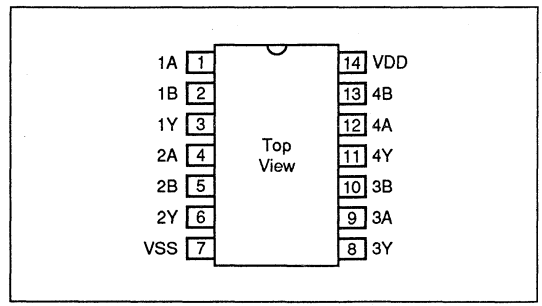


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T10 : Triple 3-Input Positive NAND Gates

The 54HSC/T10 is a Triple 3-Input Positive NAND gate.

Inputs			Outputs
A	B	C	Y
L	X	X	H
X	L	X	H
X	X	L	H
H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

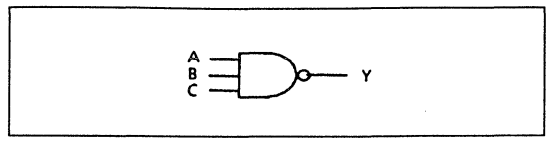


Figure 2: Logic Diagram

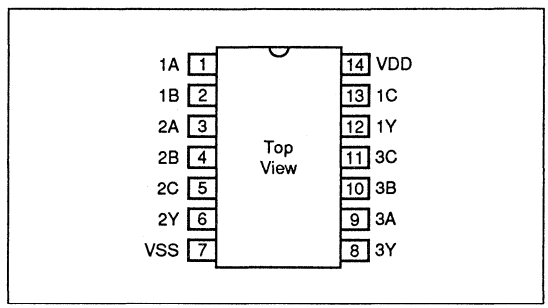


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC14 : Hex Schmitt-Trigger Inverters

The 54HSC/T14 consists of six Hex Schmitt-Trigger Inverters.

Inputs	Outputs
A	Y
L	H
H	L

H = high level, L = low level

Figure 1: Function Table

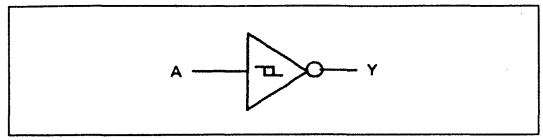


Figure 2: Logic Diagram

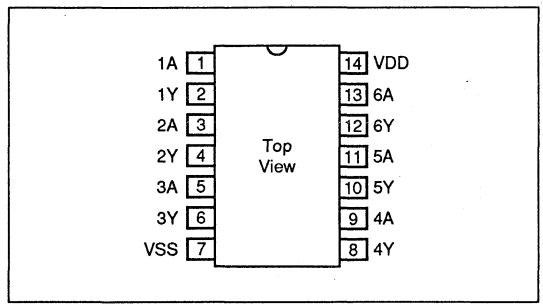


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T21 : Dual 4-Input Positive AND Gates

The 54HSC/T21 is a Dual 4-Input Positive AND gate.

Inputs				Outputs
A	B	C	D	Y
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H

H = high level, L = low level

Figure 1: Function Table

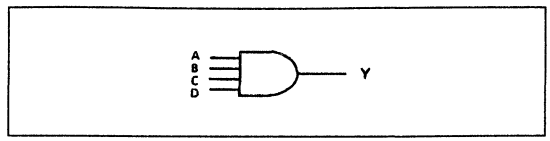


Figure 2: Logic Diagram

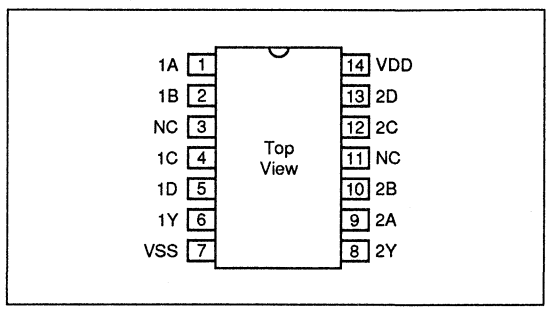


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T27 : Triple 3-Input Positive NOR Gates

The 54HSC/T27 is a Triple 3-Input Positive NOR gate.

Inputs			Outputs
A	B	C	Y
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

H = high level, L = low level

Figure 1: Function Table

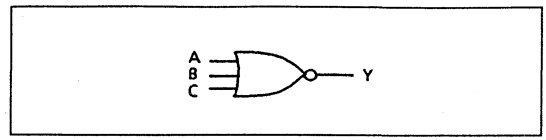


Figure 2: Logic Diagram

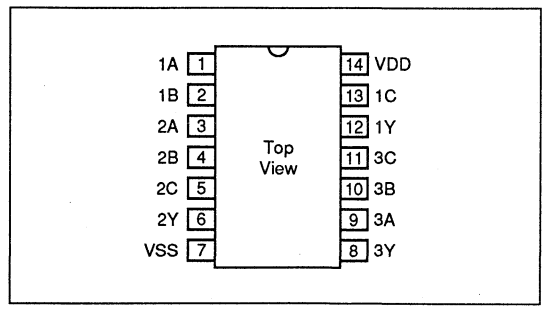


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T32 : Quadruple 2-Input Positive OR Gates

The 54HSC/T32 is a Quadruple 2-Input Positive OR gate.

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = high level, L = low level

Figure 1: Function Table

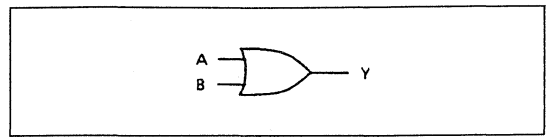


Figure 2: Logic Diagram

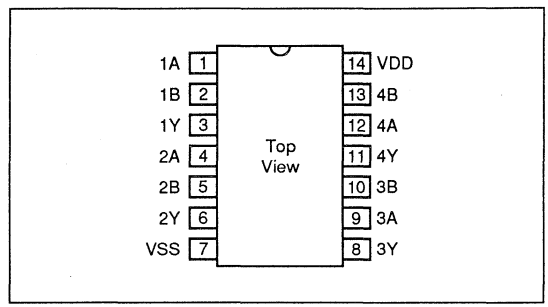


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T86 : Quadruple 2-Input Exclusive OR Gates

The 54HSC/T86 is a Quadruple 2-Input Exclusive OR gate.

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

Figure 1: Function Table

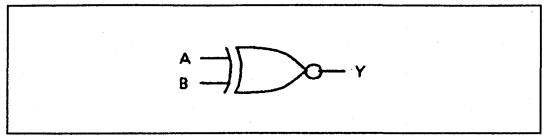


Figure 2: Logic Diagram

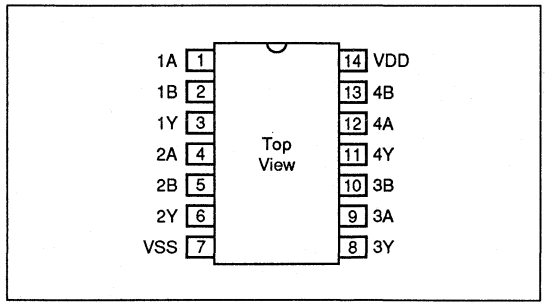


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay time, low to high level output	11	20	17	22	ns
t_{PHL}	Propagation delay time, high to low level output	10	18	18	20	ns

Figure 4: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	300	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T125 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active Low Enable)

The 54HSC/T125 is a Quadruple Bus Buffer Gate. When G is low the A input is transferred to the Y output. When G is high the output is in a high impedance state.

Inputs		Outputs
$\overline{G}$	A	Y
L	L	L
L	H	H
H	L	Z
H	H	Z

H = high level, L = low level, Z = high impedance

Figure 1: Function Table

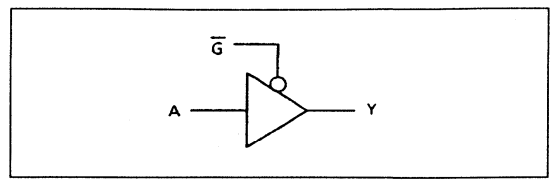


Figure 2: Logic Diagram

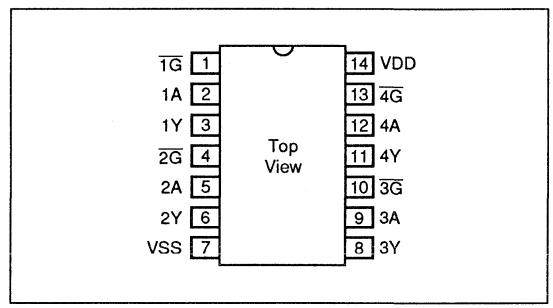


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A to Y	15	18	18	28	ns
t_{PHL}	Propagation delay A to Y	15	20	18	28	ns
t_{PZH}	Propagation delay G to Y	12	25	15	28	ns
t_{PZL}	Propagation delay G to Y	12	25	15	28	ns
t_{PHZ}	Propagation delay Y to Tri-State	12	25	15	28	ns
t_{PLZ}	Propagation delay Y to Tri-State	12	25	15	28	ns

Figure 4: Switching Characteristics

54HSC/T125 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active Low Enable)

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T126 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active High Enable)

The 54HSC/T126 is a Quadruple Bus Buffer Gate. When G is high the A input is transferred tp the Y output. When G is low the output is in a high impedance state.

Inputs		Outputs
G	A	Y
H	L	L
H	H	H
L	L	Z
L	H	Z

H = high level, L = low level, Z = high impedance

Figure 1: Function Table

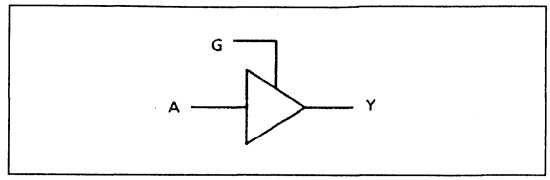


Figure 2: Logic Diagram

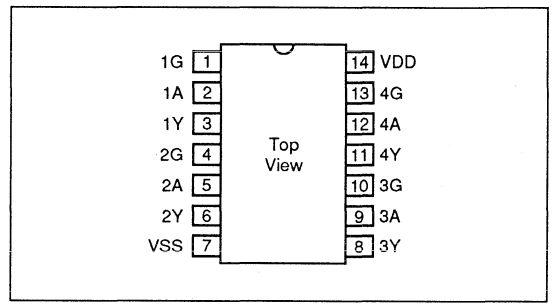


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A to Y	14	25	17	28	ns
t_{PHL}	Propagation delay A to Y	15	25	19	28	ns
t_{PZH}	Propagation delay G to Y	15	25	18	28	ns
t_{PZL}	Propagation delay G to Y	17	25	19	28	ns
t_{PHZ}	Propagation delay Y to Tri-State	17	25	20	28	ns
t_{PLZ}	Propagation delay Y to Tri-State	15	25	19	28	ns

Figure 4: Switching Characteristics

54HSC/T126 : Quadruple Bus Buffer Gates with Tri-State Outputs (Active High Enable)

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T74 : Dual D-Type Flip-Flops with Preset and Clear

The 54HSC/T74 is a Dual D-Type Flip-Flop. The D inputs are transferred to the Q outputs on the positive going edge of the clock pulse. The clear is active low.

Inputs				Output	
$\overline{\text{PRESET}}$	$\overline{\text{CLEAR}}$	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	L-H	H	H	L
H	H	L-H	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant, * = unknown return state

Figure 1: Function Table

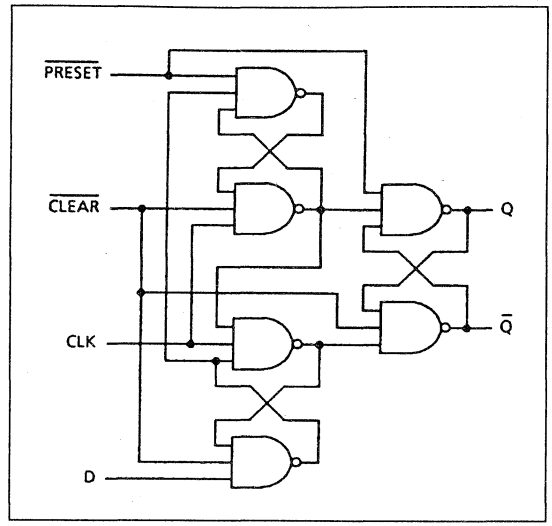


Figure 2: Logic Diagram

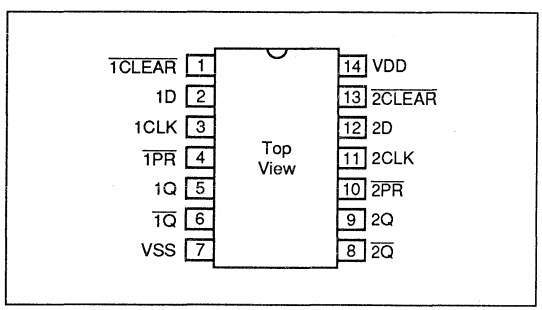


Figure 3: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Preset to Q or $\overline{Q}$.	15	20	18	24	ns
t_{PHL}	Propagation delay. Preset to Q or $\overline{Q}$.	16	20	10	24	ns
t_{PLH}	Propagation delay. Clear to Q or $\overline{Q}$.	18	20	15	24	ns
t_{PHL}	Propagation delay. Clear to Q or $\overline{Q}$.	15	20	15	24	ns
t_{PLH}	Propagation delay. Clock to Q or $\overline{Q}$.	17	25	15	25	ns
t_{PHL}	Propagation delay. Clock to Q or $\overline{Q}$.	18	25	15	25	ns

Figure 4: Switching Characteristics

54HSC/T74 : Dual D-Type Flip-Flops with Preset and Clear

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T109 : Dual J-KB Flip-Flops with Preset and Clear

The 54HSC/T109 is a Dual Positive-Edge-Triggered J-KB Flip-Flop with preset and clear.

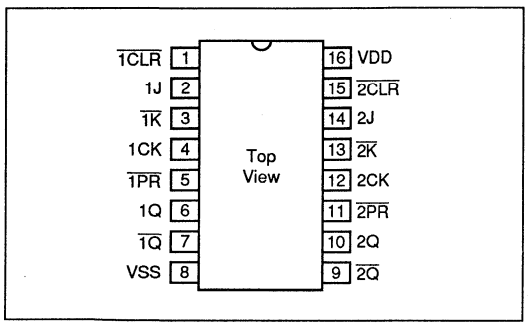


Figure 1: Pin Out

Inputs					Output	
PRESET	CLEAR	CLOCK	J	KB	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	Toggle
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = high level, L = low level, X = irrelevant, * = unknown return state

Figure 2: Function Table

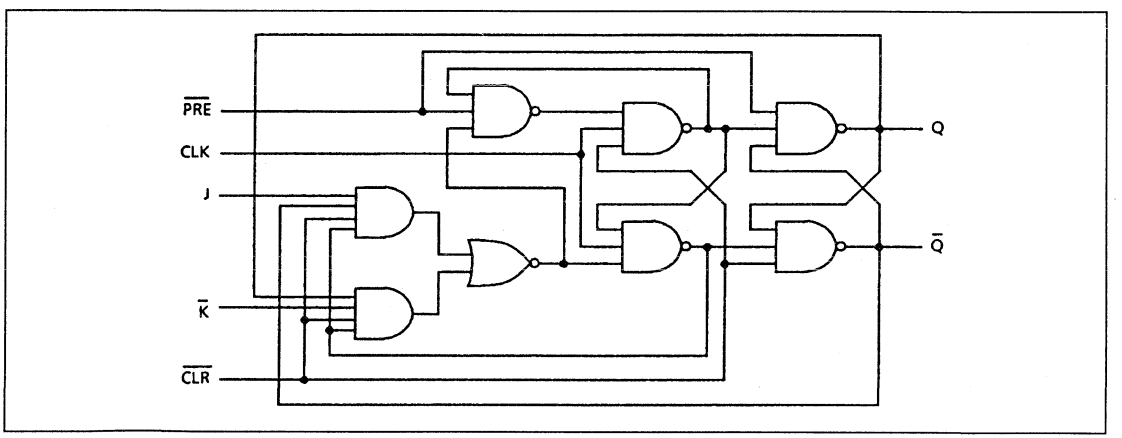


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Preset to Q or $\overline{Q}$.	15	19	17	19	ns
t_{PHL}	Propagation delay. Preset to Q or $\overline{Q}$.	16	25	19	25	ns
t_{PLH}	Propagation delay. Clear to Q or $\overline{Q}$.	17	25	20	25	ns
t_{PHL}	Propagation delay. Clear to Q or $\overline{Q}$.	15	25	18	25	ns
t_{PLH}	Propagation delay. Clock to Q or $\overline{Q}$.	18	25	21	25	ns
t_{PHL}	Propagation delay. Clock to Q or $\overline{Q}$.	15	25	18	25	ns

Figure 4: Switching Characteristics

54HSC/T109 : Dual J-KB Flip-Flops with Preset and Clear

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T273 : Octal D-Type Flip-Flops

The 54HSC/T273 is an Octal D-Type Flip-Flop with a direct active low clear. The D-Inputs are transferred to the Q-Outputs on the positive going edge of the clock pulse.

Inputs			Outputs
$\overline{CLEAR}$	CLOCK	D	Q
L	X	X	L
H	L-H	H	H
H	L-H	L	L
H	L	X	Q_0

Q_0 = level of Q before inputs were established
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

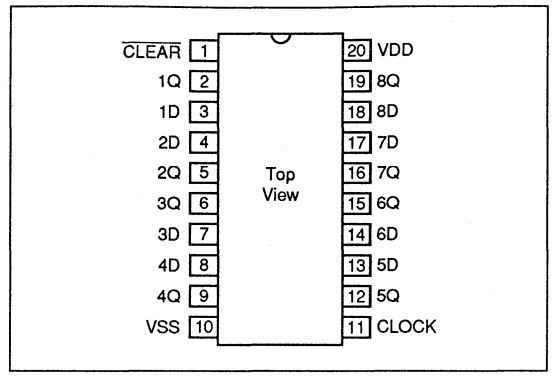


Figure 2: Pin Out

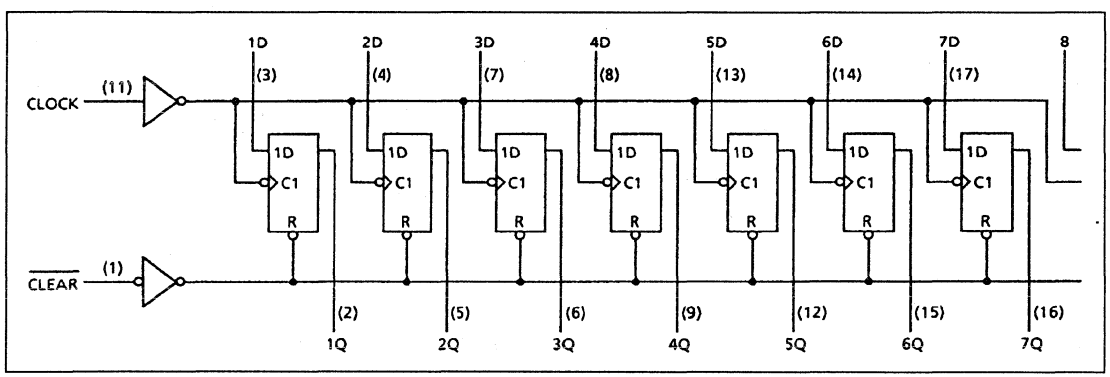


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Clear to Q or $\overline{Q}$.	14	25	17	28	ns
t_{PHL}	Propagation delay. Clear to Q or $\overline{Q}$.	16	25	19	28	ns
t_{PLH}	Propagation delay. Clock to Q or $\overline{Q}$.	15	25	18	28	ns
t_{PHL}	Propagation delay. Clock to Q or $\overline{Q}$.	17	25	20	28	ns

Figure 4: Switching Characteristics

54HSC/T273 : Octal D-Type Flip-Flops

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T374 : Octal D-Type Edge-Triggered Flip-Flops

The 54HSC/T374 consists of 8 Positive-Edge Triggered D-Type Flip-Flops with tri-state output.

Inputs			Outputs
$\overline{OC}$	CLOCK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

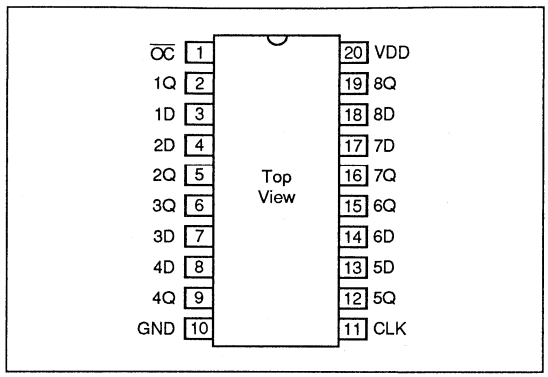


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	14	22	-	17	25	ns
t_{PHL}	Propagation delay. High to low output.	-	15	22	-	16	25	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	20	-	16	25	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	20	-	18	23	ns
t_{PLZ}	Propagation delay. Disable from low.	-	14	20	-	16	22	ns
t_{PHZ}	Propagation delay. Disable from high.	-	13	18	-	15	20	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T374 : Octal D-Type Edge-Triggered Flip-Flops

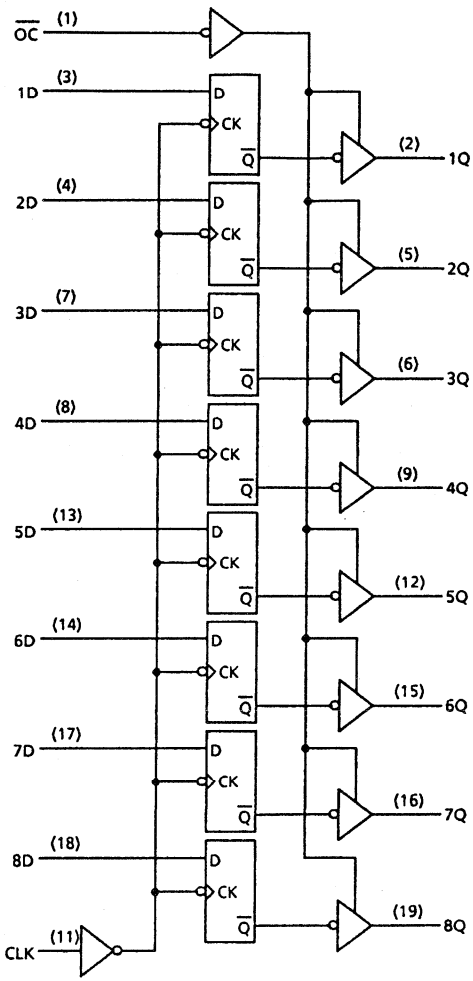


Figure 5: Logic Diagram

54HSC/T574 : Octal D-Type Edge-Triggered Flip-Flops

The 54HSC/T574 consists of 8 Positive-Edge Triggered D-Type Flip-Flops with tri-state output.

Inputs			Outputs
$\overline{OC}$	CLOCK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

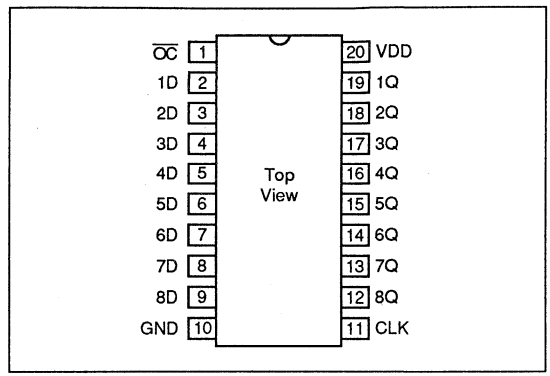


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	16	25	-	19	28	ns
t_{PHL}	Propagation delay. High to low output.	-	19	27	-	22	30	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay. Disable from low.	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay. Disable from high.	-	13	21	-	16	24	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T574 : Octal D-Type Edge-Triggered Flip-Flops

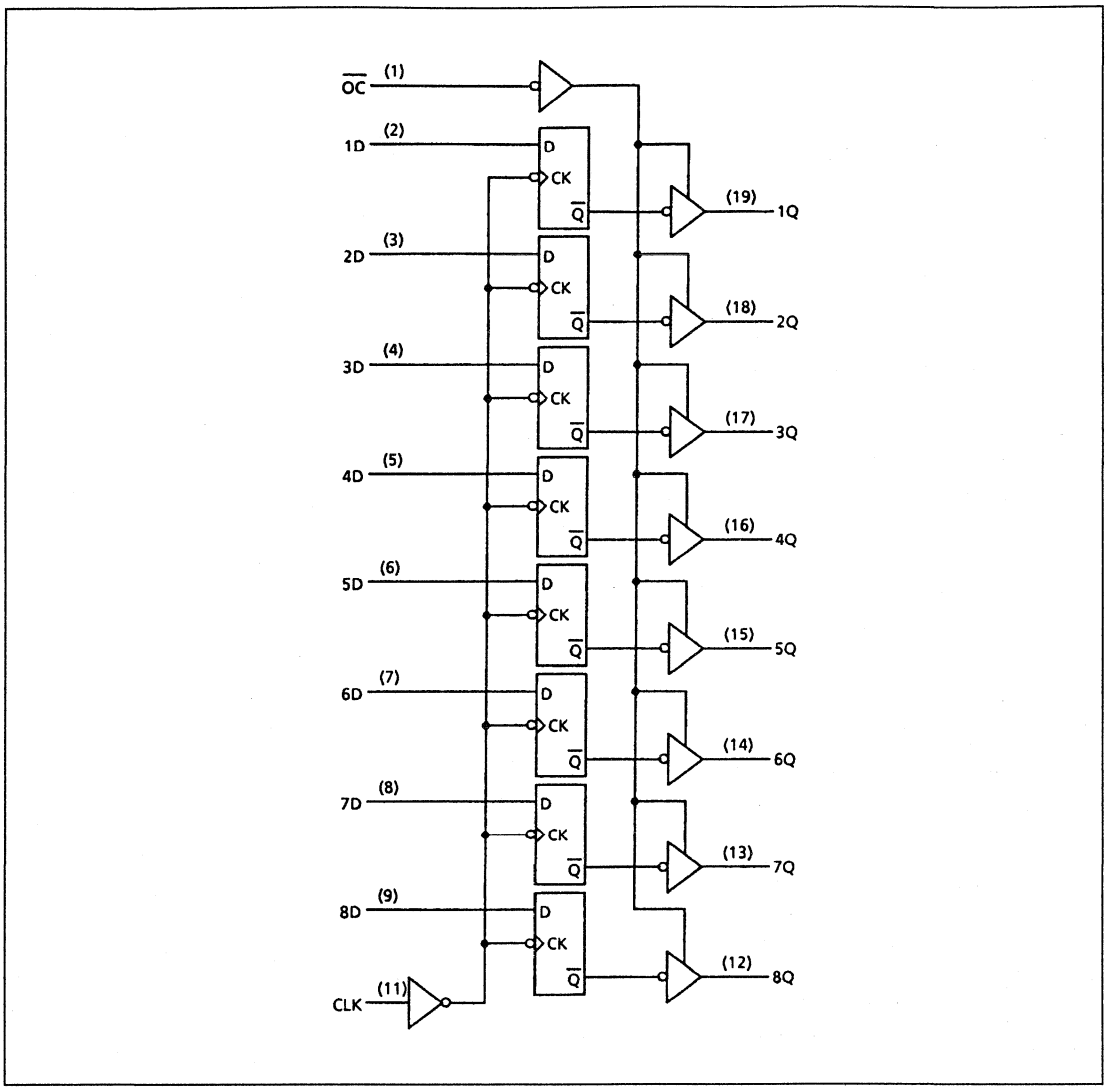


Figure 5: Logic Diagram

54HSC/T283 : 4-Bit Binary Full Adders with Fast Carry

The 54HSC/T283 are 4-Bit Binary Full Adders with fast carry.

Input				Output					
				When CO=L / When C2=L			When CO=H / When C2=H		
A1/A3	B1/B3	A2/A4	B2/B4	Σ1/Σ3	Σ2/Σ4	C2/C4	Σ1/Σ3	Σ2/Σ4	C2/C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

Figure 1: Function Table

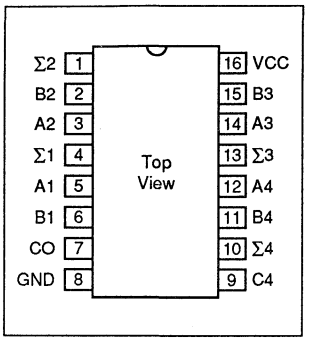


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. C0 to any Σ.	13	25	16	28	ns
t_{PHL}	Propagation delay. C0 to any Σ.	12	25	15	28	ns
t_{PLH}	Propagation delay. Ai or Bi to Σi.	14	25	17	28	ns
t_{PHL}	Propagation delay. Ai or Bi to Σi.	12	25	15	28	ns
t_{PLH}	Propagation delay. C0 to C4.	11	25	14	28	ns
t_{PHL}	Propagation delay. C0 to C4.	16	25	19	28	ns
t_{PLH}	Propagation delay. Ai or Bi to C4.	15	25	19	28	ns
t_{PHL}	Propagation delay. Ai or Bi to C4.	14	25	17	28	ns

Figure 3: Switching Characteristics

54HSC/T283 : 4-Bit Binary Full Adders with Fast Carry

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T283 : 4-Bit Binary Full Adders with Fast Carry

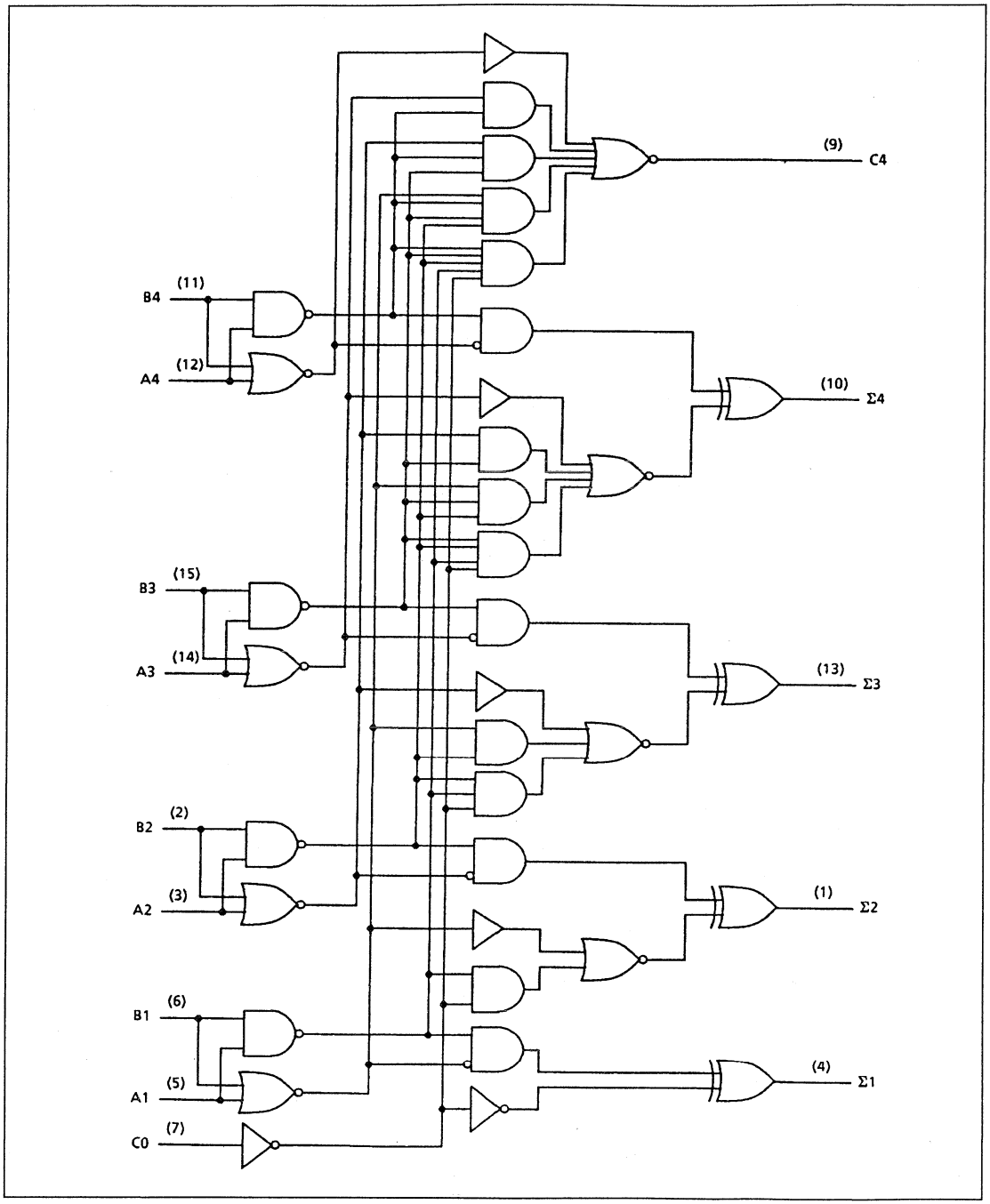


Figure 5: Logic Diagram

54HSC/T161 : 4-Bit Synchronous Binary Counter

The 54HSC/T161 is a Synchronous 4-Bit Binary Counter which features direct clear and an internal carry look-ahead.

Inputs						Output
$\overline{\text{Clear}}$	Enable P	Enable T	A→D	$\overline{\text{Load}}$	Clock	$Q_A \rightarrow Q_D$
L	X	X	X	X	X	0
H	L	X	X	H	X	Inhibit
H	X	L	X	H	X	Inhibit
H	X	X	Q_n	L	↑	Q_n
H	X	X	X	X	L	Q_0
H	X	X	X	X	H	Q_0
H	H	H	X	H	↑	Count

CARRY = H when $Q_A \rightarrow Q_D$ = H, Q_0 = previous level of Q
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

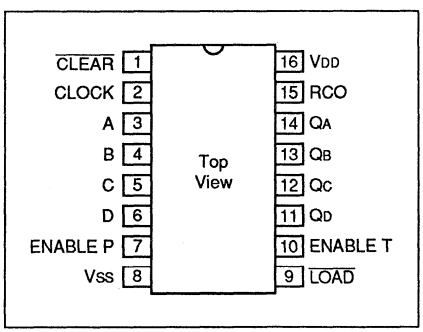


Figure 2: Pin Out

Symbol	From (Input)	To (Output)	+25°C		-55°C / +125°C		Units
			Typ.	Max.	Typ.	Max.	
t_{PLH}	CLOCK	RIPPLE CARRY	20	25	23	28	ns
t_{PHL}	CLOCK	RIPPLE CARRY	19	25	22	28	ns
t_{PLH}	CLOCK (Load Input HIGH)	Any Q Output	16	25	19	28	ns
t_{PHL}	CLOCK (Load Input HIGH)	Any Q Output	15	25	18	28	ns
t_{PLH}	CLOCK (Load Input LOW)	Any Q Output	15	25	18	28	ns
t_{PHL}	CLOCK (Load Input LOW)	Any Q Output	15	25	18	28	ns
t_{PLH}	ENABLE	RIPPLE CARRY	14	25	17	28	ns
t_{PHL}	ENABLE	RIPPLE CARRY	14	25	17	28	ns
t_{PHL}	CLEAR	Any Q Output	18	25	21	28	ns

Figure 3: Switching Characteristics

54HSC/T161 : 4-Bit Synchronous Binary Counter

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T161 : 4-Bit Synchronous Binary Counter

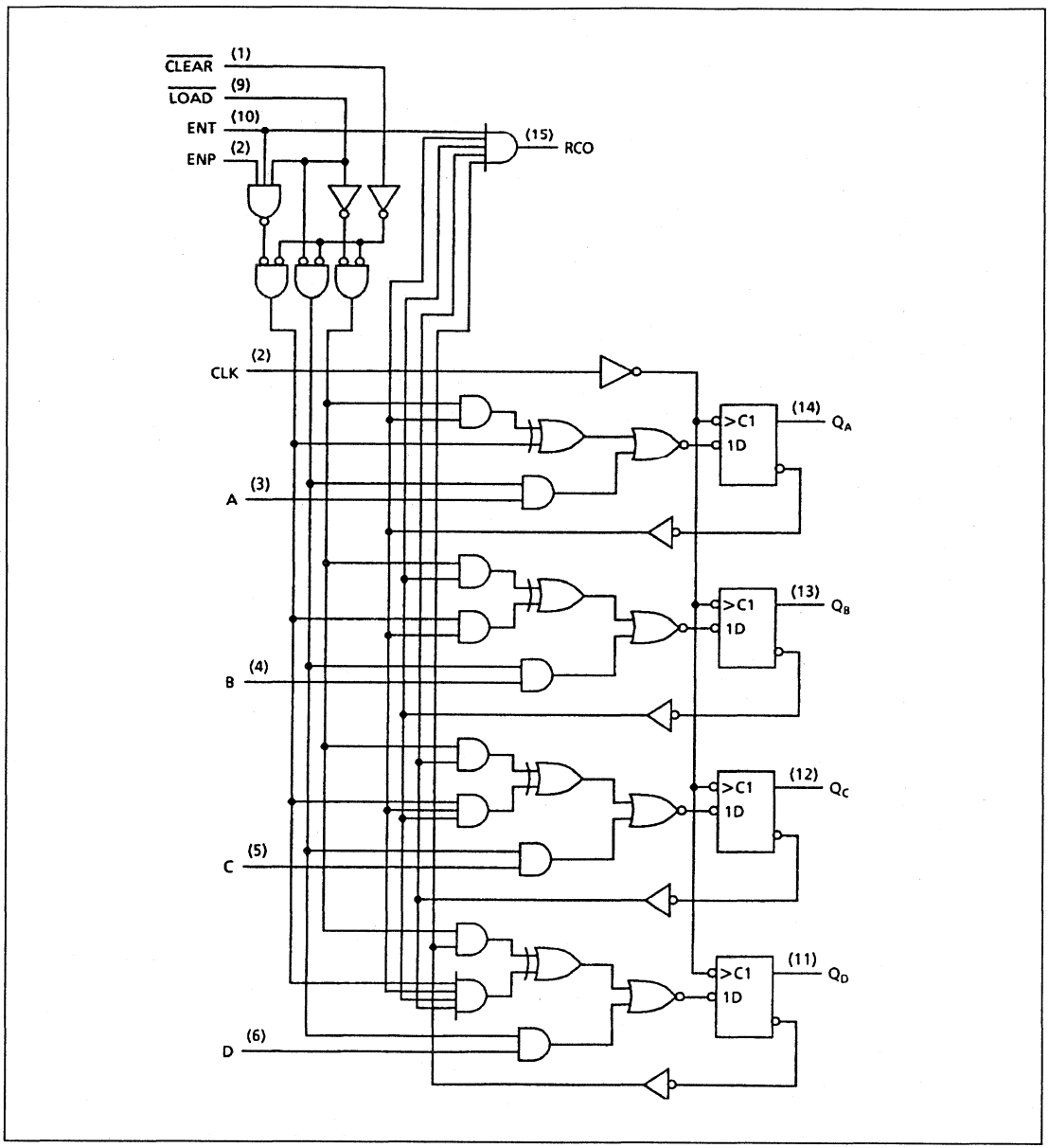


Figure 5: Logic Diagram

54HSC/T163 : Synchronous 4-Bit Counter

The 54HSC/T163 is a 4-Bit Counter with synchronous clear.

Inputs						Output
$\overline{\text{Clear}}$	Enable P	Enable T	A→D	$\overline{\text{Load}}$	Clock	$Q_A \rightarrow Q_D$
L	X	X	X	X	X	0
H	L	X	X	H	X	Inhibit
H	X	L	X	H	X	Inhibit
H	X	X	Q_n	L	↑	Q_n
H	X	X	X	X	L	Q_0
H	X	X	X	X	H	Q_0
H	H	H	X	H	↑	Count

CARRY = H when $Q_A \rightarrow Q_D$ = H, Q_0 = previous level of Q
H = high level, L = low level, X = irrelevant

Figure 1: Function Table

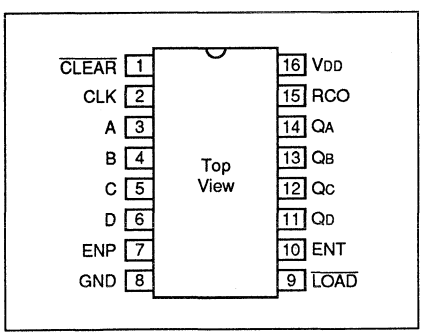


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Clock to RCO	12	20	15	22	ns
t_{PHL}	Propagation delay Clock to RCO	14	20	17	22	ns
t_{PLH}	Propagation delay Clock to any Q	15	20	18	22	ns
t_{PHL}	Propagation delay Clock to any Q	13	20	16	22	ns
t_{PLH}	Propagation delay ENT to RCO	9	15	12	17	ns
t_{PHL}	Propagation delay ENT to RCO	10	15	13	17	ns

Figure 3: Switching Characteristics

54HSC/T163 : Synchronous 4-Bit Counter

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T163 : Synchronous 4-Bit Counter

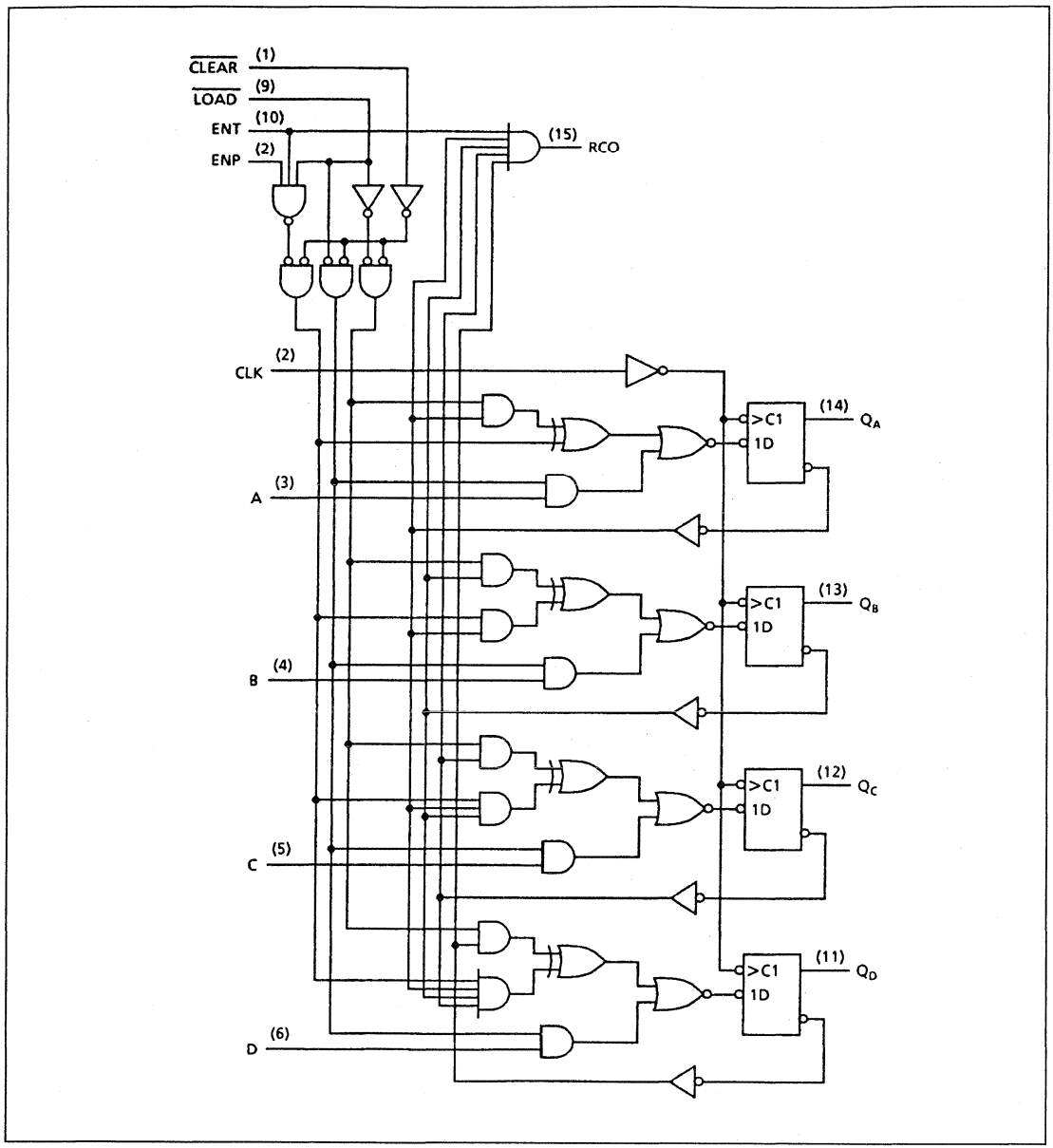


Figure 5: Logic Diagram

54HSC/T191 : Synchronous 4-Bit Counter

The 54HSC/T191 is a 4-Bit Synchronous Counter with presettable up/down and asynchronous reset.

Inputs				Function
$\overline{PL}$	$\overline{CE}$	$\overline{U}$/D	CP	
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Asyn. Preset
H	H	X	X	No Change

H = high level, L = low level, X = irrelevant, ↑ = low-to-high clock (CP) transition.
Note: $\overline{U}$/D or $\overline{CE}$ should be changed only when clock (CP) is high.

Figure 1: Function Table

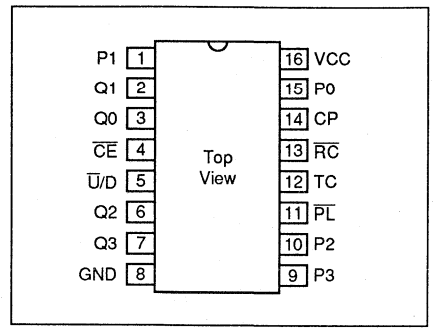


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay $\overline{PL}$ to Qn	-	29	-	33	ns
t_{PHL}	Propagation delay $\overline{PL}$ to Qn	-	32	-	36	ns
t_{PLH}	Propagation delay Pn to Qn	-	27	-	31	ns
t_{PHL}	Propagation delay Pn to Qn	-	30	-	34	ns
t_{PLH}	Propagation delay CP to Qn	-	26	-	30	ns
t_{PHL}	Propagation delay CP to Qn	-	29	-	33	ns
t_{PLH}	Propagation delay CP to $\overline{RC}$	-	20	-	23	ns
t_{PHL}	Propagation delay CP to $\overline{RC}$	-	32	-	34	ns
t_{PLH}	Propagation delay CP to TC	-	29	-	33	ns
t_{PHL}	Propagation delay CP to TC	-	32	-	36	ns
t_{PLH}	Propagation delay $\overline{U}$/D to $\overline{RC}$	-	27	-	31	ns
t_{PHL}	Propagation delay $\overline{U}$/D to $\overline{RC}$	-	30	-	34	ns
t_{PLH}	Propagation delay $\overline{U}$/D to TC	-	26	-	30	ns
t_{PHL}	Propagation delay $\overline{U}$/D to TC	-	29	-	33	ns
t_{PLH}	Propagation delay $\overline{CE}$ to $\overline{RC}$	-	22	-	25	ns
t_{PHL}	Propagation delay $\overline{CE}$ to $\overline{RC}$	-	35	-	38	ns

Figure 3: Switching Characteristics

54HSC/T191 : Synchronous 4-Bit Counter

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

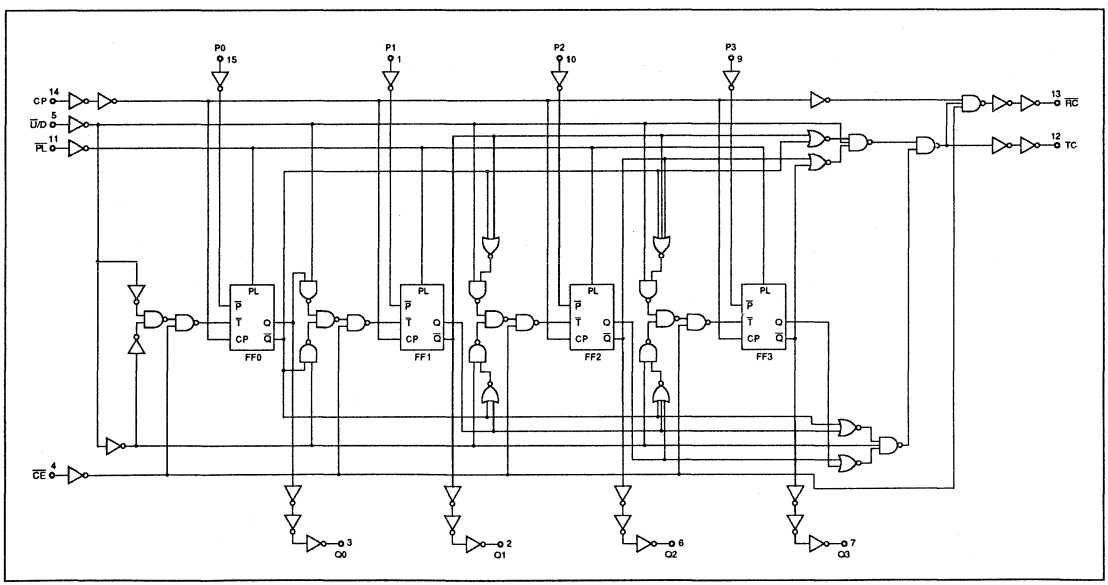


Figure 5: Logic Diagram

54HSC/T138 : 3-Line to 8-Line Decoder/Multiplexer

The 54HSC/T138 is a 3-Line to 8-Line Decoder/Multiplexer, with inverted outputs.

Enable Inputs			Select Inputs			Outputs							
G1	$\overline{G}$2A	$\overline{G}$2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

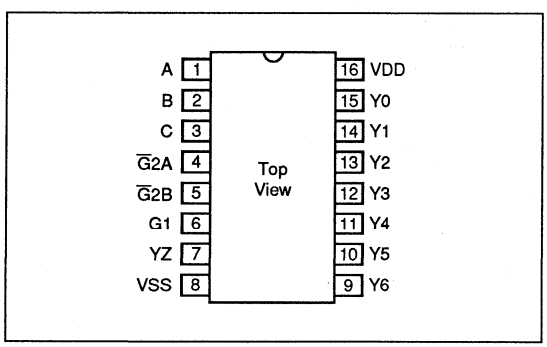


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Address to Output.	17	25	20	28	ns
t_{PHL}	Propagation delay. Address to Output.	19	25	22	28	ns
t_{PLH}	Propagation delay. G to Output.	21	25	24	28	ns
t_{PHL}	Propagation delay. G to Output.	21	25	24	28	ns

Figure 3: Switching Characteristics

54HSC/T138 : 3-Line to 8-Line Decoder/Multiplexer

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

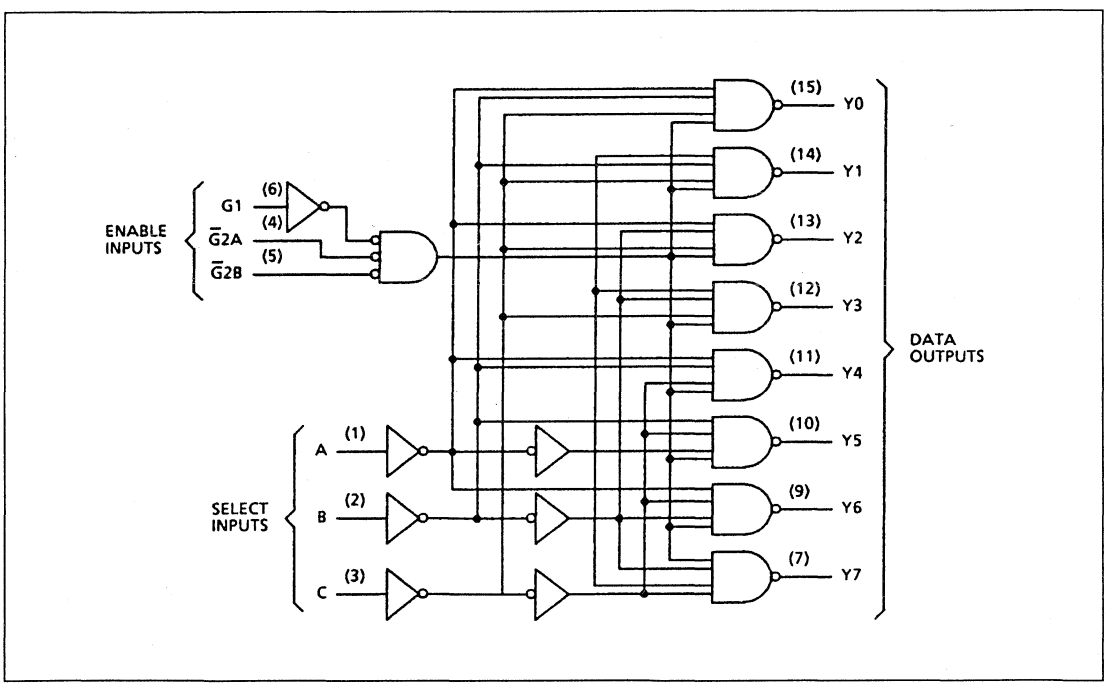


Figure 5: Logic Diagram

54HSC/T139 : Dual 2 to 4 Decoders/Multiplexers

The 54HSC/T139 consists of Two Independent 2 to 4 Line Decoder/Multiplexers.

Inputs			Output			
Enable	Select					
$\overline{G}$	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

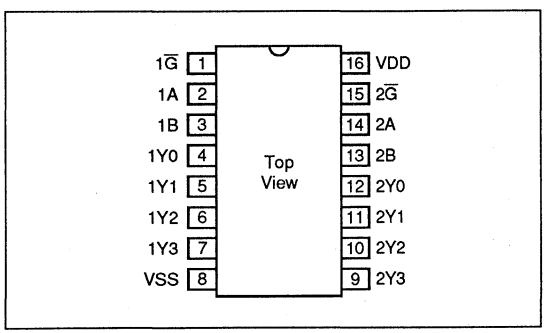


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Address to Output.	16	28	22	34	ns
t_{PHL}	Propagation delay. Address to Output.	17	28	20	34	ns
t_{PLH}	Propagation delay. G to Output.	16	22	19	25	ns
t_{PHL}	Propagation delay. G to Output.	17	22	20	25	ns

Figure 3: Switching Characteristics

54HSC/T139 : Dual 2 to 4 Decoders/Multiplexers

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	10	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

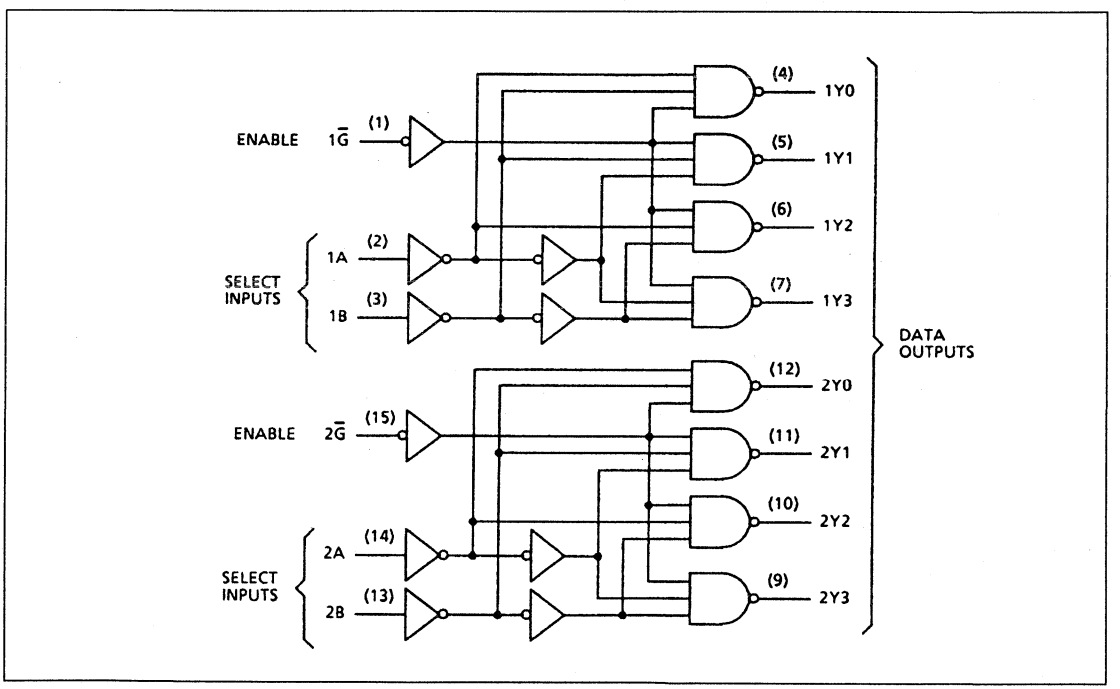


Figure 5: Logic Diagram

54HSC/T148 : 8-Line to 3-Line Octal Priority Encoders

The 54HSC/T148 is an 8 to 3 Line Priority Encoder. Data inputs and outputs are active at the low logic level. Data is accepted on the eight priority inputs (I0-I7). The binary code, corresponding to the highest priority input which is low, is generated on the address outputs (A0-A2) if the enable input is high. The group select (GS) is low when one or more priority inputs and the enable input (EI) are low. The enable output (EO) is low when all priority inputs are high and the enable is low. When the enable input is high all outputs are high.

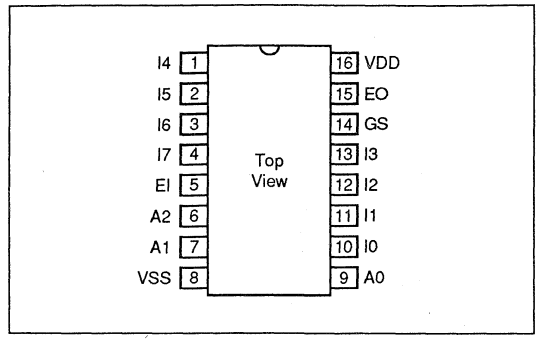


Figure 1: Pin Out

Inputs									Outputs				
EI	**I0**	**I1**	**I2**	**I3**	**I4**	**I5**	**I6**	**I7**	**A2**	**A1**	**A0**	**GS**	**EO**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high level, L = low level, X = irrelevant

Figure 2: Function Table

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay EI to A	14	22	17	28	ns
t_{PHL}	Propagation delay EI to A	15	22	18	28	ns
t_{PLH}	Propagation delay EI to GS	15	22	18	28	ns
t_{PHL}	Propagation delay EI to GS	15	22	18	28	ns
t_{PLH}	Propagation delay EI to EO	14	22	17	28	ns
t_{PHL}	Propagation delay EI to EO	15	22	18	28	ns
t_{PLH}	Propagation delay I to A	12	22	15	28	ns
t_{PHL}	Propagation delay I to A	14	22	17	28	ns

Figure 3: Switching Characteristics

54HSC/T148 : 8-Line to 3-Line Octal Priority Encoders

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T148 : 8-Line to 3-Line Octal Priority Encoders

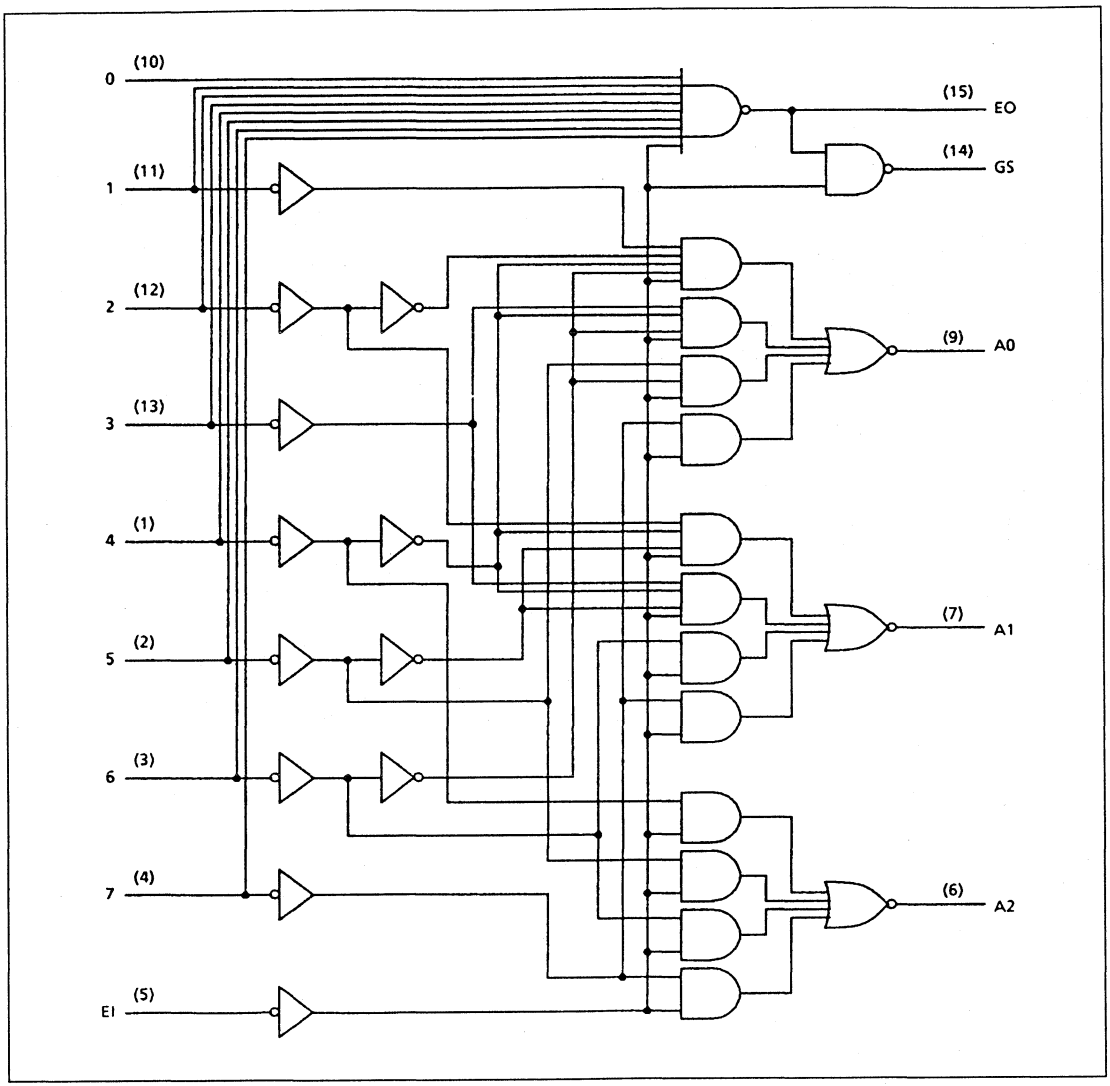


Figure 5: Logic Diagram

54HSC/T151 : 1 of 8 Data Selectors/Multiplexers

The 54HSC/T151 is a 1 of 8 Data Selector. When the strobe input is low the device is enabled. When high this forces the W-output high and the Y-output low.

Inputs				Output	
Select			Strobe		
C	B	A	$\overline{STR}$	Y	W
X	X	X	H	L	H
L	L	L	L	D_0	$\overline{D}_0$
L	L	H	L	D_1	$\overline{D}_1$
L	H	L	L	D_2	$\overline{D}_2$
L	H	H	L	D_3	$\overline{D}_3$
H	L	L	L	D_4	$\overline{D}_4$
H	L	H	L	D_5	$\overline{D}_5$
H	H	L	L	D_6	$\overline{D}_6$
H	H	H	L	D_7	$\overline{D}_7$

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

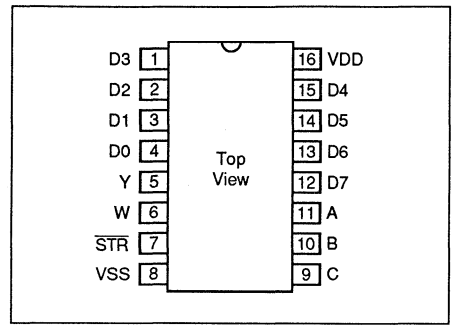


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A B or C to Y	15	22	18	25	ns
t_{PHL}	Propagation delay A B or C to Y	16	22	19	25	ns
t_{PLH}	Propagation delay A B or C to W	14	22	17	25	ns
t_{PHL}	Propagation delay A B or C to W	15	22	18	25	ns
t_{PLH}	Propagation delay Strobe to Y	14	22	17	25	ns
t_{PHL}	Propagation delay Strobe to Y	16	22	19	25	ns
t_{PLH}	Propagation delay Strobe to W	14	22	17	25	ns
t_{PHL}	Propagation delay Strobe to W	15	22	18	25	ns
t_{PLH}	Propagation delay D_0-D_7 to Y	12	22	15	25	ns
t_{PHL}	Propagation delay D_0-D_7 to Y	14	22	17	25	ns
t_{PLH}	Propagation delay D_0-D_7 to W	12	22	15	25	ns
t_{PHL}	Propagation delay D_0-D_7 to W	14	22	17	25	ns

Figure 3: Switching Characteristics

54HSC/T151 : 1 of 8 Data Selectors/Multiplexers

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T151 : 1 of 8 Data Selectors/Multiplexers

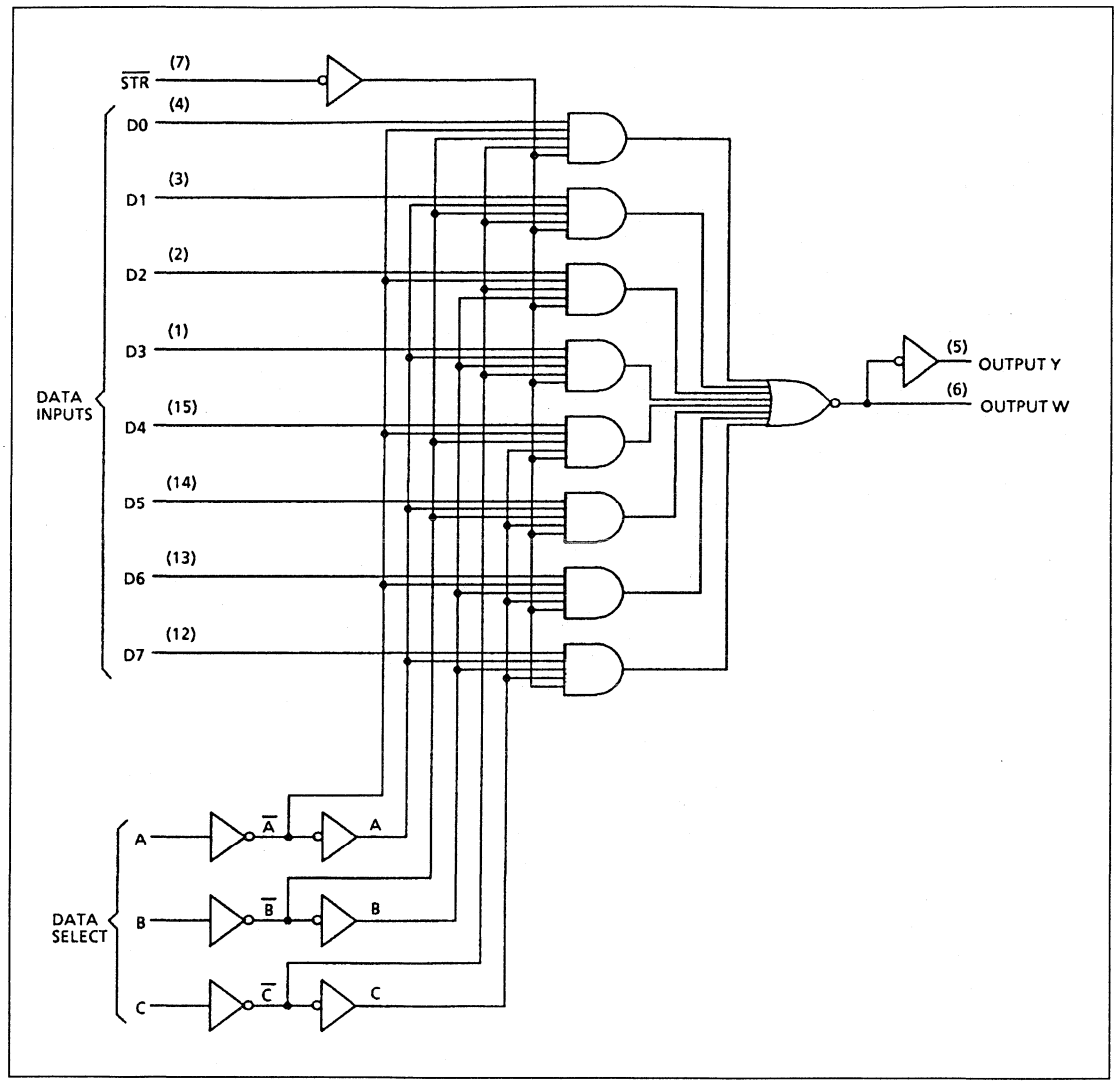


Figure 5: Logic Diagram

54HSC/T154 : 4 to 16 Line Decoders/Demultiplexers

The 54HSC/T154 consists of a 4 to 16 Line Decoder/Demultiplexer.

Inputs						Outputs															
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

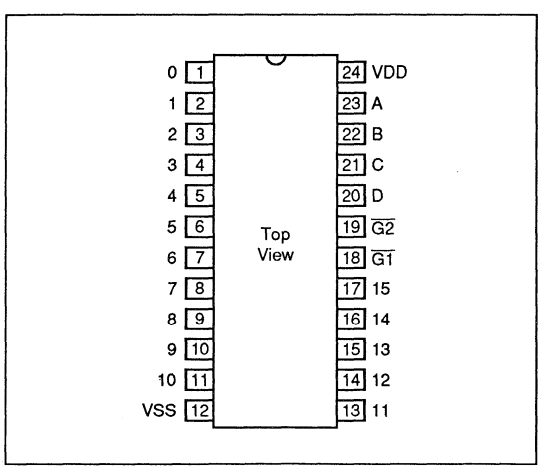


Figure 2: Pin Out

54HSC/T154 : 4 to 16 Line Decoders/Demultiplexers

Sym	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay low to high level output for change in A B C or D input	18	30	21	33	ns
t_{PHL}	Propagation delay high to low level output for change in A B C or D input	21	30	24	33	ns
t_{PLH}	Propagation delay low to high level output for change in $\overline{G1}$ or $\overline{G2}$	21	30	24	33	ns
t_{PHL}	Propagation delay high to low level output for change in $\overline{G1}$ or $\overline{G2}$	18	30	21	33	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	100	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T154 : 4 to 16 Line Decoders/Demultiplexers

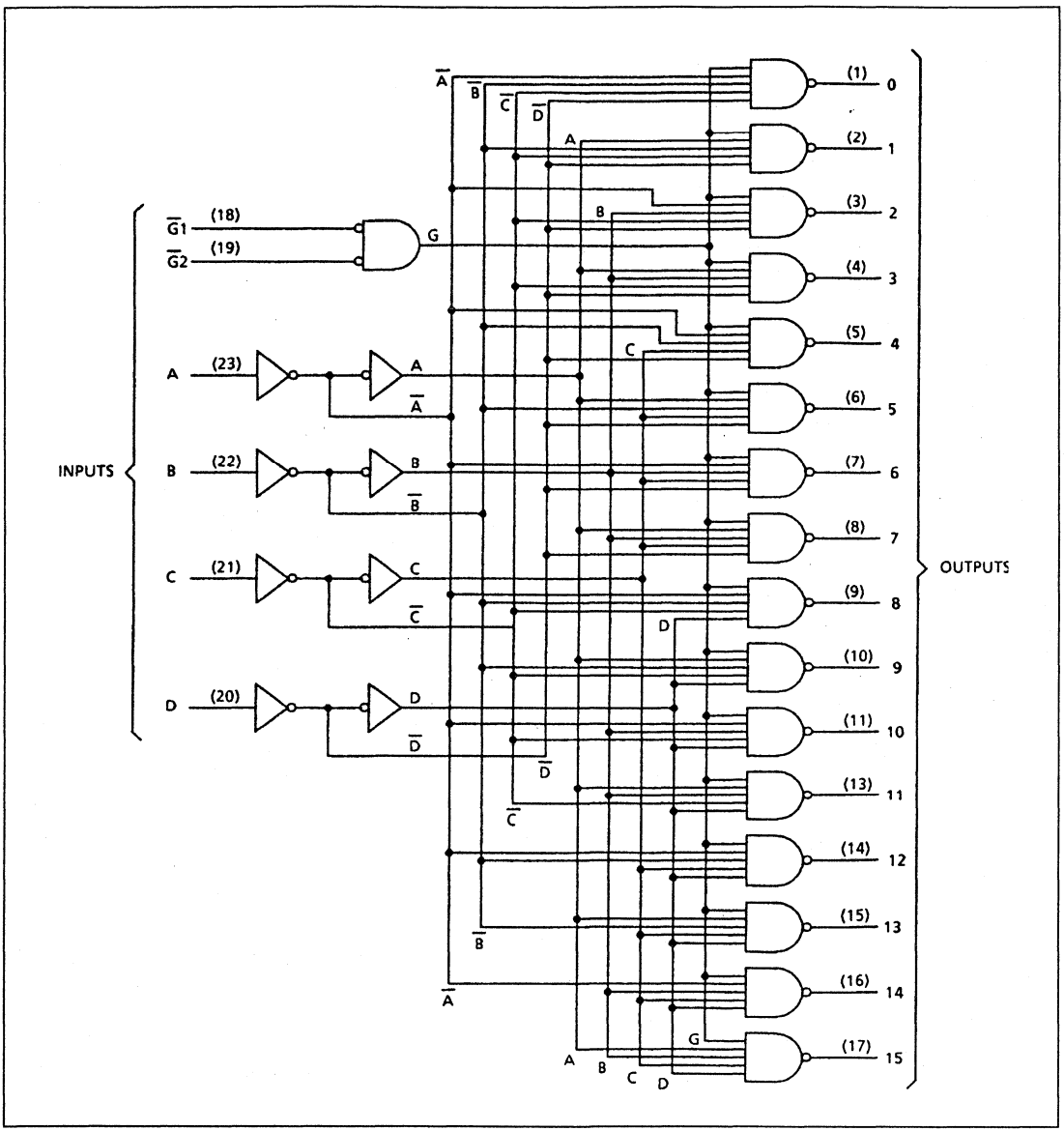


Figure 5: Logic Diagram

54HSC/T157 : Quad 2-Line to 1-Line Data Selectors/Multiplexers

The 54HSC/T157 is a Quadruple 2-Line to 1-Line Data Selector with non-inverted output. The strobe must be low to enable the device. When select is low, A is selected. When select is high, B is selected.

Inputs				Outputs
$\overline{STR}$	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

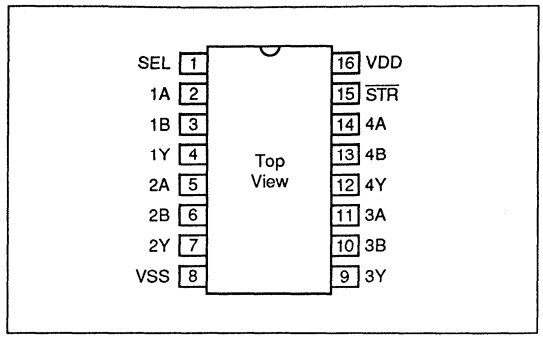


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay A or B to Y	14	25	17	25	ns
t_{PHL}	Propagation delay A or B to Y	15	20	18	22	ns
t_{PZH}	Propagation delay Strobe to Y	14	22	17	24	ns
t_{PZL}	Propagation delay Strobe to Y	15	22	18	24	ns
t_{PHZ}	Propagation delay Select to Y	14	25	17	25	ns
t_{PLZ}	Propagation delay Select to Y	15	25	18	25	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T157 : Quad 2-Line to 1-Line Data Selectors/Multiplexers

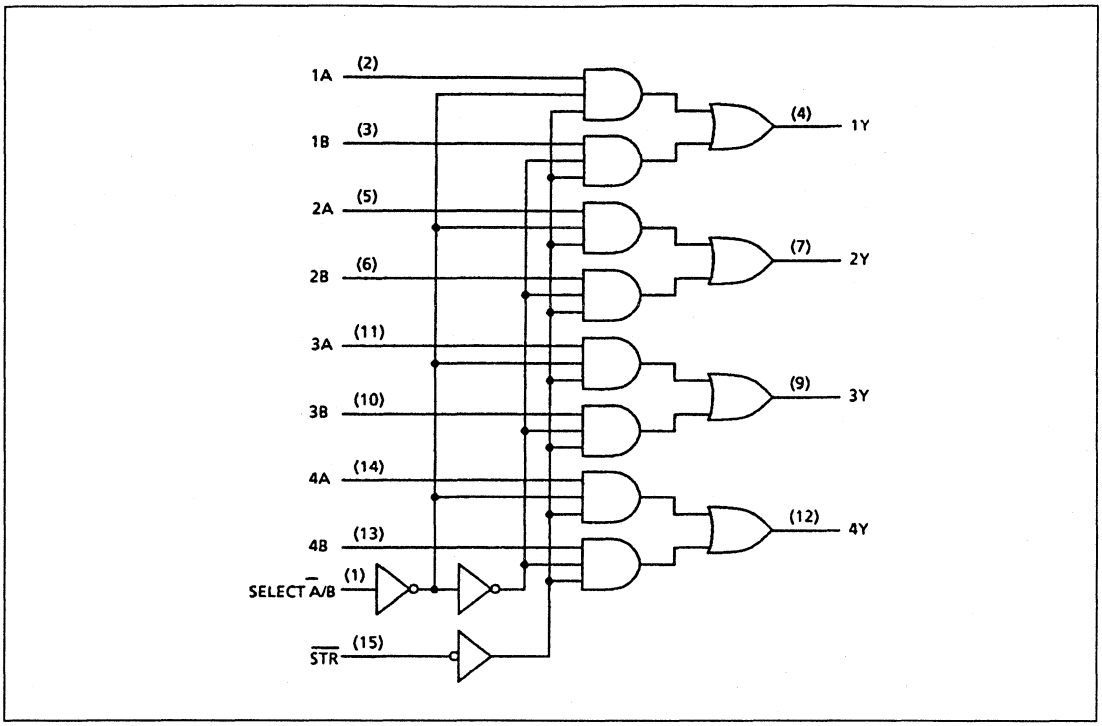


Figure 5: Logic Diagram

54HSC/T238 : 3-Line to 8-Line Decoder/Demultiplexer

The 54HSC/T238 is a 3-Line to 8-Line Decoder/Demultiplexer, with unlatched inputs and non-inverted outputs.

Enable Inputs		Select Inputs			Outputs							
E_3	$\overline{E}_2/\overline{E}_1$	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	H	H	L	L	L	H	L	L	L	L
H	L	H	L	L	L	L	L	L	H	L	L	L
H	L	H	L	H	L	L	L	L	L	H	L	L
H	L	H	H	L	L	L	L	L	L	L	H	L
H	L	H	H	H	L	L	L	L	L	L	L	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

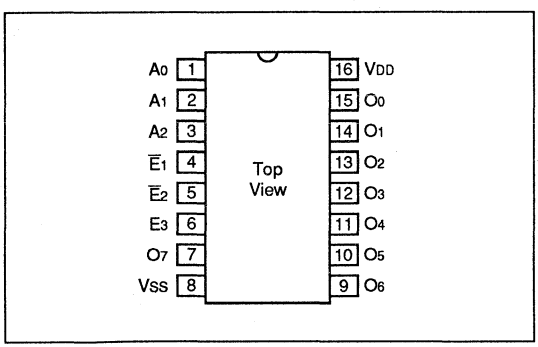


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, address to output, low to high level output	16	24	19	27	ns
t_{PHL}	Propagation delay, address to output, high to low level output	17	25	20	28	ns
t_{PLH}	Propagation delay, enable to output, low to high level output	19	27	22	30	ns
t_{PHL}	Propagation delay, enable to output, high to low level output	19	27	22	30	ns

Figure 3: Switching Characteristics

54HSC/T238 : 3-Line to 8-Line Decoder/Demultiplexer

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

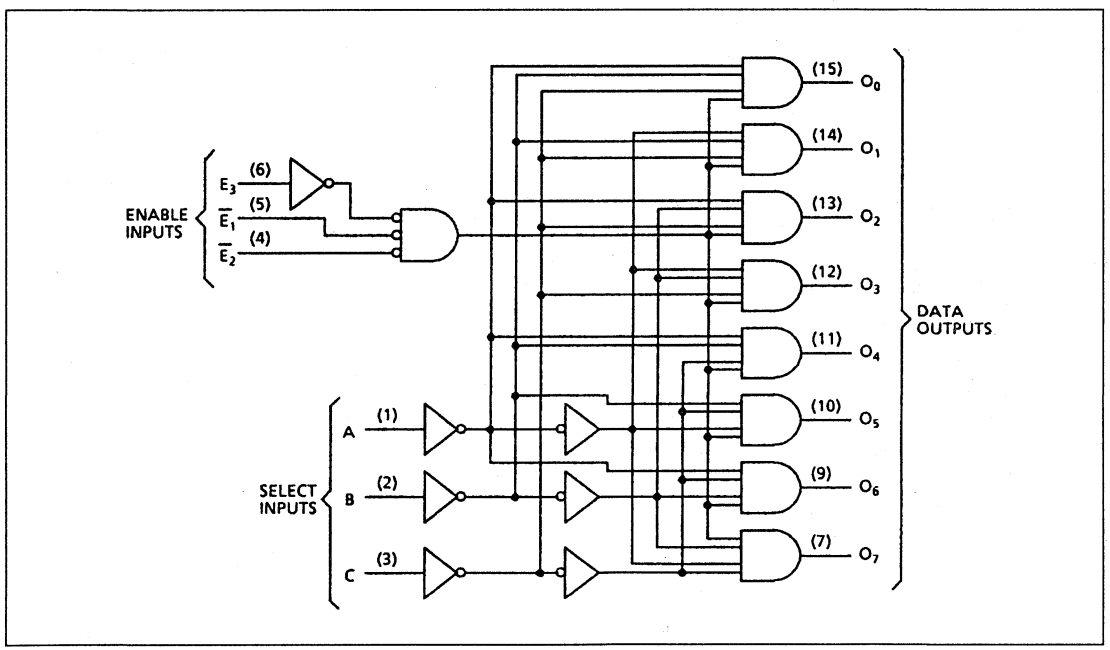


Figure 5: Logic Diagram

54HSC/T253 : Dual 4 to 1 Data Selectors/Multiplexers

The 54HSC/T253 is a Dual 4-Line to 1-Line Data Selector/Multiplexer with tri-state outputs.

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	$\overline{G}$	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 1: Function Table

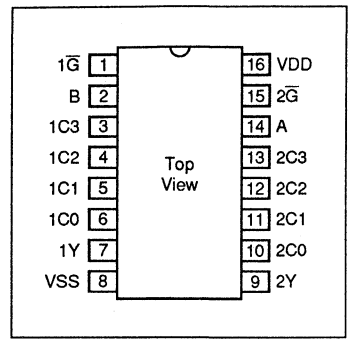


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay Data to Output	14	25	17	25	ns
t_{PHL}	Propagation delay Data to Output	15	25	18	25	ns
t_{PLH}	Propagation delay Select to Output	14	25	17	25	ns
t_{PHL}	Propagation delay Select to Output	15	25	18	25	ns
t_{PZL}	Propagation delay Tri-state to Output Low	12	25	15	25	ns
t_{PZH}	Propagation delay Tri-state to Output High	13	25	16	25	ns
t_{PLZ}	Propagation delay Low to Tri-state	12	25	15	25	ns
t_{PHZ}	Propagation delay High to Tri-state	13	25	16	25	ns

Figure 3: Switching Characteristics

54HSC/T253 : Dual 4 to 1 Data Selectors/Multiplexers

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

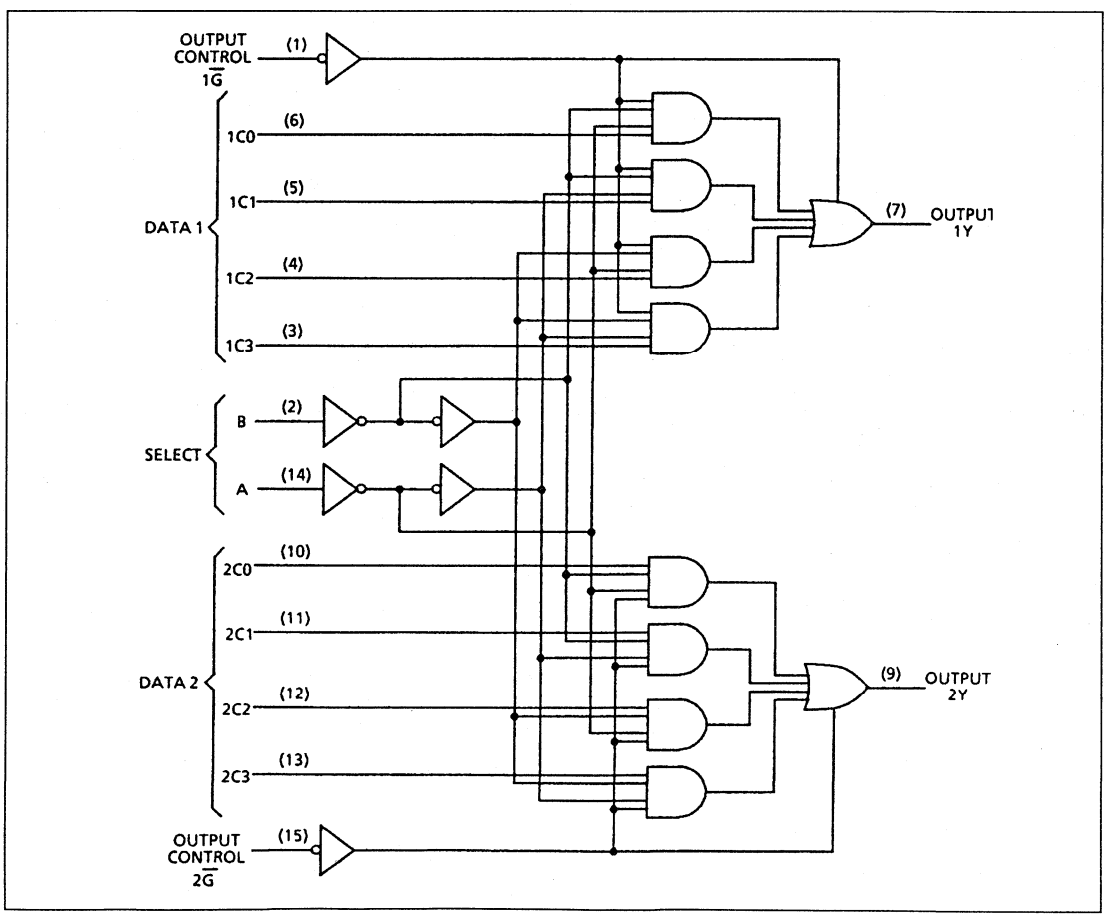


Figure 5: Logic Diagram

54HSC/T164 : 8-Bit Parallel Output Serial Shift Register

The 54HSC/T164 is an 8-Bit Parallel Output Serial Shift Register with asynchronous clear.

Inputs				Outputs		
$\overline{CLEAR}$	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	↑	H	H	H	Q_{AN}	Q_{GN}
H	↑	L	X	L	Q_{AN}	Q_{GN}
H	↑	X	L	L	Q_{AN}	Q_{GN}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high level. Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B or Q_H, respectively, before the indicated steady-state input conditions were set up. Q_{AN}, Q_{BN}, Q_{HN} = the level of Q_A or Q_G before the latest ↑ transition of the clock. Indicates a one bit shift.

Figure 1: Function Table

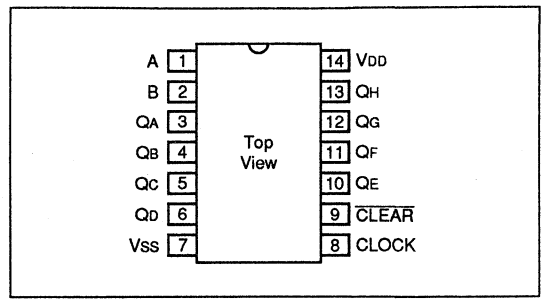


Figure 2: Pin Out

Symbol	Parameter	+25°C Typ.	+25°C Max.	-55°C / +125°C Typ.	-55°C / +125°C Max.	Units
t_{PLH}	Propagation delay. Q output from clock input, low to high level output.	15	25	18	28	ns
t_{PHL}	Propagation delay. Q output from clock input, high to low level output.	15	25	18	28	ns
t_{PHL}	Propagation delay. Q output from clear input, high to low level output.	15	25	18	28	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits +25°C Min.	Limits +25°C Max.	Limits -55°C / +125°C Min.	Limits -55°C / +125°C Max.	Units
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T164 : 8-Bit Parallel Output Serial Shift Register

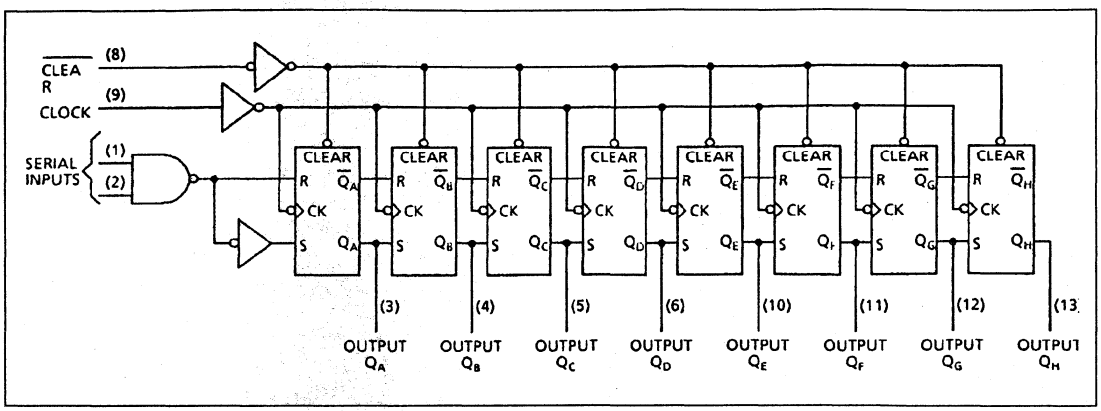


Figure 5: Logic Diagram

54HSC/T165 : Parallel Load 8-Bit Shift Register

The 54HSC/T165 is an 8-Bit Serial Shift Register that shifts the data in the direction of Q_A to Q_H when clocked.

Inputs					Internal Outputs		Output
Shift/$\overline{\text{Load}}$	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high, a...h = the level of steady state inputs at inputs A through H. Q_O = level of Q before the indicated steady state input conditions were set up. Q_N = level of Q before the most recent active transition indicated by ↑.

Figure 1: Function Table

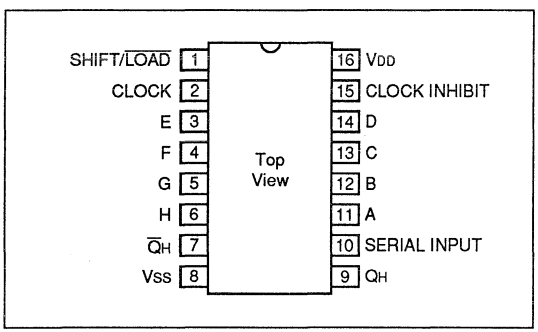


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Load to Any Output.	18	25	21	28	ns
t_{PHL}	Propagation delay. Load to Any Output.	16	25	19	28	ns
t_{PLH}	Propagation delay. Clock to Any Output.	18	25	21	28	ns
t_{PHL}	Propagation delay. Clock to Any Output.	18	25	21	28	ns
t_{PLH}	Propagation delay. H to Q_H.	18	25	21	28	ns
t_{PHL}	Propagation delay. H to Q_H.	18	25	21	28	ns
t_{PLH}	Propagation delay. H to QB_H.	18	25	21	28	ns
t_{PHL}	Propagation delay. H to QB_H.	18	25	21	28	ns

Figure 3: Switching Characteristics

54HSC/T165 : Parallel Load 8-Bit Shift Register

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

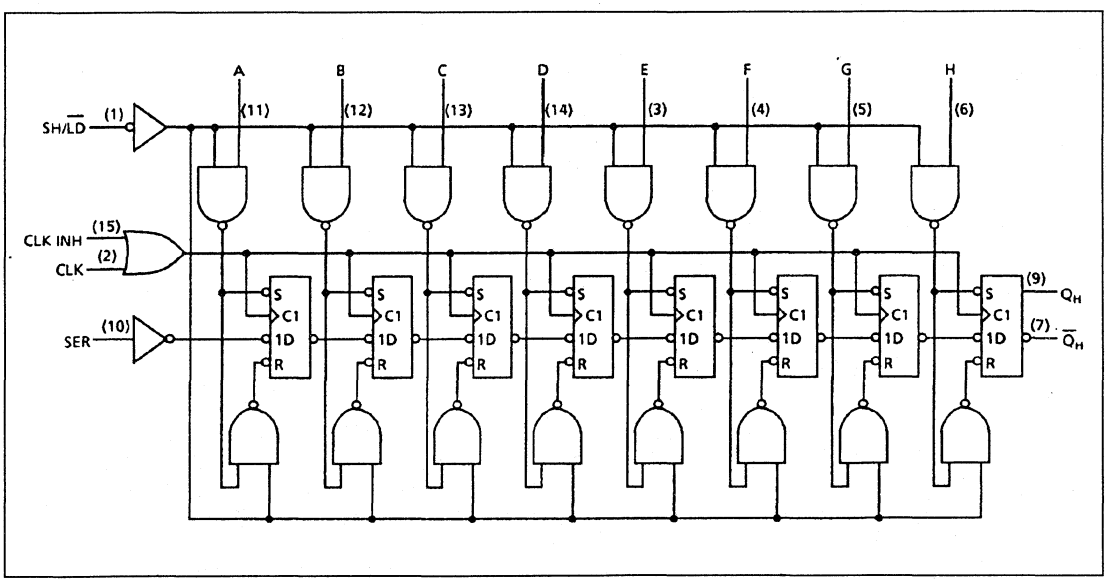


Figure 5: Logic Diagram

54HSC/T166 : 8-Bit Shift Register

The 54HSC/T166 is an 8-Bit parallel in or serial in, serial out Shift Register with a gated clock input and an overriding clear input.

Inputs						Internal Outputs		Output
$\overline{\text{Clear}}$	Shift/ $\overline{\text{Load}}$	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	X	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

H = high level, L = low level, X = irrelevant, ↑ = transition from low to high, a...h = the level of steady state inputs at inputs A through H. Q_O = level of Q before the indicated steady state input conditions were set up. Q_N = level of Q before the most recent active transition indicated by ↑.

Figure 1: Function Table

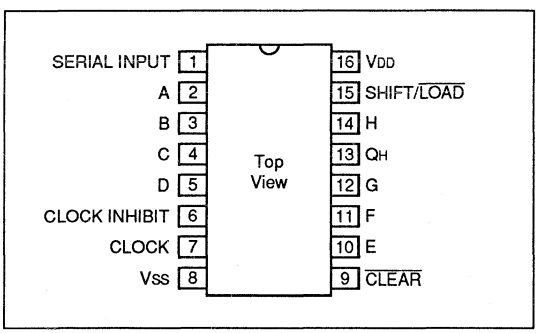


Figure 2: Pin Out

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PHL}	Propagation delay. Clear to Q_H.	15	25	18	28	ns
t_{PHL}	Propagation delay. Clock to Q_H.	15	25	18	28	ns
t_{PLH}	Propagation delay. Clock to Q_H.	15	25	18	28	ns

Figure 3: Switching Characteristics

54HSC/T166 : 8-Bit Shift Register

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	400	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T166 : 8-Bit Shift Register

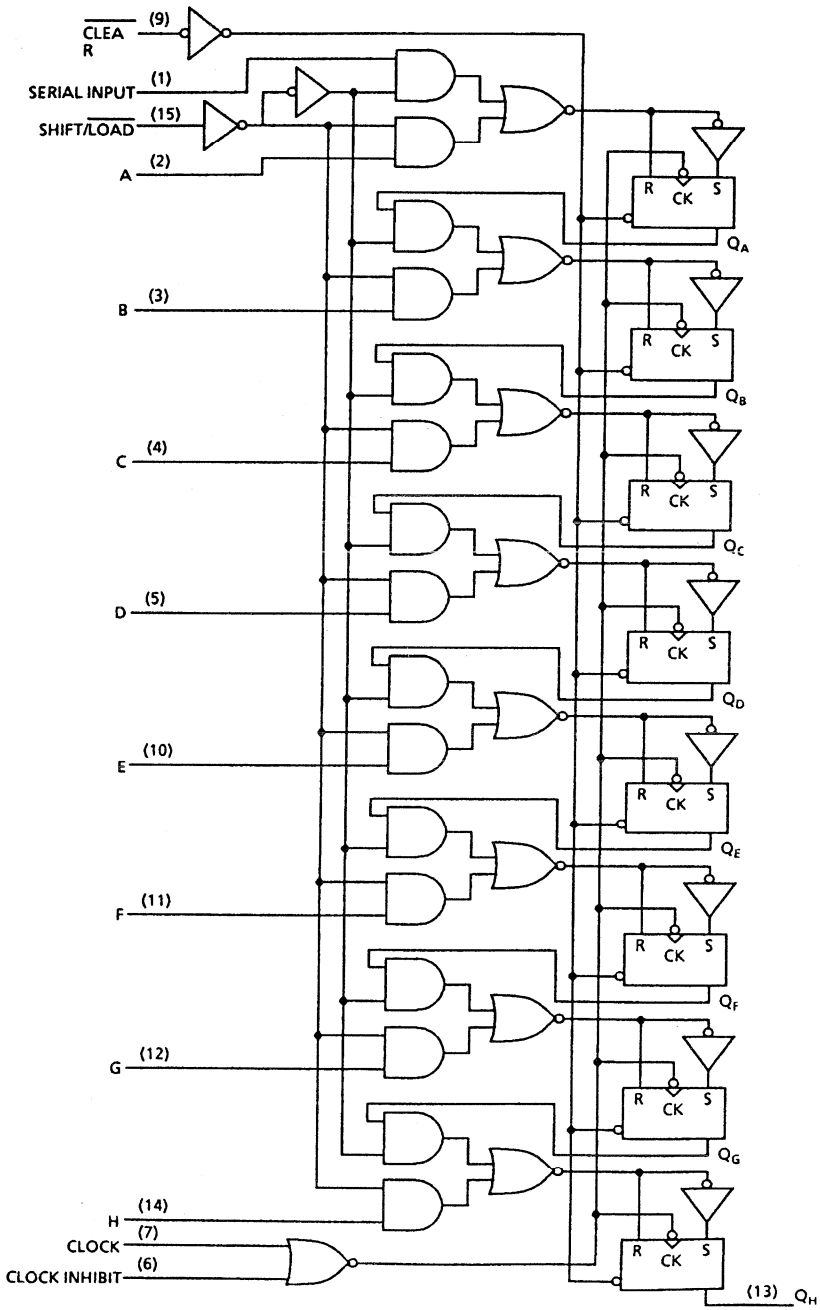


Figure 5: Logic Diagram

54HSC/T521 : 8-Bit Magnitude Comparator

The 54HSC/T521 is an 8-Bit Magnitude Comparator.

Inputs		Outputs
Data P,Q	Enable $\overline{G}$	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

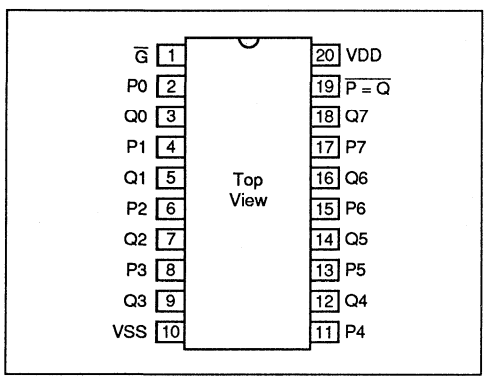


Figure 2: Pin Out

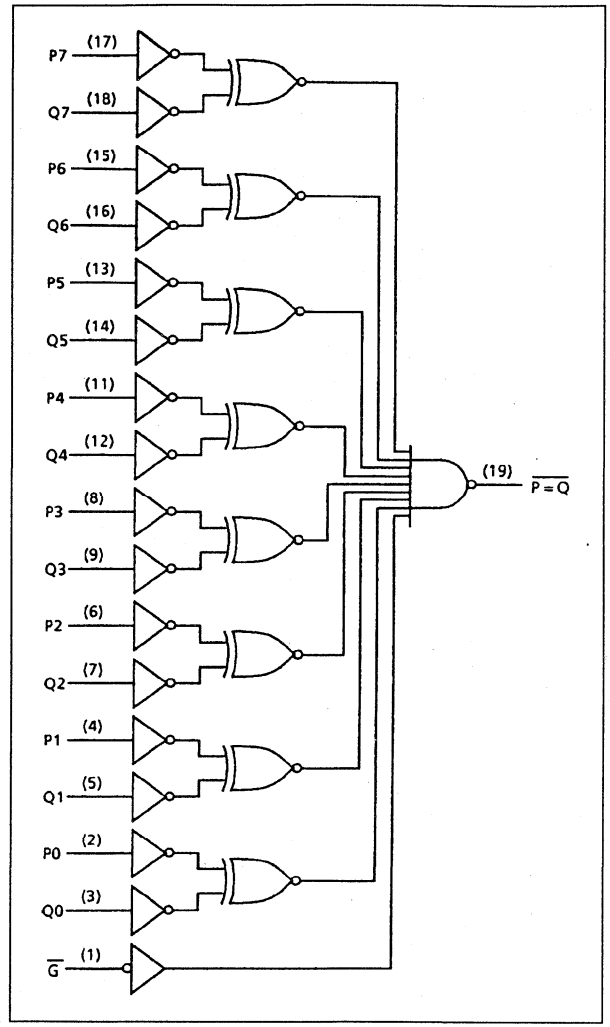


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. P or Q to PN = QN.	15	25	18	28	ns
t_{PHL}	Propagation delay. P or Q to PN = QN.	16	25	19	28	ns
t_{PLH}	Propagation delay. GN to PN = QN.	14	25	17	28	ns
t_{PHL}	Propagation delay. GN to PN = QN.	15	25	18	28	ns

Figure 4: Switching Characteristics

54HSC/T521 : 8-Bit Magnitude Comparator

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T240 : Octal 3-State Driver, Inverting

The 54HSC/T240 is an Octal 3-State Driver, inverting.

Inputs		Outputs
$\overline{E}$	I_{0-3}	$\overline{O}_{0-3}$
L	L	H
L	H	L
H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

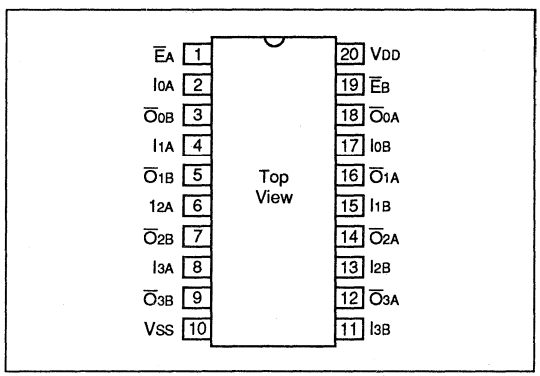


Figure 2: Pin Out

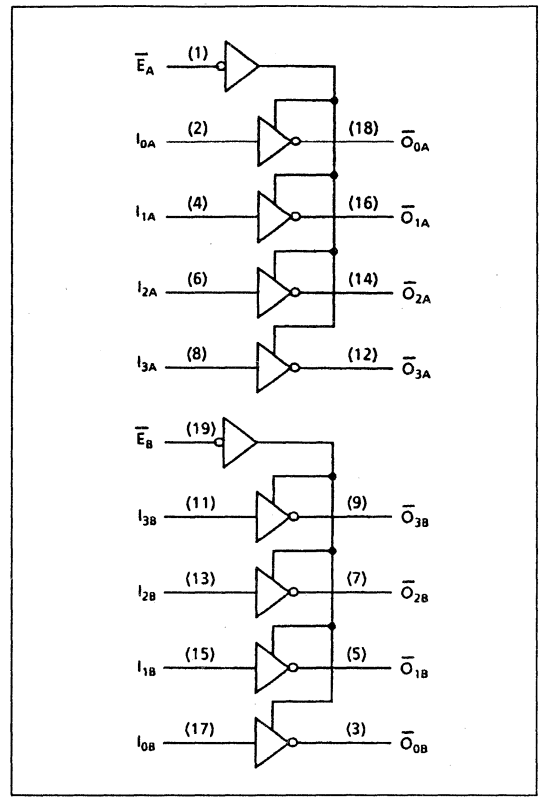


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	12	20	15	23	ns
t_{PHL}	Propagation delay, high to low level output.	14	22	17	25	ns
t_{PZL}	Propagation delay, enable to low level.	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level.	14	22	17	25	ns
t_{PLZ}	Propagation delay, disable from low.	22	30	25	33	ns
t_{PHZ}	Propagation delay, disable from high.	21	30	24	33	ns

Figure 4: Switching Characteristics

54HSC/T240 : Octal 3-State Driver, Inverting

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T241 : Octal 3-State Driver, Complementary Enable

The 54HSC/T241 is an Octal 3-State Driver, complementary enable.

Inputs			Outputs
$\overline{E}_A$	E_B	I_{0-3}	O_{0-3}
L	H	L	H
L	H	H	L
H	L	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

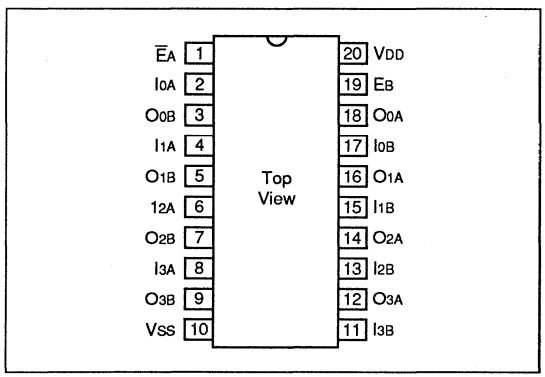


Figure 2: Pin Out

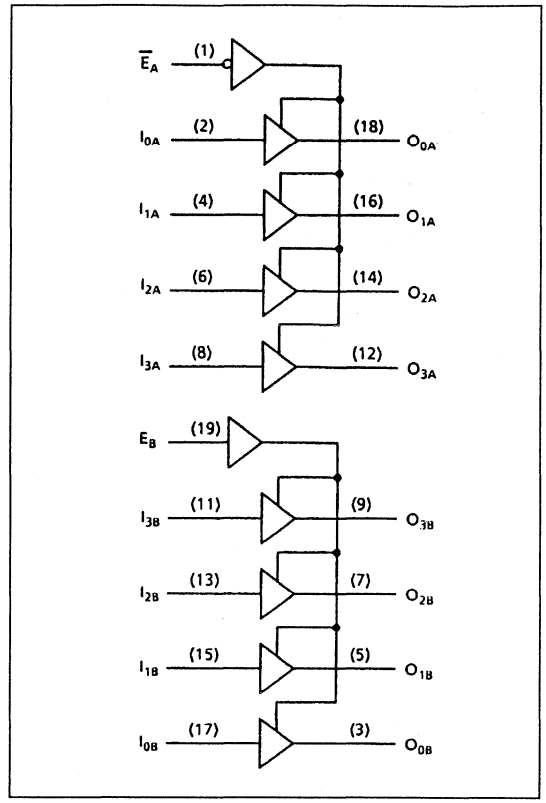


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level.	19	27	21	30	ns
t_{PZH}	Propagation delay, enable to high level.	19	27	21	30	ns
t_{PLZ}	Propagation delay, low to disable.	22	30	25	33	ns
t_{PHZ}	Propagation delay, high to disable.	21	30	24	33	ns

Figure 4: Switching Characteristics

54HSC/T241 : Octal 3-State Driver, Complementary Enable

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T244 : Octal 3-State Driver

The 54HSC/T244 is an Octal 3-State Driver.

Inputs		Outputs
$\overline{E}$	I_{0-3}	O_{0-3}
L	L	H
L	H	L
H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

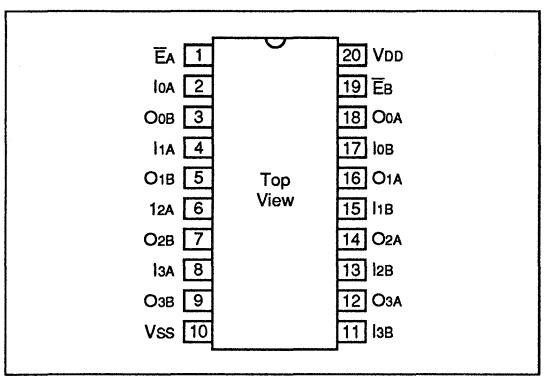


Figure 2: Pin Out

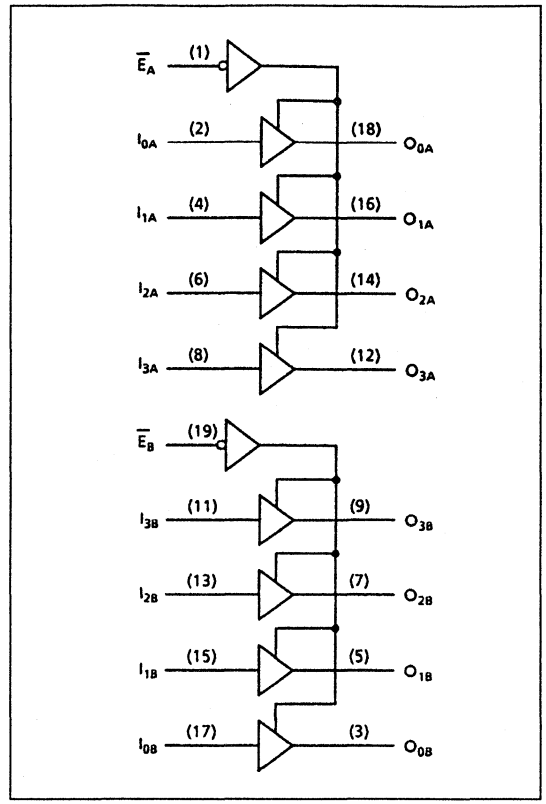


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	11	21	14	21	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	21	ns
t_{PZL}	Propagation delay, enable to low level.	19	25	21	25	ns
t_{PZH}	Propagation delay, enable to high level.	15	20	21	24	ns
t_{PLZ}	Propagation delay, low to disable.	19	25	22	25	ns
t_{PHZ}	Propagation delay, high to disable.	18	25	21	25	ns

Figure 4: Switching Characteristics

54HSC/T244 : Octal 3-State Driver

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T540 : Octal 3-State Driver/Buffer Inverting

The 54HSC/T540 is an Octal 3-State Driver/Buffer Inverting.

Inputs			Outputs
$\overline{E}_A$	$\overline{E}_B$	I_{0-7}	$\overline{O}_{0-7}$
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

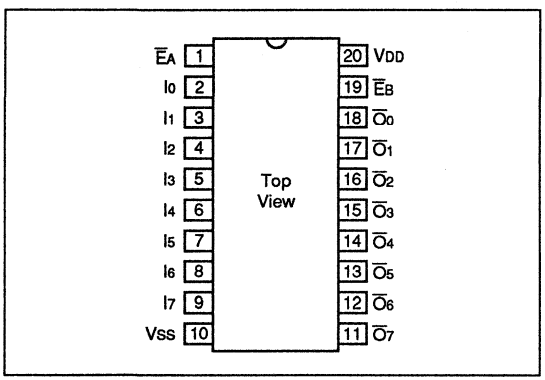


Figure 2: Pin Out

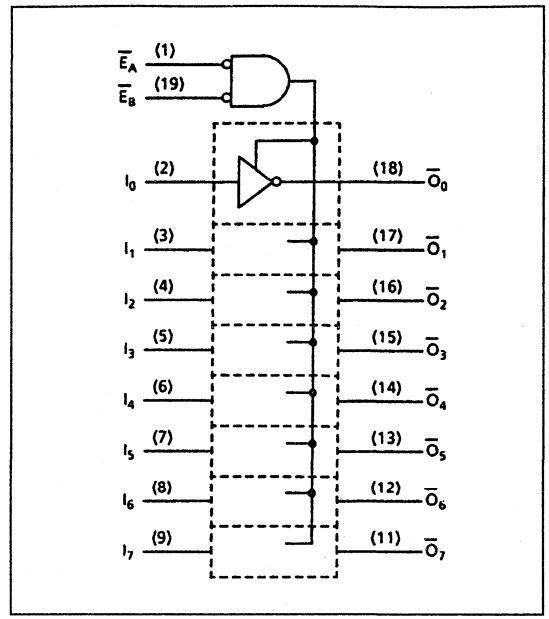


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	13	21	16	24	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	24	ns
t_{PZL}	Propagation delay, enable to low level.	21	29	24	32	ns
t_{PZH}	Propagation delay, enable to high level.	16	24	19	27	ns
t_{PLZ}	Propagation delay, low to disable.	24	32	27	35	ns
t_{PHZ}	Propagation delay, high to disable.	23	31	26	34	ns

Figure 4: Switching Characteristics

54HSC/T540 : Octal 3-State Driver/Buffer Inverting

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T541 : Octal 3-State Driver/Buffer

The 54HSC/T541 is an Octal 3-State Driver/Buffer.

Inputs			Outputs
$\overline{E}_A$	$\overline{E}_B$	I_{0-7}	O_{0-7}
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

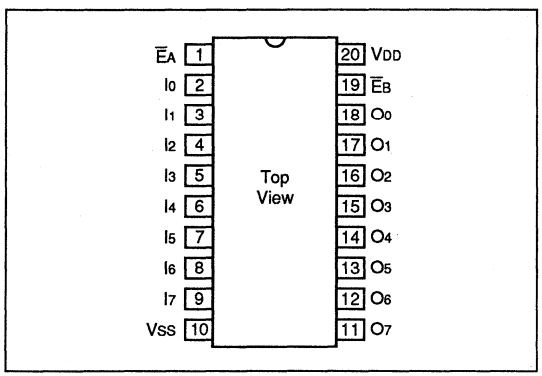


Figure 2: Pin Out

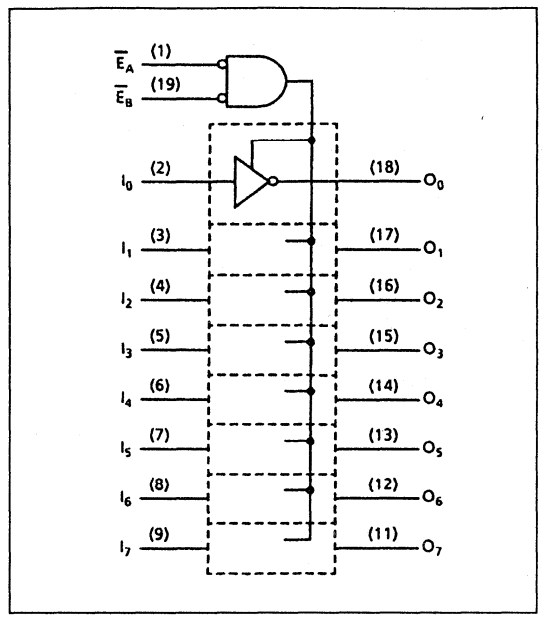


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	11	19	14	22	ns
t_{PHL}	Propagation delay, high to low level output.	13	21	16	22	ns
t_{PZL}	Propagation delay, enable to low level.	17	21	20	35	ns
t_{PZH}	Propagation delay, enable to high level.	16	24	19	30	ns
t_{PLZ}	Propagation delay, low to disable.	24	21	27	25	ns
t_{PHZ}	Propagation delay, high to disable.	23	21	26	25	ns

Figure 4: Switching Characteristics

54HSC/T541 : Octal 3-State Driver/Buffer

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T245 : Octal Bus Transceiver

The 54HSC/T245 is an Octal Bus Transceiver.

Inputs		Outputs
$\overline{E}$	DIR	
L	L	B data to Bus A
L	H	A data to Bus B
H	X	Isolation

H = high level, L = low level, X = irrelevant

Figure 1: Function Table

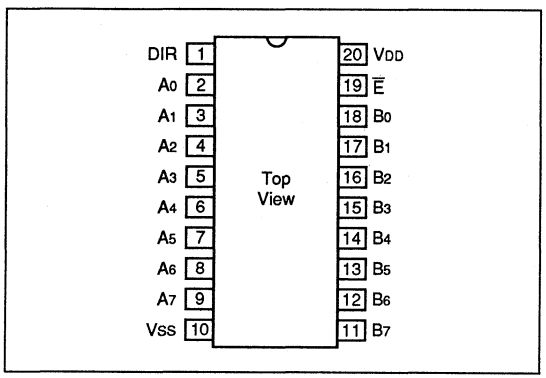


Figure 2: Pin Out

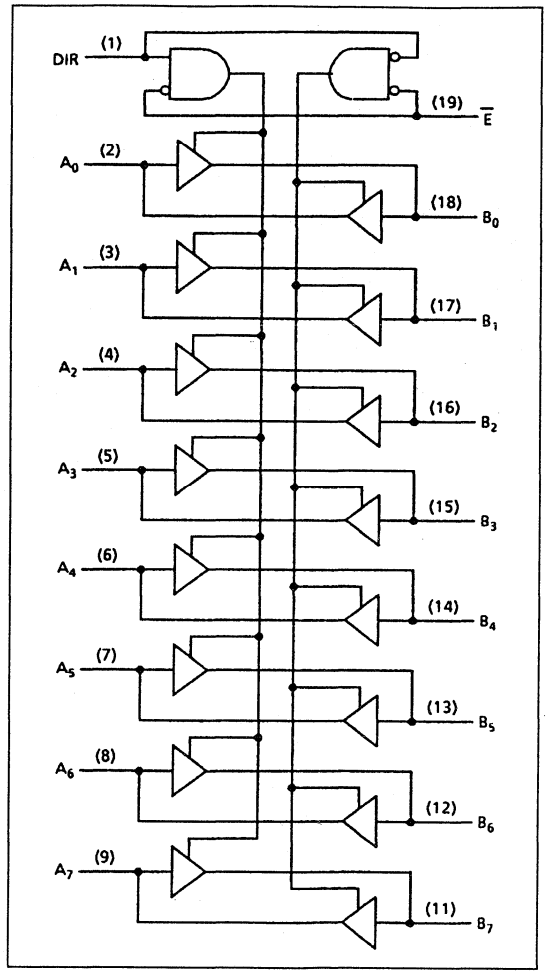


Figure 3: Logic Diagram

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay, low to high level output.	10	19	13	23	ns
t_{PHL}	Propagation delay, high to low level output.	11	19	14	23	ns
t_{PZL}	Propagation delay, enable to low level.	21	26	24	30	ns
t_{PZH}	Propagation delay, enable to high level.	16	25	19	28	ns
t_{PLZ}	Propagation delay, low to disable.	24	28	27	33	ns
t_{PHZ}	Propagation delay, high to disable.	24	28	27	33	ns

Figure 4: Switching Characteristics

54HSC/T245 : Octal Bus Transceiver

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T373 : Octal Transparent Latch, 3-State Outputs

The 54HSC/T373 is an Octal Transparent Latch with 3-State Outputs.

Inputs			Outputs
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

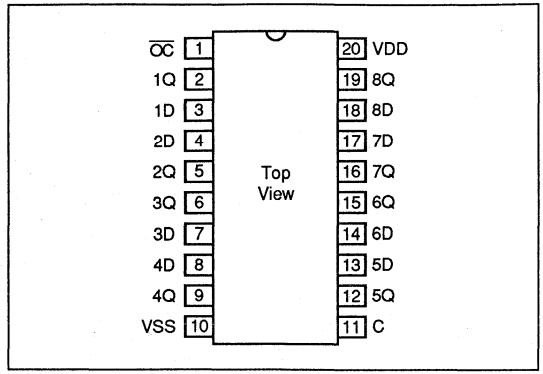


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	15	20	-	20	24	ns
t_{PHL}	Propagation delay. High to low output.	-	14	20	-	21	24	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	25	-	14	25	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	20	-	18	24	ns
t_{PLZ}	Propagation delay. Low to disable.	-	14	25	-	18	25	ns
t_{PHZ}	Propagation delay. High to disable.	-	13	25	-	19	25	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T373 : Octal Transparent Latch, 3-State Outputs

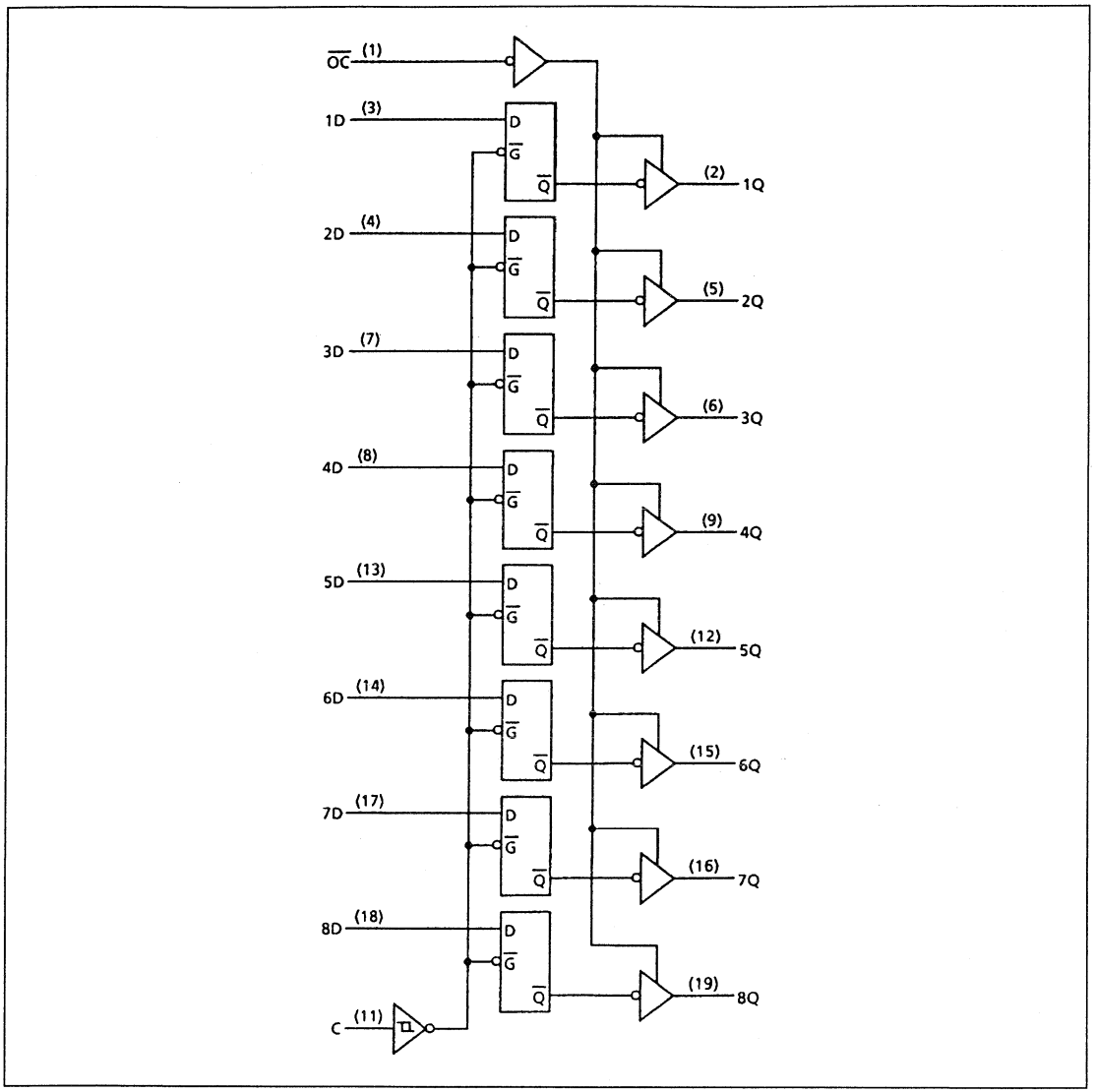


Figure 5: Logic Diagram

54HSC/T573 : Octal Transparent Latch, 3-State Outputs

The 54HSC/T573 is an Octal Transparent Latch with 3-State Outputs.

Inputs			Outputs
$\overline{OC}$	C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level
L = low level
X = irrelevant
Z = high impedance

Figure 1: Function Table

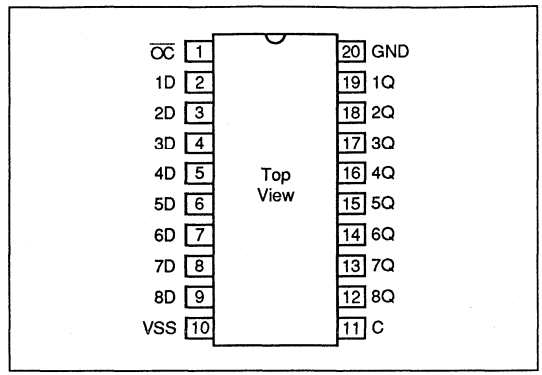


Figure 2: Pin Out

Symbol	Parameter	+25°C			-55°C / +125°C			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Propagation delay. Low to high output.	-	19	24	-	22	29	ns
t_{PHL}	Propagation delay. High to low output.	-	19	24	-	22	29	ns
t_{PZL}	Propagation delay. Enable to low.	-	13	21	-	16	24	ns
t_{PZH}	Propagation delay. Enable to high.	-	16	24	-	19	27	ns
t_{PLZ}	Propagation delay. Low to disable.	-	14	22	-	17	25	ns
t_{PHZ}	Propagation delay. High to disable.	-	13	21	-	16	24	ns

Figure 3: Switching Characteristics

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 4: DC Characteristics

54HSC/T573 : Octal Transparent Latch, 3-State Outputs

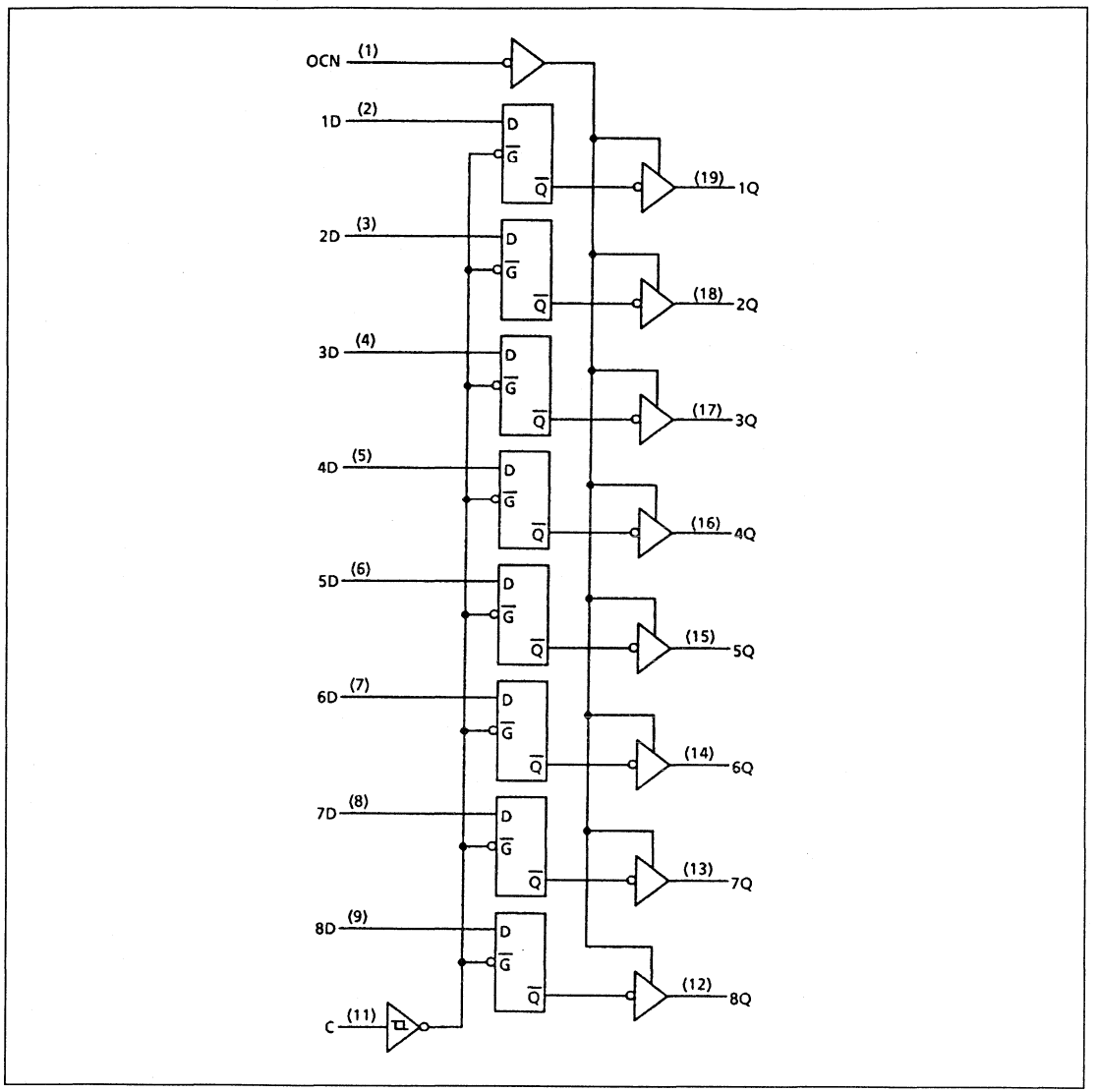


Figure 5: Logic Diagram

54HSC/T670 : 4 x 4 Register Files with Tri-State Outputs

The 54HSC/T670 is a register storing 4 words of 4 bits each. Separate on-chip decoding is provided for addressing the four word locations to either write or retrieve data. This allows simultaneous writing into one location and reading from another location.

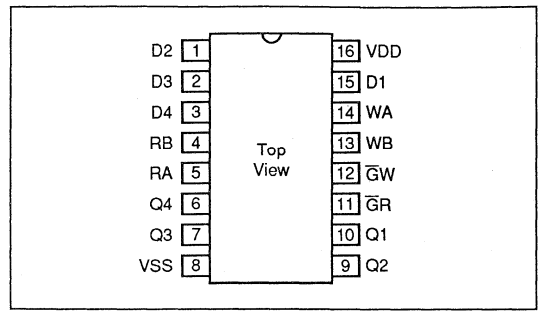


Figure 1: Pin Out

Write Inputs			Word			
WB	WA	$\overline{GW}$	1	2	3	4
L	L	L	Q = D	Q0	Q0	Q0
L	H	L	Q0	Q = D	Q0	Q0
H	L	L	Q0	Q0	Q = D	Q0
H	H	L	Q0	Q0	Q0	Q = D
X	X	H	Q0	Q0	Q0	Q0

Q0 = level of Q before inputs were established
H = high level, L = low level, X = irrelevant

Figure 2: Write Function Table

Read Inputs			Outputs			
WB	WA	$\overline{GW}$	1	2	3	4
L	L	L	W1D1	W1D2	W1D3	W1D4
L	H	L	W2D1	W2D2	W2D3	W2D4
H	L	L	W3D1	W3D2	W3D3	W3D4
H	H	L	W4D1	W4D2	W4D3	W4D4
X	X	H	Z	Z	Z	Z

H = high level, L = low level, X = irrelevant, Z = high impedance

Figure 3: Read Function Table

Symbol	Parameter	+25°C		-55°C / +125°C		Units
		Typ.	Max.	Typ.	Max.	
t_{PLH}	Propagation delay. Read select to Q.	25	30	28	33	ns
t_{PHL}	Propagation delay. Read select to Q.	18	25	21	28	ns
t_{PLH}	Propagation delay. Write enable to Q.	18	25	21	28	ns
t_{PHL}	Propagation delay. Write enable to Q.	18	25	21	28	ns
t_{PLH}	Propagation delay. Data to Q.	27	35	30	38	ns
t_{PHL}	Propagation delay. Data to Q.	23	25	26	28	ns
t_{PZH}	Propagation delay. Read Enable to Q.	18	25	21	28	ns
t_{PZL}	Propagation delay. Read Enable to Q.	18	25	21	28	ns
t_{PHZ}	Propagation delay. Read Enable to Q.	18	25	21	28	ns
t_{PLZ}	Propagation delay. Read Enable to Q.	18	25	21	28	ns

V_{CC} = 5V, T_{MAX} = +125°C, C_L = 50pF

Figure 4: Switching Characteristics

54HSC/T670 : 4 x 4 Register Files with Tri-State Outputs

Symbol	Parameter	Test Conditions	Limits				Units
			+25°C		-55°C / +125°C		
			Min.	Max.	Min.	Max.	
I_{DD}	Quiescent Current	V_{IN} = 0V or V_{DD}	-	20	-	600	µA
V_{OL}	Output Voltage Low Level	I_{OL} = 9mA	-	0.4	-	0.4	V
V_{OH}	Output Voltage High Level	I_{OH} = -11mA	2.5	-	2.5	-	V
V_{IL1}	Voltage Input Low (CMOS)	-	-	1.5	-	1.5	V
V_{IH1}	Voltage Input High (CMOS)	-	3.5	-	3.5	-	V
V_{IL2}	Voltage Input Low (TTL)	-	-	0.8	-	0.8	V
V_{IH2}	Voltage Input High (TTL)	-	2.0	-	2.0	-	V
I_{OZ}	Tri-State Leakage	V_O = 0V or V_{DD}	-	±1	-	±50	µA
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-	±0.5	-	±5.0	µA

Figure 5: DC Characteristics

54HSC/T670 : 4 x 4 Register Files with Tri-State Outputs

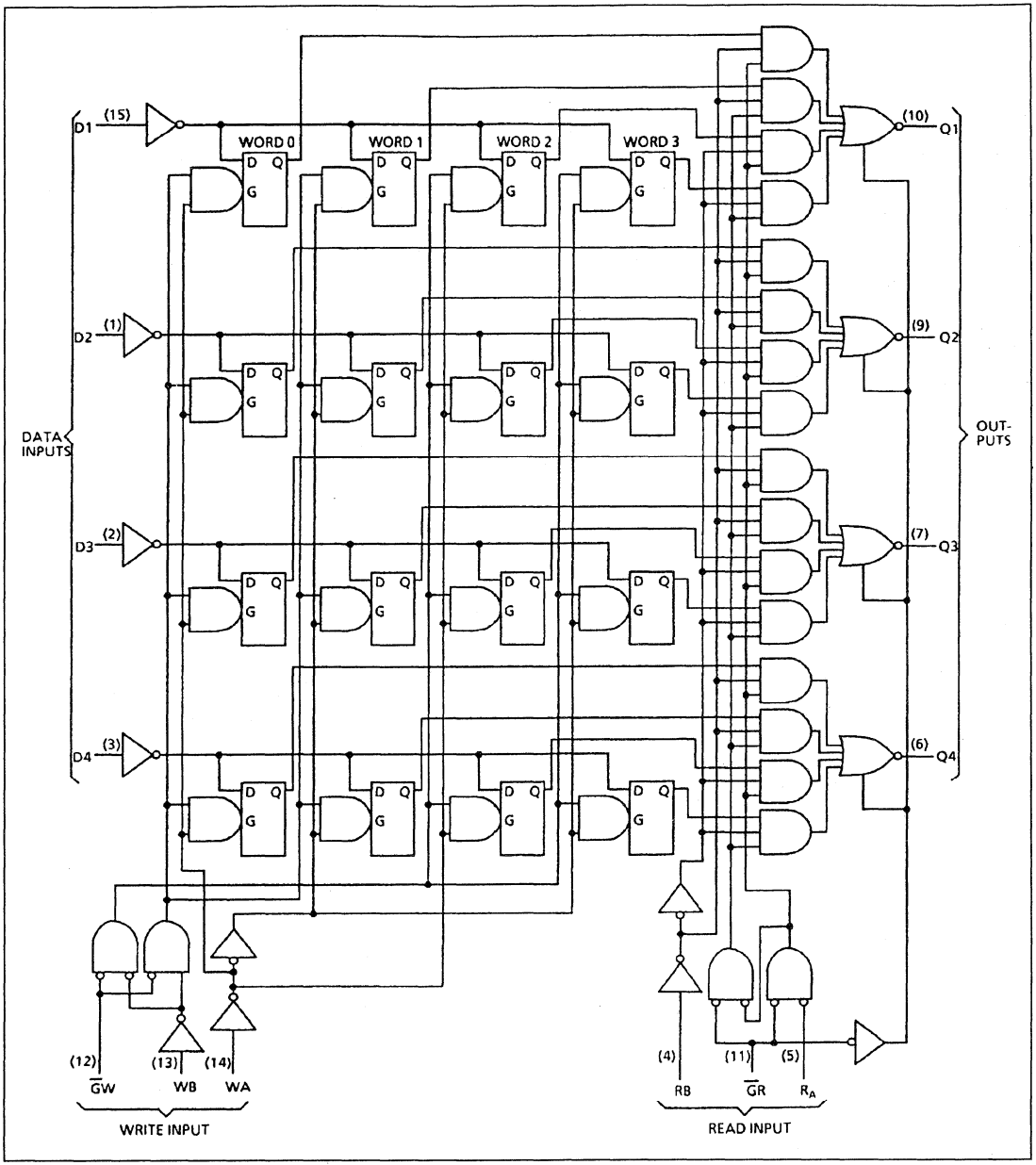


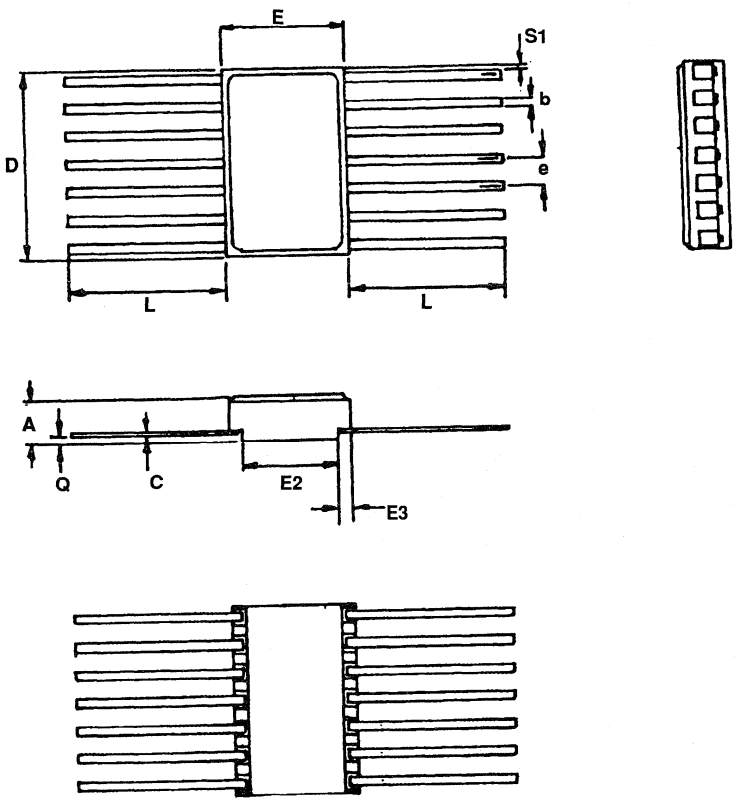
Figure 6: Logic Diagram

CHARACTERISATION DATA

Device base listing as below:

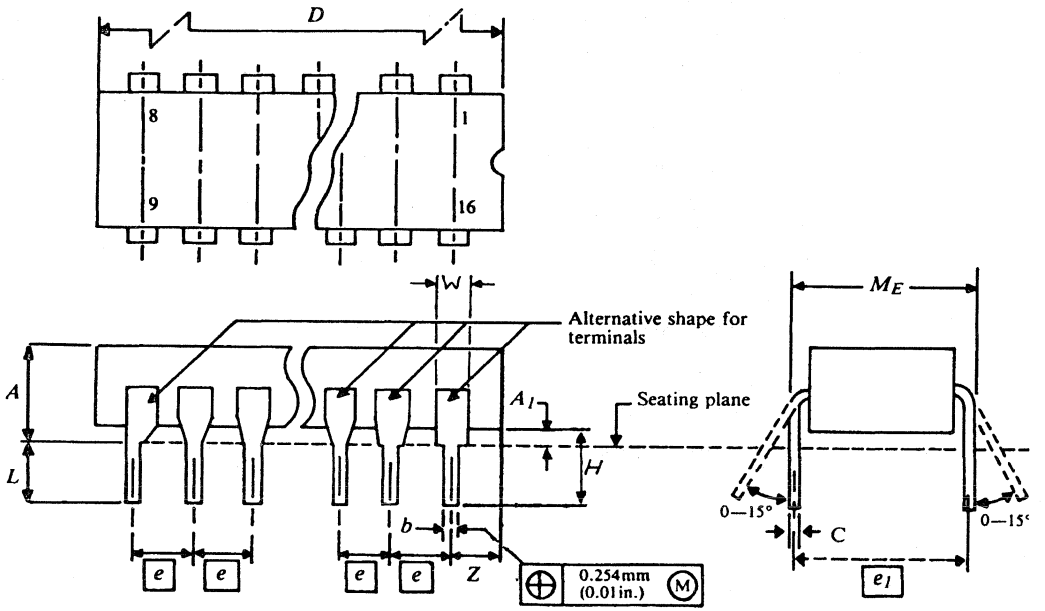
MA9003 Base	Pin Count	MA9007 Base	Pin Count	BMS011 Base	Pin Count
00	14	154	24	138	16
02	14	161	16	139	16
03	14	163	16	238	16
04	14	165	16	240	20
08	14	166	16	241	20
10	14	191	16	244	20
14	14	273	20	245	20
21	14	283	16	373	20
27	14	670	16	374	20
32	14			521	20
74	14			540	20
86	14			541	20
109	16			573	20
125	14			574	20
126	14				
148	16				
151	16				
157	16				
164	14				
253	16				

LI/AS/4/IN/02001 - 14 LEAD BOTTOMBRAZE FLATPACK (MIL-38510H)



	INCHES		
REF	MAX	NOM	MIN
A	0.105		
b	0.019		0.015
c	0.006		0.004
D	0.347		0.333
E	0.260		0.250
E2		0.175	
e		0.050	
L	0.305		0.270
Q			0.026
S1			0.005

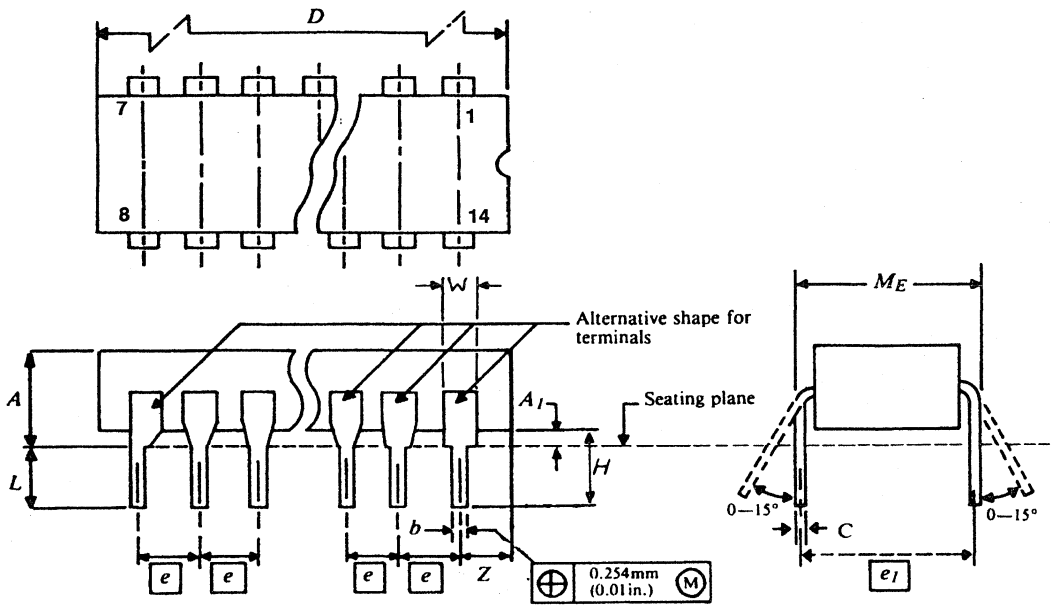
FINISHED PRODUCT OUTLINE



DIMENSION A INCLUDES ANY LID

Ref.	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.60			0.220
A_1	0.38		1.53	0.015		0.060
b	0.35		0.59	0.014		0.023
c	0.20		0.36	0.008		0.014
D			20.58			0.810
e		2.54TP			0.100TP	
e_1		7.62TP			0.300TP	
H	4.45		5.38	0.175		0.212
M_E			8.30			0.326
Z			1.27			0.050
W			1.53			0.060

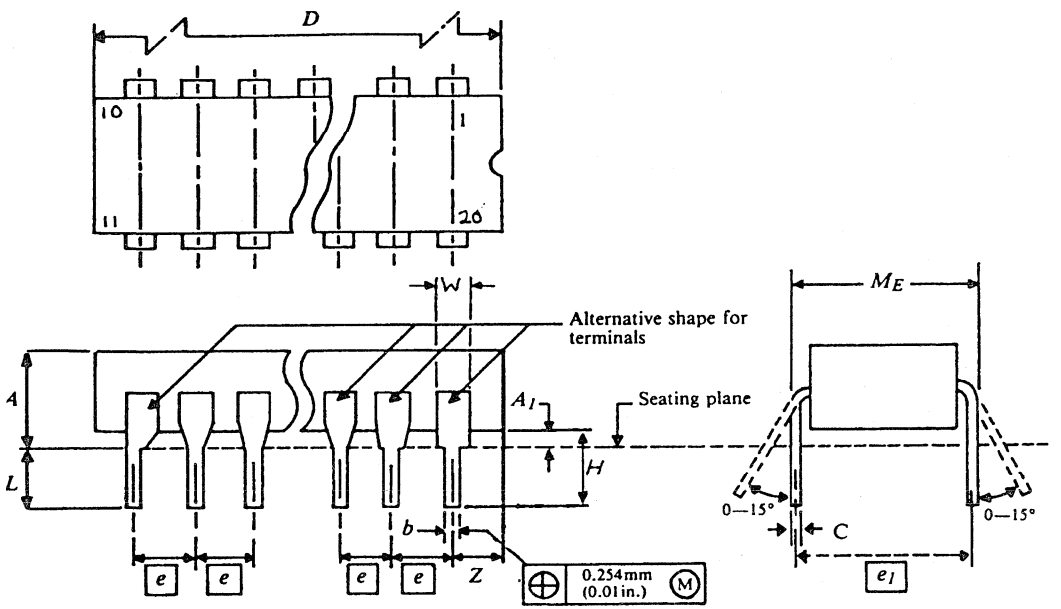
FINISHED PRODUCT OUTLINE



DIMENSION A INCLUDES ANY LID

Ref.	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.60			0.220
A_1	0.38		1.53	0.015		0.060
b	0.35		0.59	0.014		0.023
c	0.20		0.36	0.008		0.014
D			18.04			0.710
e		2.54TP			0.100TP	
e_1		7.26TP			0.300TP	
H	4.45		5.38	0.175		0.212
M_E			8.30			0.326
Z			1.27			0.050
W			1.53			0.060

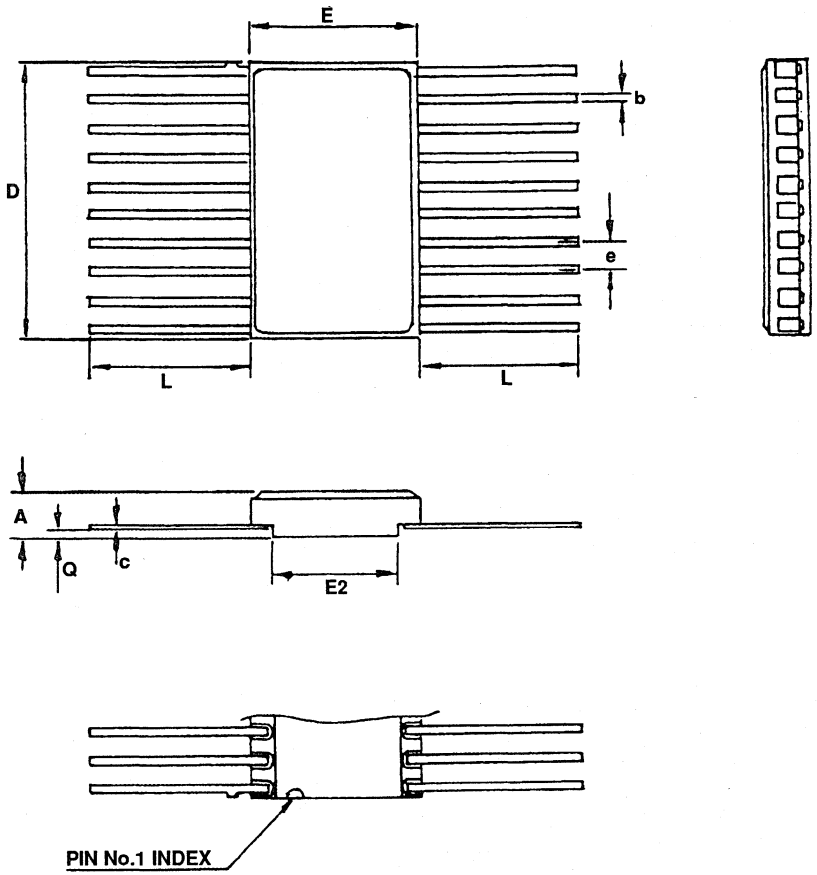
FINISHED PRODUCT OUTLINE



DIMENSION A INCLUDES ANY LID

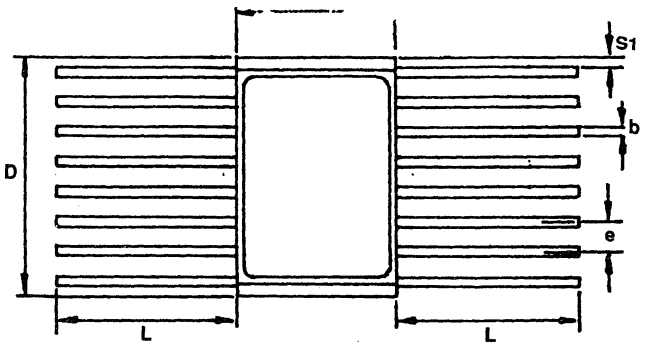
Ref.	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			5.60			0.220
A1	0.38		1.53	0.015		0.060
b	0.35		0.59	0.014		0.023
c	0.20		0.36	0.008		0.014
D			25.65			1.010
e		2.54TP			0.100TP	
e1		7.62TP			0.300TP	
H	4.71		5.38	0.185		0.212
ME			8.30			0.326
Z			1.27			0.050
W			1.53			0.060

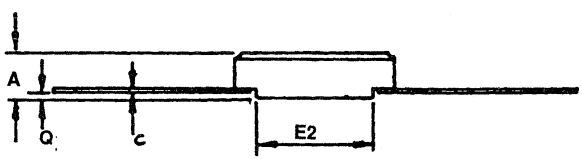
XG 527 - 20 LEAD BOTTOMBRAZE FLATPACK (MIL-STD-38510H)

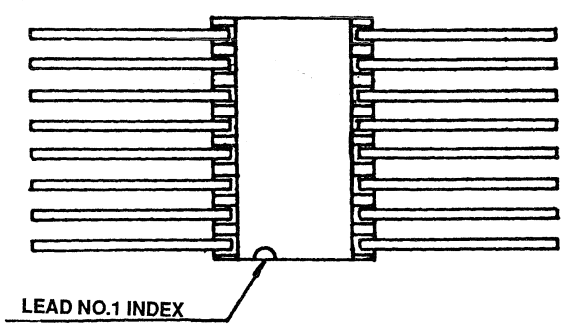


REF.	INCHES		
	MAX	NOM	MIN
A	0.106		-
b	0.019		0.015
c	0.007		0.003
D	0.490		0.470
E	0.303		0.287
E2	0.221		0.209
e	-	0.050	-
L	0.305		0.250
Q	-	-	0.026

16 LEAD BOTTOMBRAZE FLATPACK (MIL-M-38510H)



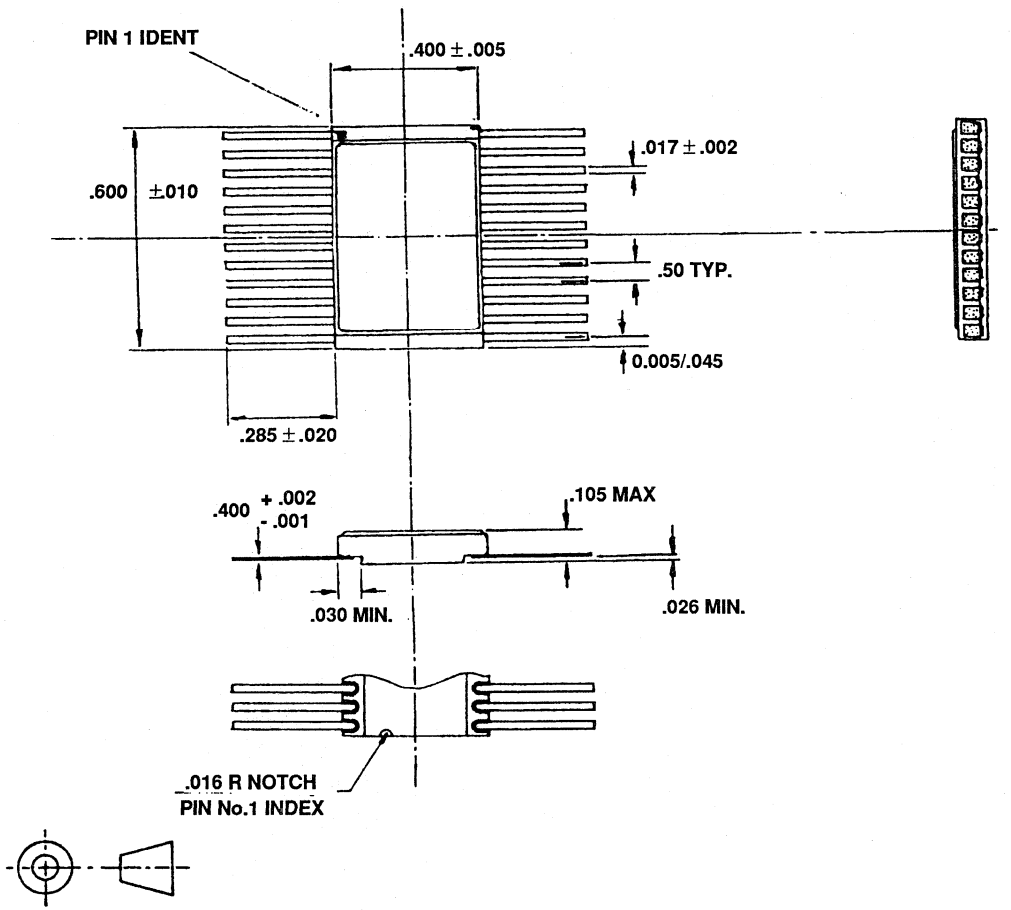




REF	INCHES		
	MAX	NOM	MIN
A	0.103		
b	0.019		0.015
c	0.006		0.004
D	0.408		0.392
E	0.276		0.264
E2	0.196		0.184
e		0.050	
L	0.305		0.250
Q			0.026
S1			0.005

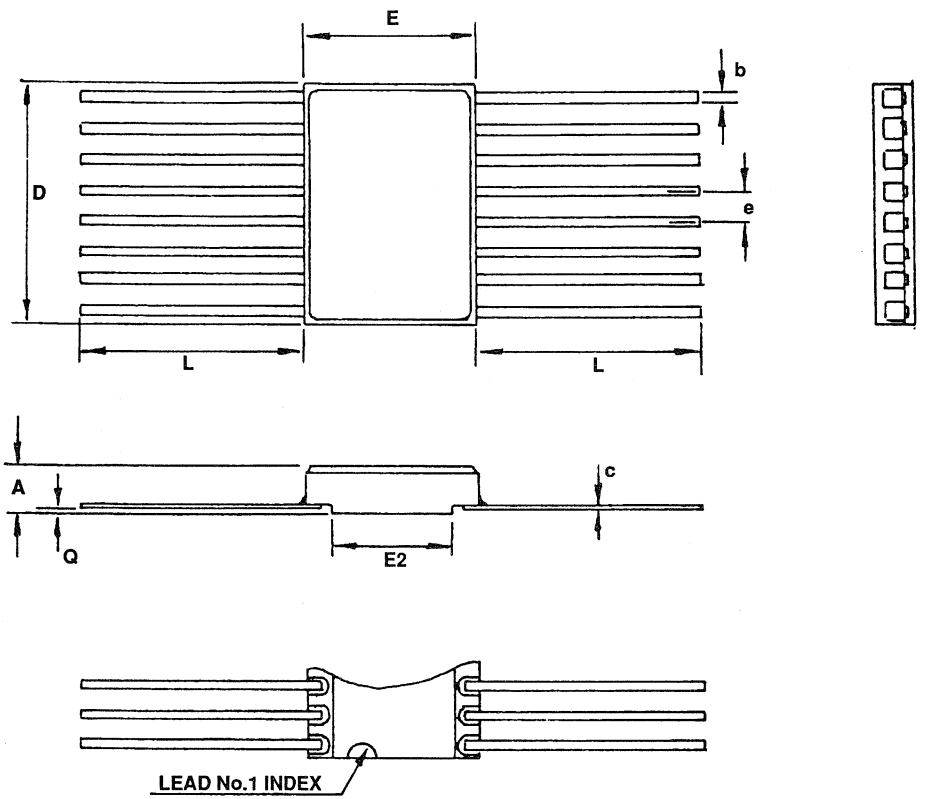
FINISHED PRODUCT OUTLINE FOR 24 LEAD CERAMIC FLATPACK (MIL-M-38510)

GPS STOCK NO - S318380



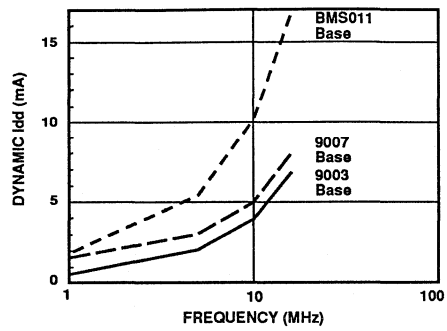
FINISHED PRODUCT OUTLINE FOR A 16 LEAD FLATPACK

(MIL-M-38510H)

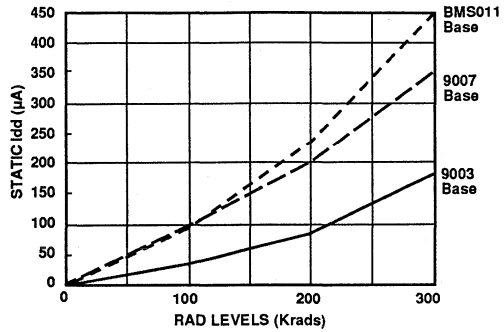


REFERENCE	INCHES		
	MAXIMUM	NOMINAL	MINIMUM
A	0.101		
b	0.019		0.015
c	0.007		0.004
D	0.418		0.402
E	0.275		0.265
E2	0.196		0.184
e		0.050	
L	0.305		0.250
Q	0.045		0.026

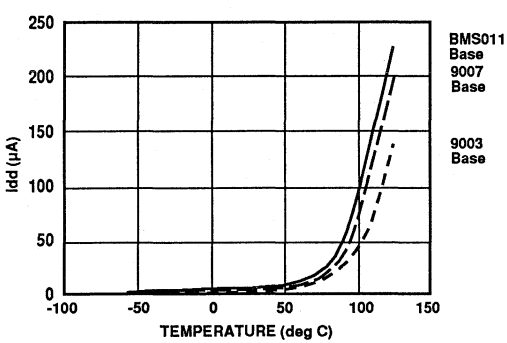
DYNAMIC Idd for OCTAL DEVICE BASES



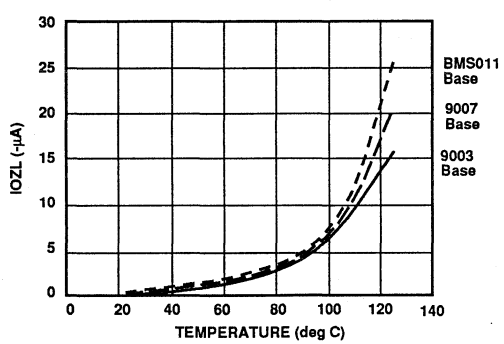
STATIC Idd Vs RADIATION



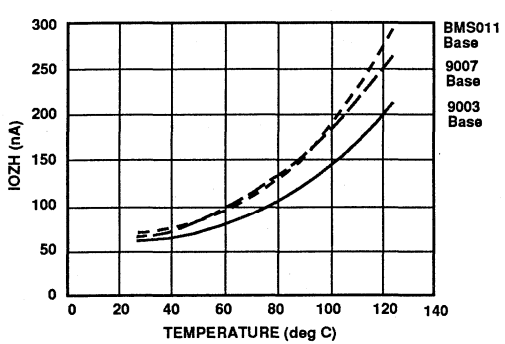
STATIC Idd Vs TEMP.



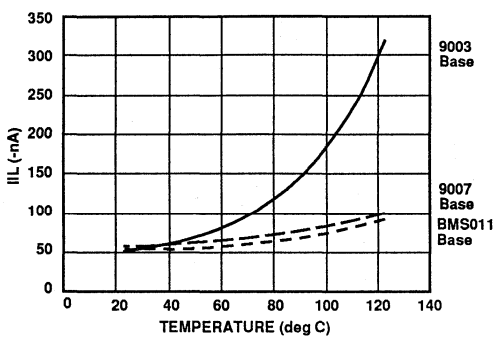
IOZL Vs TEMP.

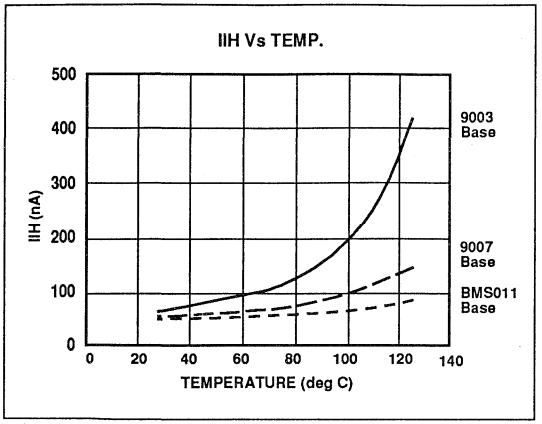


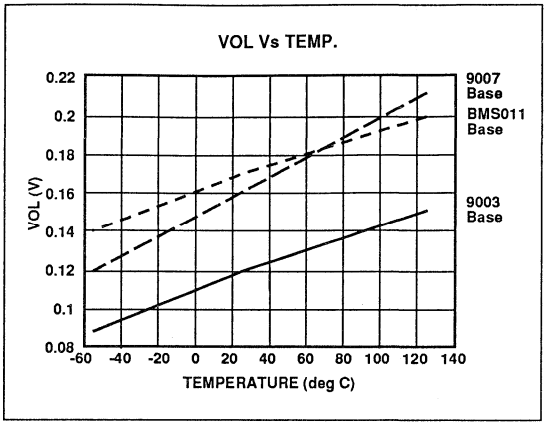
IOZH Vs TEMP.

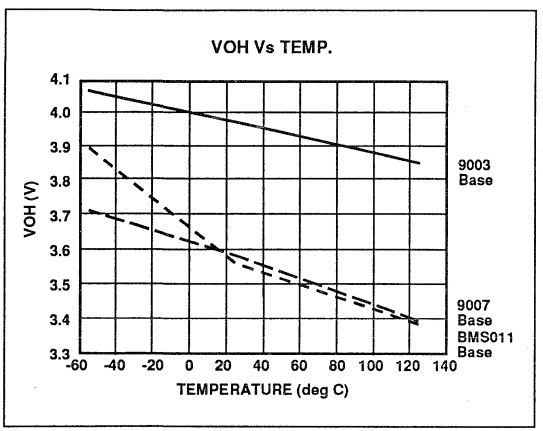


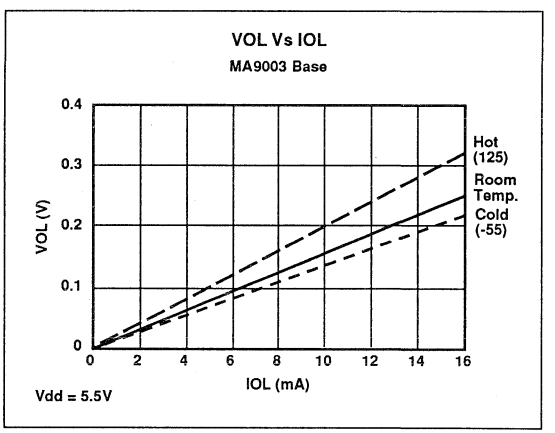
IIL Vs TEMP.

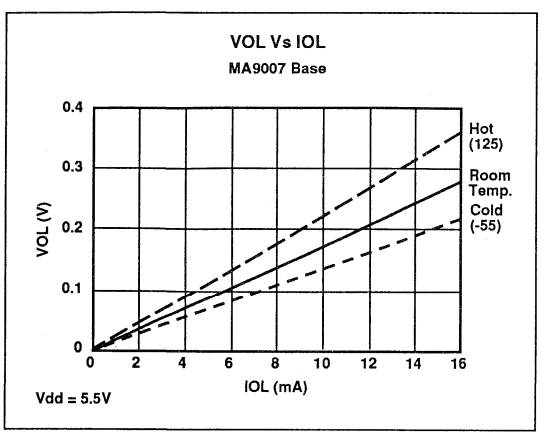


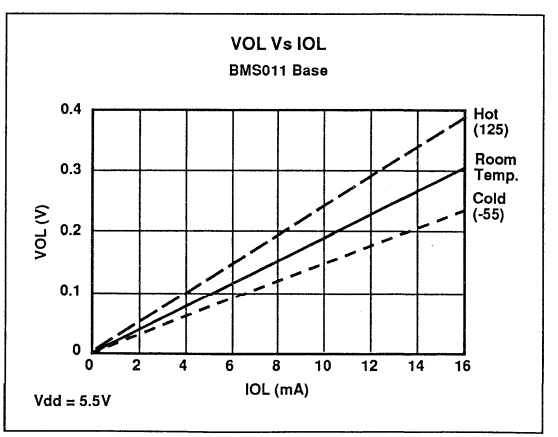

IIH Vs TEMP.
IIH (nA)
500
400
300
200
100
0
0 20 40 60 80 100 120 140
TEMPERATURE (deg C)
9003 Base
9007 Base
BMS011 Base

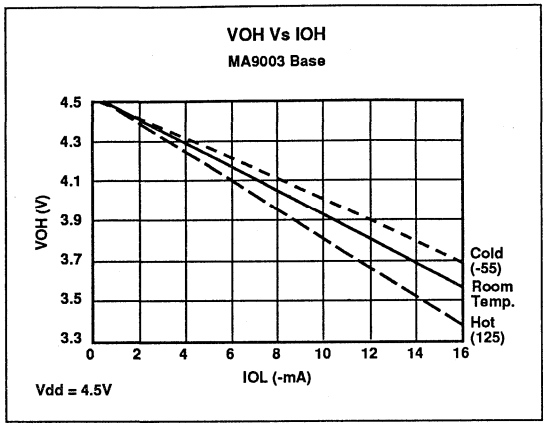

VOL Vs TEMP.
VOL (V)
0.22
0.2
0.18
0.16
0.14
0.12
0.1
0.08
-60 -40 -20 0 20 40 60 80 100 120 140
TEMPERATURE (deg C)
9007 Base
BMS011 Base
9003 Base

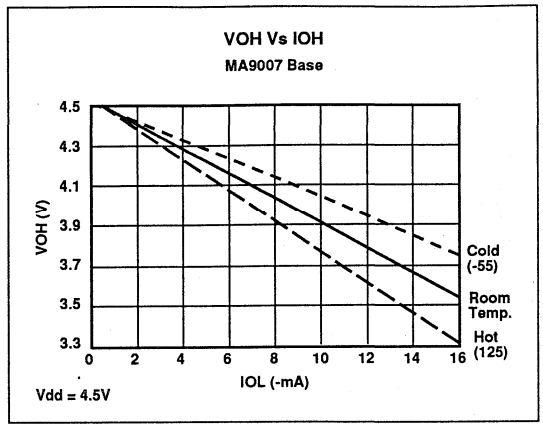

VOH Vs TEMP.
VOH (V)
4.1
4.0
3.9
3.8
3.7
3.6
3.5
3.4
3.3
-60 -40 -20 0 20 40 60 80 100 120 140
TEMPERATURE (deg C)
9003 Base
9007 Base
BMS011 Base

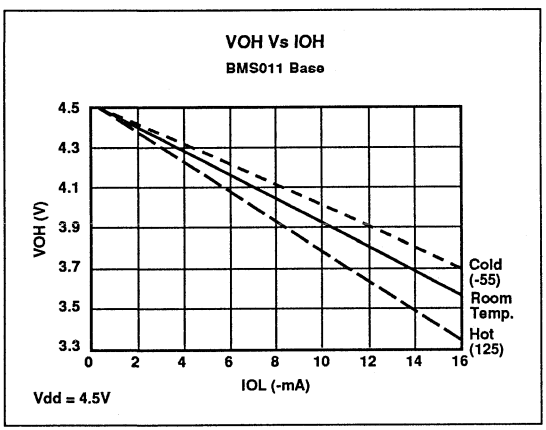

VOL Vs IOL
MA9003 Base
VOL (V)
0.4
0.3
0.2
0.1
0
0 2 4 6 8 10 12 14 16
IOL (mA)
Vdd = 5.5V
Hot (125)
Room Temp.
Cold (-55)

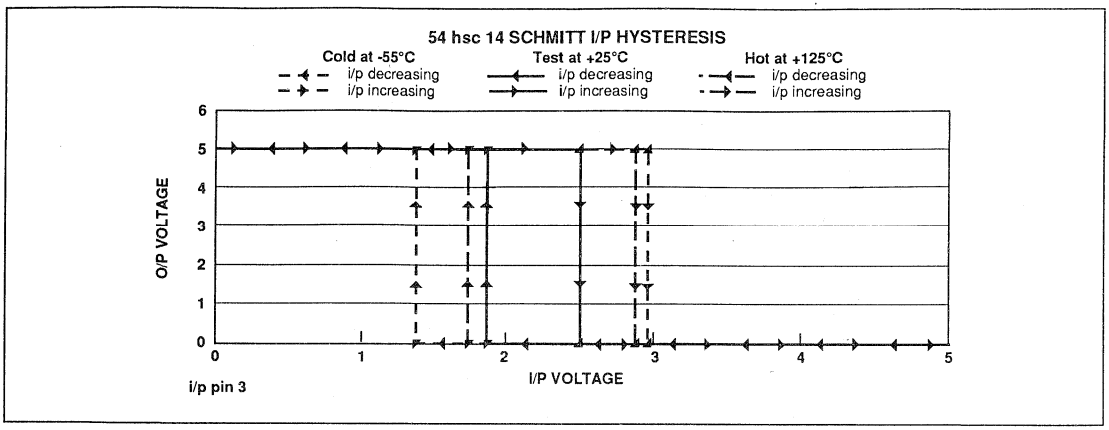

VOL Vs IOL
MA9007 Base
VOL (V)
0.4
0.3
0.2
0.1
0
0 2 4 6 8 10 12 14 16
IOL (mA)
Vdd = 5.5V
Hot (125)
Room Temp.
Cold (-55)

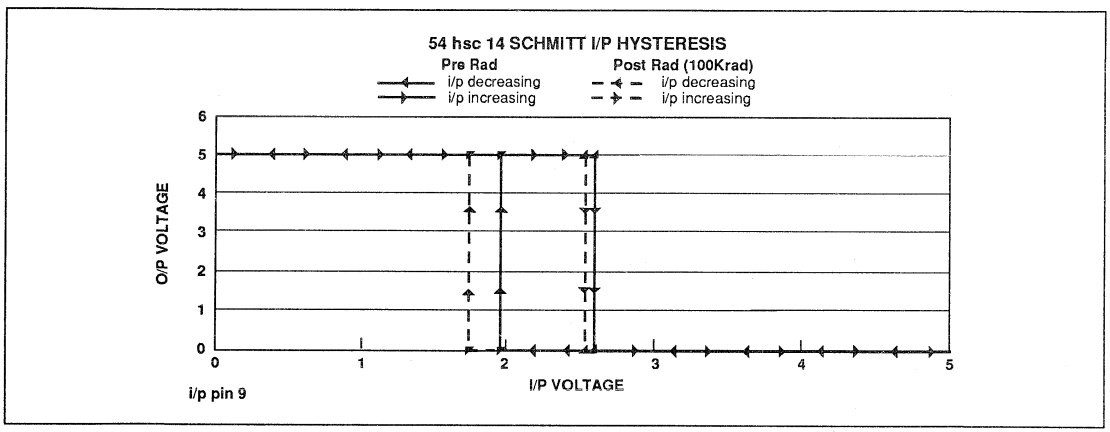

VOL Vs IOL
BMS011 Base
VOL (V)
0.4
0.3
0.2
0.1
0
0 2 4 6 8 10 12 14 16
IOL (mA)
Vdd = 5.5V
Hot (125)
Room Temp.
Cold (-55)


VOH Vs IOH
MA9003 Base
VOH (V)
4.5
4.3
4.1
3.9
3.7
3.5
3.3
0
2
4
6
8
10
12
14
16
IOL (-mA)
Cold (-55)
Room Temp.
Hot (125)
Vdd = 4.5V


VOH Vs IOH
MA9007 Base
VOH (V)
4.5
4.3
4.1
3.9
3.7
3.5
3.3
0
2
4
6
8
10
12
14
16
IOL (-mA)
Cold (-55)
Room Temp.
Hot (125)
Vdd = 4.5V


VOH Vs IOH
BMS011 Base
VOH (V)
4.5
4.3
4.1
3.9
3.7
3.5
3.3
0
2
4
6
8
10
12
14
16
IOL (-mA)
Cold (-55)
Room Temp.
Hot (125)
Vdd = 4.5V


54 hsc 14 SCHMITT I/P HYSTERESIS
Cold at -55°C
i/p decreasing
i/p increasing
Test at +25°C
i/p decreasing
i/p increasing
Hot at +125°C
i/p decreasing
i/p increasing
O/P VOLTAGE
I/P VOLTAGE
i/p pin 3


54 hsc 14 SCHMITT I/P HYSTERESIS
Pre Rad
i/p decreasing
i/p increasing
Post Rad (100Krad)
i/p decreasing
i/p increasing
O/P VOLTAGE
I/P VOLTAGE
i/p pin 9

TIMING DIAGRAMS

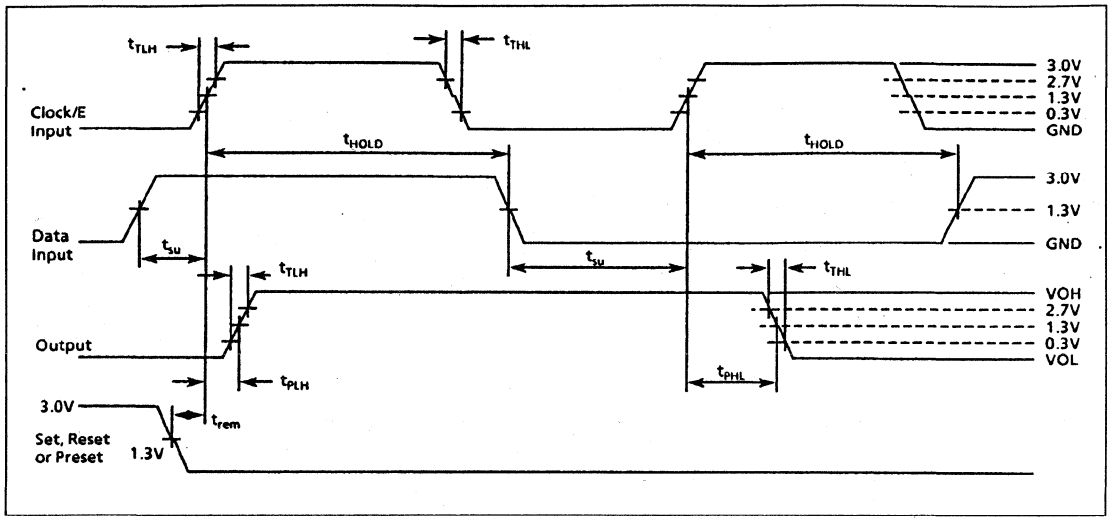


Figure 3: Set-Up Times, Hold Times, Removal Time and Propagation Delay Times

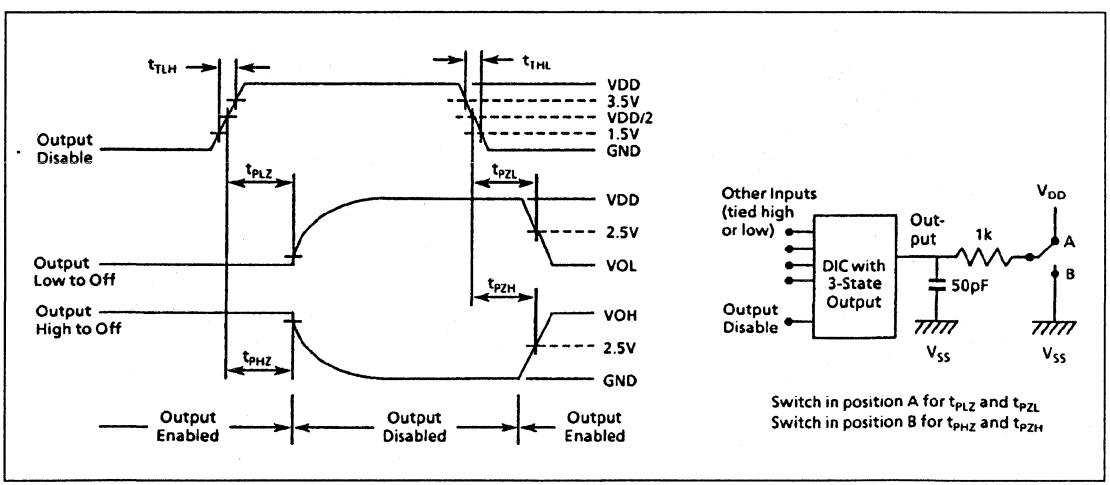


Figure 4: Three-State Propagation Delay Wave Shapes and Test Circuit

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with MIL-STD-883 test method 1019, Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$1x10^{11}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 5: Radiation Hardness Parameters

ORDERING INFORMATION

Unique Circuit Designator

54xHSC139xxxxx
54xHST139xxxxx

Radiation Tolerance

'Blank'	No tolerance implied
S	Radiation Hard Processing
R	100 kRads (Si) Guaranteed
Q	300 kRads (Si) Guaranteed
H	1000 kRads (Si) Guaranteed*

* HSC Only

Package Type

C	Ceramic DIL (Solder Seal)
F	Flatpack (Solder Seal)
L	Leadless Chip Carrier
N	Naked Die

QA/QCI Process
(See Section 9 Part 4)

Test Process
(See Section 9 Part 3)

Assembly Process
(See Section 9 Part 2)

Reliability Level

L	Rel 0
C	Rel 1
D	Rel 2
E	Rel 3/4/5/STACK
B	Class B
S	Class S

For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3595-3.4

54HSC/T630

RADIATION HARD 16-BIT PARALLEL ERROR DETECTION & CORRECTION

The 54HSC/T630 is a 16-bit parallel Error Detection and Correction circuit. It uses a modified Hamming code to generate a 6-bit check word from each 16-bit data word. The check word is stored with the data word during a memory write cycle. During a memory read cycle a 22-bit word is taken from memory and checked for errors.

Single bit errors in data words are flagged and corrected. Single bit errors in check words are flagged but not corrected. The position of the incorrect bit is pinpointed, in both cases, by the 6-bit error syndrome code which is output during the error correction cycle.

Two bit errors are flagged but not corrected. Any combination of two bit errors occurring within the 22-bit word read from memory, (ie two errors in the 16-bit data word, two bits in the 16-bit check word or one error in each) will be correctly identified.

The gross errors of all bits, low or high, will be detected.

The control signals S1 and S0 select the function to be performed by the EDAC They control the generation of check words and the latching and correction of data (see table 1) When errors are detected, flags are placed on outputs SEF and DEF (see table 2).

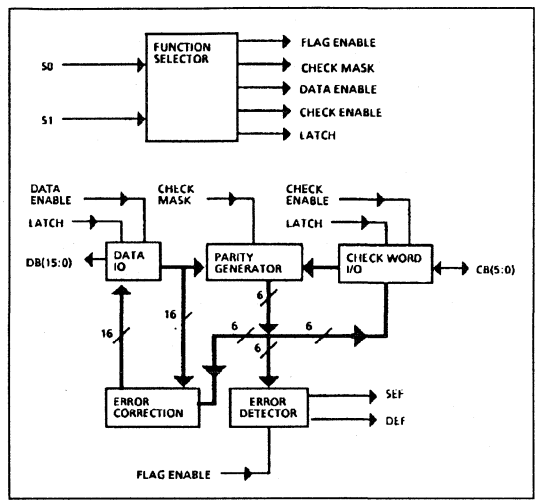


Figure 1: Block Diagram

FEATURES

- Radiation Hard:
  Dose Rate Upset Exceeding $3x10^{10}$ Rad(Si)/sec
  Total Dose for Functionality Upto $1x10^{6}$ Rad(Si)
- High SEU Immunity, Latch Up Free
- CMOS-SOS Technology
- All Inputs and Outputs Fully TTL Compatible (54HST630) or CMOS Compatible (54HSC630)
- Low Power
- Detects and Corrects Single-Bit Errors
- Detects and Flags Dual-Bit Errors
- High Speed:
  Write Cycle - Generates Checkword In 40ns Typical
  Read Cycle - Flags Errors In 20ns Typical

Cycle	Control		EDAC Function	Data UO	Checkword	Error Flags	
	S1	S0				SEF	DEF
WRITE	Low	Low	Generates Checkword	Input Data	Output Checkword	Low	Low
READ	Low	High	Read Data BCheckword	Input Data	Input Checkword	Low	Low
READ	High	High	Latch & Flag Error	Latch Data	Latch Checkword	Enabled	Enabled
READ	High	Low	Correct Data Word & Generate Syndrome Bits	Output Corrected Data	Output Syndrome Bits	Enabled	Enabled

Table 1: Control Functions

Total Number of Errors		Error Flags		Data Correction
16-bit Data	6-bit Checkword	SEF	DEF	
0	0	Low	Low	Not Applicable
1	0	High	Low	Correctlon
0	1	High	Low	Correction
1	1	High	High	Interrupt
2	0	High	High	Interrupt
0	2	High	High	Interrupt

Table 2: Error Functions

ERROR DETECTION & CORRECTION

During a memory write cycle, six check bits (CBO-CB5) are generated by eight-input parity generators using the data bits defined in Table 3. During a memory read cycle, the 6-bit checkword is retrieved along with the actual data.

Error detection is accomplished as the 6-bit checkword and the 16-bit data word from memory are applied to internal parity generators/checkers. If the parity of all six groupings of data and check bits are correct, it is assumed that no error has occurred and both error flags will be low. It should be noted that the sense of two of the check bits, bits CBO and CB1, is inverted to ensure that the gross-error condition of all lows and all highs is detected.

If the parity of one or more of the check groups is incorrect, an error has occurred and the proper error flag or flags will be set high. Any single error in the 16bit data word will change the sense of exactly three bits of the 6-bit checkword. Any single error in the 6bit checkword changes the sense of only that one bit. In either case, the single error flag will be set high while the dual error flag will remain low.

Any two-bit error will change the sense of an even number of check bits. The two-bit error is not correctable since the parity tree can only identify singlebit errors. Both error flags are set high when any two-bit error is detected.

Three or more simultaneous bit errors cause the EDAC to transmit that no error, a correctable error, or an uncorrectable error has occurred and hence produce erroneous results in all three cases.

Error correction is accomplished by identifying the bad bit and inverting it. Identification of the erroneous bit is achieved by comparing the 16-bit word and 6-bit checkword from memory with the new checkword with one (checkword error) or three (data word error) inverted bits.

As the corrected word is made available on the data word I/O port, the checkword I/O port presents a 6-bit syndrome error code. This syndrome code can be used to identify the corrupted bit in memory (see Table 4. overleaf).

Checkword Bit	16-bit Data Word															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CB0	X	X		X	X				X	X	X			X		
CB1	X		X	X		X	X		X			X			X	
CB2		X	X		X	X		X		X			X			X
CB3	X	X	X				X	X			X	X	X			
CB4				X	X	X	X	X						X	X	X
CB5									X	X	X	X	X	X	X	X

The six check bits are partly bits derived from the matrix of data bits as indicated by 'X' for each bit.

Table 3: Check Word Generation

Syndrome Error Code	Error Location																					
	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	DB8	DB9	DB10	DB11	DB12	DB13	DB14	DB15	CB0	CB1	CB2	CB3	CB4	CB5	No Error
CB0	L	L	H	L	L	H	H	H	L	L	L	H	H	L	H	H	L	H	H	H	H	H	H
CB1	L	H	L	L	H	L	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H	H
CB2	H	L	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	H	L	H	H	H	H
CB3	L	L	L	H	H	H	L	L	H	H	L	L	L	H	H	H	H	H	H	L	H	H	H
CB4	H	H	H	L	L	L	L	L	H	H	H	H	H	L	L	L	H	H	H	H	L	H	H
CB5	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	H	H	H	H	H	L	H

Table 4: Error Syndrome Codes

APPLICATIONS

Although many semiconductor memories have separate input and output pins, it is possible to design the error detection and correction function using a single EDAC. EDAC data and check bit pins function as inputs or outputs dependent upon the state of control signals S0 and S1. It becomes necessary to use wired AND logic, with fairly complex timing system, to control the EDAC and data bus. This scheme becomes difficult to implement both in terms of board layout and timing. System performance is also adversely affected, See Figure 2.

Optimised systems can be implemented using two EDAC's in parallel, One of the units is used strictly as an encoder during the memory write cycle. Both controls S0 and SI are grounded, The encoder chip will generate the 6-bit check word for memory storage along with the 16-bit data.

The second of the two EDAC's will be used as a decoder during the memory read cycle. This decoder chip requires timing pulses for correct operation. Control S1 is set low and S0 high as the memory read cycle begins. After the memory output data is valid, the control S1 input is moved from the low to a high. This low-to-high transition latches the 22-bit word from memory into internal registers of this second EDAC and enables the two error flags. If no error occurs, the CPU can accept the 16-bit word directly from memory. If a single error has occurred, the CPU must move the control SO input from the high to a low to output corrected data and the error syndrome bits. Any dual error should be an interrupt condition.

In most applications, status registers will be used to keep tabs on error flags and error syndrome bits. If repeated patterns of error flags and syndrome bits occur, the CPU will be able to recognize these symptoms as a "hard" error. The syndrome bits can be used to pinpoint the faulty memory chip, See Figure 3.

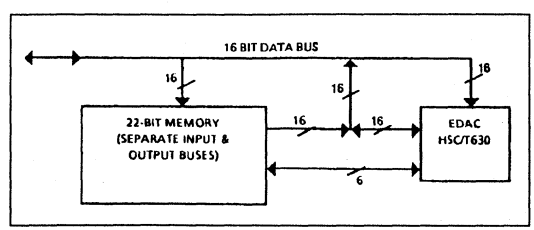
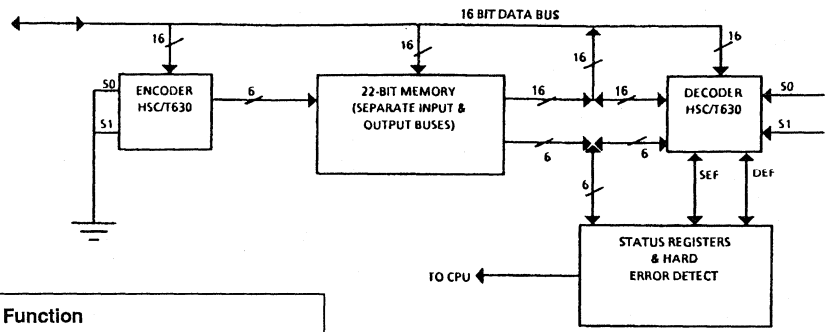


Figure 2: Error Detection and Correction Using a Single EDAC Unit



S1	S0	Function
L	H	Start READ
H	H	Latch data & flag errors
H	L	Correct data & Output syndrome bits

Figure 3: Error Detection and Correction Using Two EDAC Units

DEFINITION OF SUBGROUPS

Subgroup	Definition
1	Static characteristics specified in Table 6 at +25°C
2	Static characteristics specified in Table 6 at +125°C
3	Static characteristics specified in Table 6 at -55°C
9	Switching characteristics specified in Table 7 at +25°C
10	Switching characteristics specified in Table 7 at +125°C
11	Switching characteristics specified in Table 7 at -55°C

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Table 5: Absolute Maximum Ratings

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Total dose radiation not exceeding $3x10^5$ Rad(Si)			Units
			Min	Typ	Max	
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL Input High Voltage	-	2.0	-	-	V
V_{IL1}	TTL Input Low Voltage	-	-	-	0.8	V
V_{iH2}	CMOS Input High Voltage	-	3.5	-	-	V
V_{IL2}	CMOS Input Low Voltage	-	-	-	1.5	V
V_{OH1}	TTL Output High Voltage	I_{OH} = -4mA	2.4	-	-	V
V_{OL1}	TTL Output Low Voltage	I_{OL} = 12mA (CB or DB), I_{OL} = 4mA (SEF or DEF)	-	-	0.4	V
V_{OH2}	CMOS Output High Voltage	I_{OH} = -4mA	V_{DD}-0.5	-	-	V
V_{OL2}	CMOS Output Low Voltage	I_{OL} = 12mA (CB or DB), I_{OL} = 4mA (SEF or DEF)	-	-	0.5	V
I_{1L}	Input Low Current	V_{DD} = 5.5, V_{IN} = V_{SS}	-	-	-10	µA
I_{1H}	Input High Current	V_{DD} = 5.5, V_{IN} = V_{DD}	-	-	50	µA
I_{2L}	IO Low Current	V_{DD} = 5.5, V_{IN} = V_{SS}	-	-	-50	µA
I_{2H}	IO High Current	V_{DD} = 5.5, V_{IN} = V_{DD}	-	-	50	µA
I_{DD}	Power Supply Current	V_{DD} = Max, S0 & S1 at 5.5V, All CB & DB pins grounded, DEF & SEF open	-	-	1	mA

V_{DD} = 5V±10%, over full operating temperature range.
Mil-Std-883, method 5005, subgroups 1, 2, 3
Parameters at higher radiation levels available on request.

Table 6: Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

Parameter	From (Input)	To (Output)	Min.	Max.	Units	Conditions (HST)	Conditions (HSC)
t_{PLH} Propogation delay time, low-to-high-level output (Note 4)	DB	CB	-	58	ns	S0 = 0V, S1 = 0V	S0 = 0V, S1 = 0V
t_{PLH} Propogation delay time, low-to-high-level output (Note 4)	DB	CB	-	58	ns	S0 = 0V, S1 = 0V	S0 = 0V, S1 = 0V
t_{PLH} Propogation delay time, low-to-high-level output (Note 5)	S1 ⇑	DEF	-	29	ns	S0 = 3V	S0 = V_{DD}-1V
t_{PLH} Propogation delay time, low-to-high-level output (Note 5)	S1 ⇑	SEF	-	29	ns	S0 = 3V	S0 = V_{DD}-1V
t_{PZH} Output enable time to high level (Note 6)	S0 ⇓	CB, DB	-	40	ns	S1 = 3V (fig. 5)	S1 = V_{DD}-1V (fig. 5)
t_{PZL} Output enable time to low level (Note 6)	S0 ⇓	CB, DB	-	45	ns	S1 = 3V (fig. 4)	S1 = V_{DD}-1V (fig. 4)
t_{PHZ} Output disable time to high level (Note 7)	S0 ⇑	CB, DB	-	45	ns	S1 = 3V (fig. 5)	S1 = V_{DD}-1V (fig. 5)
t_{PLZ} Output disable time to low level (Note 7)	S0 ⇑	CB, DB	-	65	ns	S1 = 3V (fig. 4)	S1 = V_{DD}-1V (fig. 4)
t_S Set-up time to S1 ›	CB, DB	-	30	-	ns	-	-
t_H Hold time after S1 ›	CB, DB	-	15	-	ns	-	-

1. V_{DD} = 5V ±10% and CL = 50pF, over full operating temperature and total dose = 300K Rad(Si)
2. Input Pulse V_{SS} to 3.0 Volts.(TTL), V_{DD} -1V (CMOS).
3. Times Measurement Reference Level 1.5 Volts.
4. These parameters describe the time intervals taken to generate the check word during the memory write cycle.
5. These parameters describe the time intervals taken to flag errors during memory read cycle.
6. These parameters describe the time intervals taken to correct and output the data word and to generate and output the syndrome error code during the memory read cycle.
7. These parameters describe the time intervals taken to disable the CB & DB buses in preparation for a new data word during the memory read cycle.
8. Mil-Std-883, method 5005, subgroups 9, 10, 11
9. Parameters at higher radiation levels available on request.

Table 7: AC Electrical Characteristics

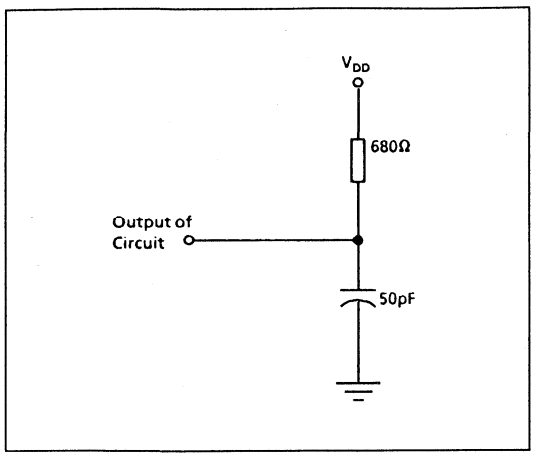


Figure 4: Output Load Circuit

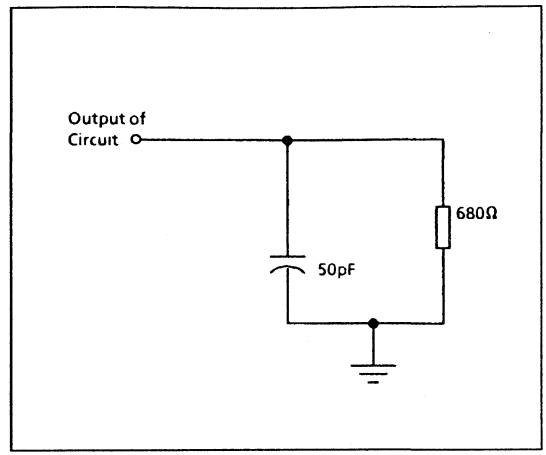


Figure 5: Output Load Circuit

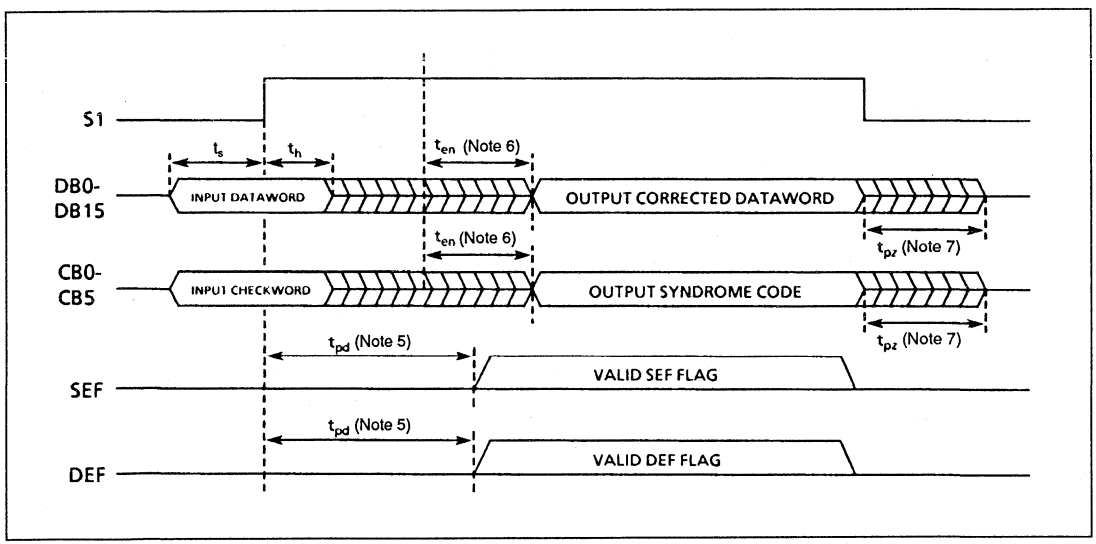


Figure 6: Read, Flag and Correct, Made Switching Waveforms

PIN ASSIGNMENTS

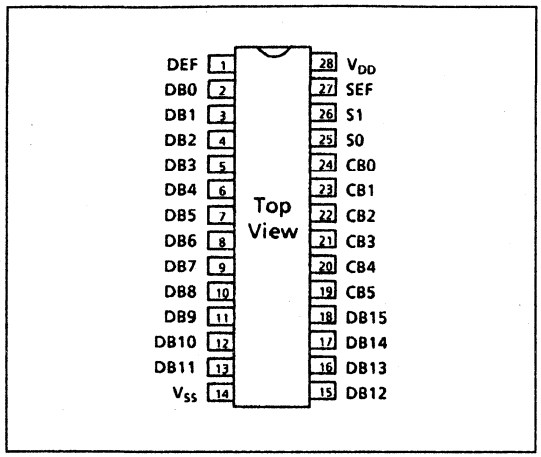


Figure 7: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

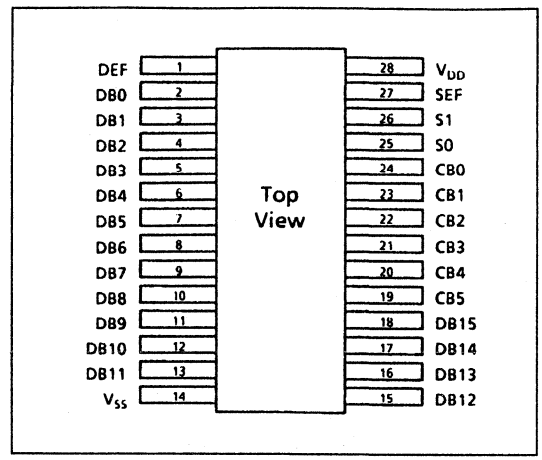


Figure 8: 28-Lead Flatpack (Solder Seal) - Package Style F

PACKAGE OUTLINES

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.715	-	-	0.225
A1	0.38	-	1.53	0.015	-	0.060
b	0.35	-	0.59	0.014	-	0.023
c	0.20	-	0.36	0.008	-	0.014
D	-	-	36.02	-	-	1.418
e	-	2.54 Typ.	-	-	0.100 Typ.	-
e1	-	15.24 Typ.	-	-	0.600 Typ.	-
H	4.71	-	5.38	0.185	-	0.212
Me	-	-	15.90	-	-	0.626
Z	-	-	1.27	-	-	0.050
W	-	-	1.53	-	-	0.060

XG404

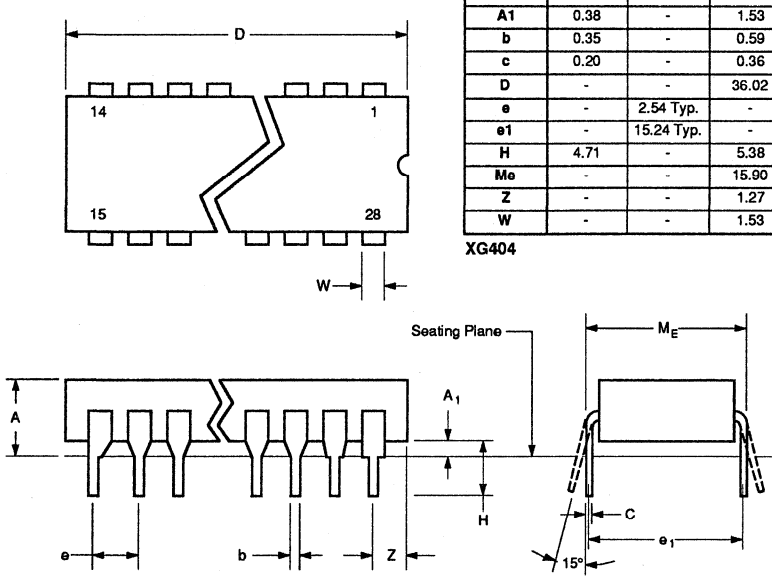


Figure 9: 28-Lead Ceramic DIL (Solder Seal) - Package Style C

Ref	Millimetres			Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	2.97	-	-	0.117
b	0.38	-	0.48	0.015	-	0.019
c	0.076	-	0.152	0.003	-	0.006
D	18.08	-	18.49	0.712	-	0.728
E	12.50	-	12.90	0.492	-	0.508
E2	9.45	-	9.85	0.372	-	0.388
e	1.14	-	1.40	0.045	-	0.055
L	8.00	-	9.27	0.315	-	0.365
Q	0.66	-	-	0.026	-	-
S	-	-	1.14	-	-	0.045

XG543

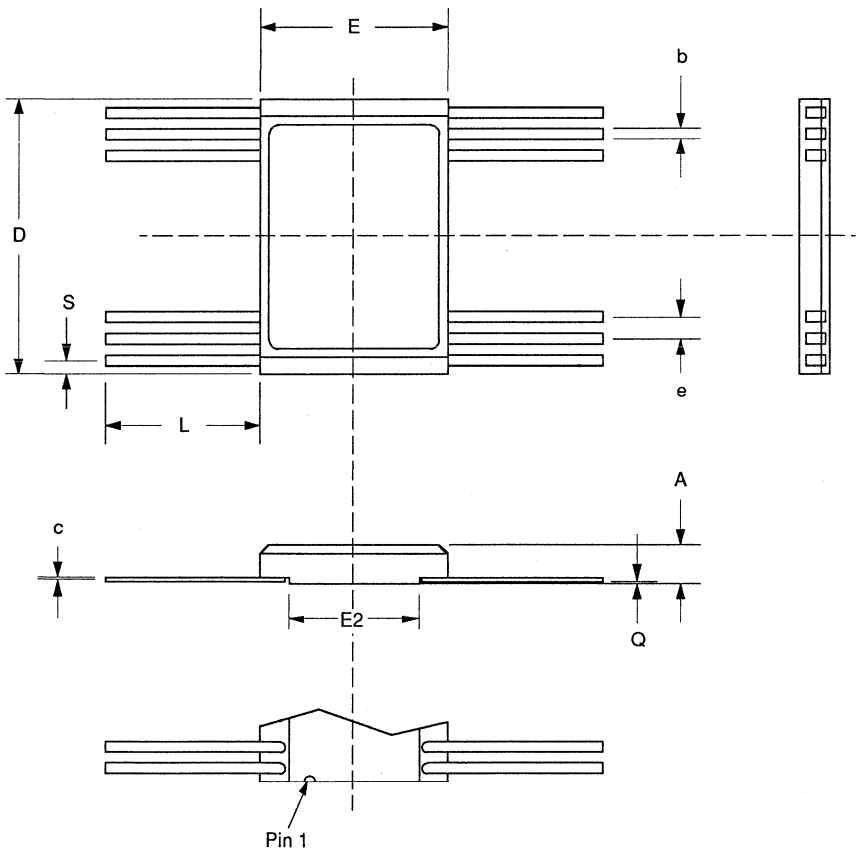


Figure 10: 28-Lead Ceramic Flatpack (Solder Seal) - Package Style F

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

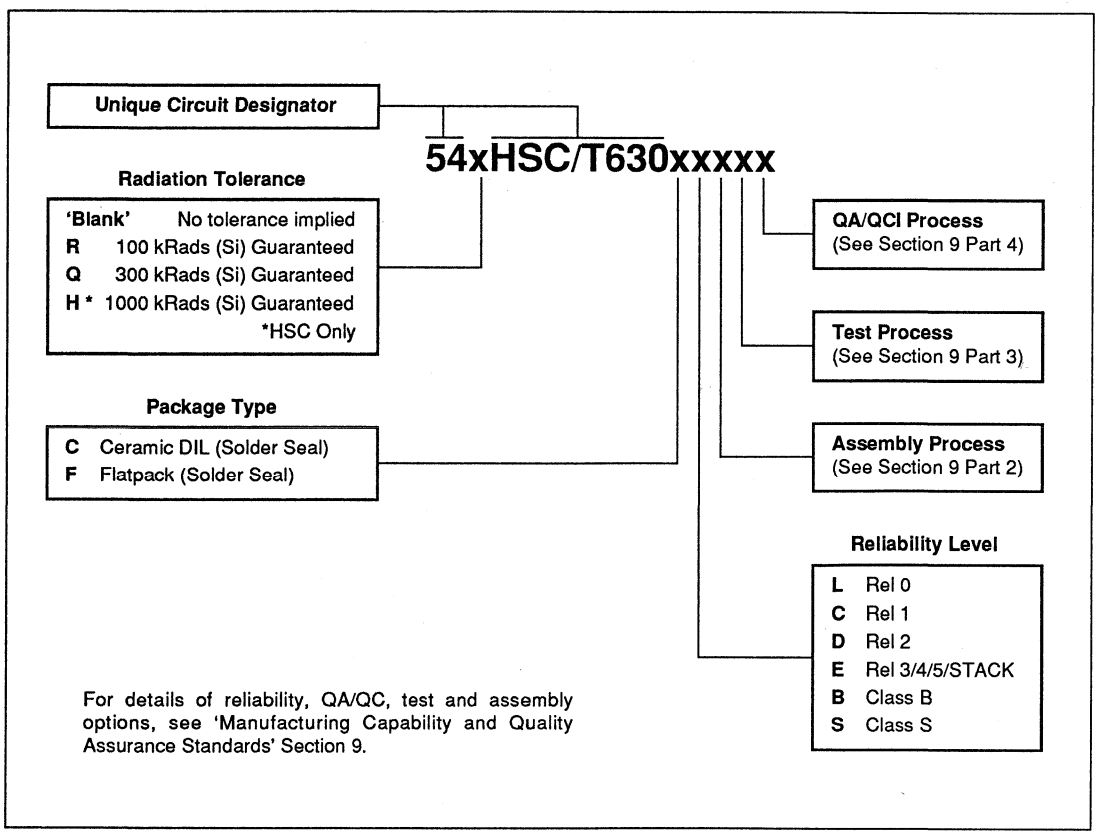
Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Figure 11: Radiation Hardness Parameters

ORDERING INFORMATION



Section 7

Semicustom ASICs & Foundry Service

MA9000A Sea of Gates

RADIATION HARD ADVANCED GATE ARRAY DESIGN SYSTEM

The logic building block is a cell-unit, equivalent in size to a two input NAND gate. Back-to-back cell units form the core of the array.

The interconnection patterns that cause groups of cell-units to become defined logic cells, and the models which are used to simulate these cells, are stored as software in libraries. Cells up to the complexity of multiple bit shift registers are treated in this way.

Schematic capture and simulation is performed using Mentor Graphics and Dazix libraries, provided by GPS. Post simulation activities are performed by GPS.

For details of VHDL and synthesis integration into the design route, please contact your local Field Applications Engineer.

The MA9000A Sea Of Gates product is enhanced by the GPS Structured Array. The Structured Array makes use of well characterised MA9000A core and peripheral cells and allows the insertion of hard macros that improve the performance of the resultant ASIC in any given application.

For example RAM and ROM cells can quickly and economically be generated via a compiler route and dropped into the Structured Array core. ASICs developed in this way offer optimum area, power and radiation performance: features essential in radiation hard applications.

Circuits with special i/o requirements can easily be accommodated on the Structured Array and using the drop-in macros performance can be tailored for high speed or low power consumption.

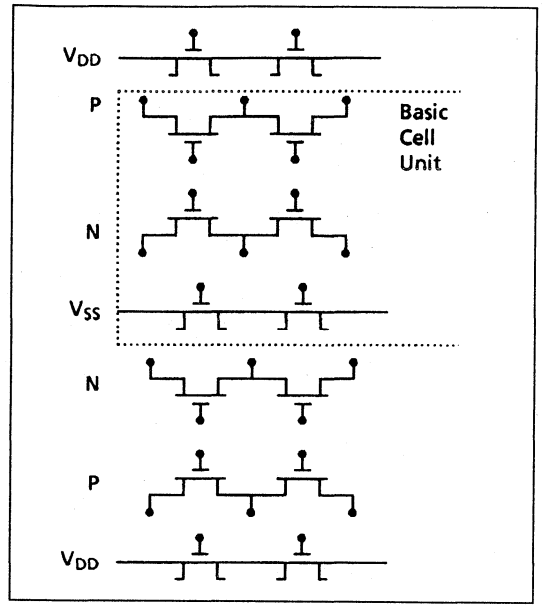


Figure 1: Basic Cell Unit

FEATURES

- Channelless Array Architecture
- Typical Gate Delay 1nS - Toggle Rates of 100MHz Achievable
- 1.25µW/MHz Power Dissipation Per Active Gate
- Extensive CAD Design and Support System
- Comprehensive Library of Logic Cells and Logic Function Building Macros, with RAM and ROM
- Double-Level-Metal CMOS/SOS Technology
- High SEU Immunity, Latch-Up Free
- Radiation Hard to 1MRad(Si)

ARRAY OPTIONS

Array Type	Cell Units	Bonding Pads		
		I/O	Power	Total
MA9140	14112	102	8	110
MA9200	20296	120	8	128
MA9300	29500	142	8	150
MA9400	37000	160	8	168
MA9500	50148	184	8	192
MA9600	60168	200	8	208

Any I/O site may be configured as a power pad to give flexible bonding options.

CHARACTERISITICS & RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification. is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 1: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	V
V_{IH2}	CMOS input high voltage	-	80	-	-	%V_{DD}
V_{IL2}	CMOS input low voltage	-	-	-	20	%V_{DD}
V_{OH1}	TTL output high voltage	I_{OH} = -2mA	2.4	-	-	V
V_{OL1}	TTL output low voltage	I_{OL} = 5mA	-	-	0.4	V
V_{OH2}	CMOS output high voltage	I_{OH} = -4mA	90	-	-	%V_{DD}
V_{OL2}	CMOS output low voltage	I_{OL} = 4mA	-	-	10	%V_{DD}
I_L	Input leakage current	-	-	-	10	µA
I_{OZ}	Output leakage current	Tristate Output	-	-	30	µA
I_{DD}	Static power supply current	-	-	0.5	*	mA

V_{DD} = 5V ±10%, over full operating temperature. Mil-Std-883, method 5005, subgroups 1, 2, 3

* Dependent on array type.

Table 2: Electrical Characteristics

AC CHARACTERISTICS

Cell Name	Function	O/P Edge	Inherent Delay	Per 1pF Load*	Units
NOP	Push/Pull Output Buffer	Rising	3.3	0.2	ns
		Falling	3.2	0.2	
NAND2	2 Input NAND	Rising	0.7	5.0	ns
		Falling	0.5	4.8	
DT	D Type	Rising CK - QB	2.7	8.9	ns
		Falling CK - QB	3.0	4.8	
		Data Set-up time	3.1	-	
		Data Hold time	1.9	-	

* 1pF is equivalent to fanout of 5 standard gates. Mil-Std-883, method 5005, subgroups 9, 10, 11

Table 3: Electrical Characteristics

Subgroup	Definition
1	Static characteristics specified in Table 2 at +25°C
2	Static characteristics specified in Table 2 at +125°C
3	Static characteristics specified in Table 2 at -55°C
7	Functional characteristics specified at +25°C
8A	Functional characteristics specified at +125°C
8B	Functional characteristics specified at -55°C
9	Switching characteristics specified in Table 3 at +25°C
10	Switching characteristics specified in Table 3 at +125°C
11	Switching characteristics specified in Table 3 at -55°C

Table 4: Definition of Subgroups

PROPAGATION DELAY

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 50% of those listed.

Use the following normalised graphs to predict delays at any other working temperature or voltage:

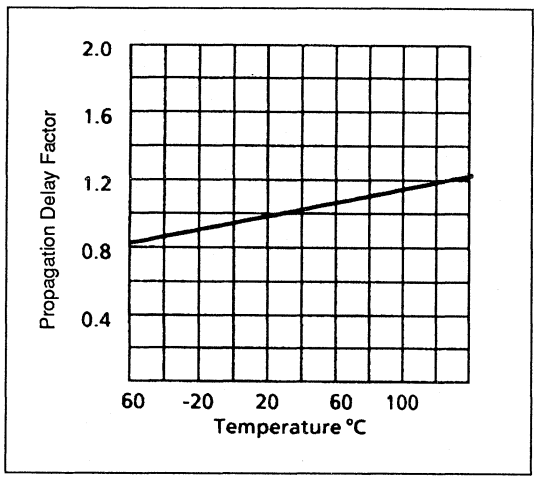


Figure 2: Propogation Delay vs Temperature

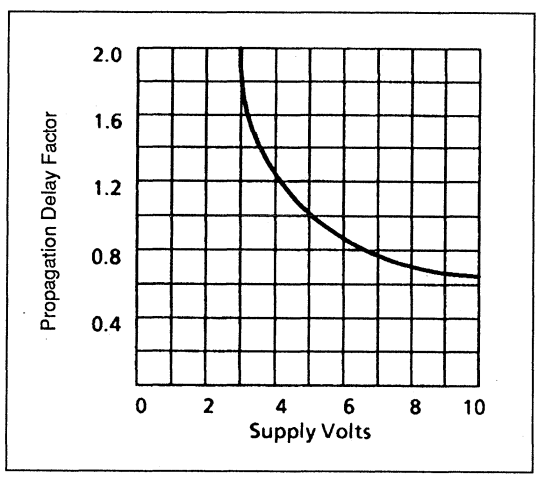


Figure 3: Propogation Delay vs Supply Voltage

STANDARD PACKAGE OPTIONS

GPS offer a wide range of packages as standard. Other package styles are available. If you require a package not covered on this list, contact GPS.

Ceramic DIL	24	28	40	48	64	-
Cerdip	24	28	40	48	-	-
Leaded Flatpack	28	42	48	64	84	132
Pin Grid Array	68	84	100	120	144	-
Ceramic LCC	(40)	44	(48)	68	84	-
Cerquad	44	68	84	-	-	-

Table 5: Standard Package Options

DEVELOPMENT INTERFACES

All design activities prior to mask creation, including automatic layout may be carried out by the equipment manufacturer, and may be delegated to a GPS design centre.

GPS offers schematic capture and simulation support for Mentor Graphics and Dazix CAD environments.

DAZIX is a trademark of Intergraph UK
MENTOR is a trademark of Mentor Graphics Corporation

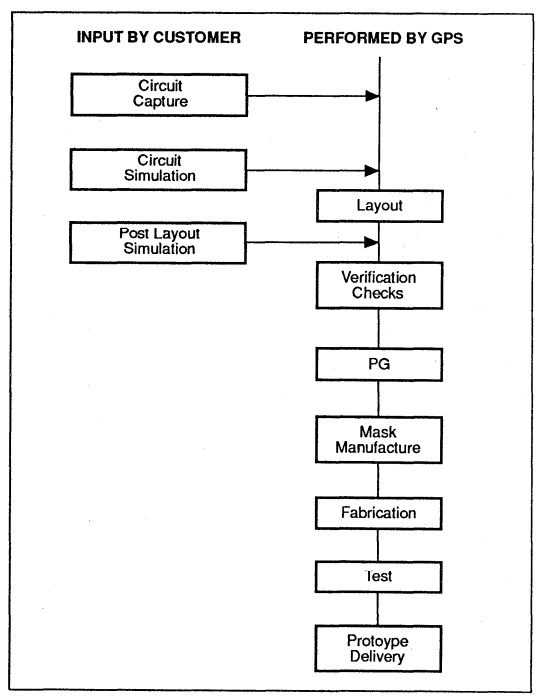


Figure 4: Development Interfaces

RADIATION TOLERANCE

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GPS can provide radiation testing compliant with MIL-STD-883 test method 1019 Ionizing Radiation (Total Dose).

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-11}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 5: Radiation Hardness Parameters

MACRO DESIGN SERVICE

Marconi offer a flexible macro design service to support customer requirements for non-standard cells. Listed are examples of some customer specified Macros that have been designed.

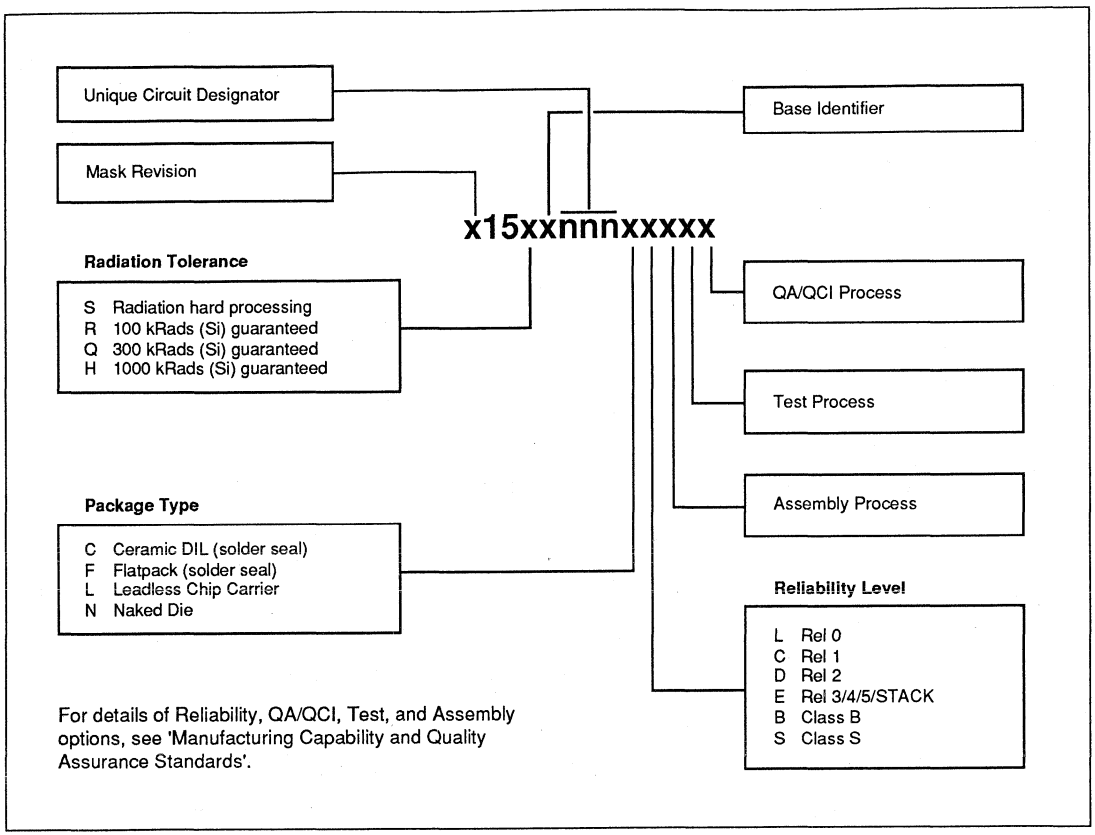
- MA29xx bit slice series elements.
- ALU
- Asynchronous counters
- Parity detectors
- Ripple carry adders
- Selectors
- Gray counters
- Johnson counters
- Lookahead adders

The MA9000A Sea of Gates is a particularly effective route for creating RAM macros. For more information on Macros and additions to the family contact our nearest office.

Cell Name	Function	Cell Units
COMBINATIONAL GATES		
INV	Inverter	1
INVB	Fast inverter	1
INVC	Super fast inverter	2
BUFF	Non-inverting buffer	1
BUFFB	Fast non-inverting buffer	2
BUFFC	Super fast non-inverting buffer	3
NAND2	2 input NAND	1
NAND2B	Fast 2 input NAND	2
NAND3	3 input NAND	2
NAND4	4 input NAND	2
AND2	2 input AND	2
AND3	3 input AND	2
AND4	4 input AND	3
NOR2	2 input NOR	1
NOR2B	Fast 2 input NOR	2
NOR3	3 input NOR	2
NOR4	4 input NOR	2
OR2	2 input OR	2
OR3	3 inputOR	2
OR4	4 input OR	3
ANDNOR	2 + 2 input AND/NOR	2
ORNAND	2 + 2 OR/NAND	2
EXNOR	Exclusive NOR	4
EXOR	Exclusive OR	4
SEL1NV	Select 1 of 2 (inverting)	4
SEL2	Select 1 of 2	4
SEL41NV	4 bit data selector (inverting)	8
SEL4	4 bit data selector	8
ARITHMETIC		
HAD	Half adder	4
FAD	Fulladder	8
FLAD	Fast look ahead adder	6
LAH2	2 bit look ahead unit	12
LAH3	3 bit look ahead unit	16
LAH4	4 bit look ahead unit	25
SIMPLE LATCHES		
NASR	NAND set reset-latch	3
NOSR	NOR set-reset latch	3
CLOCKED LATCHES		
DL	D-latch (Activelow)	4
DLH	D-latch(Active high)	4
SDL	Set D-latch	4
RDL	ResetD-latch	4
SRDL	SeVreset D-latch	6
EDGE TRIGGERED LATCHES		
RETS		8
SRETS		8

Cell Name	Function	Cell Units
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	6
D2T	Dual input D-type	8
SDT	Set D-type	4
RDT	Reset D-type	8
SRDT	Set/reset D-type	8
TOGGLE FLIP-FLOPS		
STT	Set T-type	8
RTT	Reset T-type	8
SRTT	Set/reset T-type	8
SYNCHRONOUS COUNTER		
SYNC	Synchronous counter stage	8
REGISTERS / SHIFT REGISTERS		
SHR4	Multibit serial register	30
SHR8	Multibit serial register	54
RSHR4	Multibit serial reg.with reset	30
RSHR8	Multibit serialreg.withreset	54
DREG4	Multibit parallel register	15
DREG8	Multibit parallel register	27
DREGT4	Multibit parallel register with tri-state outputs	25
DREGT8	Multibit parallel register with tri-state outputs	45
INVERTING TRI-STATE BUFFERS		
TRIBUFF	Tristate buffer (enable high)	2
TRIBUFFL	Tristate buffer (enable low)	2
TRINV	Tristate inv. buffer (enable high)	2
TRINVL	Tristate inv. buffer (enable low)	2
INPUT OUTPUT AND PERIPHERAL CELLS		
TTLIP	TTLIN Non-inverting	
TTLIPN	TTLIN Invertmg	
CMOSIP	CMOSIN Non-inverting	
CMOSIPN	CMOSIN Inverting	
CSCHMITT	CMOS Schmitt Non-inverting	
CSCHMITTN	CMOS Schmitt Inverting	
CSCHMITN	CMOS Schmitt Inverting	
BOP	Buffered Output Non-inverting	
NOP	Buffered Output Inverting	
TRIOUT	Tri-state Output Non-inverting	
TRIOUTN	Tri-state Output Inverting	
BODN	Buffered Open Drain Output Pull Down	
NODN	Inverted Open Drain Output Pull Down	
BODP	Buffered Open Drain Output Pull Up	
NODP	Inverted Open Drain Output Pull Up	
PDOL	Pull Down 25k ohms approx	
PDOH	Pull Down 50k ohms approx	
PUPL	Pull Up 25k ohms approx	
PUPH	Pull Up 50k ohms approx	
POWER SUPPLY PADS		
VDD		
VSS		

ORDERING INFORMATION



DS3597-2.4

MACROSOS 1

RADIATION HARD STANDARD CELL DESIGN SYSTEM

GPS's Silicon on Sapphire process provides significant advantages over other CMOS technologies The absence of the bulk silicon substrate reduces parasitic capacitance, giving an improvement in speed and reduction in power consumption. The use of a selfaligning silicon gate gives further improvements in both of the above parameters and achieves higher packing densities. The sapphire substrate also removes the risk of 'latch-up' allowing greater flexibility of use in electrically severe environments, and a significant improvement in radiation hardness.

Double level metal interconnect techniques further enhance the speed capabilities of the MACROSOS 1, and eliminates the possibility of layout dependent timing problems.

The cells in the core area are designed to have a common height, the cell width being dependent on the complexity of the cell. The cell width is the minimum possible although, in some circumstances, this is increased to achieve adequate drive capability. The cells and the interconnect between cells are placed on a regular grid in such a way that design rule infringements are impossible.

A range of standard input and output buffers are available for use in the peripheral areas. These buffers, and the interconnect from them to the core area are placed on the same grid as the core area for the same reason.

The cell layout method eliminates design faults, giving a much better chance of first time success than with other design methodologies. However, the normal constraints of logic design apply. Circuits must be designed with due attention to timing and testability etc. Good digital design techniques combined with the use of our simulation software and cell libraries gives the highest probability of first time design success.

Special cells may be configured by GPS for nonstandard functions. For example, higher output current buffers and special input cells can be designed on request. GPS's extensive MACROSOS 1 library support covers initial circuit capture to layout including post layout simulation.

Schematic capture libraries for DAZIX and Mentor Graphics CAE tools are available for design capture and simulation.

FEATURES

- Functionality to 1MRad(Si)
- High SEU Immunity, Latch-up Free
- Double-Level-Metal CMOS/SOS Technology
- 2.5 Micron Design Rules
- Typical Gate Delay 1.2nS - Toggle Rates of 70MHz Achievable
- Comprehensive Library of Logic Cells and Logic Function Building Macros
- Configurable RAM and ROM Macro Blocks
- 3μW/MHz Power Dissipation Per Active Gate
- Extensive CAD Design and Support System

CAPABILITY APPROVAL

The MACROSOS 1 standard cell design route is covered by ESA Certificate of Capability Approval No. 195 dated 26th March 1993. This approval certifies MACROSOS 1 for use in ESA space programmes according to ESA/SCC Generic Specification 9000.

DC CHARACTERISTICS AND RATINGS

Parameter	Min	Max	Units
Supply Voltage	-0.5	7	V
Input Voltage	-0.3	V_{DD}+0.3	V
Current Through Any Pin	-20	+20	mA
Operating Temperature	-55	125	°C
Storage Temperature	-65	150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1: Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL Input High Voltage	-	2.0	-	-	V
V_{IL1}	TTL Input Low Voltage	-	-	-	0.8	V
V_{IH2}	CMOS Input High Voltage	-	70	-	-	% V_{DD}
V_{IL2}	CMOS Input Low Voltage	-	-	-	30	% V_{DD}
V_{OH}	Output High Voltage	I_{OH} = -4mA	90	-	-	% V_{DD}
V_{OL}	Output Low Voltage	I_{OL} = 4mA	-	-	0.4	V
I_L	Input Leakage Current	V_{IN} = V_{DD} or V_{SS}	-10	-	10	µA
I_{OZ}	Output Leakage Current	Tristate Output	-30	-	30	µA
I_{DD}	Power Supply Current	-	-	0.1	*	mA

V_{DD} = 5V±10%, over full operating temperature range, up to 100KRad. (Ratings for higher doses available on request).
* Dependent on gate count.

Figure 2: Electrical Characteristics

AC CHARACTERISTICS

Cell Name	Function	O/P Edge	Delay	Inherent Load*	Per 1pF Units
CI02	CMOS input/output	Rising Falling	0.3 0.3	0.2 0.2	ns
NOR2	2 input NOR	Rising Fallmg	0.8 0.8	5.5 3.6	ns
RDT	Reset D type	Rising CK - QB Falling CK - QB Data set-up time Data hold time	3.8 4.4 2.8 0.7	5.0 5.1 - -	ns

*1pF is equivalent to fanout of 7 standard gates.

Figure 3: Electrical Characteristics

PROPAGATION DELAY

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 60% of those listed.

Use the following normalised graphs to obtain conversion factors to predict delays at any other working temperature or voltage.

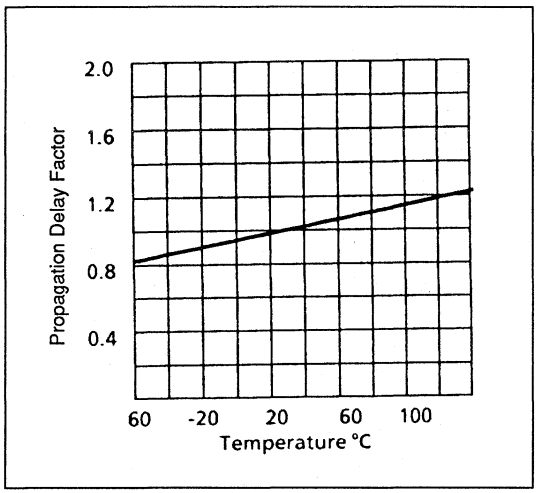


Figure 4: Propagation Delay vs Temperature

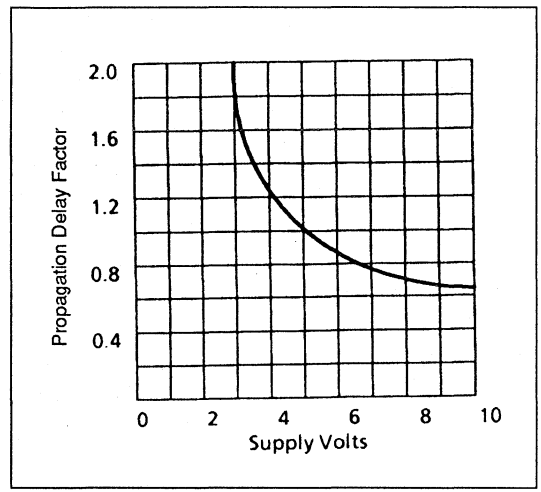


Figure 5: Propagation Delay vs Supply Voltage

STANDARD PACKAGE OPTIONS

GPS offer a wide range of packages as standard. Other package styles are available. If you require a package not covered on this list, contact GPS.

Ceramic DIL	24	28	40	48	64	-	-
Cerdip	24	28	40	48	-	-	-
Leaded Flatpack	28	42	48	64	68	84	132
Pin Grid Array	68	8	100	120	144	-	-
Ceramic LCC	(40)	44	(48)	68	84	-	-

Figure 6: Standard Package Option

DEVELOPMENT INTERFACES

Circuit design, capture and simulation activities are carried out by the customer. Schematic capture and simulation libraries for DAZIX and Mentor Graphics CAE systems are provided by GPS.

GPS will accept a simulated design and perform layout, verification checks and PG. GPS will then procure masks and fabricate and test POD parts prior to delivery.

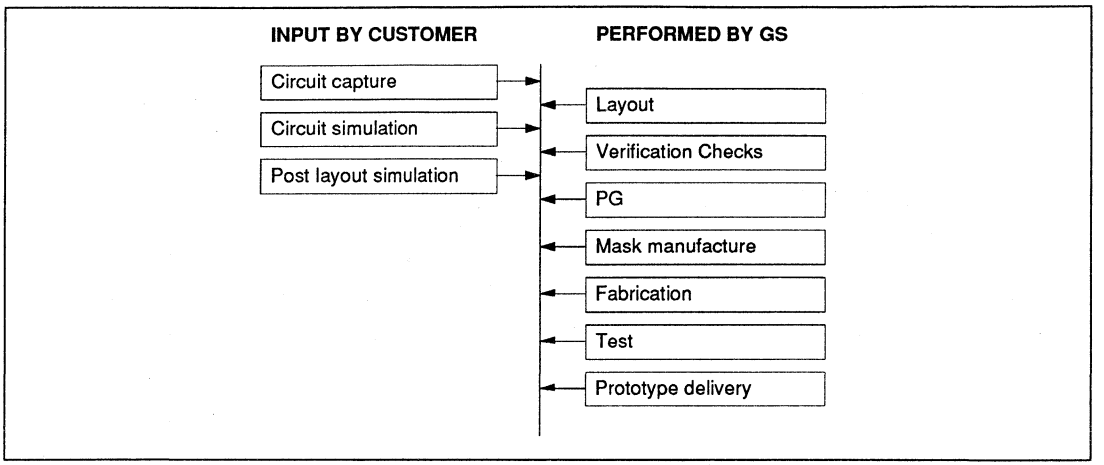


Figure 7: Development Interfaces

RADIATION TOLERANCE

Total Dose Radiation Testing

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GEC Plessey Semiconductors can provide radiation testing compliant with Mil-Std-883 method 1019 Ionizing Radiation (total dose) test.

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 8: Radiation Hardness Parameters

LSI MACROS

MEMORY
- Configurable static RAM and ROM.

BIT SLICE ELEMENTS
- 4 bit Microprocessor Slice
- 4 bit Sequencer
- 12 bit Microprogram Controller
- Status and Shift Control Units
- DMA Address Generator

MICROPROCESSOR PERIPHERALS
- Parallel Peripheral Interface
- Programmable Communications Interface
- DMA Controller

INTERFACE FAMILY
- Memory Error Detector and Corrector
- Manchester Encoder / Decoder
- Octal Latches
- Octal Buffers
- Octal Tranceivers
- Address Decoders

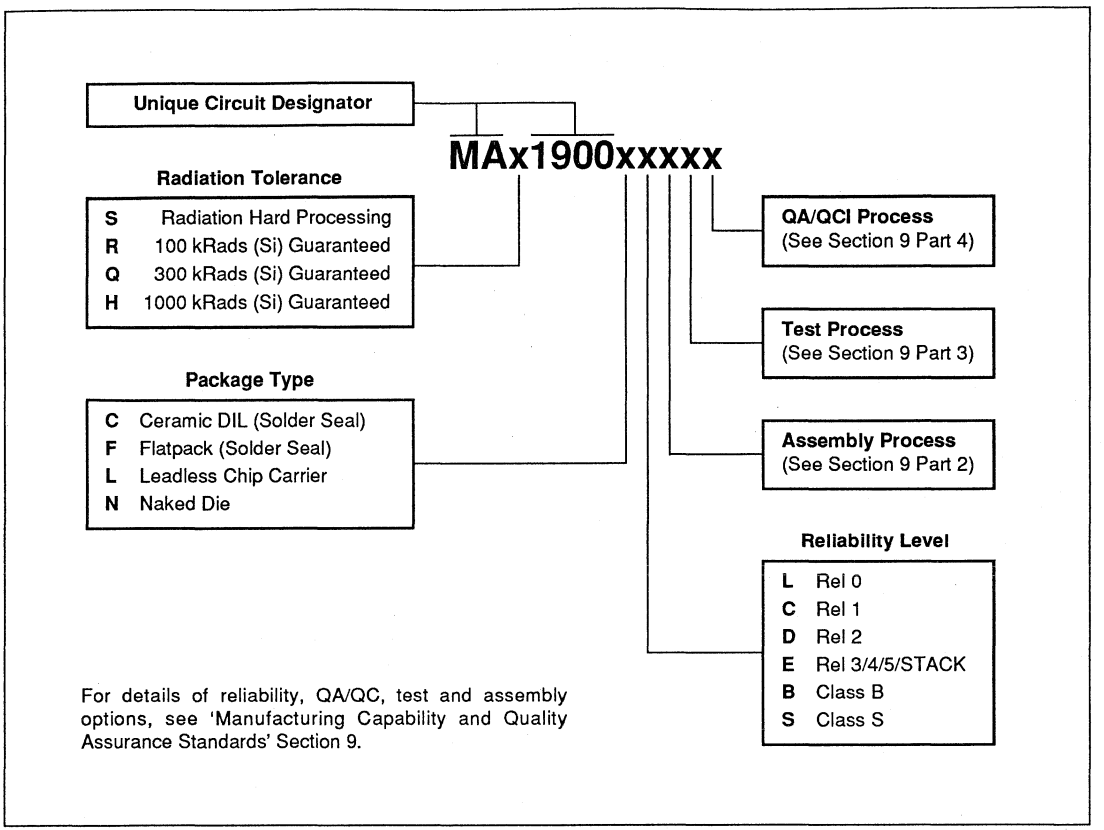
For more information on LSI Macros and additions to the family contact your nearest office.

CELL LIBRARY QUICK GUIDE

Cell Name	Function	Cell Width
COMBINATIONAL GATES		
INV	Inverter	3
INVB	Fast inverter	6
BUFF	Non-inverting buffer	8
BUFFB	Fast non-inverting buffer	13
BUFFC	Super fast non-inverting buffer	18
BUFFD	Highdrive non-inverting buffer	23
NAND2	2 input NAND	4
NAND3	3 input NAND	5
NAND4	4 input NAND	6
AND2	2 input AND	6
AND3	3 Input AND	7
AND4	4 input AND	8
NOR2	2 input NOR	4
NOR3	3 input NOR	5
NOR4	4 input NOR	6
OR2	2 Input OR	6
OR3	3 inputOR	7
OR4	4 input OR	8
ANDNOR	2 + 2 input AND/NOR	7
ANDOR	2 + 2 Input AND/OR	9
A2NO1	AND 2 NOR 1	6
A2O1	AND 2 OR 1	7
A2NO2	AND 2 NOR 2	7
A2O2	AND 2 OR 2	8
A3NO1	AND 3 NOR 1	7
A3O1	AND 3 NOR 1	8
O2NA1	OR 2 NAND 1	6
O2A1	OR 2 AND 1	7
O2NA2	OR 2 NAND 2	7
O2A2	OR 2 AND 2	8
O3NA1	OR 3 NAND 1	7
O3A1	OR 3 AND 1	8
ORNAND	2 + 2 OR/NAND	6
ORAND	2 + 2 OR/AND	8
EXNOR	Exclusive NOR	6
EXORN	Exclusive OR	6
SEL2INV	Select 1 of 2 (Invertlng)	7
SEL2	Select 1 of 2	8
ARITHMETIC		
FAD	Full adder	14

Cell Name	Function	Cell Width
SIMPLE LATCHES		
NASR	NAND set reset-latch	11
NOSR	NOR set-reset latch	11
TRANSPARENT LATCHES		
DL	D-latch (Active low)	8
DLH	D-latch (Active high)	8
RDL	Reset D-latch	9
RDLH	Set/reset D-latch	9
EDGE TRIGGERED LATCHES		
RETS	Reset latch	12
RETSN	Reset negative edge trigger latch	16
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	14
D2T	Dual input D-type	18
SDT	Set D-type	17
RDT	Reset D-type	17
SRDT	Set/reset D-tvpe	19
RDTN	Negative edge triggered reset type	17
TOGGLE FLIP-FLOPS		
STT	Set T-type	17
RTT	Reset T-type	16
SRTT	Set/reset T-type	18
RTTTOG	Reset T-type with low level toggle enable	20
RTTTOGH	Reset T-type with high level toggle enable	20
INVERTING TRI-STATE BUFFERS		
TRINV	Tristate inverting buffer (enable high)	6
TRINVL	Tristate inverting buffer (enable low)	6
I, O & P cells		
POWER SUPPLY PADS		
VDD	V_{DD} pad	
VSS	V_{SS} pad	

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

DS3598-3.4

MA9000 Series

SILICON-ON-SAPPHIRE RADIATION HARD GATE ARRAYS

The logic building block for the GPS double level metal CMOS/SOS gate arrays is a four transistor 'cell-unit' equivalent in size to a 2 input NAND gate. Back to back cell-units as illustrated, organised in rows, form the core of the array

The interconnection patterns that cause groups of cell units within a row, to become defined logic cells, and the models which are used to simulate these cells, are stored as software in LIBRARIES. Cells up to the complexity of, say, multiple bit shift registers are treated in this way.

Higher complexity functions are described by MACROS as the interconnection of defined cells. Macros are 'hard', 'soft', or 'firm' according to the constraints that are applied to the distribution of the component cells within the array and whether the full function is simulated by a model or by the additive effects of the component cells.

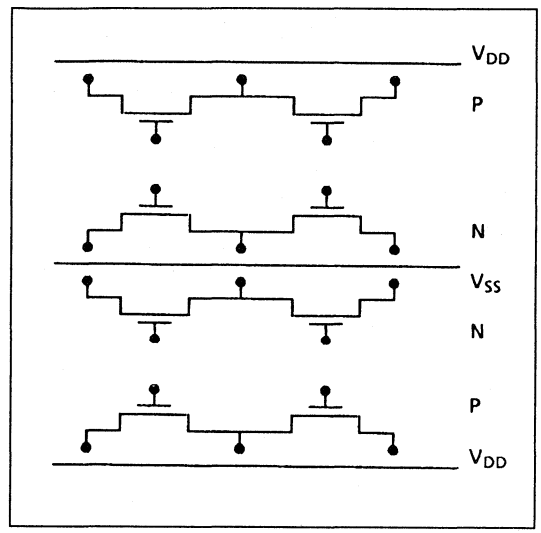


Figure 1: Cell Unit

FEATURES

- Radiation Hard to 1MRad(Si)
- High SEU Immunity, Latch-Up Free
- Double-Level-Metal CMOS/SOS Technology
- 2.5 Micron Design Rules
- Typical Gate Delay 1.2nS With 2 Loads, 60MHz Toggle Speeds
- Comprehensive Library of Logic Cells and Logic Function Building Macros
- 100% Automatic Place and Route for Typically 70% Utilisation

ARRAY OPTIONS

Array Type	Cell Units	Bonding Pads		
		I/O	Power	Total
MA9007	748	46	2	48
MA9024	2484	80	4	84
MA9040	4048	102	4	106

Each cell-unit is equivalent to a 2 input NAND gate.

Any I/O site may be configured as a power pad to give flexible bonding options, but to standardise testing, preferred positions exist.

CHARACTERISITICS & RATINGS

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply voltage	-0.5	7	V
V_I	Input voltage	-0.3	V_{DD} + 0.3	V
T_A	Operating temperature	-55	125	°C
T_S	Storage temperature	-65	150	°C

Table 1: Absolute Maximum Ratings

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification. is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DD}	Supply voltage	-	4.5	5.0	5.5	V
V_{IH1}	TTL input high voltage	-	2.0	-	-	V
V_{IL1}	TTL input low voltage	-	-	-	0.8	V
V_{IH2}	CMOS input high voltage	-	80	-	-	$\%V_{DD}$
V_{IL2}	CMOS input low voltage	-	-	-	20	$\%V_{DD}$
V_{OH1}	TTL output high voltage	I_{OH} = -2mA	2.4	-	-	V
V_{OL1}	TTL output low voltage	I_{OL} = 5mA	-	-	0.4	V
V_{OH2}	CMOS output high voltage	I_{OH} = -4mA	90	-	-	$\%V_{DD}$
V_{OL2}	CMOS output low voltage	I_{OL} = 4mA	-	-	10	$\%V_{DD}$
I_L	Input leakage current	-	-	-	10	µA
I_{OZ}	Output leakage current	Tristate Output	-	-	30	µA
I_{DD}	Power supply current	-	-	0.1	*	mA

V_{DD} = 5V ±10%, over full operating temperature.
* Dependent on array type.

Table 2: Electrical Characteristics

AC CHARACTERISTICS

Cell Name	Function	O/P Edge	Inherent Delay	Per 1pF Load*	Units
NOP	Push/Pull Output Buffer	Rising	0.5	0.4	ns
		Falling	0.3	0.2	
NOR2	2 Input NOR	Rising	1.6	13.6	ns
		Falling	0.8	5.0	
RDT	Reset D Type	Rising CK - QB	4.6	13.7	ns
		Falling CK - QB	7.8	13.6	
		Data Set-up time	7.1	-	
		Data Hold time	4.4	-	

* 1pF is equivalent to fanout of 5 standard gates

Table 3: Electrical Characteristics

PROPAGATION DELAY

Worst case maximum propagation delays for 5 volts working and 25°C are stated in the cell libraries. These are for the data change or state change which gives the greatest delay. Typical process figures under the same conditions are generally 60% of those listed.

Use the following normalised graphs to obtain converstion factors to predict delays at any other working temperature or voltage:

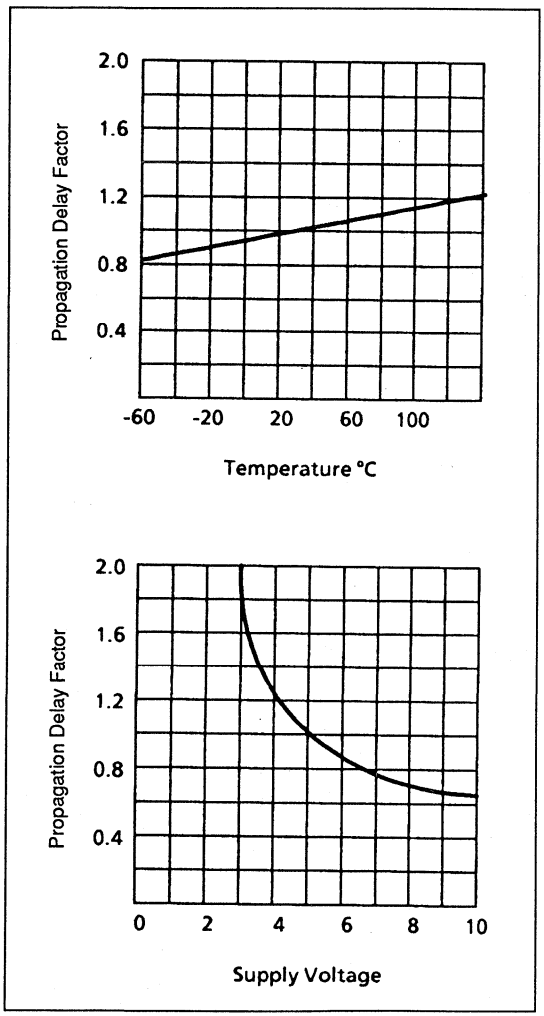


Figure 2: Propogation Delay vs Temperature & Propogation Delay vs Supply Voltage

PACKAGE OPTIONS

	MA9007 196 x 129	MA9024 247 x 240	MA9040 301 x 302
DIL14	X		
DIL16	X		
DIL20	X		
DIL24	X	X	
DIL28	X	X	
DIL40	X	X	
DIL48		X	X
DIL64		X	X
LCC28	X		
LCC40	X	X	
LCC44	X		
LCC48		X	X
LCC68		X	X
LCC84		X	X
FPK16	X		
FPK20	X		
FPK24	X		
FPK28	X	X	
FPK64		X	X
FPK68		X	X
FPK84		X	X
PGA68		X	X
PGA84		X	X
PGA120		X	X
PGA144		X	X

DIL = Dual in line
LCC = Leadless chip carrier
FPK = Leaded flatpack
PGA = Pin grid array

These are standard packages. If your package requirement is not shown above, discuss other options with an applications engineer.

RADIATION TOLERANCE

For product procured to guaranteed total dose radiation levels, each wafer lot will be approved when all sample devices from each lot pass the total dose radiation test.

The sample devices will be subjected to the total dose radiation level (Cobalt-60 Source), defined by the ordering code, and must continue to meet the electrical parameters specified in the data sheet. Electrical tests, pre and post irradiation, will be read and recorded.

GPS can provide radiation testing compliant with MIL-STD-883C remote sensing method 1019 notice 5.

Total Dose (Function to specification)*	$3x10^5$ Rad(Si)
Transient Upset (Stored data loss)	$5x10^{10}$ Rad(Si)/sec
Transient Upset (Survivability)	$>1x10^{12}$ Rad(Si)/sec
Neutron Hardness (Function to specification)	$>1x10^{15}$ n/cm^2
Single Event Upset**	$<1x10^{-10}$ Errors/bit day
Latch Up	Not possible

* Other total dose radiation levels available on request

** Worst case galactic cosmic ray upset - interplanetary/high altitude orbit

Table 4: Radiation Hardness Parameters

CELL LIBRARY QUICK GUIDE

Cell Name	Function	Cell Units
COMBINATIONAL GATES		
INV	Inverter	1
DUALINV	Dual inverter	1
INVB	Fast inverter	1
INVC	Super fast inverter	2
BUFF	Non-inverting buffer	1
BUFFB	Fast non-inverting buffer	2
BUFFC	Super fast non-inverting buffer	3
NAND2	2 input NAND	1
NAND2B	Fast 2 input NAND	2
NAND3	3 input NAND	2
NAND4	4 input NAND	2
NAND8	8 input NAND	6
NAND12	12 input NAND	8
NAND16	16 input NAND	11
AND2	2 input AND	2
AND3	3 input AND	2
AND4	4 input AND	3
NOR2	2 input NOR	1
NOR2B	Fast 2 input NOR	2
NOR3	3 input NOR	2
NOR4	4 input NOR	2
NOR8	8 input NOR	6
NOR12	12 input NOR	8
NOR16	16 input NOR	11
OR2	2 input OR	2
OR3	3 input OR	2
OR4	4 Input OR	3
ANDNOR	2 + 2 input AND/NOR	2
ANDOR	2 + 2 input AND/OR	3
ORNAND	2 + 2 OR/NAND	2
ORAND	2 + 2 OR/AND	3
A2N01	2 + 1 Input AND/NOR	2
A201	2 + 1 input AND/OR	2
02NA1	2 + 1 input OR/NAND	2
02A1	2 + 1 input OR/AND	2
EXNOR	Exclusive NOR	3
EXORN	Exclusive OR	3
SEL21NV	Select 1 of 2 (inverting)	3
SEL2	Select 1 of 2	3
SEL41NV	4 bit data selector (inverting)	6
SEL4	4 bit data selector	7

Cell Name	Function	Cell Units
DECODERS		
DEC2T4	2 to 4 line decoder	6
DEC3T8	3 to 8 line decoder	11
DEC4T16	4 to 16 line decider	40
ARITHMETIC		
HAD	Half adder	5
FAD	Full adder	8
FLAD	Fast look ahead adder	6
LAH2	2 bit look ahead unit	10
LAH3	3 bit look ahead unit	14
LAH4	4 bit look ahead unit	24
ADD4	4 bit look ahead adder	50
ADD8	8 bit look ahead adder	106
SIMPLE LATCHES		
NASR	NAND set reset-latch	3
NOSR	NOR set-reset latch	3
TRANSPARENT LATCHES		
DL	D-latch (Active low)	4
DLH	D-latch(Actlve high)	4
SDL	Set D-latch	4
RDL	Reset D-latch	4
SRDL	Set/reset D-latch	5
EDGE TRIGGERED LATCHES		
RETS	Latch with reset	7
SRETS	Latch with reset and set	8
MASTER-SLAVE FLIP-FLOPS		
DT	D-type	6
D2T	Dual input D-type	8
SDT	Set D-type	7
RDT	Reset D-type	7
SRDT	Set/reset D-type	8
JK	JK flip-flop	10
SDK	JK flip-flopwith set	11
RJK	JK flip-flop with reset	11
SRJK	JK flip-flop with reset and set	12
TOGGLE FLIP-FLOPS		
STT	Set T-type	7
RTT	Reset T-type	7
SRTT	Set/reset T-type	8
SYNCHRONOUS COUNTER		
SYNC	Synchronous counter stage	10

Cell Name	Function	Cell Units
REGISTERS / SHIFT REGISTERS		
SHRx	Multibit (x = 2-8) serial register	16-46
RSHRx	Multibit (x = 2-8) serial reg. with reset	18-54
DREGx	Multibit parallel register (x = 2-8)	8-22
DREGTx	Multibit parallel register (x = 2-8) with tri-state outputs	12-36
HPLSx	Half parallel loading shift registers (x = 2-8)	22-64
INVERTING TRI-STATE BUFFERS		
TRIBUFF	Tristate buffer (enable high)	2
TRIBUFFL	Tristate buffer (enable low)	2
TRINV	Tristate inv buffer (enable high)	2
TRINVL	Tristate inv. buffer (enable low)	2
INPUT OUTPUT AND PERIPHERAL CELLS		
DIP	Direct input (protection cicuit only)	
PUP	Pull up (approx 30 Kohms)	
PDO	Pull down (approx 40 Kohms)	
TSCHMITT	TTL compatible Schmitt	6
CSCHMITT	CMOS compatible Schmitt	6
CMOSIN	CMOS buffer (non-inverting)	1
TTLIN	TTL buffer (non-inverting)	3
NOP	Push/pull output buffer (inverting)	
WNOP	Multiple NOP	
BOP	Push/pull output buffer (non inverting)	
ZOP	Tri-state output buffer	
ODN	Open drain output pull down	
ODP	Open drain output pull up	
TRIOP	Tristate I/O buffer	4
BUSINT	Bus interface	6
STEPUP	Output Buffer	6
POWER SUPPLY PADS		
VDD	V_{DD} pad	
VSS	V_{SS} pad	

MACROS

The following Macros are included in the MA9000 library. GPS are constantly adding new Macros to the library, please contact our nearest office for information on the latest additions.

Macro name	Macro name
ACOUNTn	Asynchronous counters
ALU4	ALU
GCOUNTn	Gray counters
JCOUNTn	Johnson counters
LADDn	Lookahead adders
MCOMPn	Magnitude comparators
PARITYn	Parity detectors
RADDn	Ripple carry adders
SEL8	Select 1 of 8
SEL16	Select 1 of 16
M2901	4 bit slice microprocessor
M2909	4 bit microprogram controller
M2902	Look ahead carry unit
M2910	12 bit microprogram sequencer
M2918	Pipeline register

DEVELOPMENT INTERFACES

Circuit design, captive and simulation activities are carried out by the customer. Schematic capture and simulation libraries for Dazix and Mentor Graphics CAE systems are provided by GPS. GPS will accept a simulated design and perform layout, verification checks and PG. GPS will then procure masks and fabricate and test parts prior to prototype delivery. The MA9000 arrays fall within the ESA capability domain.

DAZIX is a trademark of Intergraph UK

Mentor Graphics is a trademark of Mentor Graphics Corporation.

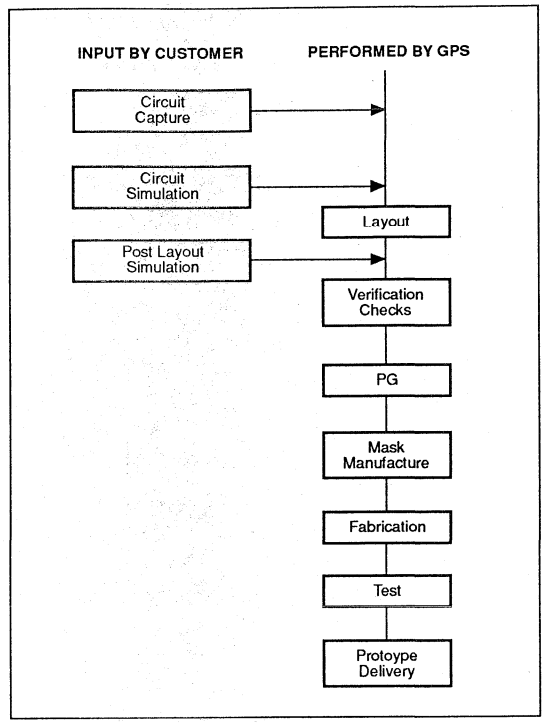
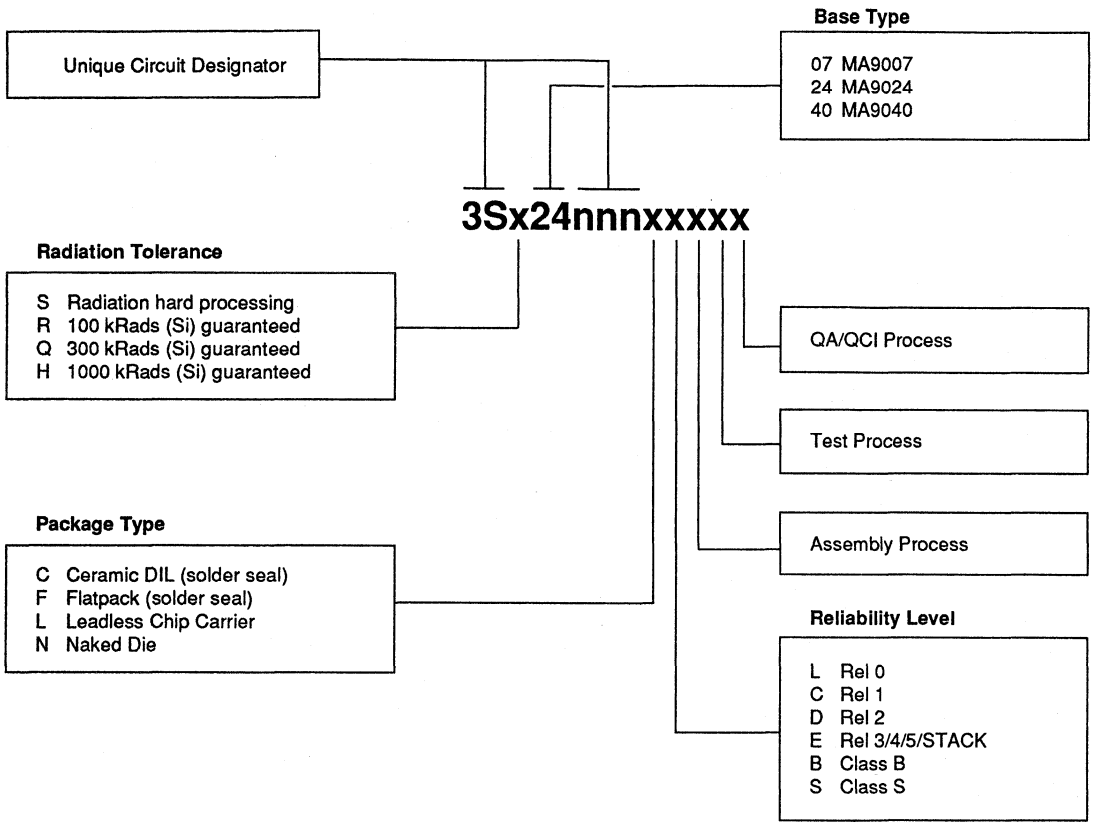


Figure 3: Development Interfaces

ORDERING INFORMATION

For details of Reliability, QA/QCI, Test, and Assembly options, see 'Manufacturing Capability and Quality Assurance Standards'.



ASIC Design Routes

CAD SUPPORT

GPS support Mentor Graphics and Dazix platforms for design entry and logic simulation of SOS ASIC designs.

The design route GPS ASIC designs use is illustrated in figure 1.

For details of VHDL and synthesis integration into the design route, please contact your local GPS Field Applications Engineer.

The SOS ASIC design routes are the subject of a GPS Quality Assurance specification, (spec. number RG 001) which is available on request.

THE DESIGN INTERFACE

It is possible for customers with the appropriate design tools and ASIC design experience to perform some of the tasks in the design route, for example schematic capture, simulation and even layout of SOS designs. The point in the design cycle at which the customer hands over the design data to GPS is called the 'Design Interface'. GPS field application engineers are available to discuss the most appropriate design interface for a particular development.

The design interfaces supported by GPS are illustrated in figure 1 and are described in the following sections.

DESIGN INTERFACE 1 - FULL DESIGN INTERFACE

The customer provides a full requirement specification and GPS perform all design functions from schematic capture to the production of tested samples.

A summary of the deliverables expected from the two parties when using this interface point follows:

The customer shall provide GPS with the following:

- Target functional specification, including block diagrams and circuit diagrams where available.
- Inspection/screening requirements.
- Required package type and pinout, if known.
- Environmental specification (supply voltage, temperature range etc).
- Interface specification (e.g. CMOS/TTL output drive).
- Timing requirements(e.g maximum clock speed, critical paths, with timing diagams where appropriate).

GPS shall provide the customer with the following:

- Fully tested samples of the device using a pinout previously agreed with the customer if not originally specified .
- Colour plot of ASIC.

DESIGN INTERFACE 2 - POST SIMULATION INTERFACE

The customer performs schematic capture and simulation and passes a 'fault free' design database to GPS. GPS then perform the layout, supplying track capacitance data to the customer for post layout simulation. When a successful post layout simulation has been performed, GPS take the design to the production of tested samples.

A summary of the deliverables expected from the two parties when using this interface point follows:

The customer shall provide GPS with the following:

- Circuit description database.
- Test vectors.
- Procurement specification.
- Circuit diagram.
- Target Pinout.
- Timing information (including critical paths).

GPS shall provide the customer with the following:

- Track capacitance file to enable the customer to perform post-layout simulation.
- Tested samples of the device.
- Colour plot of ASIC.

DESIGN INTERFACE 3 - POST LAYOUT INTERFACE

The customer performs schematic capture, simulation and layout. GPS carries out design checks, produces the PG tape and masks, and finally the tested samples,

A summary of the deliverables expected from the two parties when using this interface point follows:

The customer shall provide GPS with the following:

- Circuit description file database.
- Test vectors.
- Procurement specification.
- Circuit diagram.
- GDSII layout file.
- Target Pinout.
- Timing information (including critical paths).
- Bonding diagram.

GPS shall provide the customer with the following:

- Tested samples of the device.
- Colour plot of ASIC.

QUALITY ASSURANCE PROCEDURES

It is obviously necessary to clearly define the respective responsiblities of the customer and GPS in the case of each design interface. This is defined initially in a design work statement completed jointly by both parties. The subsequent monitoring of the development project is a subject of a GPS Quality Assurance document QAP 014E, and entails a number of design reviews at defined stages (control points) of the project. The completed control point forms, form a record of development progress. Both the QAP 014E document and the associated QAP 014E forms are available on request.

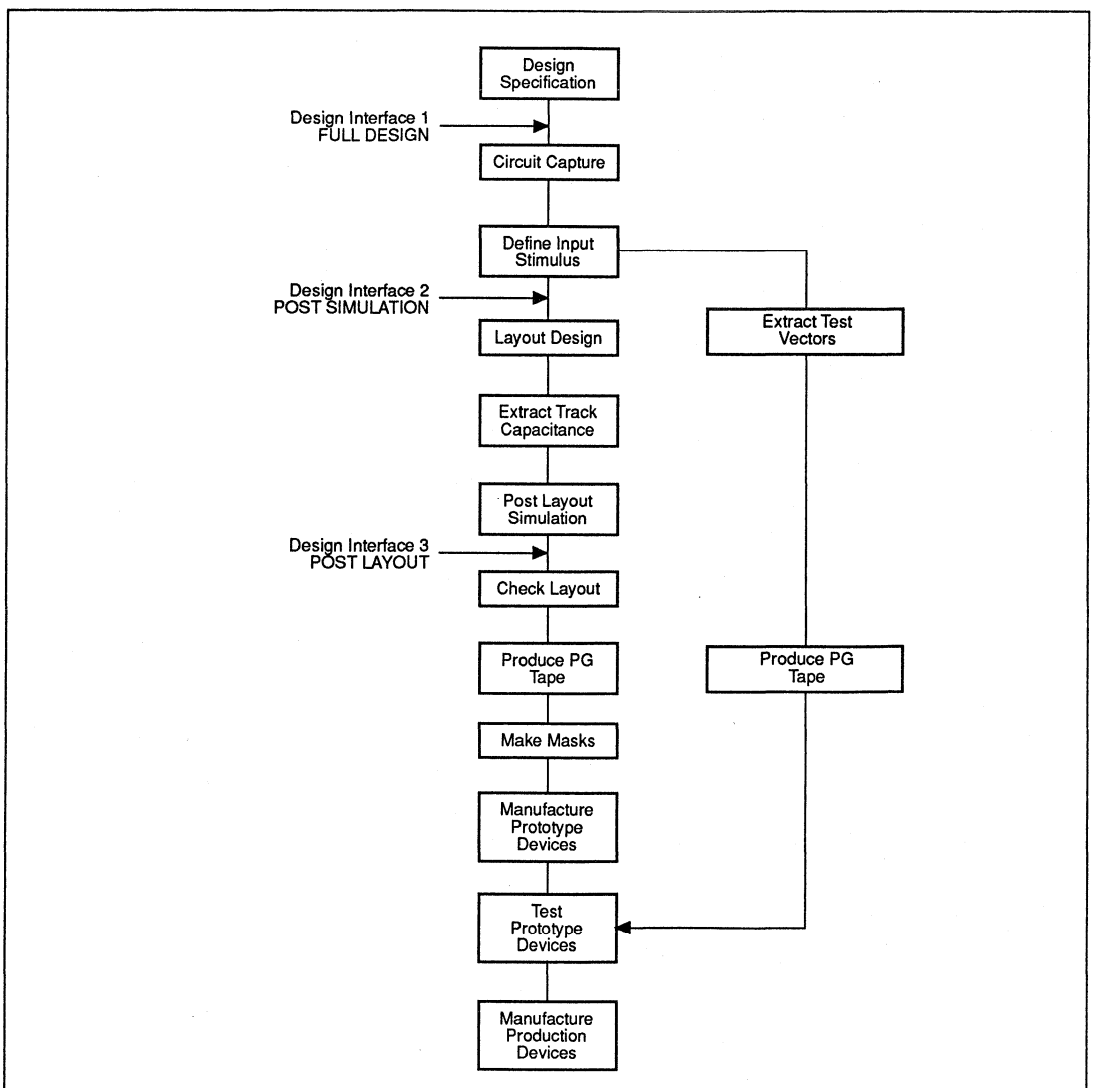


Figure 1: SOS ASIC design interfaces

Section 8
Bipolar Products

GEC PLESSEY
SEMICONDUCTORS

Bipolar Processes and Products

Bipolar Space

GPS not only offer an extensive digital CMOS line that covers most of the needs of spacecraft On Board Processing but also provide a complementary bipolar product range that meets many of the front end RF and mixed signal requirements.

GPS bipolar products have a long history of space procurement. Most of the processes have had extensive radiation testing and characterisation. The products have the benefit of being manufactured on wafer fabrication lines used for high volume commercial applications, with an ensuing high level of reliability and repeatability of manufacture.

The DESC listed SMDs represent a small number of the bipolar products available from GPS. These devices are listed in the GPS Professional Products Handbook. Full datasheets on the DESC listed parts are also to be found in the Professional Products Handbook.

For more details concerning GPS bipolar products for high reliability and space applications can be obtained through your local GPS sales office.

Bipolar Processes and Products

RF Bipolar Processes

GPS' commitment to high speed bipolar technology enables us to remain at the forefront of RF and high performance digital products for the communications, media and military markets.

Our newest RF process features an f_{max} of 40GHz.

Utilising the latest developments in stepper lithography, this process gives equivalent performance to GaAs technology up to 2.5GHz but with the added advantages of easy integration and lower cost.

Features of the 0.5µ process include:

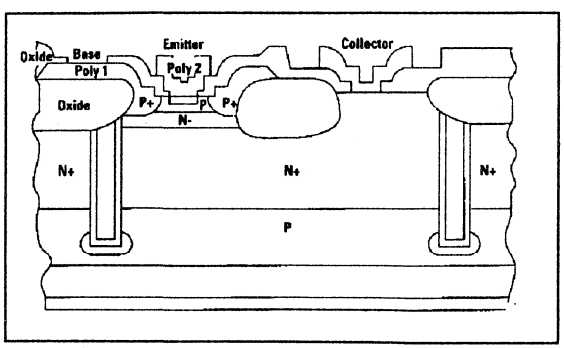
- Optimised for both analog and digital functions
- 0.3µ emitter width
- Process optimised for high f_T at low currents
- Gate delays of 25pS
- On-chip capacitors and inductors maximise RF performance

Mixed Signal Bipolar Processes

For products and markets where analog flexibility and significant amounts of logic are needed, we offer a true complementary process with optimised PNP and NPN transistors and nitride capacitors. The process uses trench isolation and polysilicon emitters to dramatically reduce junction capacitance when compared with other mixed signal processes. Fully integrated design methodologies have been developed based on the Cadence Artist platform.

Features include:

- Complementary transistors - 2.5GHz PNP, 10GHz NPN
- Dual layer metal
- Minimum feature size of 1.0µ
- ±5V capability
- Nitride capacitors - 0.3nF/mm^2



Trench isolated bipolar

RF Bipolar Process Development

	1994/95	1995/96	1996/97	1997/98
Emitter Width	1.0	0.5		0.35
Metal Pitch	4.0	2.0		1.4

Interconnect	Three Layer Metal		
f_{max}	14GHz	40GHz	75GHz
Gate Delay	50 ps	25 ps	20 ps
Capacitors	Intermetal with nitride		

Standard Militarized Drawings (SMDs)

GEC Plessey Semiconductors has actively pursued a program of obtaining SMDs for our Professional products.

These products are qualified and approved as SMDs by DESC (Defense Electronics Supply Center), Ohio, USA.

As products are approved, they are listed in MIL-BUL-103 (list of standardized military drawings) and are 'preferred' for use in projects requesting the use of SMD qualified parts.

GPS products with approved SMDs conform to class 'M' (non-Jan Class 'B' microcircuits in accordance with para.1.2.1. of MIL-STD-883 latest revision. These are generally equivalent to the earlier GPS 'AC' series of devices.

SMD Number	Device	Product Description
5962-9231501M2C	SL2524	1.3GHz dual wideband log amplifier
5962-9079201MXC	SL521	150MHz wideband log amplifier
5962-9079201MXA	SL521	150MHz wideband log amplifier
5962-8980301XC	SL523	100MHz dual wideband log amplifier
5962-8980301XA	SL523	100MHz dual wideband log amplifier
5962-9208401MXC	SL531	250MHz true log IF amplifier
5962-9208401MXA	SL531	250MHz true log IF amplifier
5962-9052101XC	SL532	Low phase shift limiter
5962-9052101XA	SL532	Low phase shift limiter
5962-9052001XC	SL560	300MHz low noise amplifier
5962-9052001XA	SL560	300MHz low noise amplifier
5962-9205901MXC	SP8602	500MHz/2 frequency divider
5962-9205901MXA	SP8602	500MHz/2 frequency divider
5962-9097001MCA	SP8620	400MHz/5 frequency divider
5962-9200301MCA	SP8630	600MHz/10 frequency divider
5962-9061801MEA	SP8647	250MHz/10/11 frequency divider
5962-9208801MCA	SP8670	600MHz/8 frequency divider
5962-8767801EA	SP8690	200MHz/10/11 frequency divider
5962-8861701PA	SP8718	520MHz low current two modulus divider
5962-9057701MEA	SP8720	300MHz/3/4 frequency divider
5962-9159001MEA	SP8741	300MHz/6/7 frequency divider
5962-8868401CA	SP8755	1200MHz/64 frequency divider
5962-9208901MPA	SP8782	1GHz/16/17, 32/33 multi-modulus divider
5962-9176101MPA	SP8799	225MHz/10/11 two modulus divider
5962-9066101MPA	SP8802	3.3GHz/2 fixed modulus divider
5962-9056701MPA	SP8804	3.3GHz/4 fixed modulus divider
5962-9157801MPA	SP8808	3.3GHz/8 fixed modulus divider
5962-9157201MPA	SP8830	1.5GHz/10 prescaler

KEY

The 4 suffix letters are explained as follows:-

First Letter - Device Class Designator

M = the device class for all Swindon products (para 1.2.3 SMD)

You will note that some SMDs do not have the first letter 'M'. This is because they were approved prior to DESC introducing this requirement. They are:-

5962-8980301XC	SL523	100MHz dual wideband log amplifier
5962-8980301XA	SL523	100MHz dual wideband log amplifier
5962-9052101XC	SL532	Low phase shift limiter
5962-9052101XA	SL532	Low phase shift limiter
5962-9052001XC	SL560	300MHz low noise amplifier
5962-9052001XA	SL560	300MHz low noise amplifier
5962-8767801EA	SP8690	200MHz/10/11 frequency divider
5962-8861701PA	SP8718	520MHz low current two modulus divider
5962-8868401CA	SP8755	1200MHz/64 frequency divider

Second letter - Case Outline (package type and number of leads)

P = 8 lead DIL
C = 14 lead DIL
E = 16 lead DIL
X = 8 lead TO5
2 = 20 leadless chip carrier

Third letter - Lead Finish

A = solder dip (all DIL SMDs are solder dipped)
C = gold plate (this is the standard finish for TO5s, but we do offer solder dipped leads 'A')
X = optional, this allows the supplier to supply any lead finish and will be coded with the relevant lead finish 'A' or 'C' not X.

Fourth letter - Compliance Indicator

C = 'Class M' products.

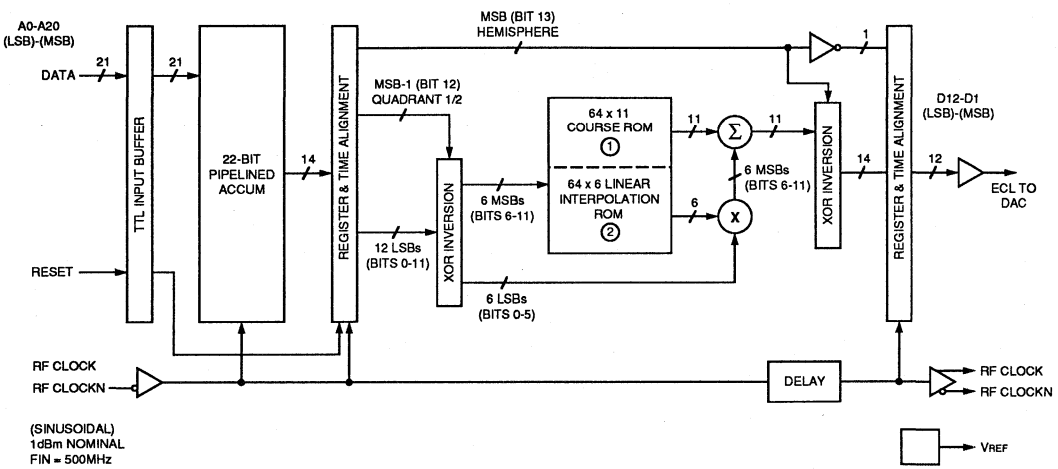
MA12003

22 BIT PHASE ACCUMULATOR / SINE ROM

The MA12003 is a 22 bit phase accumulator / sine read only memory (ROM) ASIC, it is a 21 bit parallel TTL input device with a 12 bit single ended ECL data output and differential ECL Clock outputs. An accumulator reset with TTL input clears the accumulator contents. This device is generally suitable for use in high-reliability space applications.

FEATURES

- 500MHz RF Clock Performance
- Radiation Hard Isolated Bipolar Process
- Low Power Consumption



① Course ROM

	0	1	2	3	4	5	6	7	8	9
0:	0	50	100	150	200	249	299	348	397	446
1:	495	543	591	639	686	733	779	825	871	916
2:	960	1004	1047	1090	1132	1173	1213	1253	1292	1330
3:	1368	1404	1440	1475	1509	1542	1574	1606	1636	1665
4:	1693	1721	1747	1772	1796	1819	1841	1862	1882	1900
5:	1918	1934	1949	1963	1976	1987	1997	2007	2015	2021
6:	2027	2031	2034	2036						

② Linear Interpolation ROM

	0	1	2	3	4	5	6	7	8	9
0:	50	50	50	50	49	50	49	49	49	49
1:	48	48	48	47	47	46	46	46	45	44
2:	44	43	43	42	41	40	40	39	38	38
3:	36	36	35	34	33	32	32	30	29	28
4:	28	26	25	24	23	22	21	20	18	18
5:	16	15	14	13	11	10	10	8	6	6
6:	4	3	2	0						

Figure 1: Block Diagram / Architecture

TIMING DIAGRAMS

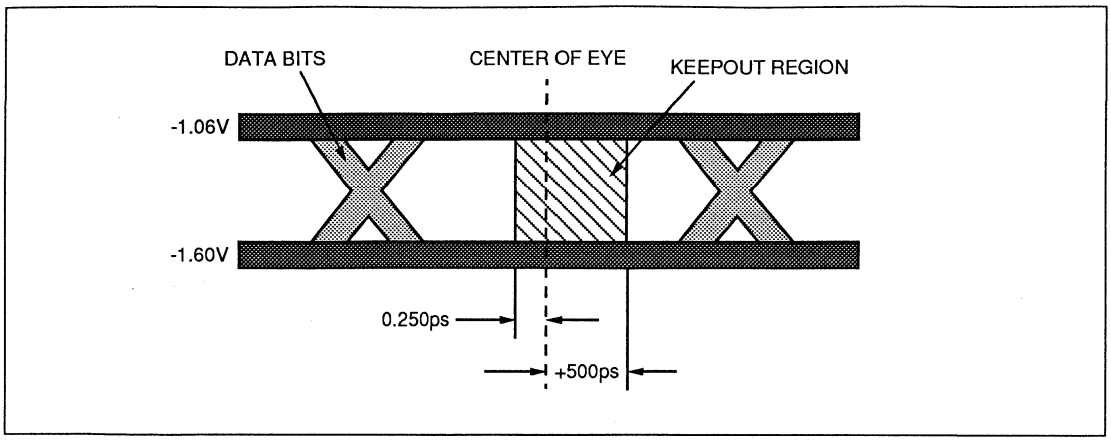


Figure 2: Data Eye

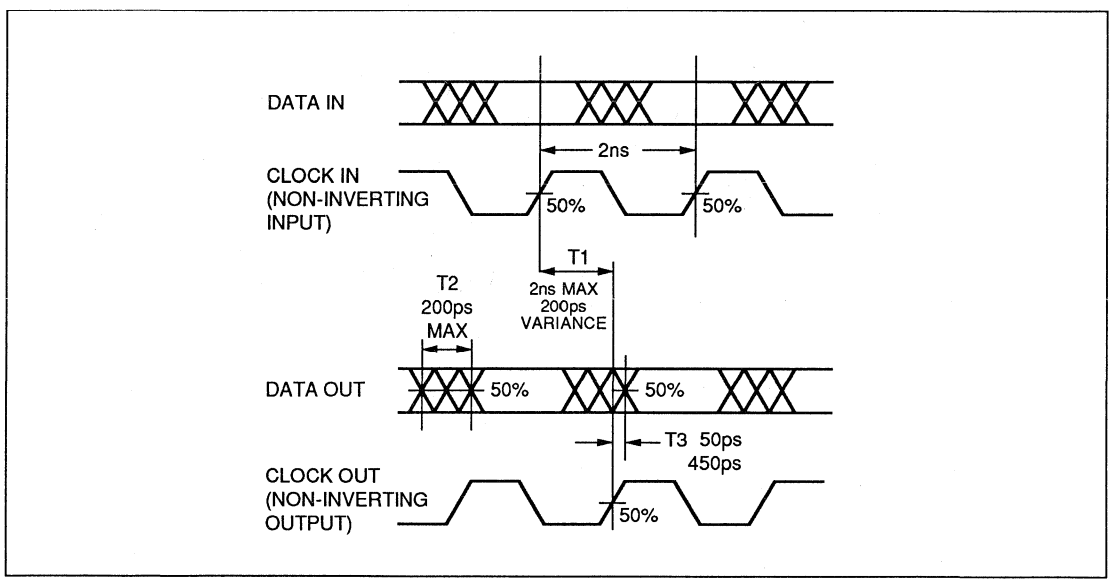


Figure 3: ACCROM Timing

DC CHARACTERISTICS AND RATINGS

Positive Supply Voltage	V_{CC}	6.0V
Negative Supply Voltage	V_{EE}	-6.0V
Input Voltage (TTL)	V_{IN}, TTL	-0.5V to V_{CC}+0.5V
RF Clock Input Power	P_{IN}	10dbm
Thermal Resistance	Θ_{JC}	15°C/W max
Ambient Storage Temp. Range	T_{stg}	-65 to +150°C
Maximum Junction Temp.	T_J	+150°C
Operating Case Temp. Range	T_{op}	-20 to +85°C *

Figure 4: Absolute Maximum Ratings

* This device has been designed to meet the AC/DC performance characteristics with a function temperature from -20 to +100°C. It is possible to use the device with junction temperatures from -55 to +150°C without damage. However, outputs will not be ECL 10kH compatible outside the design temperature range.

Symbol	Parameter	Conditions (Note 1)	Min	Max	Units
V_{IH} (TTL)	TTL Input High Voltage	-	2.0	V_{CC}	V
V_{IL} (TTL)	TTL Input Low Voltage	-	0	0.8	V
V_{OH} (ECL)	ECL Output High Voltage (Note 3)	-	V_{REF}+0.3	-0.5	V
V_{OL} (ECL)	ECL Output Low Voltage (Note 3)	-	V_{TT}	V_{REF}-0.3	V
V_{REF1}	V_{REF} Output Voltage (Note 4)	-	V_{RE-50}	V_{RE+50}	mV
V_{REF2}		-	-1.5	-1.1	V
I_{IH} (TTL)	TTL Input High Current (Note 2)	V_{IH}=V_{CC}	-	200	µA
I_{IL} (TTL)	TTL Input Low Current (Note 2)	V_{IL}=0Vdc	-	-100	µA
I_{CC}	Positive Supply Current	V_{CC}=+5.5vdc, Outputs Open	-	20	mA
I_{EE}	Negative Supply Current	V_{EE}=-5.5vdc, Outputs Open	-	450	mA

Notes: 1. Unless otherwise specified, -5.5V≤V_{EE}≤-4.9V; 4.9V≤V_{CC}≤5.5V; ECL outputs including V_{REF} shall be tied to V_{TT}=-2.1±0.1V through 50Ω and 50pF; T_{case}=[-20, +25, +85]°C.

2. Guaranteed but not tested at -20°C.
3. Measure at V_{EE}=-5.5V, V_{CC}=+5.5V, V_{TT}=-2.2V
4. $V_{RE}=\frac{V_{OH}(ECL)+V_{OL}(ECL)}{2}$
5. Mil-Std-883, method 5005, subgroups 1, 2, 3.

Figure 5: DC Characteristics

Symbol	Parameter	Conditions
F_T	Functionality	V_{EE} -5.5V, V_{CC} +5.5V, freq = 1MHz V_{EE} -4.9V, V_{CC} +4.9V, freq = 1MHz V_{ILT} = 0.8V, V_{IHT} = 2.0V, V_{TT} = -2.1±0.1V Through 50Ω and 50pF. T_{CASE} = -20 to +85°C

1. Mil-Std-883, method 5005, subgroups 7, 8A, 8B

Figure 6: Functionality

AC CHARACTERISTICS (Note 9)

Symbol	Parameter	Conditions (Note 1)	Min	Max	Units
	Input Signals				
t_r (TTL)	TTL Rise Time	0.8 to 2.0V	-	20	ns
t_f (TTL)	TTL Fall Time	2.0 to 0.8V	-	20	ns
f_{TTLMAX}	TTL Inpt Data Rate	-	20	-	kHz
f_{CLOCK}	RF Clock Frequency (Note 6)	-	500	-	MHz
-	RF Clock Input Voltage (Note 6)	RF CLKN=-1.3±0.1V	600	1200	mVp-p
-	RF Clock Duty Cycle	-	45	55	%
	Output Signals				
V_{OH} (ECL)	Output High (Notes 3, 7)	DATA=004100_{HEX} measured in a window of -250/+500ps around center of data eye (see Figure 3)	V_{REF}+0.25	-	V
V_{OL} (ECL)	Output Low (Notes 3, 7)	DATA=004100_{HEX} measured in a window of -250/+500ps around center of data eye (see Figure 3)	-	V_{REF}-0.25	V
t_r/t_f	Output Rise/Fall Times (Note 3)	20% to 80%	-	-	-
t_r/t_{f1}	Data Outputs (Note 3)	-	-	500	ps
t_r/t_{f2}	RF Clock Output (Note 3)	-	-	400	ps
T_2	Output Data Skew (Notes 3, 8)	See Figure 4	-	200	ps
T_3	Clock Output to Data Skew (Note 3)	See Figure 4	-	450	ps
T_1	Clock In to Clock Out Delay (Note 9)	See Figure 4	-	2	ns
-	Clock Delay Variation Over Temp. and Supply Condition Of (Note 1)	-	-	200	ps
-	Maximum Output Frequency	-	(Note 10)	-	MHz
t_{SETTLE}	Time From Last Valid Input Data to Valid Output Data (Notes 3, 6)	-	-	50	ns
-	Input Clock to Output Clock Duty Cycle Degradation	-	-2.4	2.4	%
	RF Performance (Note 9)				
-	Residual Phase Noise at Clock Output (due to ACC/ROM only) (Notes 9, 11)	$f_{out}=3/8xf_{CLK}$ IN; 100kHz offset from carrier	-	-145	dBc/Hz
-	Average Output Clock Jitter (Notes 3, 11)	-	-	10	ps

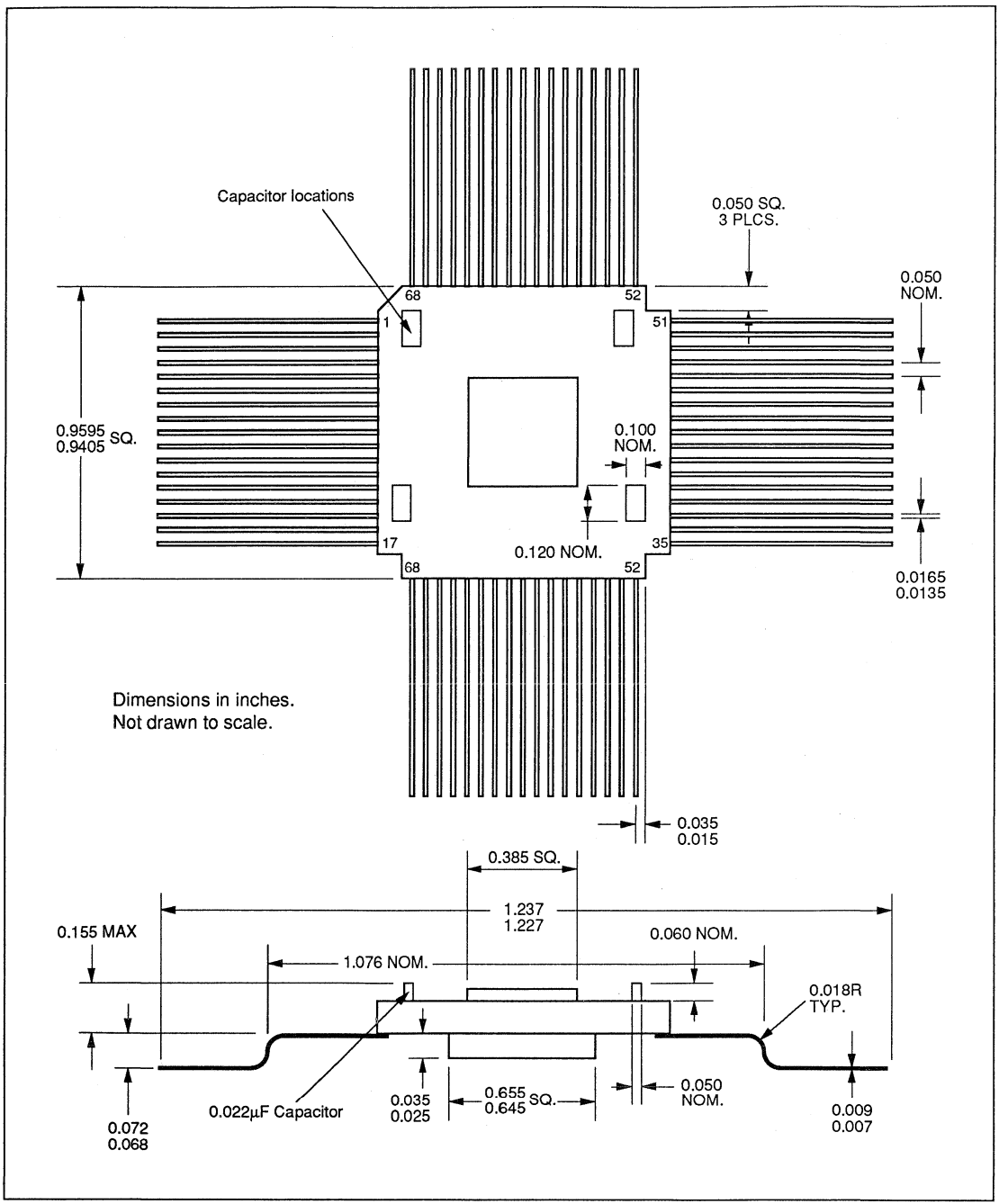
Notes: 1. Unless otherwise specified, $-5.5V \le V_{EE} \le -4.9V$; $4.9V \le V_{CC} \le 5.5V$; ECL outputs including V_{REF} shall be tied to V_{TT}=-2.1±0.1V through 50Ω and 50pF; T_{case}=[-20, +25, +85]°C.
3. Measure at V_{EE}=-5.5V, V_{CC}=+5.5V, V_{TT}=-2.2V
6. Guaranteed, but not tested only under conditions specified in note 5.
7. Parallel input data (binary)=(msb) 0 0000 0100 0001 0000 0000 (lsb).
8. Data skew is the time from the 50% point of the first valid output to the 50% point of the last valid output.
9. Guaranteed by characterisation but not tested.
10. f_{CLOCK}/2-1LSB.
11. Clock measured single ended.

Figure 7: AC Characteristics

Subgroup	Definition
1	Static characteristics specified in Figure 5 at +25°C case temperature
2	Static characteristics specified in Figure 5 at +85°C case temperature
3	Static characteristics specified in Figure 5 at -20°C case temperature
7	Functional characteristics specified in Figure 6 at +25°C case temperature
8a	Functional characteristics specified in Figure 6 at +85°C case temperature
8b	Functional characteristics specified in Figure 6 at -20°C case temperature
9	Switching characteristics not yet available
10	Switching characteristics not yet available
11	Switching characteristics not yet available

Table 8: Definition of Subgroups

PACKAGE OUTLINE

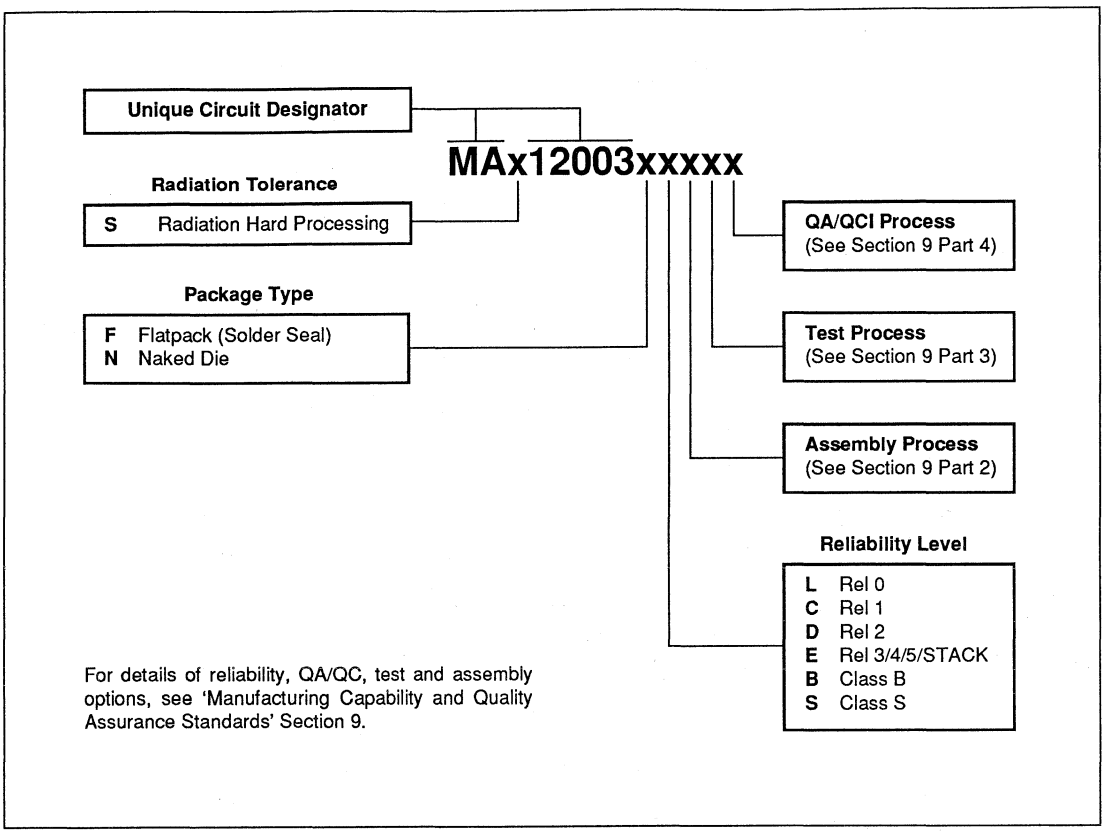


PIN DESCRIPTIONS

Pin No.	Signal Name	Description
3	D11	Data output (ECL) . . . LSB+1
4	D10	Data output (ECL) . . .
6	D9	Data output (ECL) . . .
7	D8	Data output (ECL) . . .
9	D7	Data output (ECL) . . .
10	D6	Data output (ECL) . . .
12	D5	Data output (ECL) . . .
13	D4	Data output (ECL) . . .
15	D3	Data output (ECL) . . .
16	D2	Data output (ECL) . . .
20	D1	Data output (ECL) . . . MSB
21	NC	No connection
23	OCLK (Note 2)	True output of differential clock output (ECL)
24	OCLKN	Complement of differential clock output (ECL)
26	RESET	Reset input (TTL) . . . active high
27	A(20)	Parallel data input (TTL) . . . MSB
29	A(19)	Parallel data input (TTL) . . .
30	A(18)	Parallel data input (TTL) . . .
32	A(17)	Parallel data input (TTL) . . .
33	A(16)	Parallel data input (TTL) . . .
37	A(15)	Parallel data input (TTL) . . .
38	A(14)	Parallel data input (TTL) . . .
40	A(13)	Parallel data input (TTL) . . .
41	A(12)	Parallel data input (TTL) . . .
43	A(11)	Parallel data input (TTL) . . .
44	A(10)	Parallel data input (TTL) . . .
46	A(9)	Parallel data input (TTL) . . .
47	A(8)	Parallel data input (TTL) . . .
49	A(7)	Parallel data input (TTL) . . .
50	A(6)	Parallel data input (TTL) . . .
54	A(5)	Parallel data input (TTL) . . .
55	A(4)	Parallel data input (TTL) . . .
57	A(3)	Parallel data input (TTL) . . .
58	A(2)	Parallel data input (TTL) . . .
60	A(1)	Parallel data input (TTL) . . .
61	A(0)	Parallel data input (TTL) . . . LSB
63	ICLKN	Complement of differential clock input (ECL)
64	ICLK (Note 3)	True input of differential clock input (ECL)
66	VREF	ECL reference
67	D12	Data output (ECL) . . . LSB

Notes: 1. Pins 1, 35 = V_{EE} = -5.2V; pins 18, 52 = V_{CC} = +5.2V; pins 2, 5, 8, 11, 14, 17, 19, 22, 25, 28, 31, 34, 36, 39, 42, 45, 48, 51, 53, 56, 59, 62, 65, 68 = GND.
2. Output data transitions on the rising edge of OCLK.
3. Input data is captured on the rising edge of ICLK.
4. The output of this device is not phase continuous during the settling time, t_{SETTLE}.
5. The package thermal characteristics are designed such that the die junction temperature will be 100°C maximum when the case temperature is 85°C.
6. The reset input is active high.
7. For proper operation, input rise/fall times (20 to 80%) should be 10ns maximum.
8. The impedance of the clock input is 1kilohm in parallel with 4pF (typical).

ORDERING INFORMATION



For details of reliability, QA/QC, test and assembly options, see 'Manufacturing Capability and Quality Assurance Standards' Section 9.

Section 9

Manufacturing Capability Document

GEC PLESSEY
SEMICONDUCTORS

PART 1

Introduction and Using the Document

Introduction

At the GPS Lincoln site, a systematic manufacturing code has been adopted to enable easier specification of the manufacturing and quality inspection requirements for all integrated circuits.

The new code is directly related to process modules on the site CAM system. This minimises the risk of any process related manufacturing errors whilst at the same time enabling a large variety of flow options to be offered to the customer.

This capability document attempts to present the new code and the manufacturing options offered by it in a concise manner. Information is also contained on related issues such as radiation testing and class S datapacks.

Please consult with factory services or marketing in Lincoln if any more information is required.

Using the Manufacturing Capability Document.

On the next page is a diagram showing the form of the device name and manufacturing code used for integrated circuits at GPS Lincoln.

Each empty "box" represents an alphabetic character. The options for the first three of these "boxes" are shown on the diagram. Reference to parts 2, 3 and 4 of this document will explain in detail the assembly, test and QA/QCI options offered for the last three. Using just five characters after the device name in this way allows for many package, rel and manufacturing options to be specified whilst causing a minimum of confusion.

In parts 2, 3 and 4 the specific options for each manufacturing area are indicated by letters in the appropriate character position. Parts of the code not applicable to that area are simply shown using a "-" character.

The document can be used in two ways, either as a reference to check what a particular code represents or as an options specification to build up the code for a specific requirement.

For example: A device of name: **MAS17501FSBAF**

The letter S at position MA**S**I7501FSBAF signifies a rad hard process.
The letter F at position MAS17501**F**SBAF signifies a flatpack package.
The letter S at position MASI7501F**S**BAF signifies Class S manufacture.

The code BAF is built up using parts 2, 3 and 4 of the document as follows:

S	B			for the assembly process (from Part 2)
S		A		for the test process (from Part 3)
S			F	for the QA/QCI process (from Part 4)

Thus, device **MAS17501FSBAF** is manufactured on a rad hard process, in a flatpack package to a standard space assembly but less PIND and bond pull tests. It is then tested to a standard (3 burnin) MILSTD Class S test process and is subject to a QCI involving group A and B tests, with generic group D data being supplied with the shipment.

Note regarding naked dice:

The manufacturing code for naked dice consists of three letters.

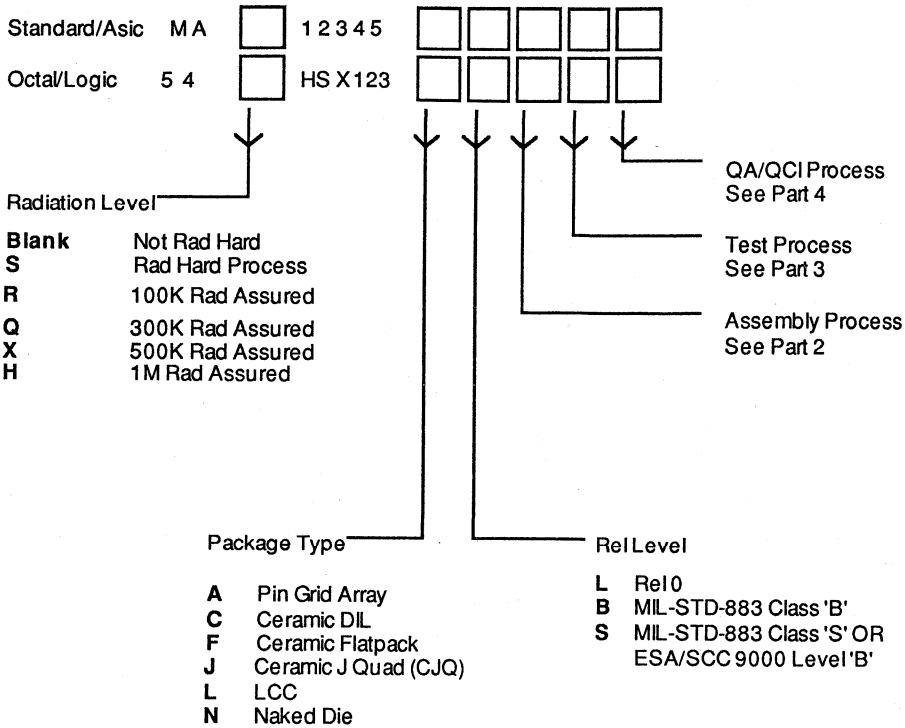
First letter : is always N

Second letter : describes the optical inspection criteria as follows;
C (Rell/Commercial with 2nd optical inspection to BS9400)
B (Class B with 2nd optical inspection to MILSTD 883 2010 condition B)
S (Class S with 2nd optical inspection to MILSTD 883 2010 condition A)

Third letter : describes whether a "per lot" sample is taken for assembly and test analysis before shipment;
A No sample required.
B Sample required to datasheet or customer specification.

For example : NBA represents MILSTD class B inspection with no sampling. NSB represents MILSTD class S inspection with sampling.

Structure of IC name and Manufacturing Code



NOTE : For naked dice, the last two code letters are not applicable.
For wafers, the last four code letters are not applicable.

Guide to Radiation Testing

Steady state total dose radiation testing is performed to ensure that the radiation performance of a device meets the required standard as specified by the "radiation level" letter in the IC manufacturing code (see page 4).

Radiation testing procedures are based on, and are compatible with, the requirements of MIL STD 883, method 5005.

Note that neutron irradiation performance (subgroup 1) is not checked on SOS technology but a neutron fluence in excess of 10^{15} neutrons/cm^2 is generically guaranteed. Similarly, transient ionising radiation performance (subgroup 3) is not checked but is generically guaranteed to be in excess of 10^{10} rads/sec for upset and in excess of 10^{12} rads/sec for survivability.

Sampling Plans for Radiation Testing

The table below indicates the standard sampling plans offered for both class B and class S products. These meet the requirements of the majority of customers whilst being the most economic in terms of devices used. Note that, although strictly speaking the MILSTD requirement for class S is always to use a qualification by wafer, this is often considered to be over zealous and a qualification by lot is usually specified as being adequate.

If sampling plans are unspecified GPS will, as standard, perform a lot qualification for all except small octal/logic devices which undergo a wafer qualification.

Special, customer specific sampling plans can be implemented on request. These must be detailed at the time of order placement.

Type of Qualification :	Device Category :	Sampling Plan :
Qualification by lot :	All devices	5 units/lot (0)
Qualification by wafer :	< 4000 transistors	4 units/wafer (0) *
	> 4000 transistors	2 units/wafer (0) *

The number in brackets indicates the quantity of fails allowed.

* Up to a maximum of 22 per lot for Class B only (this quantity would then fully satisfy the MIL-STD lot requirement.

Devices having < 4000 transistors are typically octals, logic's and small ASICs.

Devices having > 4000 transistors are typically RAMs, 1750 microprocessors, peripherals and larger ASICs.

GPS reserve the right to perform a wafer qualification even if only a lot qualification has been specified if this is felt to be justified for technical reasons.

Biasing Arrangements for Radiation Testing

All standard parts have biasing configurations which have been designed to apply worst case conditions to devices undergoing irradiation. Details of these biasing arrangements are available on request. Special biasing configurations to individual customer specifications can be used if required but this may lead to an increased leadtime and cost.

PART 2

Assembly Processes

Assembly Processes

Manufacturing Code	REL Level	Description	Page
- L B - -	REL 0	Solder Seal, DIL/Flatpack Packages	7
- L D - -	REL 0	Solder Seal, PGA/LCC/CJQ Packages	7
- B A - -	MIL-STD-883 Class B	Standard Solder Seal, DIL/Flatpack Packages (Note 2)	8
- B B - -	MIL-STD-883 Class B	Standard Solder Seal, PGA/LCC/CJQ Packages (Note 2)	8
- B C - -	MIL-STD-883 Class B	Solder Seal, DIL/Flatpack Packages with PIND and Customer Precap (Note 2)	8
- B D - -	MIL-STD-883 Class B	Solder Seal, DIL/Flatpack Packages with PIND (Note 2)	8
- B E - -	MIL-STD-883 Class B	Solder Seal, DIL/Flatpack Packages with Solder Dip (Note 2)	8
- B F - -	MIL-STD-883 Class B	Solder Seal, PGA/LCC/CJQ Packages with PIND and Customer Precap (Note 2)	9
- B G - -	MIL-STD-883 Class B	Solder Seal, PGA/LCC/CJQ Packages with PIND (Note 2)	9
- B H - -	MIL-STD-883 Class B	Standard Solder Seal, DIL/Flatpack Packages with Serial Number Traceability (Note 2)	9
- B I - -	MIL-STD-883 Class B	Standard Solder Seal, PGA/LCC/CJQ Packages with Serial Number Traceability (Note 2)	9
- S A - -	MIL-STD-883 Class S	Standard Solder Seal, DIL/Flatpack Packages (Note 2)	10
- S B - -	ESA 9000 Level C	Standard Solder Seal, DIL/Flatpack Packages	11
- S C - -	ESA 9000 Level B	Standard Solder Seal, DIL/Flatpack Packages (Note 1)	11
- S D - -	MIL-STD-883 Class S	Standard Solder Seal, PGA/LCC/CJQ Packages (Note 2)	10
- S E - -	ESA 9000 Level C	Standard Solder Seal, PGA/LCC/CJQ Packages	11
- S F - -	ESA 9000 Level B	Standard Solder Seal, PGA/LCC/CJQ Packages (Note 1)	11
- S L - -	MIL-STD-883 Class S	Standard Solder Seal, Flatpacks with 2 tier bonding	10

Note

1. GEC Plessey Semiconductors is ESA/SCC 9000 Capability Approved to manufacture 2.5/3µm SOS products on these flows.
2. GEC Plessey Semiconductors is Self Certified to MIL-STD-883 paragraph 1.2.1 for the manufacture of Class 'B' and 'S' Devices.

REL 0 - Assembly Flows

Operation	Assembly Rel 0 Manufacturing Codes	
	-LB--	-LD--
Pack Offshore Wafers for Shipment		
Tracking Offshore Assembly		
Incoming Inspection of Devices Assembled Offshore		
Die Attach	♦	♦
Inspect Die Attach (Low Power)	♦	♦
Wire Bond	♦	♦
3rd Optical Inspection	♦	♦
QA 3rd Optical Inspection	♦	♦
Solder Seal	♦	♦
Glass Seal		
Plate Glass Seal Packages		
Solder Dip		
Gross Leak		
Symbolise	♦	♦
Crop Leads	♦	
QA Visual Inspection	♦	♦

Key : ♦ indicates operation performed.

MIL-STD-883 Class B - Assembly Flows

Operation	Assembly MIL-STD-883 Class B Manufacturing Codes				
	-BA--	-BB--	-BC--	-BD--	-BE--
Die Attach	♦	♦	♦	♦	♦
Die Attach Inspection (Low Power)	♦	♦	♦	♦	♦
Die Attach Inspection (High Power)			♦		
QA Die Attach Inspection	♦	♦	♦	♦	♦
Wire Bond	♦	♦	♦	♦	♦
3rd Optical Inspection	♦	♦	♦	♦	♦
QA 3rd Optical Inspection	♦	♦	♦	♦	♦
Customer Precap			♦		
Solder Seal	♦	♦	♦	♦	♦
QA Seal Inspection	♦	♦	♦	♦	♦
Temperature Cycle (10 Cycles)	♦	♦	♦	♦	♦
Centrifuge	♦	♦	♦	♦	♦
PIND Test			♦	♦	
QA PIND Test Inspection			♦	♦	
Symbolise	♦	♦	♦	♦	♦
Serialise			♦		
Fine Leak Test	♦	♦	♦	♦	♦
Gross Leak Test	♦	♦	♦	♦	♦
Crop Leads	♦		♦	♦	♦
Solder Dip					♦
QA Visual Inspection	♦	♦	♦	♦	♦

Key : ♦ indicates operation performed.

MIL-STD-883 Class B - Assembly Flows

Operation	Assembly MIL-STD-883 Class B Manufacturing Codes			
	-BF--	-BG--	-BH--	-BI--
Die Attach	♦	♦	♦	♦
Die Attach Inspection (Low Power)	♦	♦	♦	♦
Die Attach Inspection (High Power)	♦			
QA Die Attach Inspection	♦	♦	♦	♦
Wire Bond	♦	♦	♦	♦
3rd Optical Inspection	♦	♦	♦	♦
QA 3rd Optical Inspection	♦	♦	♦	♦
Customer Precap	♦			
Solder Seal	♦	♦	♦	♦
QA Seal Inspection	♦	♦	♦	♦
Temperature Cycle (10 Cycles)	♦	♦	♦	♦
Centrifuge	♦	♦	♦	♦
PIND Test	♦	♦		
QA PIND Test Inspection	♦	♦		
Symbolise	♦	♦	♦	♦
Serialise	♦		♦	♦
Fine Leak Test	♦	♦	♦	♦
Gross Leak Test	♦	♦	♦	♦
Crop Leads			♦	
Solder Dip				
QA Visual Inspection	♦	♦	♦	♦

Key : ♦ indicates operation performed.

MIL-STD-883 Class S - Assembly Flows

Operation	MIL-STD-883 Class S Assembly Manufacturing Codes		
	-SA--	-SD--	-SL--
Die Attach	♦	♦	♦
Die Attach Inspection (Low Power)	♦	♦	♦
Die Attach Inspection (High Power)	♦	♦	♦
QA Die Attach Inspection	♦	♦	♦
Wire Bond	♦	♦	
100% Non-Destructive Bond Pull	♦	♦	
Wire Bond (lower tier)			♦
100% Non-Destructive Bond Pull (lower tier)			♦
Wire Bond (upper tier)			♦
100% Non-Destructive Bond Pull (upper tier)			♦
Space 3rd Optical Inspection	♦	♦	♦
QA Space 3rd Optical Inspection	♦	♦	♦
Customer Precap	♦	♦	♦
Solder Seal	♦	♦	♦
QA Seal Inspection	♦	♦	♦
Temperature Cycle (10 Cycles)	♦	♦	♦
Centrifuge	♦	♦	♦
PIND Test	♦	♦	♦
QA PIND Test Inspection	♦	♦	♦
Symbolise	♦	♦	♦
Serialise	♦	♦	♦
Radiographic Inspection	♦	♦	♦
Crop Leads	♦		♦
QA Visual Inspection and Final Check	♦	♦	♦

Key : ♦ indicates operation performed.

ESA/SCC 9000 Level B and C - Assembly Flows

Operation	ESA/SCC 9000 Assembly Manufacturing Codes			
	-SB--	-SC--	-SE--	-SF--
Die Attach	♦	♦	♦	♦
Die Attach Inspection (Low Power)	♦	♦	♦	♦
Die Attach Inspection (High Power)	♦	♦	♦	♦
QA Die Attach Inspection	♦	♦	♦	♦
Wire Bond	♦	♦	♦	♦
Space 3rd Optical Inspection	♦	♦	♦	♦
QA Space 3rd Optical Inspection	♦	♦	♦	♦
Customer Precap	♦	♦	♦	♦
Solder Seal	♦	♦	♦	♦
QA Seal Inspection	♦	♦	♦	♦
High Temperature Storage (48 hours)	♦	♦	♦	♦
Temperature Cycle (10 Cycles)	♦	♦	♦	♦
Centrifuge	♦	♦	♦	♦
PIND Test		♦		♦
QA PIND Test Inspection		♦		♦
Symbolise	♦	♦	♦	♦
Serialise	♦	♦	♦	♦
Radiographic Inspection		♦		♦
Crop Leads	♦	♦		
QA Visual Inspection and Final Check	♦	♦	♦	♦

Key : ♦ indicates operation performed.

PART 3

Test Processes

Test Processes

Manufacturing Code	Standard	Description	Page
- L - B -	REL 0	Standard	15
- B - A -	MIL-STD-883 Class B	Standard (Note 2)	16
- B - B -	MIL-STD-883 Class B	With Datalogs (Note 2) (Assembly Flow must include Serialisation)	16
- B - C -	MIL-STD-883 Class B	With Datalogs and Delta Calculations (Note 2) (Assembly Flow must include Serialisation)	16
- B - D -	MIL-STD-883 Class B	With Two Special Static Burnins, Datalogs and Delta Calculations (Note 2) (Assembly Flow must include Serialisation)	16
- B - E -	MIL-STD-883 Class B	With Solder Dip (Note 2) (LCC packages only)	16
- B - F -	MIL-STD-883 Class B	With 240 Hour Burnin, Datalogs and Delta Calculations (Note 2) (Assembly Flow must include Serialisation)	17

Note

1. These manufacturing flows are based on MIL-STD-883 Method 5004 but include variations.
2. GEC Plessey Semiconductors is Self Certified to MIL-STD-883 paragraph 1.2.1 for the manufacture of Class 'B' and 'S' Devices.

Test Processes

Manufacturing Code	Standard	Description	Page
- S - A -	MIL-STD-883 Class S	Standard (Note 4)	18
- S - B -	MIL-STD-883 Class S	With Two 48 Hour Static Burnins (Note 4)	18
- S - C -	MIL-STD-883 Class S	With No Static Burnin (Note 1)	18
- S - D -	MIL-STD-883 Class S	With No Static Burnin but a 168 Hour Pre Conditioning Dynamic Burnin (Note 1)	18
- S - E -	MIL-STD-883 Class S	With One 48 Hour Static Burnin (Note 4)	18
- S - F -	ESA 9000 Level B	Standard (Note 2)	22
- S - G -	ESA 9000 Level B	With 48 Hour Static Burnins	22
- S - H -	ESA 9000 Level B	With No Static Burnins	22
- S - I -	ESA 9000 Level C	Standard (168 hour burnin)	22
- S - K -	MIL-STD-883 Class S	With Two 96 Hour Static Burnins (Note 4)	19
- S - L -	MIL-STD-883 Class S	With Three 96 Hour Static Burnins (Note 3,4)	19
- S - M -	MIL-STD-883 Class S	For packages with External Capacitors Fitted (Note 4)	20
- S - N -	MIL-STD-883 Class S	With One 48 Hour Static Burnin for packages with External Capacitors Fitted (Note 1)	20
- S - O -	MIL-STD-883 Class S	With Two 48 Hour Static Burnin and extra 85°C hot test (Note 1)	21
- S - P -	MIL-STD-883 Class S	Standard, with extra engineering analysis tests (Note 1)	21
- S - Q -	MIL-STD-883 Class S	With 48 Hour Static Burnin stages and extra engineering analysis tests (Note 1)	21
- S - R -	MIL-STD-883 Class S	With 48 Hour Static Burnins, extra 85°C hot test and extra engineering analysis tests (Note 1)	21

Note

1. These manufacturing flows are based on MIL-STD-883 Method 5004 but include variations.
2. GEC Plessey Semiconductors is ESA/SCC 9000 Capability Approved to manufacture 2.5/3µm SOS products on these flows.
3. This flow should only be used on devices whose tristate outputs can be disabled during burnin.
4. GEC Plessey Semiconductors is Self Certified to MIL-STD-883 paragraph 1.2.1 for the manufacture of Class 'B' and 'S' Devices.

REL 0 - Test Flows

Operation	Rel 0 Test Manufacturing Codes
	-L-B-
Test 25°C	♦
Test 25°C / Pack / Inspect	
Test 125°C	
Test -55°C	
Pack / Inspect	♦
0.1% AQL Sample Test	
Ship to Stores	
Tape and Reel Pack	
Ship	♦

Key : ♦ indicates operation performed.

MIL-STD-883 Class B - Test Flows

Operation	MIL-STD-883 Class B Test Manufacturing Codes				
	-B-A-	-B-B-	-B-C-	-B-D-	-B-E
Initial Test @ 25°C	♦				♦
Initial Test @ 125°C		♦	♦	♦	
Pre Burnin Test @ 25°C (Datalogs)		♦			
Pre Burnin Test @ 25°C (Datalogs/Deltas)			♦	♦	
Datalog Check		♦	♦	♦	
Static 1 Burnin (24 Hours)				♦	
Int. 1 Test @ 25°C (Datalogs/Deltas)				♦	
Datalog Check				♦	
Static 2 Burnin (24 Hours)				♦	
Int. 2 Test @ 25°C (Datalogs/Deltas)				♦	
Datalog Check				♦	
Dynamic Burnin (168 Hours)	♦	♦	♦	♦	♦
Final Test @ 25°C	♦				♦
Final Test @ 25°C (Datalogs)		♦			
Final Test @ 25°C (Datalogs/Deltas)			♦	♦	
Datalog Check		♦	♦	♦	
Final Test @ 125°C	♦				♦
Final Test @ 125°C (Datalogs)		♦	♦	♦	
Datalog Check		♦	♦	♦	
Final Test @ -55°C	♦				♦
Final Test @ -55°C (Datalogs)		♦	♦	♦	
Datalog Check		♦	♦	♦	
PDA Calculation		♦	♦	♦	
Solder Dip					♦
Pack and Lead Inspection	♦	♦	♦	♦	♦
Ship to FPA	♦	♦	♦	♦	♦

Key : ♦ indicates operation performed

MIL-STD-883 Class B - Test Flows

Operation	MIL-STD-883 Class B Test Manufacturing Codes
	-B-F-
Initial Test @ 125°C	♦
Pre Burnin Test @ 25°C (Datalogs/Deltas)	♦
Datalog Check	♦
Dynamic Burnin (240 Hours)	♦
Final Test @ 25°C (Datalogs/Deltas)	♦
Datalog Check	♦
Final Test @ 125°C (Datalogs)	♦
Datalog Check	♦
Final Test @ -55°C (Datalogs)	♦
Datalog Check	♦
PDA Calculation	♦
Pack and Lead Inspection	♦
Ship to FPA	♦

Key : ♦ indicates operation performed

MIL-STD-883 Class S - Test Flows

Operation	MIL-STD-883 Class S Test Manufacturing Codes				
	-S-A-	-S-B-	-S-C-	-S-D-	-S-E-
Initial Test @ 125°C	♦	♦	♦	♦	♦
Pre Burnin Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦	♦
Static 1 Burnin (24 Hours)	♦				
Static 1 Burnin (48 Hours)		♦			♦
Int. 1 Test @ 25°C (Datalogs/Deltas)	♦	♦			♦
Datalog Check	♦	♦			♦
Static 2 Burnin (24 Hours)	♦				
Static 2 Burnin (48 Hours)		♦			
Int. 2 Test @ 25°C (Datalogs/Deltas)	♦	♦			
Datalog Check	♦	♦			
Dynamic Burnin (168 Hours)				♦	
Post Pre-conditioning Test @ 25°C (Datalogs/Deltas)				♦	
Datalog Check				♦	
Dynamic Burnin (240 Hours)	♦	♦	♦	♦	♦
Final Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦	♦
Final Test @ 125°C (Datalogs)	♦	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦	♦
Final Test @ -55°C (Datalogs)	♦	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦	♦
Fine and Gross Leak	♦	♦	♦	♦	♦
PDA Calculation	♦	♦	♦	♦	♦
Ship to FPA	♦	♦	♦	♦	♦

Key : ♦ indicates operation performed

MIL-STD-883 Class S - Test Flows

Operation	MIL-STD-883 Class S Test Manufacturing Codes	
	-S-K-	-S-L-
Initial Test @ 125°C	♦	♦
Pre Burnin Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Static 1 Burnin (96 Hours)	♦	♦
Int. 1 Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Static 2 Burnin (96 Hours)	♦	♦
Int. 2 Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Static 3 Burnin (96 Hours)		♦
Int. 3 Test @ 25°C (Datalogs/Deltas)		♦
Datalog Check		♦
Dynamic Burnin (240 Hours)	♦	♦
Final Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Final Test @ 125°C (Datalogs)	♦	♦
Datalog Check	♦	♦
Final Test @ -55°C (Datalogs)	♦	♦
Datalog Check	♦	♦
Fine and Gross Leak	♦	♦
PDA Calculation	♦	♦
Ship to FPA	♦	♦

Key : ♦ indicates operation performed

MIL-STD-883 Class S with External Capacitors - Test Flows

Operation	MIL-STD-883 Class S with External Capacitors - Test Manufacturing Codes	
	-S-M-	-S-N-
Initial Test @ 125°C	♦	♦
Pre Burnin Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Static 1 Burnin (24 Hours)	♦	
Static 1 Burnin (48 Hours)		♦
Int. 1 Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Static 2 Burnin (24 Hours)	♦	
Int. 2 Test @ 25°C (Datalogs/Deltas)	♦	
Datalog Check	♦	
Dynamic Burnin (240 Hours)	♦	♦
Final Test @ 25°C (Datalogs/Deltas)	♦	♦
Datalog Check	♦	♦
Final Test @ 125°C (Datalogs)	♦	♦
Datalog Check	♦	♦
Final Test @ -55°C (Datalogs)	♦	♦
Datalog Check	♦	♦
Fine and Gross Leak	♦	♦
Fit External Capacitors	♦	♦
Conformal Coating	♦	♦
Inspect	♦	♦
Final Test @ 25°C	♦	♦
PDA Calculation	♦	♦
Ship to FPA	♦	♦

Key : ♦ indicates operation performed

MIL-STD-883 Class S - Test Flows

Operation	MIL-STD-883 Class S Test Manufacturing Codes			
	-S-O-	-S-P-	-S-Q-	-S-R-
1st Engineering Test (Datalogs)		♦	♦	♦
2nd Engineering Test (Datalogs)		♦	♦	♦
Engineering Data Analysis		♦	♦	♦
Initial Test @ 125°C	♦	♦	♦	♦
Pre Burnin Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦
Static 1 Burnin (24 Hours)		♦		
Static 1 Burnin (48 Hours)	♦		♦	♦
Int. 1 Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦
Static 2 Burnin (24 Hours)		♦		
Static 2 Burnin (48 Hours)	♦		♦	♦
Int. 2 Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦
Dynamic Burnin (240 Hours)	♦	♦	♦	♦
Final Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦
Final Test @ 85°C (Datalogs)	♦			♦
Datalog Check	♦			♦
Final Test @ 125°C (Datalogs)	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦
Final Test @ -55°C (Datalogs)	♦	♦	♦	♦
Datalog Check	♦	♦	♦	♦
Fine and Gross Leak	♦	♦	♦	♦
PDA Calculation	♦	♦	♦	♦
Ship to FPA	♦	♦	♦	♦

Key : ♦ indicates operation performed

ESA/SCC 9000 Level B and C - Test Flows

Operation	ESA/SCC 9000 Test Manufacturing Flows			
	-S-F-	-S-G-	-S-H-	-S-I-
Initial Test @ 125°C	♦	♦	♦	♦
Initial Test @ -55°C	♦	♦	♦	♦
Pre Burnin Test @ 25°C				♦
Pre Burnin Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	
Datalog Check	♦	♦	♦	
Static 1 Burnin (24 Hours)	♦			
Static 1 Burnin (48 Hours)		♦		
Int. 1 Test @ 25°C (Datalogs/Deltas)	♦	♦		
Datalog Check	♦	♦		
Static 2 Burnin (24 Hours)	♦			
Static 2 Burnin (48 Hours)		♦		
Int. 2 Test @ 25°C (Datalogs/Deltas)	♦	♦		
Datalog Check	♦	♦		
Dynamic Burnin (168 Hours)				♦
Dynamic Burnin (240 Hours)	♦	♦	♦	
Final Test @ 25°C				♦
Final Test @ 25°C (Datalogs/Deltas)	♦	♦	♦	
Datalog Check	♦	♦	♦	
Final Test @ 125°C				♦
Final Test @ 125°C (Datalogs)	♦	♦	♦	
Datalog Check	♦	♦	♦	
Final Test @ -55°C				♦
Final Test @ -55°C (Datalogs)	♦	♦	♦	
Datalog Check	♦	♦	♦	
Fine and Gross Leak	♦	♦	♦	♦
PDA Calculation	♦	♦	♦	♦
Ship to FPA	♦	♦	♦	♦

Key : ♦ indicates operation performed

PART 4

Quality Conformance Inspection Processes

Class B Options : General

All Class B options include traveller verification and the supply of a certificate of conformance and a test performance report.

All group and sub-group names refer to MIL-STD-883 Method 5005 for class B. Good devices required for group C, D3 and D4 tests are shipped with the order. All other devices used for QCI are scrapped. For LCC packages, group D7 tests are not performed.

The Class B options are shown in tabular form on the next page. A key to this table appears below.

Key to Class B Options Table

Group A :	Group A tests to MIL-STD-883 Method 5005, table 1.
Extra Group A :	Additional group A tests to special request, indicated by suitable package marking.
Group B:	Group B2a, B3 and B5a tests to MIL-STD-883 Method 5005.
Group C :	Group Ca and Cb tests to MIL-STD-883 Method 5005 (using group A test endpoint parameters at 25C, 125C and -55C with read and record data).
Group D:	Group D1, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D5a, D5b, D5c, D6 and D7 tests (using group A test end parameters at 25C for D3 and D4 tests with read and record data).
Devices Typically Required :	Indicates the number of devices over and above the quantity ordered that would be required for QCI using standard MIL-STD-883 rules. This quantity is variableat customer request.

MIL-STD-883 Class B Quality Conformance Inspection Processes

Class B Options Table

Manufacturing Code	Group A	Extra Group A	Group B	Group C	Group D	Devices Typically Required
- B - - A	N	N	N	N	N	0
- B - - B	Y	N	N	N	N	0
- B - - C	Y	N	Y	N	N	4
- B - - D	Y	N	Y	G	G	4
- B - - F	Y	N	Y	Y	G	49
- B - - G	Y	N	Y	Y	Y	84
- B - - M	Y	Y	Y	G	G	4
- B - - N	Y	Y	Y	Y	Y	84

Key to Table

N **Not Carried Out**

Y **Carried Out**

G **Generic Data Supplied**

Class S Options : General

Class S options are divided into two sections, MIL-STD-883 Class S and ESA9000. These are dealt with seperately although some comments apply to them both.

All options, both MIL STD 883 and ESA9000, include the supply of a datapack as follows:

Space Datapack Contents :

Certificate of Conformance

SEM reports

Test Performance report

Radiographic report

PDA calculations

Failed components list

Radiation test results (where appropriate)

Lead certificate

List of devices shipped

List of devices retained

QCI report

Electrical read and record data (in paper or ASCII file form)

Appendix containing any other information (eg concessions)

Quality Conformance Inspection Processes

MIL STD 883 Class S Options

For MIL-STD-883 Class S options, good devices required for B5,B6,D3 and D4 tests are shipped with the order, other QCI devices are scrapped.

The MIL-STD-883 Class S options are shown in tabular form on the next page. A key to this table appears below.

Note that only options -S--F and -S--G comply with the full inspection requirements of MIL-STD-883 Method 5005.

Key to MIL STD Class S Options Table

Group A : Group A tests to MIL-STD-883 Method 5005, table 1. Read and record data available to special order.

Group B : Group B1a, B2a, B2b, B2c, B2d, B3a, B4a, B4b, B5a, B5b, B5c, B6a, B6b, B6c, B6d, B6e tests refer to MIL-STD-883 Method 5005, table IIa for class S. Endpoint parameters for B5 are the group A requirements at 25C, 125C and -55C with read and record data. Read and record data at 240 and 500 hours is available to special order for B5b tests. Endpoint parameters for B6 are the Group A requirements at 25C with read and record data (also available at 125C and -55C to special order).

Group D : Group D1a, D2a, D3a, D3b, D3c, D3d, D3e, D3f, D4a, D4b, D4c, D4d, D4e, D4f, D5a, D5b, D5c, D6a, D7a (not for LCC) tests to MIL-STD-883 Method 5005. One fail is allowed in D6 tests. Endpoint parameters for D3/D4 are the Group A requirements at 25C with read and record data (also available at 125C and -55C to special order).

Indicates the number of devices over and above the quantity Typically ordered that would be required for QCI using standard Required : MIL-STD-883 rules and assuming a single device type. Note that this quantity Is variable at customer request and that QCI quantities may be lotted up across members of a structurally similar chipset if required.

MIL-STD-883 Class S Option Table

Option	Group A	Group B						Group D							Devices Typically Required
		1	2	3	4	5	6	1	2	3	4	5	6	7	
-S--A	N	N	N	N	N	N	N	N	N	N	N	N	N	N	0
-S--B	Y	N	N	N	N	N	N	N	N	N	N	N	N	N	0
-S--C	Y	Generic						Generic							0
-S--D	Y	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	64
-S--F	Y	Y	Y	Y	Y	Y	Y	G	G	G	G	G	G	G	64
-S--G	Y	N	Y	Y	N	Y	Y	Y	Y	Y	Y	Y	Y	Y	99
-S--J	Y	Y	Y	Y	Y	Y	N	N	N	N	N	N	N	N	26
-S--V	N	N	Y	Y	N	Y	N	Y	Y	Y	N	N	N	N	7

Note : -S--V is based on MIL-HBK-339

Key to Table

N	**Not Carried Out**
Y	**Carried Out**
Generic	**Generic Data Supplied**

ESA 9000 Lot Acceptance Test Processes

For ESA 9000 options, end point electrical tests for LAT1 and LAT 2 are performed at 25°C.
Good devices required for LAT 1 and LAT 2 are shipped with the order. LAT 3 electrical verification units are shipped as flight quality units.

LAT 1 : Tests are carried out as follows :

Option	Level 1	Level 2	Level 3
- S - - P	Shock Vibration Acceleration Thermal Shock Moisture Seal Test Electrical Test 25°C External Visual	Operating Life Electrical Test 25°C External Visual	Electrical Test 25°C Electrical Test 125°C Electrical Test -55°C External Visual Solderability Terminal Strength Permanence of Marking

(Devices typically required : 56)

LAT 2 : Tests are carried out as follows :

Option	Level 1	Level 2	Level 3
- S - - Q	No Tests	Operating Life Electrical Test 25°C External Visual	Electrical Test 25°C Electrical Test 125°C Electrical Test -55°C External Visual Solderability Terminal Strength Permanence of Marking

(Devices typically required : 40)

LAT 3 : Tests are carried out as follows :

Option	Level 1	Level 2	Level 3
- S - - R	No Tests	No Tests	Electrical Test 25°C Electrical Test 125°C Electrical Test -55°C External Visual Solderability Terminal Strength Permanence of Marking

(Devices typically required : 25)

Section 10

GEC Plessey Semiconductors Locations

Headquarters Operations

UNITED KINGDOM	Cheney Manor, Swindon, Wiltshire, United Kingdom, SN2 2QW. Tel: (01793) 518000 Fax: (01793) 518411
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel:(408) 438 2900 Fax: (408) 438 5576

Customer Service Centres

FRANCE & BENELUX	Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France.Tel: (1) 69 18 90 00. Fax: (1) 64 46 06 07
GERMANY, AUSTRIA and SWITZERLAND	Ungererstraße 129, 80805 München, Germany. Tel: 089/36 0906-0. Fax: 089/36 0906-55
ITALY	Via Raffaello Sanzio, 4, 20092 Cinisello Balsamo (MILAN). Tel: (02) 66040867. Fax: (02) 66040993.
JAPAN	CTS Kojimachi Building (4th Floor), 2-12, Kojimachi, Chiyoda-ku, Tokyo 102. Tel: (03) 5276-5501. Fax: (03) 5276-5510.
NORTH AMERICA	P O Box 660017, 1500 Green Hills Road, Scotts Valley, California 95067-0017, USA. Tel: (408) 438 2900. Fax: (408) 438 7023
SOUTH EAST ASIA	No. 3 Tai Seng Drive, GEC Building, Singapore 1953. Tel: (65) 3827708. Fax: (65) 3828872
SWEDEN	Katarina Bangata 79, 116 42 Stockholm. Tel: 46 8 7029770. Fax: 46 8 6404736
TAIWAN, ROC	Room 503, 5F, 131 Min-Sheng E Road, Sec 3, Taipei. Tel: 886 2 5461260. Fax: 886 2 7190260
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North American Sales Offices

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Semad, 6815 8th St. N.E., Ste. 175, Calgary, Alberta T2E 7H7.
Tel: (403) 252-5664 Fax: (604) 420-0124.
Semad, 8563 Government St, Burnaby, BC V3N 4S9.
Tel: (604) 420-9889. Fax: (604) 420-0124.

CHINA — **Gain Tune Ltd,** Room 709, Oriental Building, 39 Jianshe Road,
Shenzen, China.Tel: 755-2284970. Fax: 755-2284971.
World Peace Industrial Co Ltd, Room 709, Oriental Building, 39 Jianshe Road,
Shenzen, China.Tel: 755-2284970. Fax: 755-2284972.

CZECH REPUBLIC — **Macro Weil SRO,** Bechynova 3, 160 00 Prague 6.
Tel: 42 2 3112182. Fax: 42 2 24310335.

DENMARK — **Scansupply A/S,** Gladsaxevej 356, DK-2860 Soeborg.
Tel: 45 39 66 50 90. Fax: 45 39 66 50 40.
Scansupply A/S, Marselisborg Havnevej 36, 8000 Arhus C.
Tel: 45 86 12 77 88. Fax: 45 86 12 77 18.

EASTERN EUROPE — **FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany.
Tel: 80 41 41 676 Fax: 80 41 71 504 Tx: 526246 FABD.

FRANCE — **3D:**
6-8 rue Ambroise Croisat, Z.I. des Glaises, 91120 Palaiseau. Tel: 1 64 47 29 29.
Fax: 1 64 47 00 84.
3 rue Berthelot, 69627 Villeurbanne CEDEX. Tel: 72 35 22 00. Fax: 72 34 67 72.
Z.I. du terroir, rue de l'industrie, 31140 Saint Alban.
Tel: 61 37 44 00. Fax: 61 37 44 29.
Parc Club du golf, Batiment 1, 13856 Aix-en-Provence CEDEX 3. Tel: 42 16 77 88
Fax: 42 39 4728.
1 rue de la Faisandereie, Bat B1 P.C. de Tanneries, F-67883 Tanneries CEDEX.
Tel: 88 77 26 46. Fax: 88 76 13 30.
6 rue Abbe Henri Gregorie, F-35000 Rennes. Tel: 99 32 44 33. Fax: 99 51 33 93
22 rue de Seclin, F-59175 Vendeville. Tel: 20 62 07 67. Fax: 20 62 07 66.
Omnitech Sertronique:
C.A. de Montheard, 11 rue Edgar Brant, 72016 Le Mans CEDEX.
Tel: 43 86 74 74. Fax: 43 86 74 86.
165 boulevard de Valmy, Evolic Batiment 1, 92706 Colombes.
Tel: 1 46 13 07 80. Fax: 1 46 13 07 90.
ZAC des Petites Landes, 44470 Thouare-sur-Loire. Tel: 40 49 90 90.
Fax: 40 68 06 72.

99 boulevard de l'Artillerie, 69007 Lyon. Tel: 72 73 11 87. Fax: 72 73 18 00.
37 rue Saint-Eloi, 76000 Rouen. Tel: 35 88 00 38. Fax: 35 15 06 22.
20 rue Cabanis, 59041 Lille. Tel: 20 43 96 44. Fax: 20 56 00 49.
Parc Cadera Sud, Batiment F, 33700 Bordeaux Merignac. Tel: 56 34 46 00.
Fax: 56 34 47 13.

GERMANY **AS Electronic Vertriebs GmbH,** In den Garten 2, D-61352 Bad Homburg.
Tel: 06172 458931. Fax: 06172 42000.
Farnell Electronic Services GmbH, Bahnhofstrasse 44, 71696 Moglingen.
Tel: 071 41-4 87-0. Fax: 071 41-4 87-210.
Micronetics GmbH, Dieselstrasse 12, D-71272 Renningen. Tel: 07159-925830.
Fax: 07159-9258355.
Weisbauer Elektronik GmbH, Heiliger Weg 1, D-44135 Dortmund. Tel: 0231 579547.
Fax: 0231 577514.

GREECE **Impel Ltd.,** 30 Rodon Str, Korydallos, Piraeus, Greece. Tel: 010 30 1 49 67815.
Tlx: 213835. Fax: 01 49 54041.

HONG KONG **Gain Tune Ltd,** Room 809, 8th Floor, Hunghom Commercial Centre, Tower B,
37-39 Ma Tau Wai Road,Hunghom, Kowloon, Hong Kong. Tel: 852-3654860.
Fax: 852-7641129.

HUNGARY **Macro Group,** Etele ut 68,Budapest 1115. Tel: 36 1 2698110/1853111.
Fax: 36 1 1850061.

INDIA **Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg,
New Delhi, 100 001 India Tel: 11 3312110 Fax: 11 3712155.

ITALY **Adelsy - Divisione della Generalmusic SpA,** Via Novara 570, 20153 Milano.
Tel: 02 3810310. Fax: 02 38002988.
Eurelettronica SpA, Via E. Fermi 8, 20090 Assago (MI). Tel: 02 457841.
Fax: 02 4880275.
Fanton Srl, Milano - Torino - Bologna - Firenze - Roma - Padova.
Tel: 02 48912963. Fax: 02 4890902.

JAPAN **Cornes & Company Ltd.,** Ryukakasan Building, 2-5-12, Kanda, Chiyoda-ku,
Tokyo 101. Tel: 3-5821-1651. Fax: 3-5821-1904.
Cornes & Company Ltd., 1-13-40 Nishi-hommachi, Nishi-ku, Osaka 550.
Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850.

KOREA **KML Corporation,** 6th Floor, Dukmyung Building, (A-Dong) 113-3, Banpo-Dong,
Shucho-Gu, CPO Box 7981, Seoul. Tel: 2 595 9101-6. Fax: 2 595 9107.

MALAYSIA **Adequip Enterprise Sdn Bhd,** #6-01 6th Floor, Wisjma Stephens,
88 Jalan Raya Chulan, 50200 Kualar Lumpur, Malaysia. Tel: 2423522. Fax: 2423264.

NETHERLANDS **Tekelek-Airtronic B.V.,** PO Box 63, NL-2700 AB Zoetermeer. Tel: 079 310100.
Fax: 079 417504

NORWAY **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, Postboks 99 Veitvet, Oslo 5.
Tel: 22 64 11 50. Tx: 71963 Fax: 22 64 34 43.

POLAND **Macropol Co. Ltd,** Ul Bitwy Warszawskiej 11, 02 366 Warsaw. Tel: 48 22 224337.
Fax: 48 22 229136.

PORTUGAL **Anatronic SL,** Urbanisazao Do, Infantado, Lote 18, 2º ESQ, Loures. Tel: 1 79 33 2 99.

RUSSIA **Anastasia Neklusova,** St Petersburg, Ul Zamshina 15. Tel: 7 812 545 0723.
Fax: 7 812 254 51256.

SLOVAK REPUBLIC **Macro Zilinia,** Vysokoskolakov 6, 010-01 Zilinia. Tel: 42 89 634181/45041.
Fax: 42 89 634109.

SOUTH AFRICA **T.E.C. Tellumat Electronic Components,** 1 Jansen Road, Jet Park, Boksburg 1459,
P.O. Box 8174, Elandsfontein 1406. Tel: 2711 823 2950. Fax: 2711 823 2668.

SPAIN **Anatronic SA,** Avda de Valladolid 27, 28008 Madrid. Tel: 91 542 4455/6.
Fax: 91 2486975.
Anatronic SA, Bailen, 176, Estresuelo 1°, 08037 Barcelona. Tel: 93 258 1906/7.
Fax: 93 258 7128.

SWEDEN **Pronesto AB (Microwave Products Only),** Finlandsgatan 18, 16475 Kista.
Tel: (08) 752 9080. Fax: (08) 751 4111.

SWITZERLAND **Basix für Electronik AG,** Hardturmstr 181, CH-8010 Zuerich. Tel: 1 2761111. Fax: 1 2764199.

TAIWAN **Prospect Technology Corporation,** 5, Lane 55, Long-Chiang Road, Taipei, Taiwan. Tel: (886-2) 721-9533. Fax: (886-2) 773-3756.
World Peace Industrial Co Ltd, 8th Floor, 76 Cheng Kung Road, Sec. I., Nankang District, Taipei, Taiwan ROC. Tel: (886-2) 788-5200. Fax: (886-2) 788-3255.

THAILAND **Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak, Bangkok 10900. Thailand. Tel: 2 5125531. Fax: 2 2365949.

TURKEY **EMPA,** 34630, Besyol Londra Asfalti Florya Is Merkezi Sefakoy, Istanbul. Tel: (1) 599 30 50 Tx: 21137 Etna tr Fax: (1) 598 53 53.

UNITED KINGDOM **Farnell Celdis,** 300 Kings Road, Reading, Berks RG1 4GA. Tel: (01734) 666676. Fax: (01734) 263100.
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Farnell Electronic Services, Edinburgh Way, Harlow, Essex CM20 2DF. Tel: (01279) 626777. Fax: (01279) 441687.
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USA: Alabama **Pioneer Technologies,** 4835 University Square #5, Huntsville, AL 35816. Tel: (205) 837-9300. Fax: (205) 837-9358.
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Ohio	**Pioneer Standard,** 4800 East 131st St., Cleveland, OH 44105. Tel: (216) 587-3600. Fax: (216) 587-3906.
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Pioneer Standard, 1826-D Kramer Ln., Austin. TX 78758. Tel: (512) 835-4000. Fax: (512) 835-9829.
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UK Export

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GEC Plessey Semiconductors , Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts, UK SN2 5AF. Tel: (01793) 518527/518566. Fax: (01793) 518582.
Whiteaway Laidlaw (Overseas) Ltd., PO Box 93, Ambassador House, Devonshire Street North, Manchester M60 6BU Tel: (0161) 273 3228. Fax: (0161) 274 3757.

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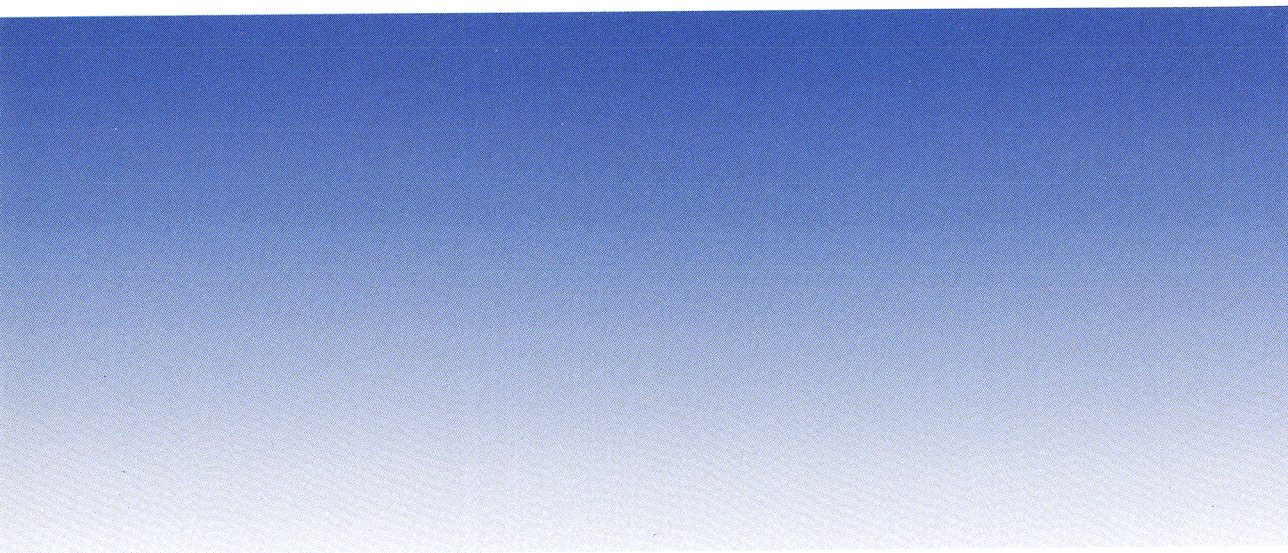

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